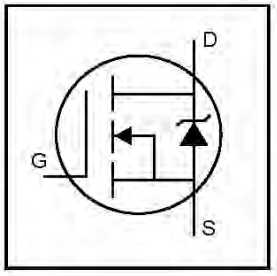
International
IOR Rectifier

PD - 95001

# IRFP064NPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free




$V_{DSS}$ = 55V

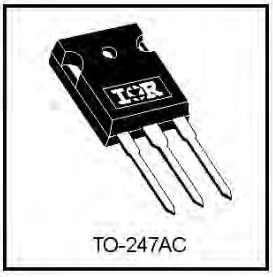
$R_{DS(on)}$ = 0.008Ω

$I_D$ = 110A⑥

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 110⑥ | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 80⑥ | |
| $I_{DM}$ | Pulsed Drain Current ①⑤ | 390 | |
| $P_D$ @ $T_C$ = 25°C | Power Dissipation | 200 | W |
| | Linear Derating Factor | 1.3 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy②⑤ | 480 | mJ |
| $I_{AR}$ | Avalanche Current① | 59 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | 20 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③⑤ | 5.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
| | Mounting torque, 6-32 or M3 srew | 10 lbf•in (1.1N•m) | |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | 0.75 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | 0.24 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 40 | |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 55 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.057 | — | V/°C | Reference to 25°C, $I_D$ = 1mA⑤ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.008 | Ω | $V_{GS}$ = 10V, $I_D$ = 59A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $g_{fs}$ | Forward Transconductance | 42 | — | — | S | $V_{DS}$ = 25V, $I_D$ = 59A⑤ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 25 | µA | $V_{DS}$ = 55V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 44V, $V_{GS}$ = 0V, $T_J$ = 150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | — | — | 170 | nC | $I_D$ = 59A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 32 | | $V_{DS}$ = 44V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 74 | | $V_{GS}$ = 10V, See Fig. 6 and 13 ④⑤ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 14 | — | ns | $V_{DD}$ = 28V |
| $t_r$ | Rise Time | — | 100 | — | | $I_D$ = 59A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 43 | — | | $R_G$ = 2.5Ω |
| $t_f$ | Fall Time | — | 70 | — | | $R_D$ = 0.39Ω, See Fig. 10④⑤ |
| $L_D$ | Internal Drain Inductance | — | 5.0 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 13 | — | | |
| $C_{iss}$ | Input Capacitance | — | 4000 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 1300 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 480 | — | | $f$ = 1.0MHz, See Fig. 5⑤ |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 110⑥ | | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 390 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 59A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 110 | 170 | ns | $T_J$ = 25°C, $I_F$ = 59A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 450 | 680 | nC | di/dt = 100A/µs ④⑤ |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② $V_{DD}$ = 25V, starting $T_J$ = 25°C, L = 190µH $R_G$ = 25Ω, $I_{AS}$ = 59A. (See Figure 12)

③ $I_{SD}$ ≤ 59A, di/dt ≤ 290A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF3205 data and test conditions

⑥ Caculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

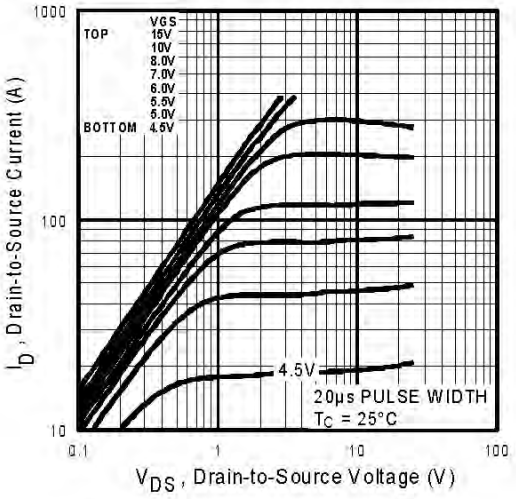



**Fig 1.** Typical Output Characteristics

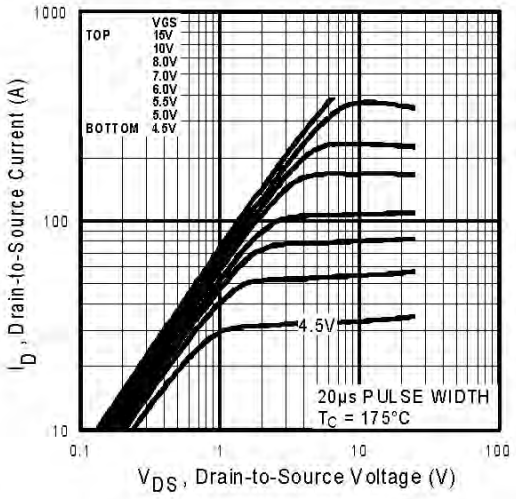



**Fig 2.** Typical Output Characteristics

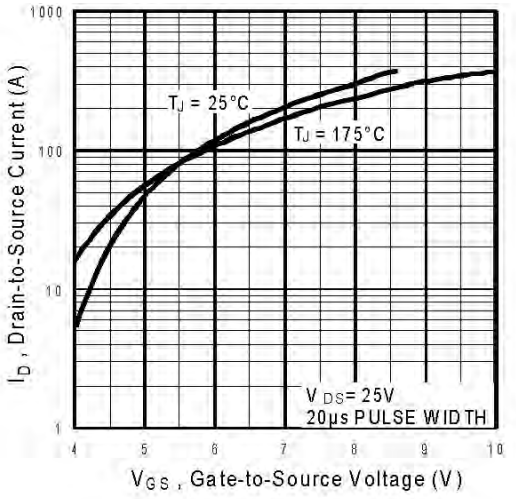



**Fig 3.** Typical Transfer Characteristics

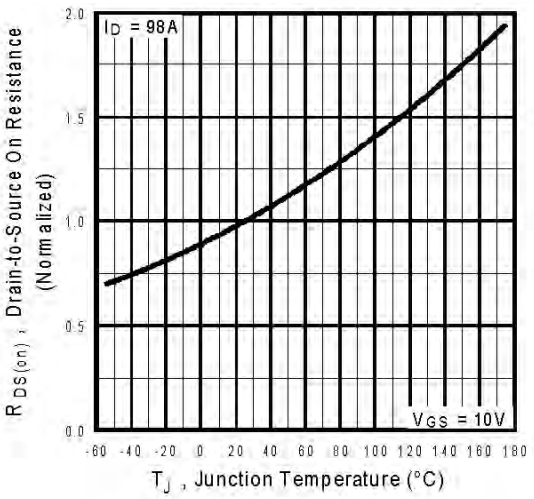



**Fig 4.** Normalized On-Resistance Vs. Temperature

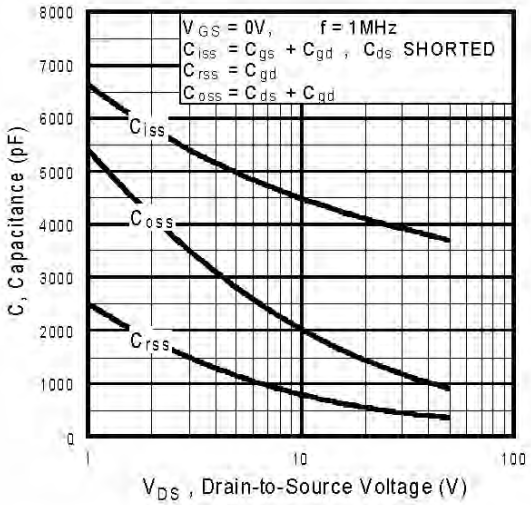



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

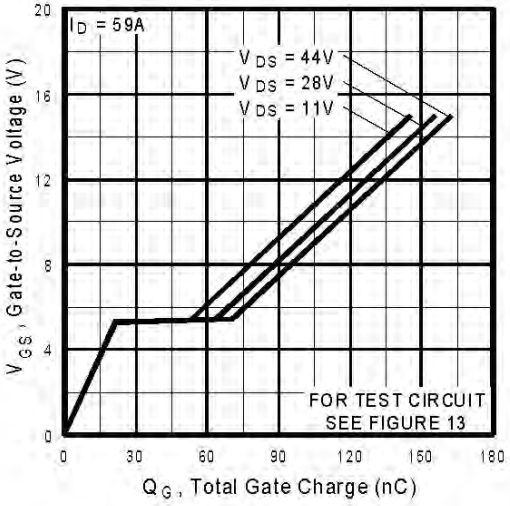



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

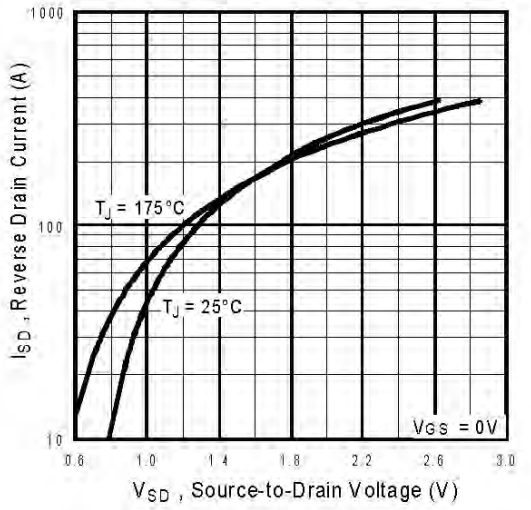



**Fig 7.** Typical Source-Drain Diode Forward Voltage

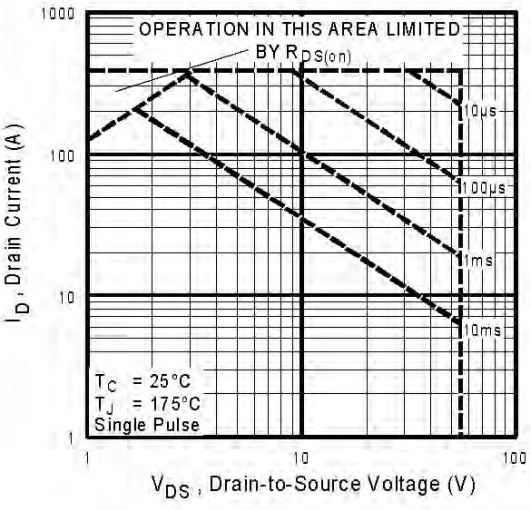



**Fig 8.** Maximum Safe Operating Area

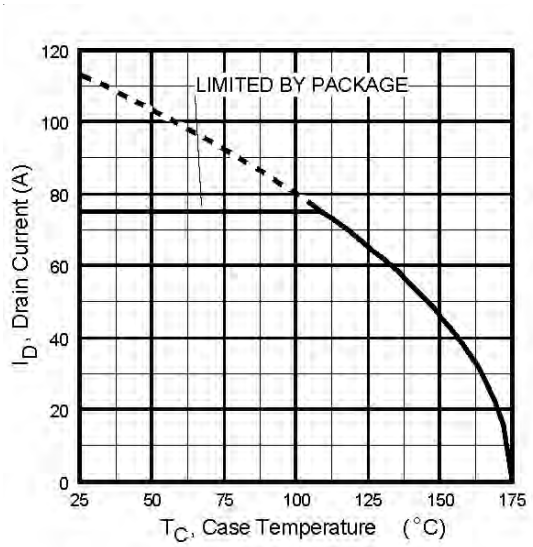



**Fig 9.** Maximum Drain Current Vs. Case Temperature

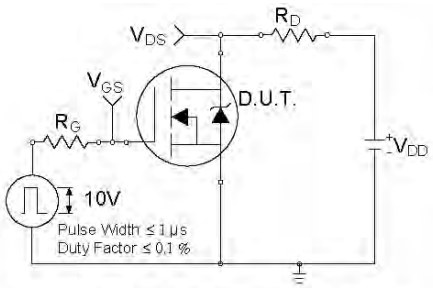



**Fig 10a.** Switching Time Test Circuit

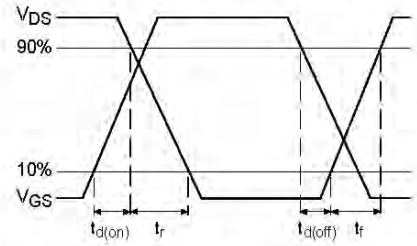



**Fig 10b.** Switching Time Waveforms

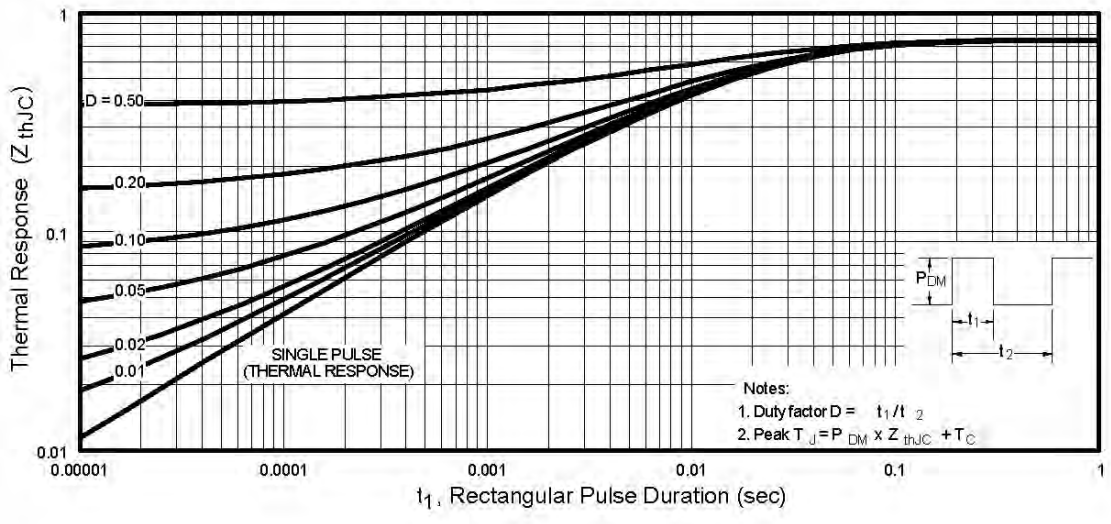



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

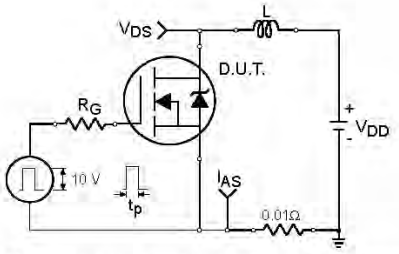



**Fig 12a.** Unclamped Inductive Test Circuit

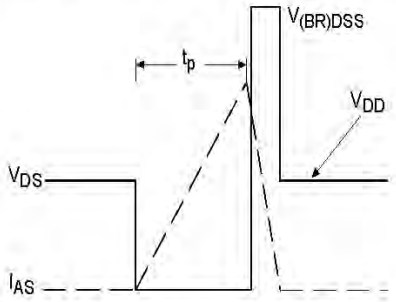



**Fig 12b.** Unclamped Inductive Waveforms

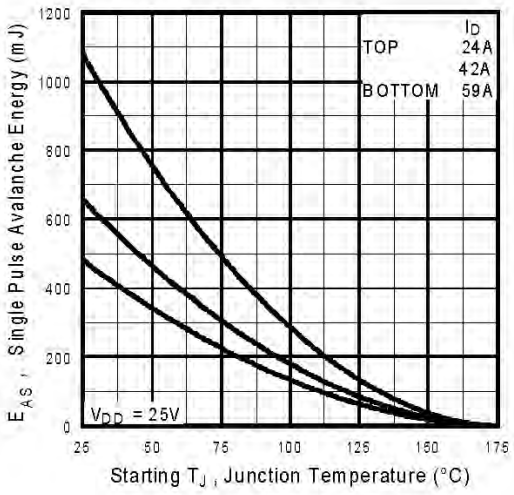



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

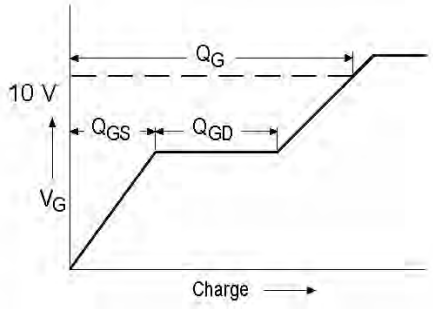



**Fig 13a.** Basic Gate Charge Waveform

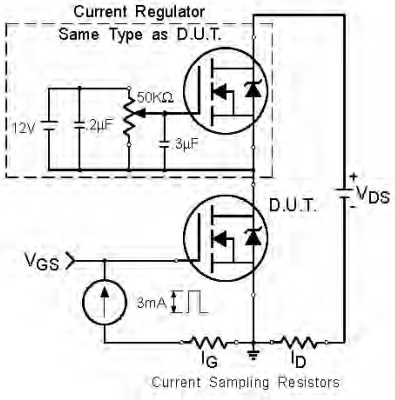



**Fig 13b.** Gate Charge Test Circuit

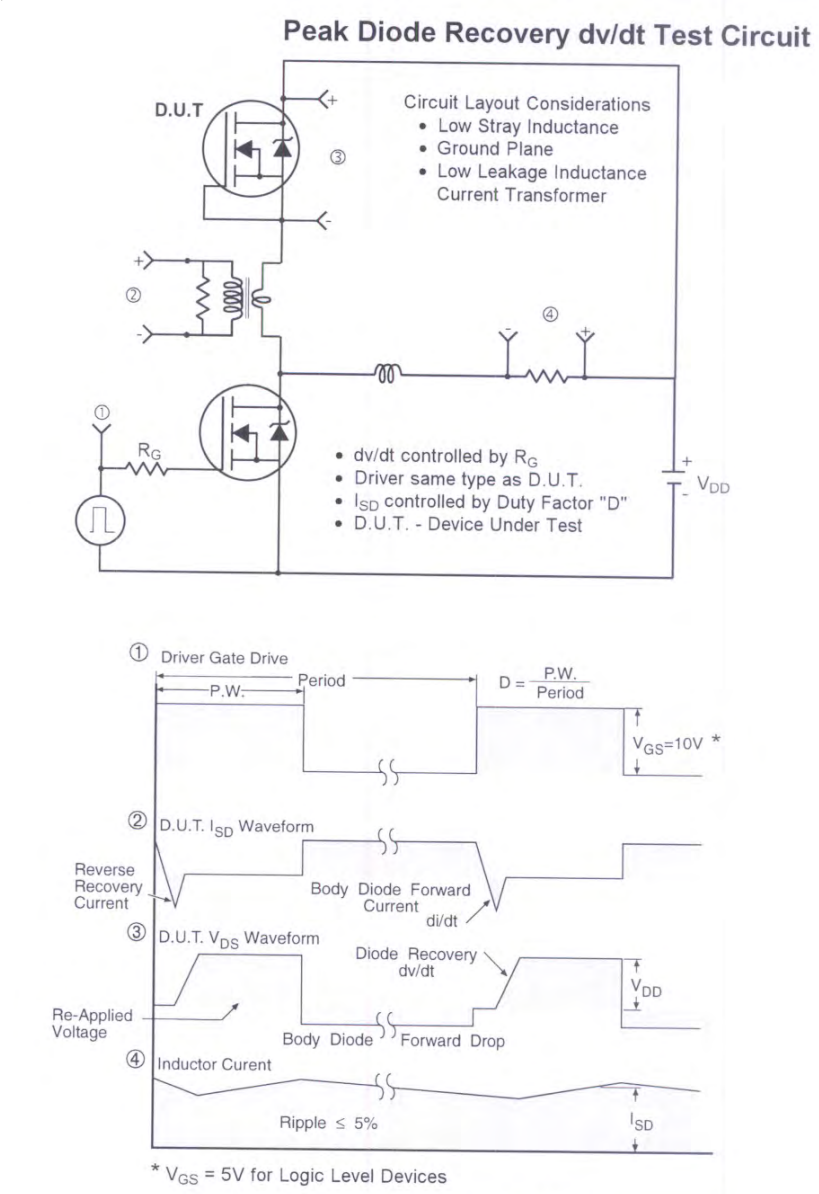
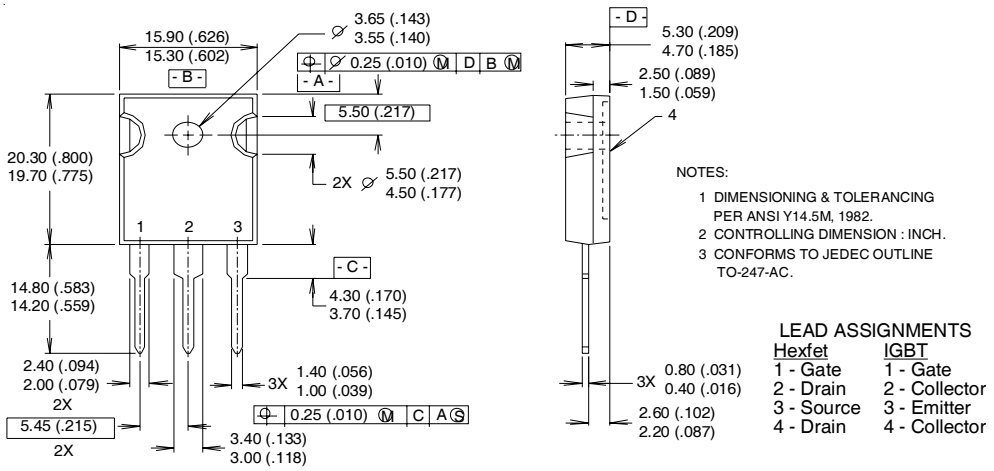



**Fig 14.** For N-Channel HEXFETS

## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)




NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

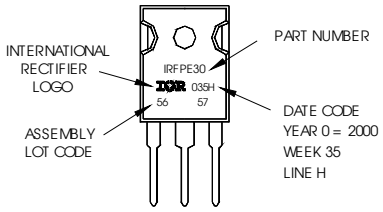
LEAD ASSIGNMENTS

| Hexfet | IGBT |
|---|---|
| 1 - Gate | 1 - Gate |
| 2 - Drain | 2 - Collector |
| 3 - Source | 3 - Emitter |
| 4 - Drain | 4 - Collector |

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

**Note:** "P" in assembly line position indicates "Lead-Free"

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Note:  For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

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