

HEXFET® Power MOSFET

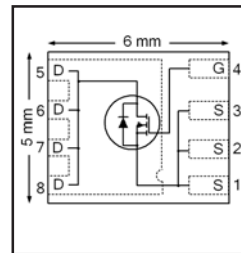
Applications

- Control MOSFET of Sync-Buck Converters used for Notebook Processor Power
- Control MOSFET for Isolated DC-DC Converters in Networking Systems

Benefits

- Very low $R_{DS(ON)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 100% Tested for R_G
- Lead-Free (Qualified up to 260°C Reflow)
- RoHS compliant (Halogen Free)
- Low Thermal Resistance
- Large Source Lead for more reliable Soldering

V_{DS}	$R_{DS(on)}$ max	Qg
30V	3.5mΩ @ $V_{GS} = 10V$	20nC



Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRFH7934PBF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7934TRPBF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	24	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	19	
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	76	
I_{DM}	Pulsed Drain Current ①	190	
P_D @ $T_A = 25^\circ C$	Power Dissipation ⑤	3.1	W
P_D @ $T_A = 70^\circ C$	Power Dissipation ⑤	2.0	
	Linear Derating Factor ⑤	0.025	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	2.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	40	

Notes ① through ⑤ are on page 10

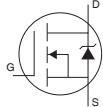
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

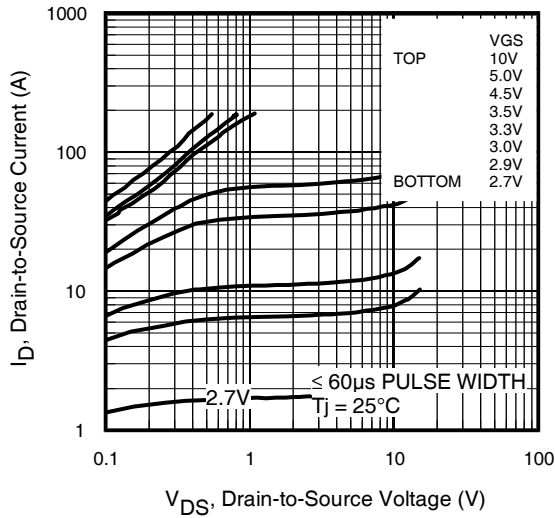
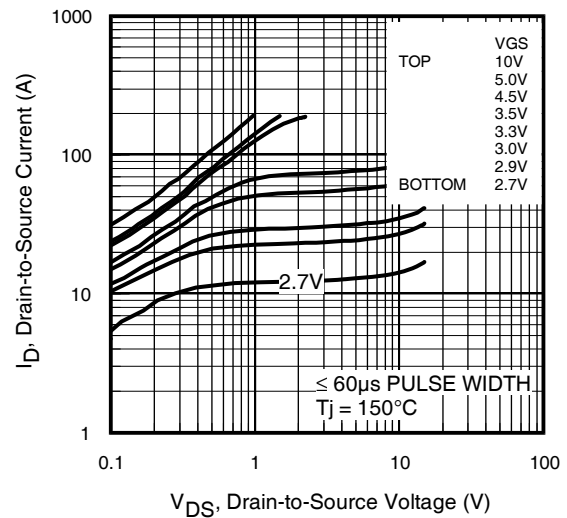
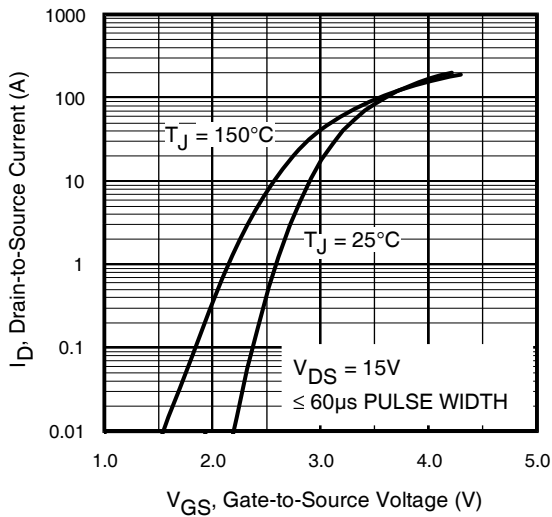
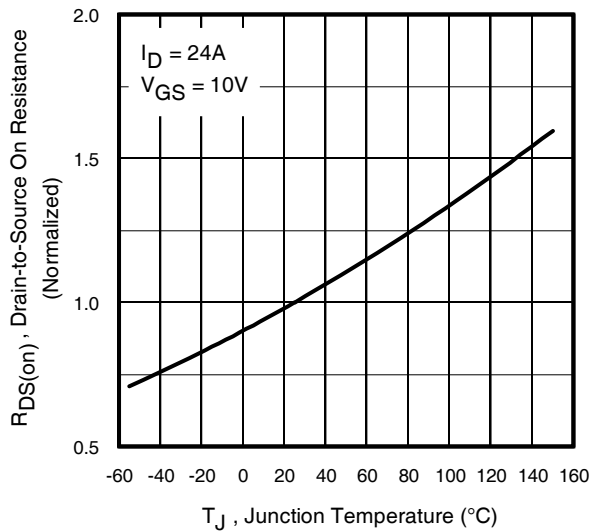
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.021	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.9	3.5	$m\Omega$	$V_{GS} = 10V, I_D = 24A$ ③
		—	4.2	5.1		$V_{GS} = 4.5V, I_D = 19A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-6.5	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	110	—	—	S	$V_{DS} = 15V, I_D = 19A$
Q_g	Total Gate Charge	—	20	30	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 19A$ See Fig.17 & 18
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	4.8	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.5	—		
Q_{gd}	Gate-to-Drain Charge	—	6.3	—		
Q_{godr}	Gate Charge Overdrive	—	6.4	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	8.8	—		
Q_{oss}	Output Charge	—	15	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.7	3.1	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ $I_D = 19A$ $R_G = 1.8\Omega$ See Fig.15
t_r	Rise Time	—	16	—		
$t_{d(off)}$	Turn-Off Delay Time	—	14	—		
t_f	Fall Time	—	7.5	—		
C_{iss}	Input Capacitance	—	3100	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	623	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	241	—		$f = 1.0MHz$

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	97	mJ
I_{AR}	Avalanche Current ①	—	19	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.9	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	190		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 19A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	20	30	ns	$T_J = 25^\circ\text{C}, I_F = 19A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	28	42	nC	$di/dt = 325A/\mu s$ ③ See Fig.16
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

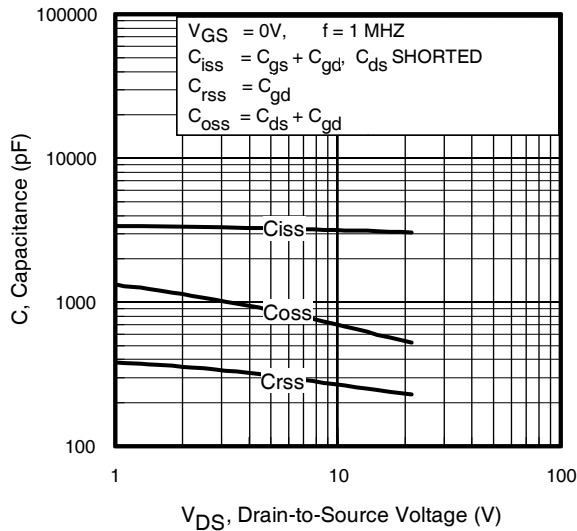


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

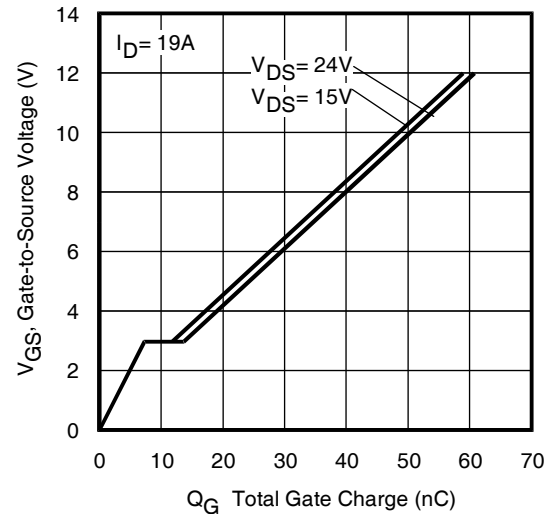


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

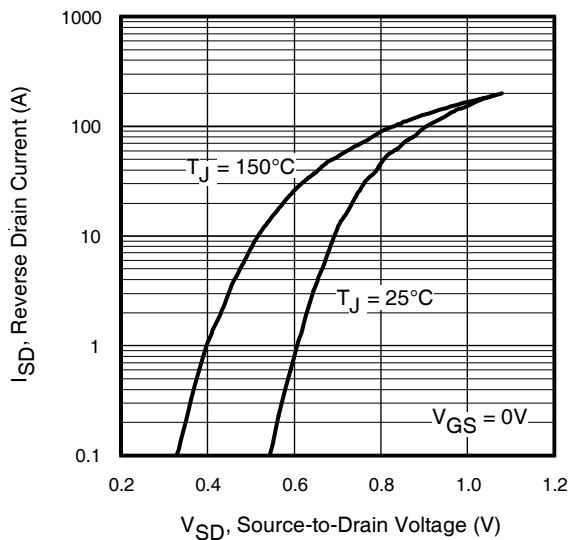


Fig 7. Typical Source-Drain Diode Forward Voltage

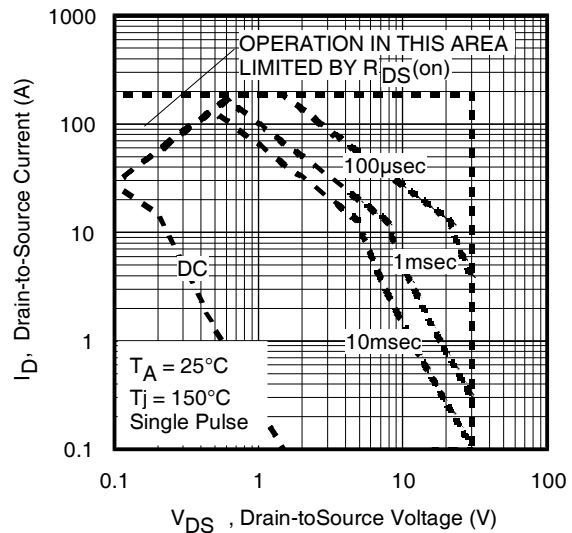


Fig 8. Maximum Safe Operating Area

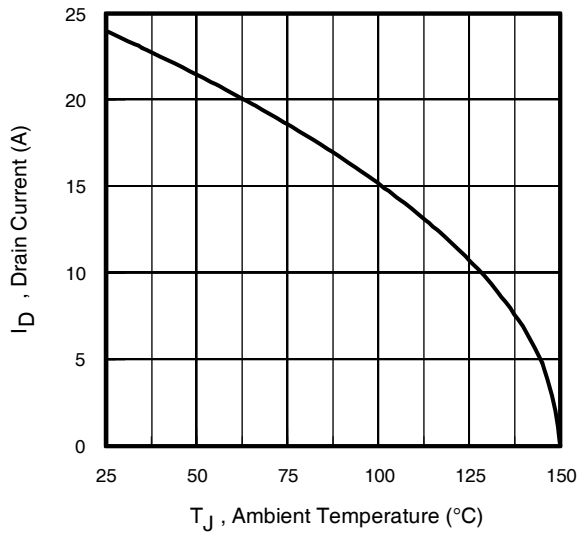


Fig 9. Maximum Drain Current vs. Ambient Temperature

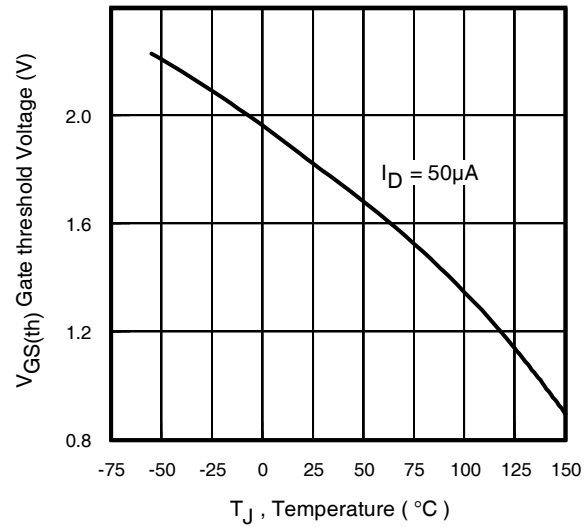


Fig 10. Threshold Voltage vs. Temperature

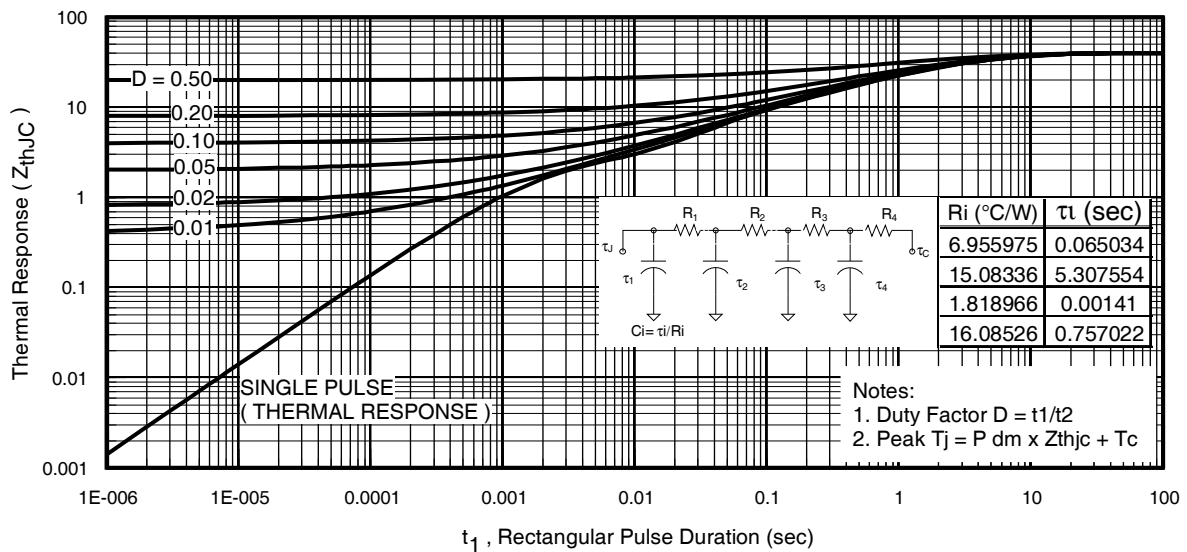
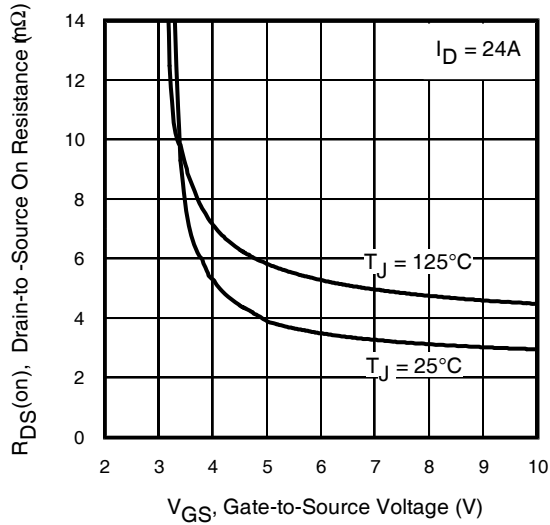
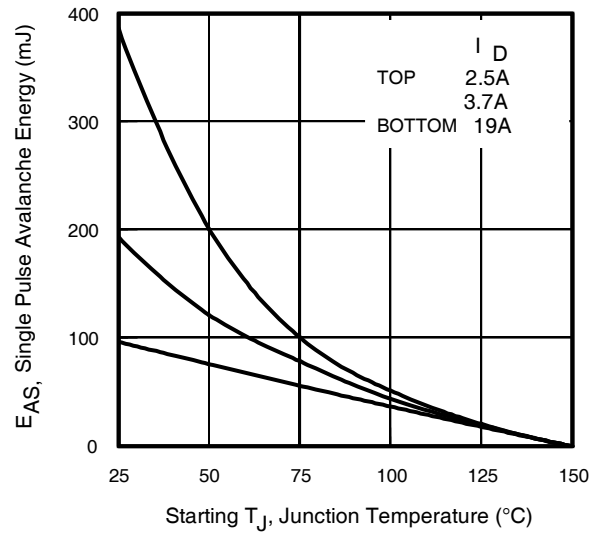
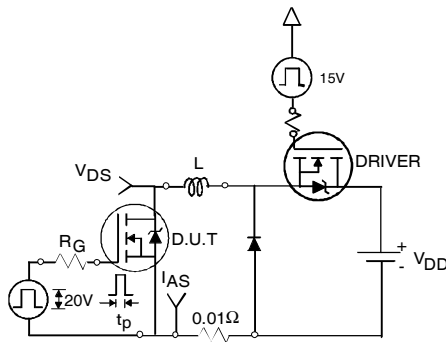
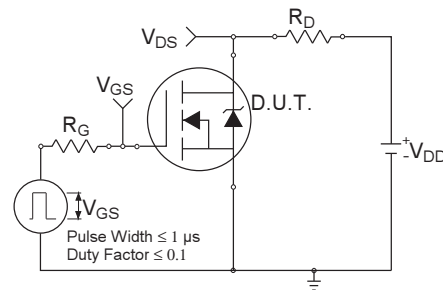
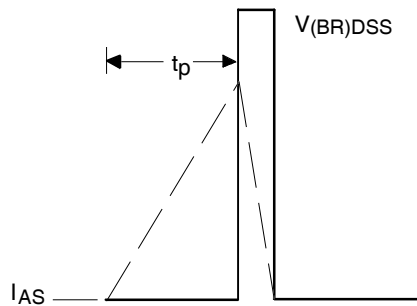
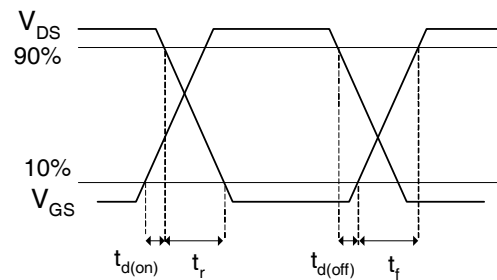
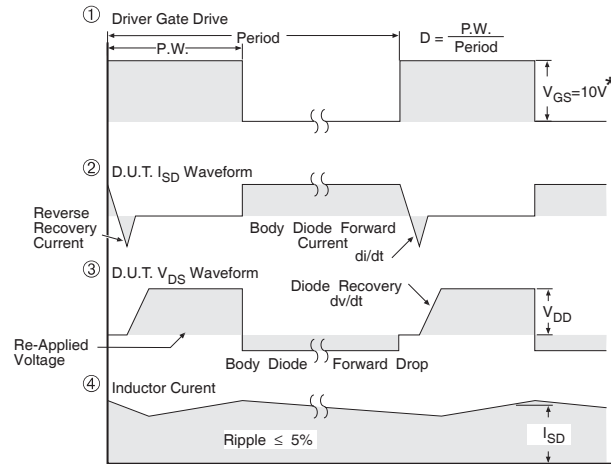
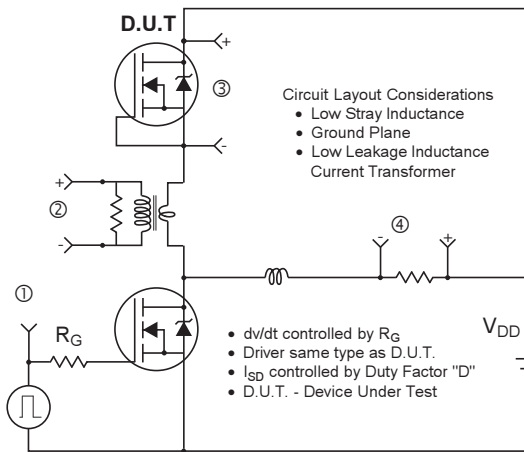


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14a. Unclamped Inductive Test Circuit

Fig 15a. Switching Time Test Circuit

Fig 14b. Unclamped Inductive Waveforms

Fig 15b. Switching Time Waveforms



* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

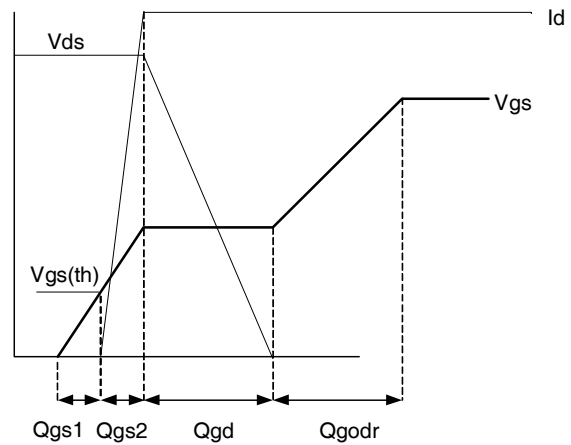
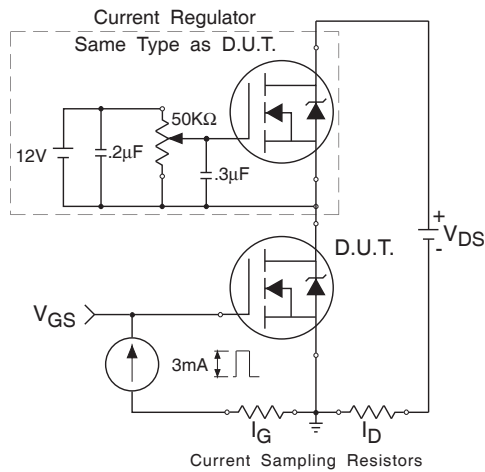
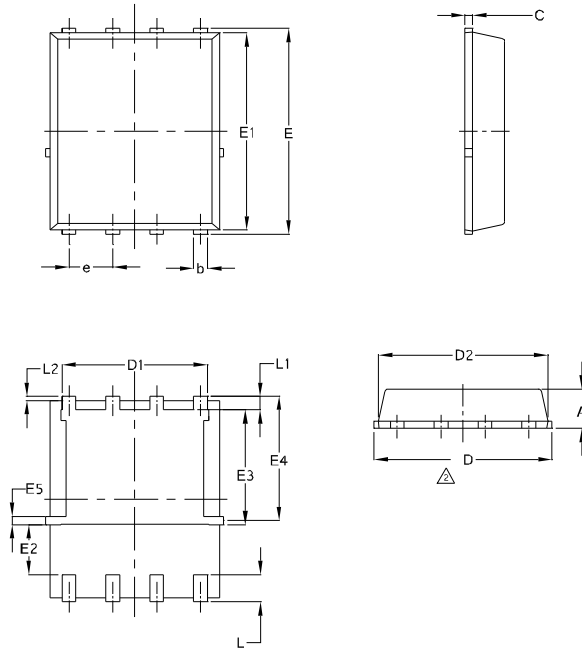


Fig 17. Gate Charge Test Circuit

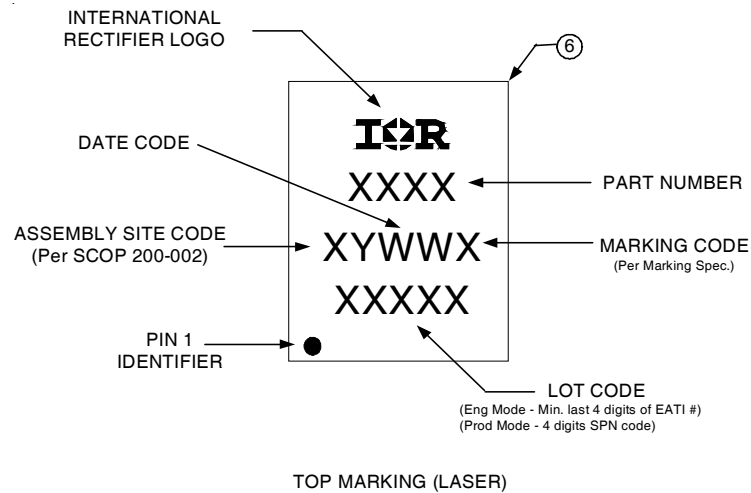
Fig 18. Gate Charge Waveform

PQFN 5x6 Option "E" Package Details



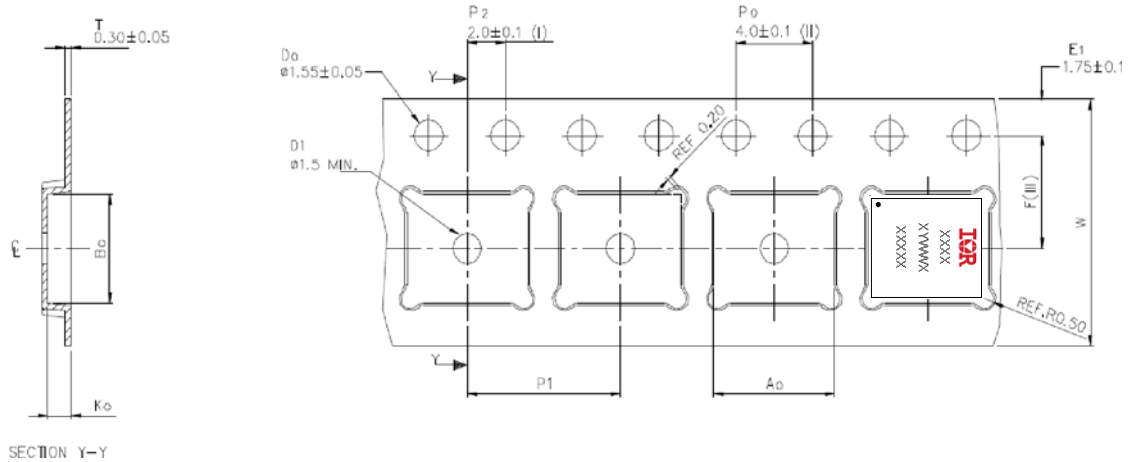
SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.17	0.0354	0.0461
b	0.31	0.51	0.0130	0.0189
C	0.195	0.300	0.0077	0.0118
D	4.80	5.25	0.1890	0.2028
D1	3.91	4.31	0.1539	0.1697
D2	4.80	5.10	0.1890	0.1968
E	5.90	6.25	0.2323	0.2421
E1	5.65	6.15	0.2224	0.2362
E2	1.10	—	0.0594	—
E3	3.32	3.78	0.1307	0.1480
E4	3.52	3.72	0.1346	0.1409
E5	0.13	0.32	0.0071	0.0126
e	1.27	BSC	0.050	BSC
L	0.51	0.86	0.0020	0.0098
L1	0.38	0.71	0.0150	0.0260
L2	0.05	0.25	0.0201	0.0339
I	0	0.18	0	0.0071

PQFN Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN Tape and Reel



A ₀	6.30 +/− 0.1
B ₀	5.30 +/− 0.1
K ₀	1.20 +/− 0.1
F	5.50 +/− 0.1
P ₁	8.00 +/− 0.1
W	12.00 +/− 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.
- (V) Typical SR of form tape Max 10⁻⁹ OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL ^{††††} (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.
Please contact your International Rectifier sales representative for further information:

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^{†††} Applicable version of JEDEC standard at the time of product release.

^{††††} Higher MSL ratings may be available for the specific package types listed here.
Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.535\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 19\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Rthjc is guaranteed by design
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.

Revision History

Date	Comments
08/06/2013	- Updated the package outline drawing, on page 8. - This drawing change is related to PCN Hana-GTBF-GEM 5x6 PQFN Public.

International
 Rectifier

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To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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