

IRF7329PbF

HEXFET® Power MOSFET

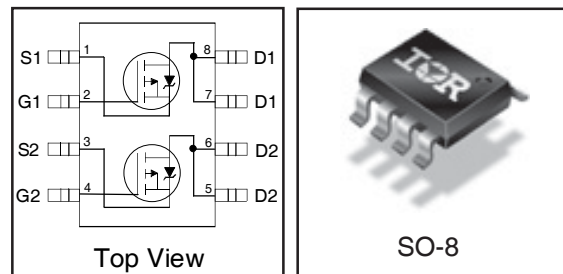
- Trench Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Low Profile (<1.8mm)
- Available in Tape & Reel
- Lead-Free

V _{DSS}	R _{DS(on)} max (mΩ)	I _D
-12V	17 @ V _{GS} = -4.5V	±9.2A
	21 @ V _{GS} = -2.5V	±7.4A
	30 @ V _{GS} = -1.8V	±4.6A

Description

New P-Channel HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infrared, or wave soldering techniques.



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain- Source Voltage	-12	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ -4.5V	-9.2	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ -4.5V	-7.4	
I _{DM}	Pulsed Drain Current ①	-37	
P _D @ T _A = 25°C	Power Dissipation ③	2.0	W
P _D @ T _A = 70°C	Power Dissipation ③	1.3	
	Linear Derating Factor	16	mW/°C
V _{GS}	Gate-to-Source Voltage	± 8.0	V
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJL}	Junction-to-Drain Lead	—	20	°C/W
R _{θJA}	Junction-to-Ambient ③	—	62.5	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-12	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.007	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	17	m Ω	$V_{GS} = -4.5V$, $I_D = -9.2A$ ②
		—	—	21		$V_{GS} = -2.5V$, $I_D = -7.4A$ ②
		—	—	30		$V_{GS} = -1.8V$, $I_D = -4.6A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.40	—	-0.90	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	25	—	—	S	$V_{DS} = -10V$, $I_D = -9.2A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -9.6V$, $V_{GS} = 0V$
		—	—	-25		$V_{DS} = -9.6V$, $V_{GS} = 0V$, $T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -8.0V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 8.0V$
Q_g	Total Gate Charge	—	38	57	nC	$I_D = -9.2A$
Q_{gs}	Gate-to-Source Charge	—	6.8	10		$V_{DS} = -6.0V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	8.1	12		$V_{GS} = -4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = -6.0V$
t_r	Rise Time	—	8.6	—		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	340	—		$R_D = 6.0\Omega$
t_f	Fall Time	—	260	—		$V_{GS} = -4.5V$ ②
C_{iss}	Input Capacitance	—	3450	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1000	—		$V_{DS} = -10V$
C_{rss}	Reverse Transfer Capacitance	—	640	—		$f = 1.0MHz$

Source-Drain Ratings and Characteristics

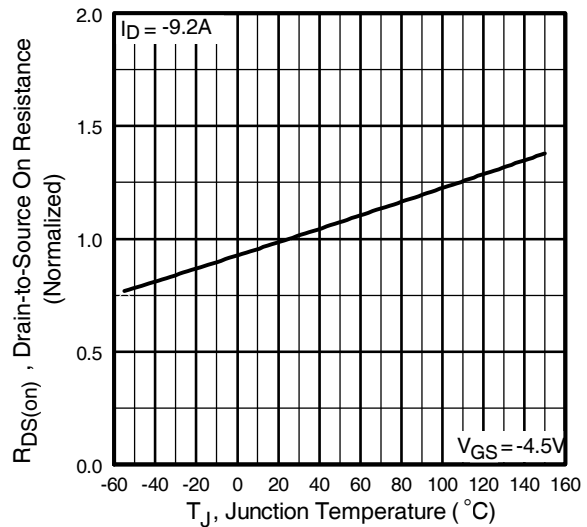
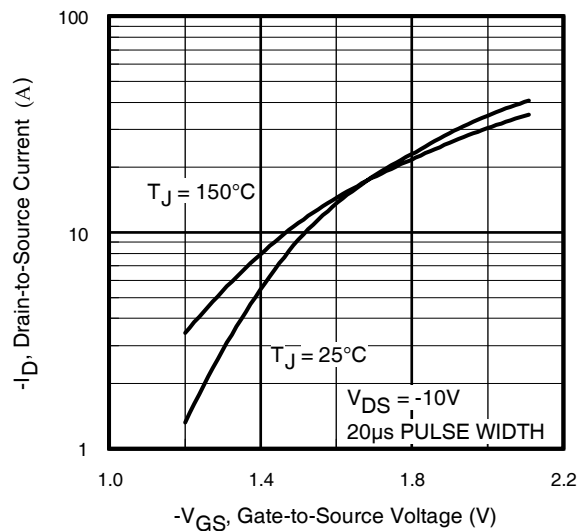
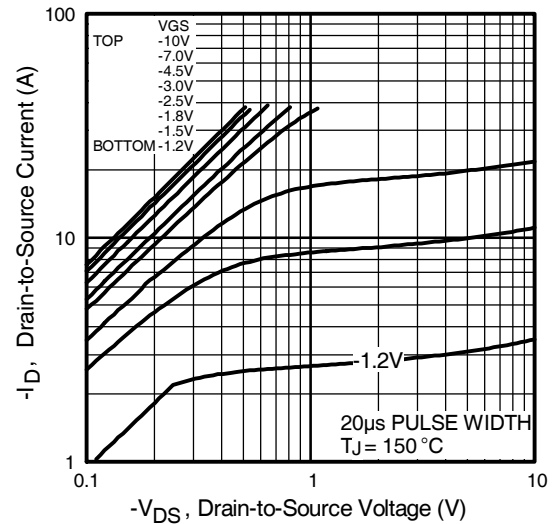
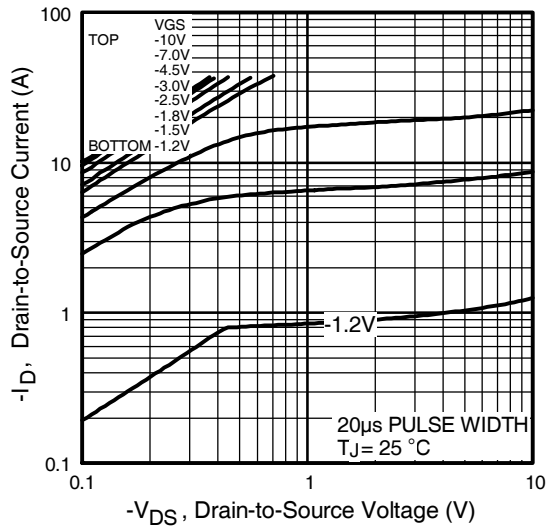
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-37		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}$, $I_S = -2.0A$, $V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}$, $I_F = -2.0A$
Q_{rr}	Reverse Recovery Charge	—	48	72	nC	$di/dt = -100A/\mu s$ ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

③ When mounted on 1 inch square copper board.



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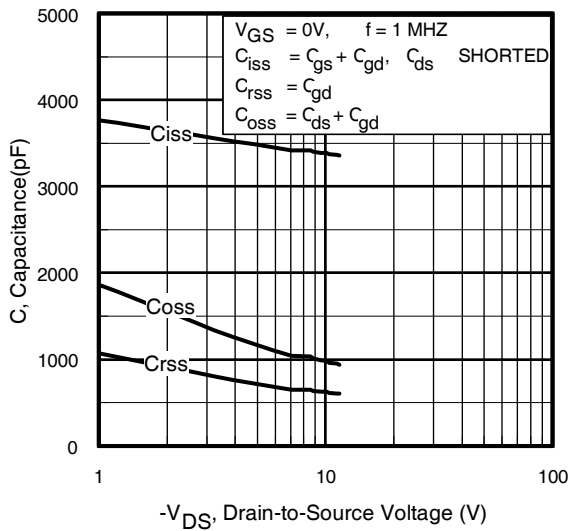


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

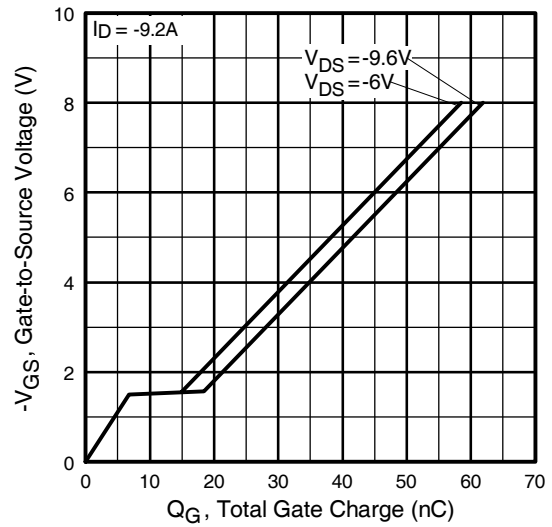


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

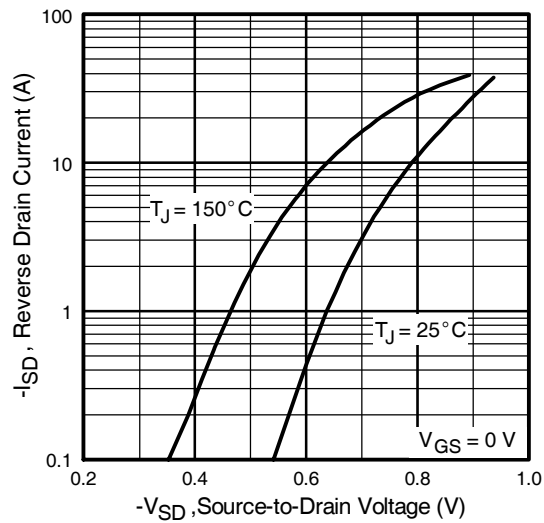


Fig 7. Typical Source-Drain Diode Forward Voltage

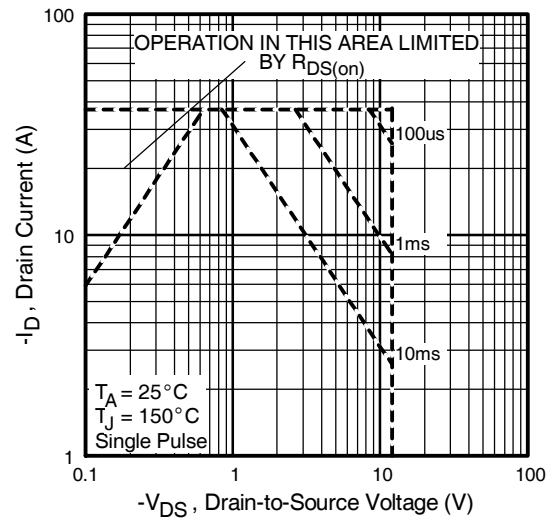


Fig 8. Maximum Safe Operating Area

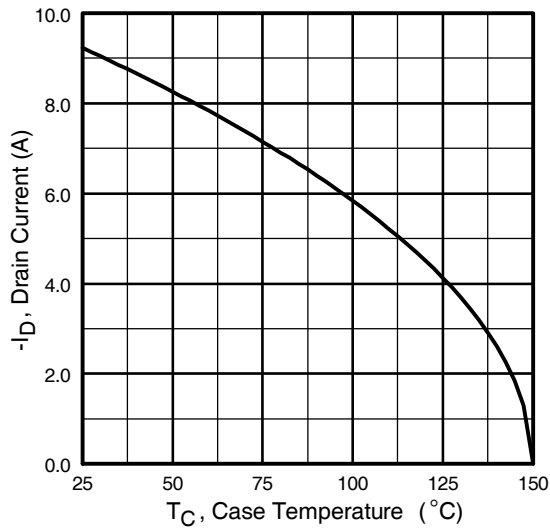


Fig 9. Maximum Drain Current Vs. Case Temperature

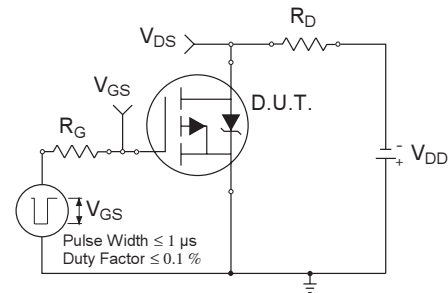


Fig 10a. Switching Time Test Circuit

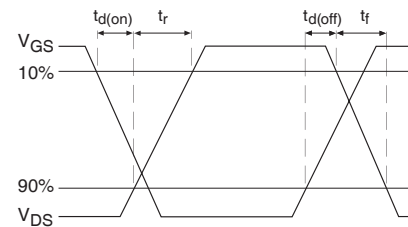


Fig 10b. Switching Time Waveforms

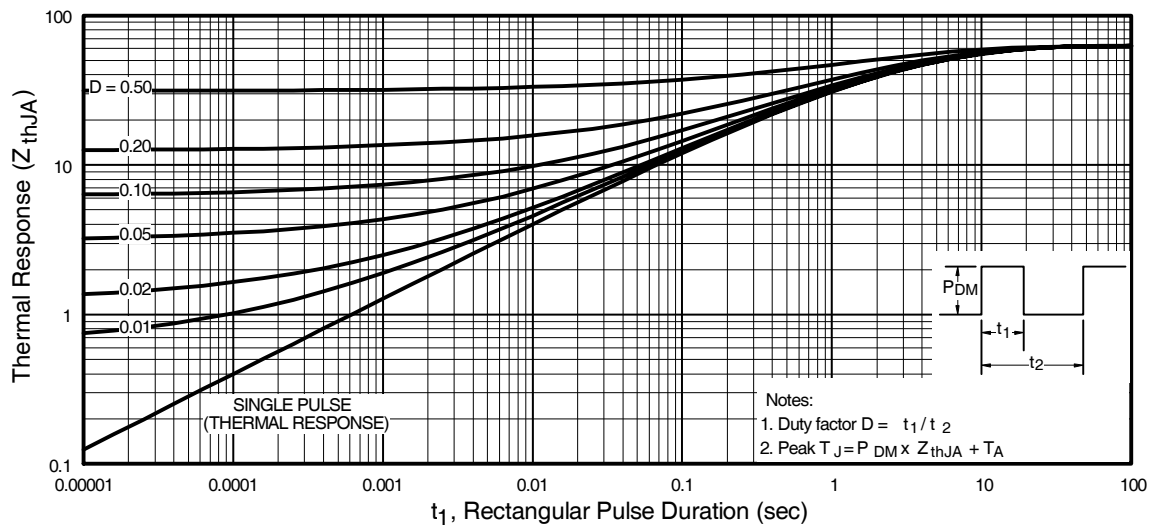


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

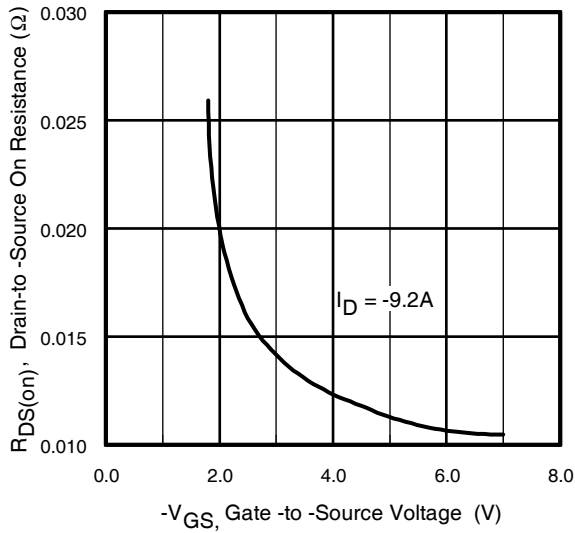


Fig 12. Typical On-Resistance Vs. Gate Voltage

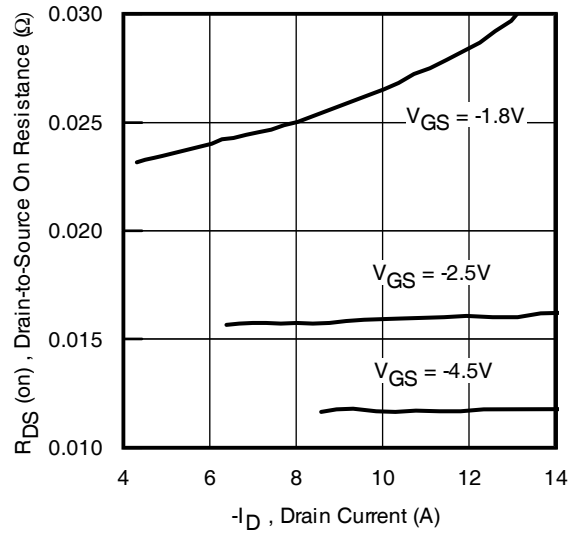


Fig 13. Typical On-Resistance Vs. Drain Current

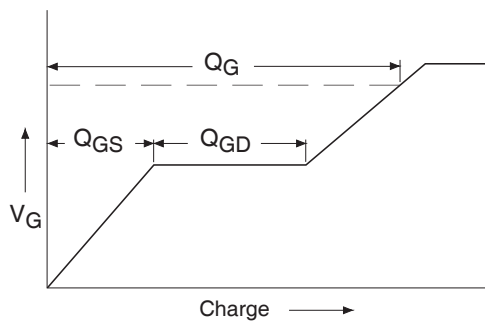


Fig 14a. Basic Gate Charge Waveform

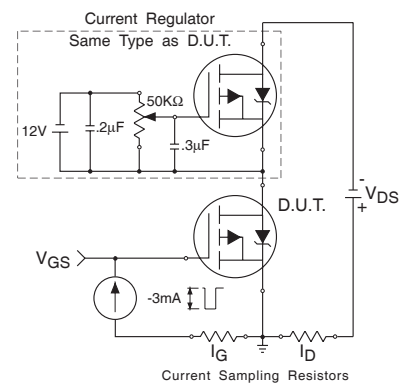


Fig 14b. Gate Charge Test Circuit

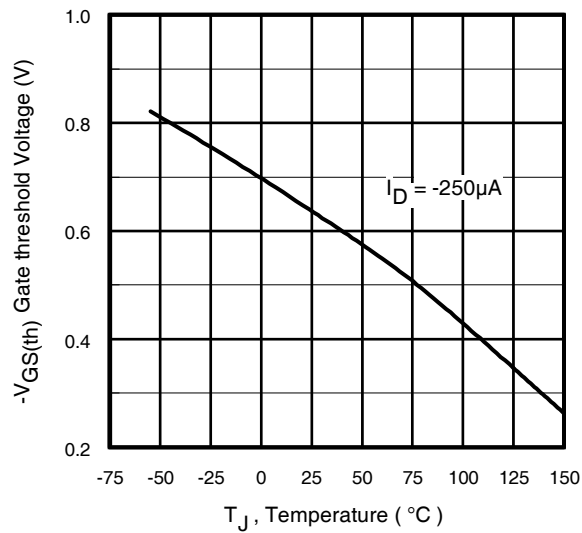


Fig 15. Typical $V_{GS(th)}$ Vs. Junction Temperature

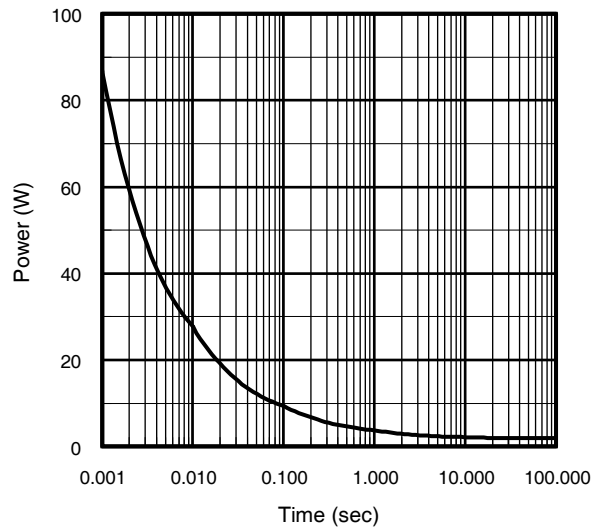


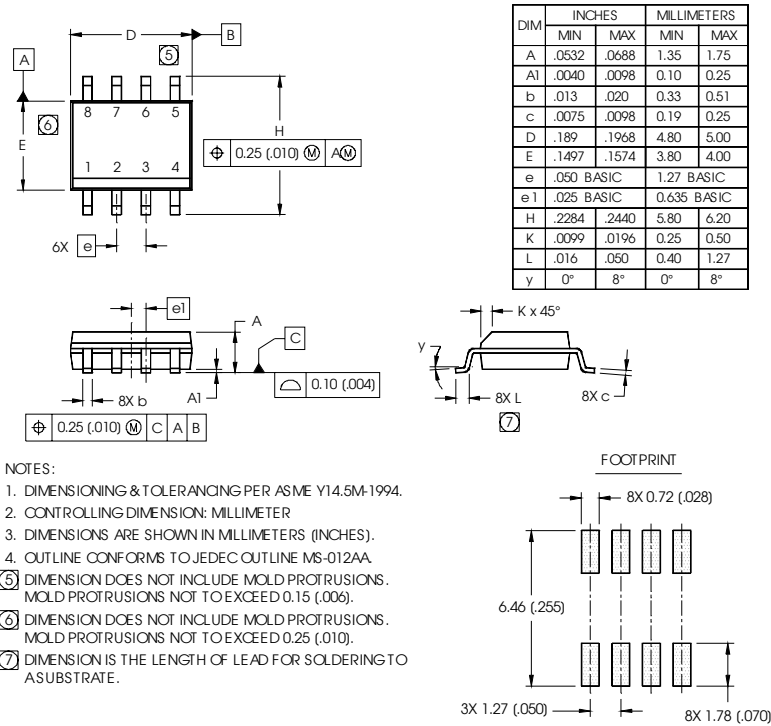
Fig 16. Typical Power Vs. Time

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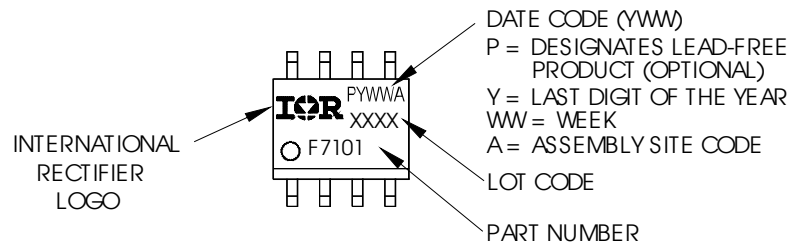
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



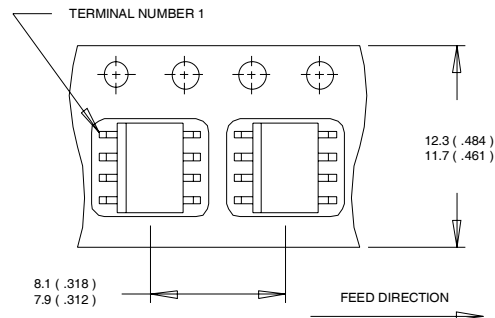
SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

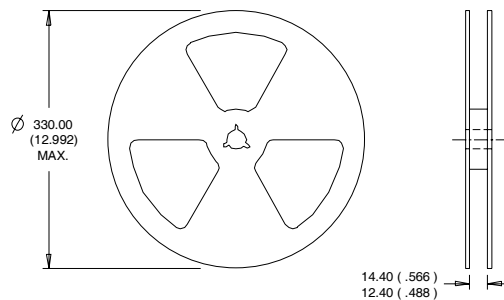


SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



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