FEATURES

- Peak efficiency up to 95% at 1.2V
- Integrated pair of control and synchronous MOSFETs in a single PQFN package
- Proprietary package minimizes package parasitic and simplifies PCB layout
- Input voltage (VIN) range of 4.5V to 21V
- Output current capability of 60A/phase
- Switching frequency up to 1.0MHz
- Ultra-low Rg MOSFET technology minimizes switching losses for optimized high frequency performance
- Synchronous MOSFET with monolithic integrated Schottky diode reduces dead-time and diode reverse recovery losses
- Enhanced top side cooling through exposed pad
- Small 6mm x 6mm x 0.65mm PQFN package
- RoHS compliant, Halogen-Free

APPLICATIONS

- High current, low profile DC-DC converters
- Voltage Regulators for CPUs, GPUs, and DDR memory arrays

DESCRIPTION

The IRF3575DPbF exposed-top integrated Power Block is a single-phase synchronous buck converter with a pair of co-packed control and synchronous MOSFETs. It is optimized internally for PCB layout, heat transfer and package inductance. Coupled with the latest generation of IR MOSFET technology, the IRF3575DPbF provides higher efficiency at lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

Up to 1.0MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. Integrates two high performance MOSFETs in one package while providing superior efficiency and thermals, the IRF3575DPbF enables smallest size and lower solution cost.

The IRF3575DPbF uses IR's latest generation of low voltage MOSFET technology providing ultra-low(<0.5Ω) gate resistance (Rg) and gate charge that results in minimized switching losses. The low RDSon resistance of the synchronous MOSFET, optimizes conduction losses and features a monolithic integrated Schottky to significantly reduce dead-time and diode conduction and reverse recovery losses.

The IRF3575DPbF is optimized specifically for CPU core power delivery in 12Vin applications like servers, narrow VDC notebooks, GPU and DDR memory designs.

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF3575DPBF	PQFN 6mm x 6mm	Tape and Reel	3000	IRF3575DTRPBF

PINOUT DIAGRAM

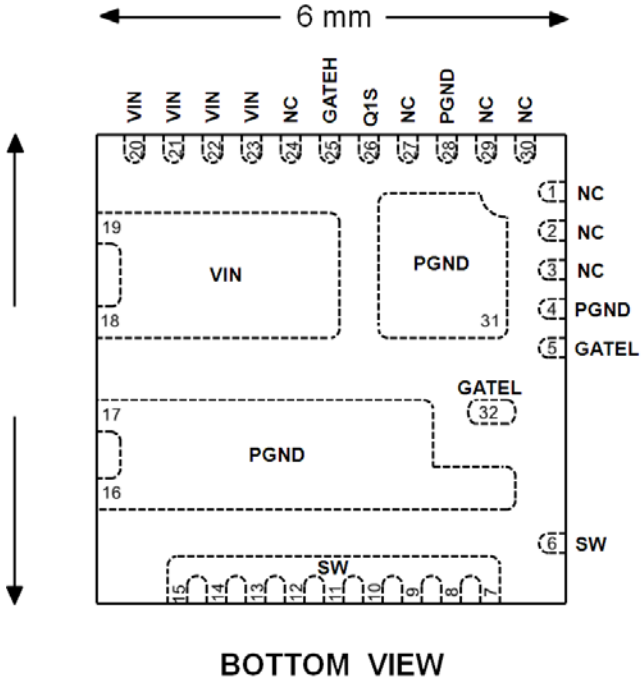


Figure 1: IRF3575DPbF Bottom View

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1-3,24, 27,29,30	No Connect	No connects. These pins can be connected to the VIN or PGND planes to reduce PCB trace resistances.
4,16,17, 28,31	PGND	High current Power Ground. Connected to Source of Q2. Note all pads are internally connected in the package. Provide low resistance connections to the ground plane and respective output capacitors.
5, 32	GATEL	Gate connection of the low side MOSFET Q2.
6-15	SW	Pins 6-15 are the High Current Switch Node output connected to Source of Q1 and Drain of Q2.
26	Q1S	Pin 26 is internally wire-bonded to the Source of Q1 where the floating high side driver return can be connected.
18-23	VIN	High current input supply pads. Connected to Drain of Q1. Recommended operating range is 4.5V to 21V. Connect at least two 10uF 1206 ceramic capacitors and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN pins (18/19) and PGND pins (16/17). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IRF3575.
25	GATEH	Gate connection of the high side MOSFET Q1.

FUNCTIONAL BLOCK DIAGRAM

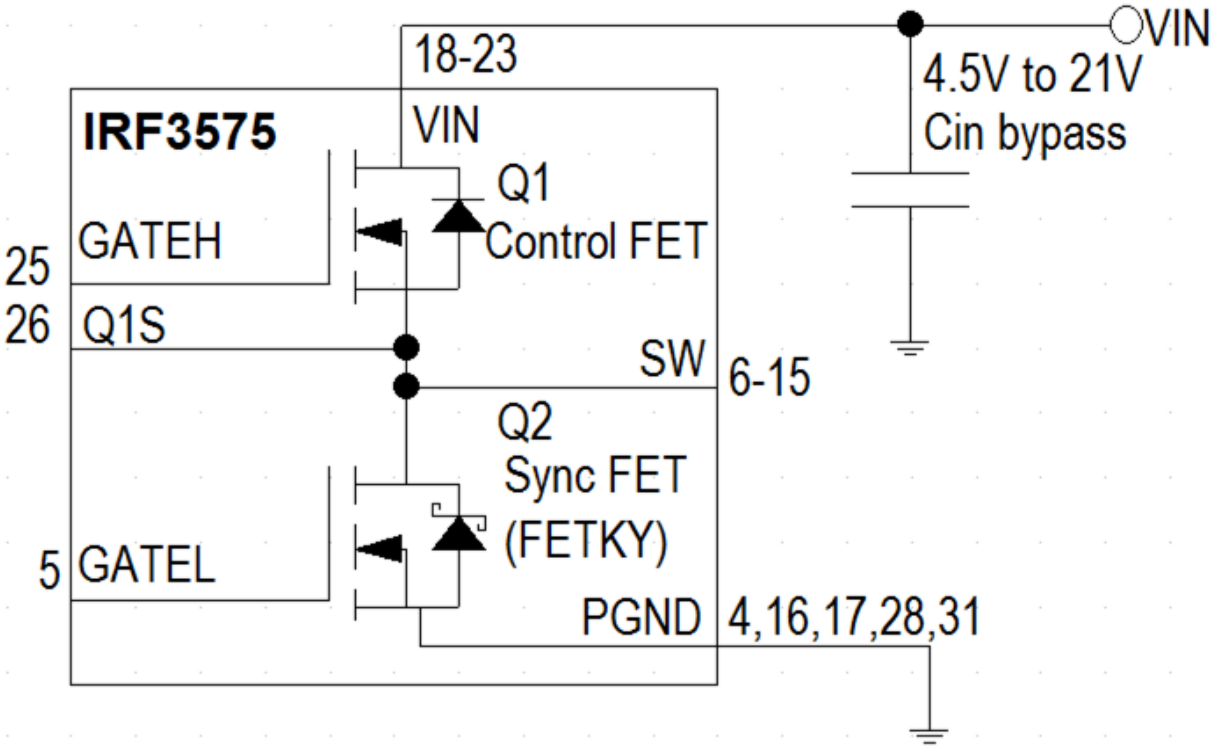


Figure 2: Block Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

	Parameter	Q1 Max.	Q2 Max.	Units
V_{DS}	Drain-to-Source Voltage	25		V
V_{GS}	Gate-to-Source Voltage	±16		V
I_D @T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	86	303	A
I_D @T_C = 70°C	Continuous Drain Current, V_{GS} @ 10V	69	243	A
I_{DM}	Pulse Drain Current	180	525	A
E_{AS}	Single Pulse Avalanche Energy	71 NOTE 1	481 NOTE 2	mJ

Note:

1. T_J =25°C, L =0.14mH, R_G =50Ω, I_{AS} =32A.
2. T_J =25°C, L =0.24mH, R_G =50Ω, I_{AS} =63A.

THERMAL INFORMATION	
Thermal Resistance, Junction to Top (θ_{JC_TOP})	0.8°C/W
Thermal Resistance, Junction to PCB (pin 28) (θ_{JB})	1.7 °C/W
Thermal Resistance (θ_{JA})[1]	19.1 °C/W
Maximum Operating Junction Temperature	-40°C to 150°C
Maximum Storage Temperature Range	-55°C to 150°C
MSL Rating	3
Reflow Temperature	260°C

Note:

1. Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency						
Power Block per-channel Peak Efficiency	η	Note 2		95		%
		Note 3		93		%
Control MOSFETs (Q1)						
Drain-to-Source On-Resistance	$R_{DS(ON)\_4.5V\_25°C}$	V_{GS}=4.5V, I_D=27A, T_J=25°C		3.20	4.10	mΩ
Drain-to-Source On-Resistance	$R_{DS(ON)\_10V\_25°C}$	V_{GS}=10V, I_D=27A, T_J=25°C		2.20	2.75	mΩ
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA, T_J=25°C	25			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	Reference to 25°C, Note 1		0.023		V/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V, T_J=25°C			1	uA
Gate-to-Source Forward Leakage Current	I_{GSS}	V_{GS}=16V			100	nA
Gate-to-Source Reverse Leakage Current	I_{GSS}	V_{GS}=-16V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=35uA	1.1	1.6	2.1	V
Gate Threshold Voltage Coefficient	$\Delta V_{GS(th)}$	V_{DS}= V_{GS}, I_D=35uA		-5.8		mV/°C
Total Gate Charge	Q_g	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A, Note 1		13	20	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		3.6		nC
Post-Vth Gate-to-Source Charge	Q_{gs2}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		1.3		nC
Gate-to-Drain Charge	Q_{gd}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		5.2		nC
Gate Charge Overdrive	Q_{godr}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		2.9		nC
Switch Charge (Q_{gs2} +Q_{gd})	Q_{SW}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		6.5		nC
Output Charge	Q_{oss}	V_{DS}= 16V, V_{GS}=0V		14		nC
Gate Resistance	R_g			0.5		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD}= 13V, V_{GS}=4.5V, I_D=14A, R_G=1.8 Ω		11		ns
Rise Time	t_r	V_{DD}= 13V, V_{GS}=4.5V, I_D=14A, R_G=1.8 Ω		33		ns
Turn-Off Delay Time	$t_{d(off)}$	V_{DD}= 13V, V_{GS}=4.5V, I_D=14A, R_G=1.8 Ω		14		ns
Fall Time	t_f	V_{DD}= 13V, V_{GS}=4.5V, I_D=14A, R_G=1.8 Ω		12		ns
Input Capacitance	C_{iss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		1735		pF
Output Capacitance	C_{oss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		493		pF
Reverse Transfer Capacitance	C_{rss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		137		pF
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=13A, T_J=25°C		0.77	0.88	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		19	29	ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		16	24	nC

Synchronous MOSFETs (Q2)						
Drain-to-Source On-Resistance	$R_{DS(ON)\_4.5V\_25°C}$	V_{GS}=4.5V, I_D=27A, T_J=25°C		1.0	1.35	mΩ
Drain-to-Source On-Resistance	$R_{DS(ON)\_10V\_25°C}$	V_{GS}=10V, I_D=27A, T_J=25°C		0.7	0.9	mΩ
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=1mA, T_J=25°C	25			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	Reference to 25°C, Note 1		0.021		V/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V, T_J=25°C			500	uA
Gate-to-Source Forward Leakage Current	I_{GSS}	V_{GS}=16V			100	nA
Gate-to-Source Reverse Leakage Current	I_{GSS}	V_{GS}=-16V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=100uA	1.1	1.6	2.1	V
Gate Threshold Voltage Coefficient	$\Delta V_{GS(th)}$	V_{DS}= V_{GS}, I_D=1mA		-7.8		mV/°C
Total Gate Charge	Q_g	V_{DS}= 13V, V_{GS},=4.5V, I_D=23A, Note 1		35	53	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}	V_{DS}= 13V, V_{GS}=4.5V, I_D=23A		8.6		nC
Post-Vth Gate-to-Source Charge	Q_{gs2}	V_{DS}= 13V, V_{GS}=4.5V, I_D=23A		3.8		nC
Gate-to-Drain Charge	Q_{gd}	V_{DS}= 13V, V_{GS}=4.5V, I_D=23A		13		nC
Gate Charge Overdrive	Q_{godr}	V_{DS}= 13V, V_{GS}=4.5V, I_D=23A		9.6		nC
Switch Charge (Q_{gs2} +Q_{gd})	Q_{SW}	V_{DS}= 13V, V_{GS}=4.5V, I_D=23A		16.8		nC
Output Charge	Q_{oss}	V_{DS}= 16V, V_{GS}=0V		41		nC
Gate Resistance	R_g			0.4		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD}= 13V, V_{GS}=4.5V, I_D=23A, R_G=1.0 Ω		17		ns
Rise Time	t_r	V_{DD}= 13V, V_{GS}=4.5V, I_D=23A, R_G=1.0 Ω		54		ns
Turn-Off Delay Time	$t_{d(off)}$	V_{DD}= 13V, V_{GS}=4.5V, I_D=23A, R_G=1.0 Ω		24		ns
Fall Time	t_f	V_{DD}= 13V, V_{GS}=4.5V, I_D=23A, R_G=1.0 Ω		16		ns
Input Capacitance	C_{iss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		4765		pF
Output Capacitance	C_{oss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		1577		pF
Reverse Transfer Capacitance	C_{rss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		370		pF
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=30A, T_J=25°C		0.61	0.76	V
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=16A, T_J=25°C		0.55	0.66	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		34	51	ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		54	81	nC

Notes

1. Guaranteed by design but not tested in production.
2. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 300kHz, L=210nH (0.2mΩ), VDRV=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, 400LFM airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss, driver loss and inductor loss are not included.
3. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VDRV=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, no airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss, driver loss and inductor loss are not included.

Q1 - Control FET

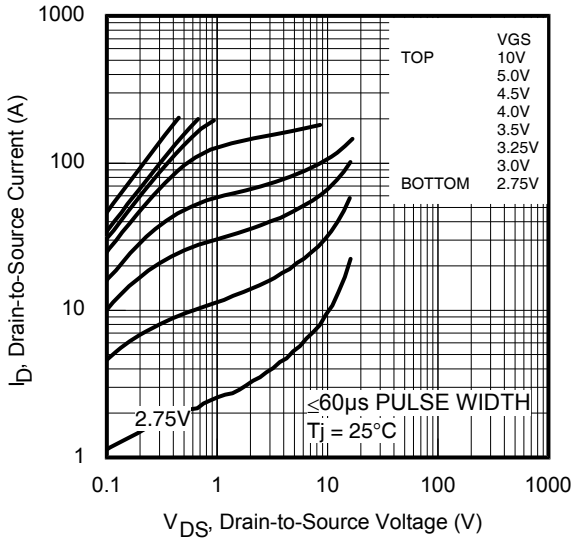


Fig 1. Typical Output Characteristics

Q2 - Synchronous FET

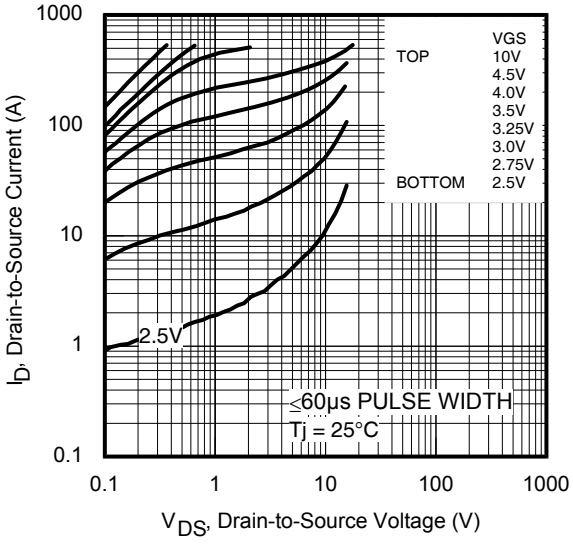


Fig 2. Typical Output Characteristics

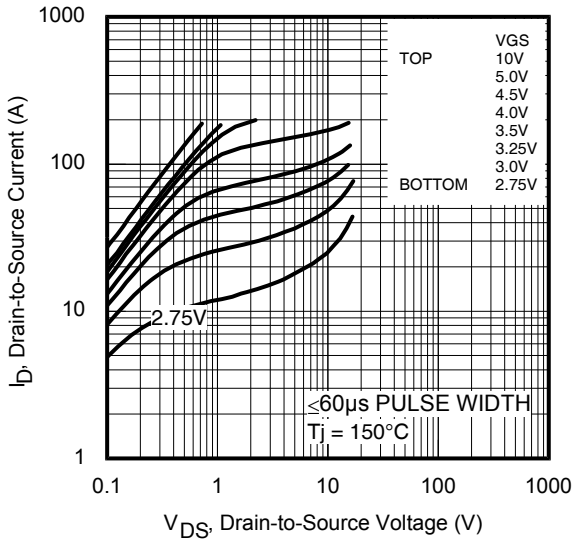


Fig 3. Typical Output Characteristics

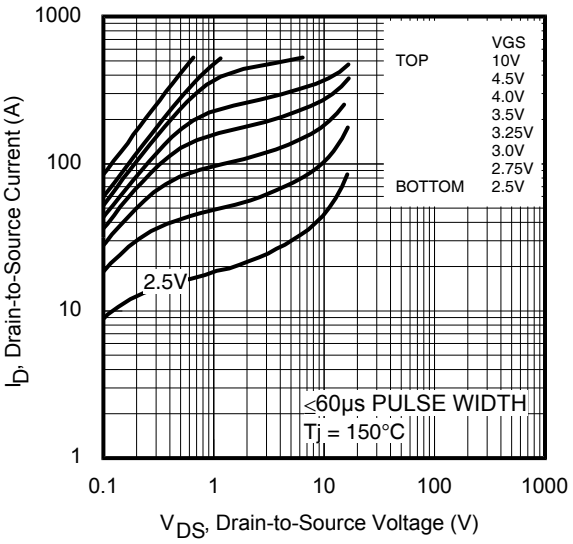


Fig 4. Typical Output Characteristics

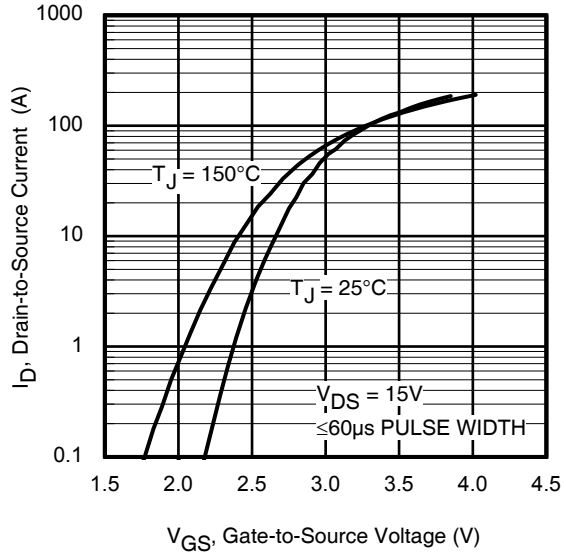


Fig 5. Typical Transfer Characteristics

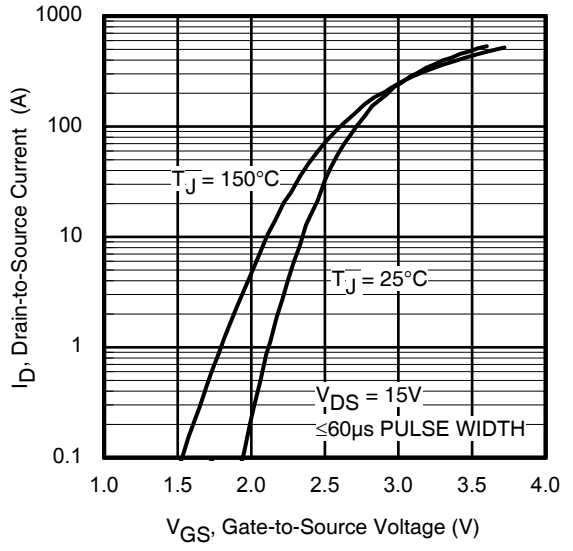


Fig 6. Typical Transfer Characteristics

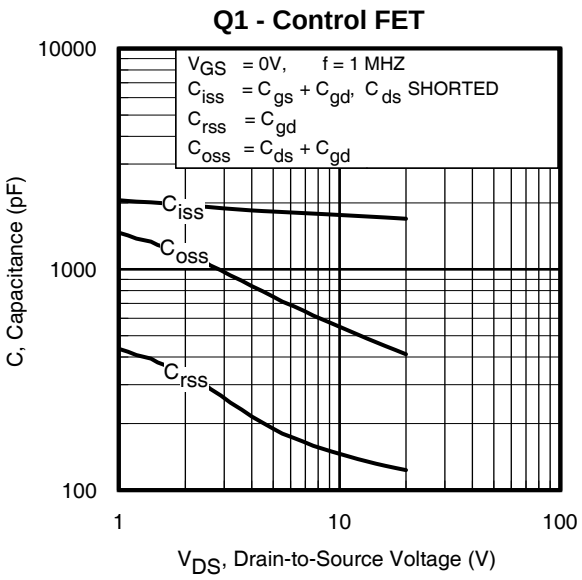


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

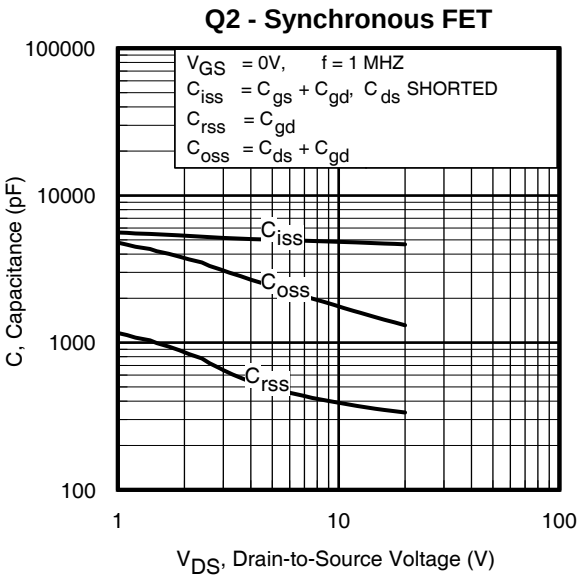


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

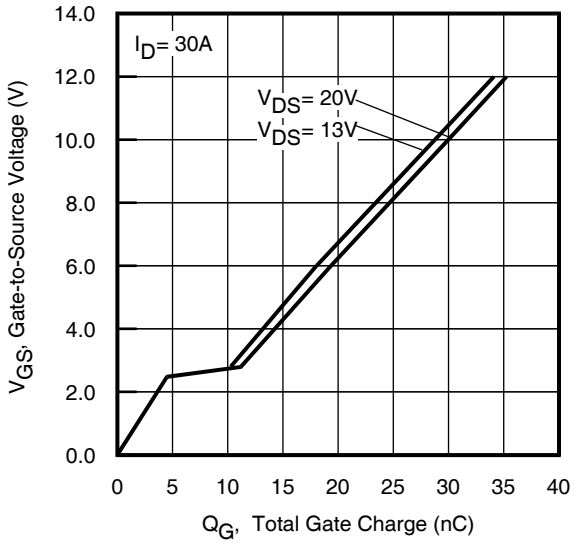


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

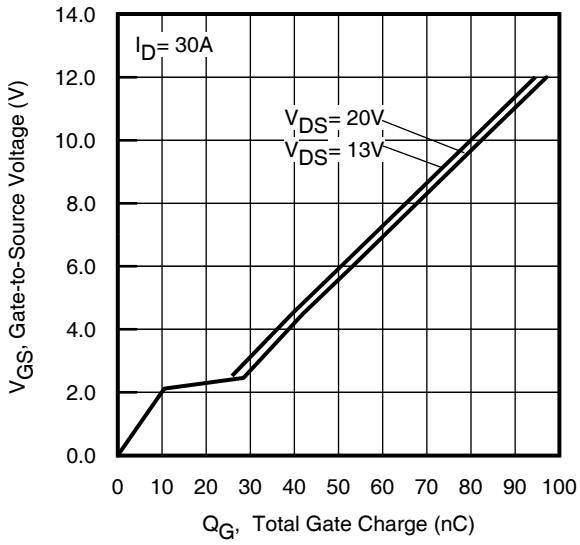


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

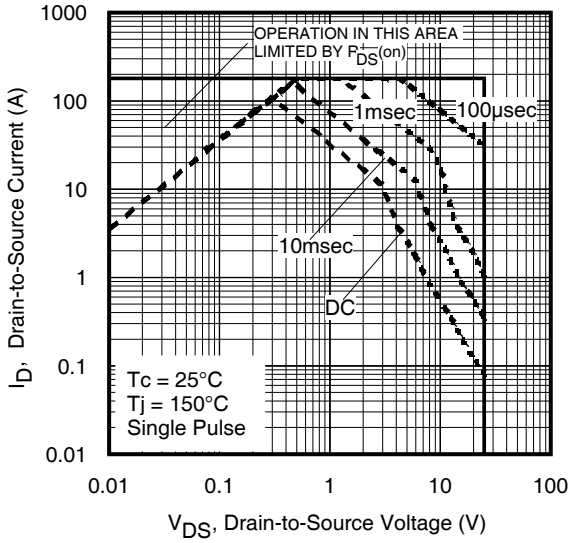


Fig 11. Maximum Safe Operating Area

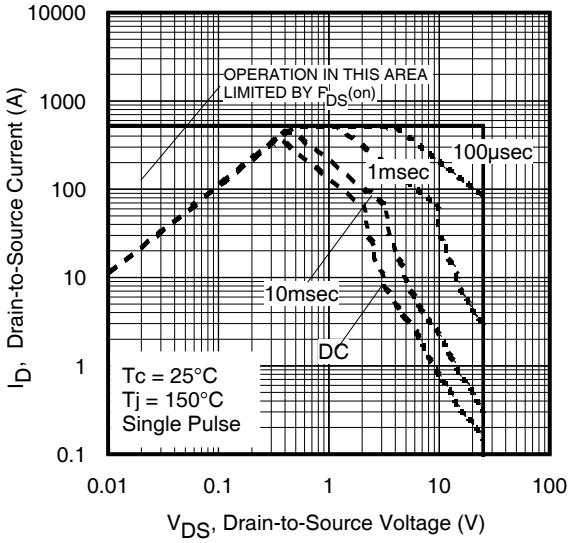


Fig 12. Maximum Safe Operating Area

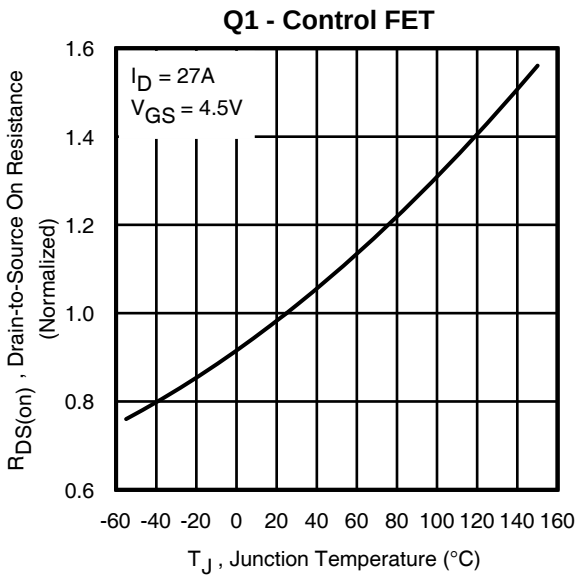


Fig 13. Normalized On-Resistance vs. Temperature

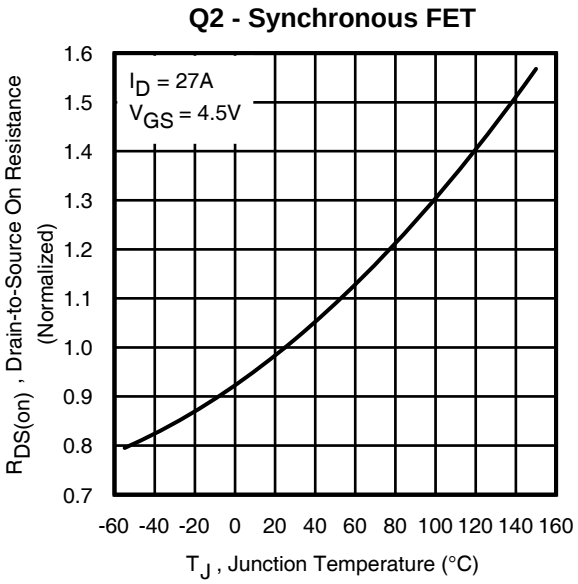


Fig 14. Normalized On-Resistance vs. Temperature

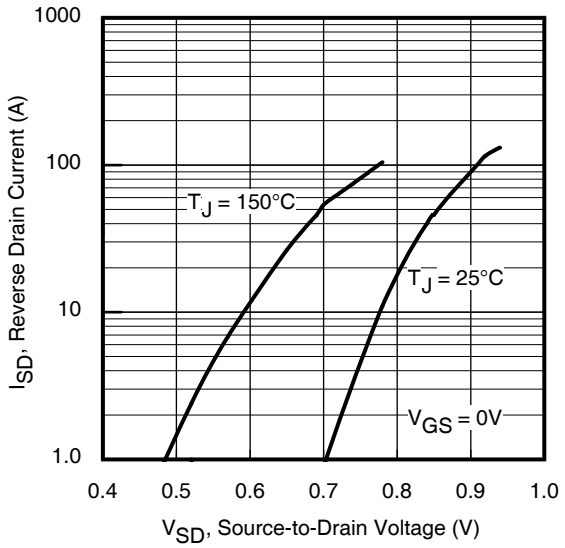


Fig 15. Typical Source-Drain Diode Forward Voltage

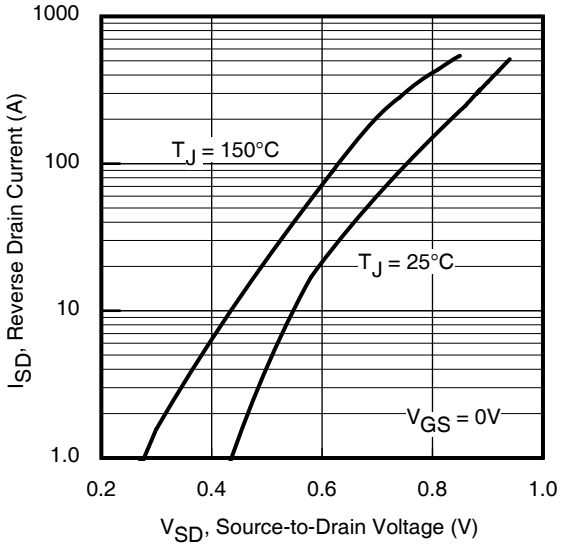


Fig 16. Typical Source-Drain Diode Forward Voltage

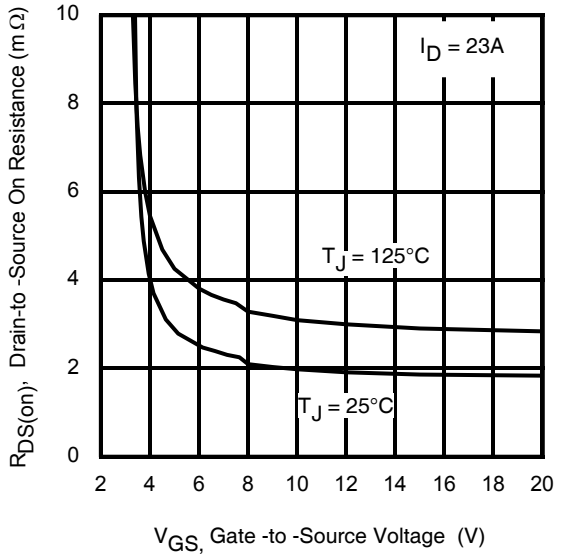


Fig 17. Typical On-Resistance vs. Gate Voltage

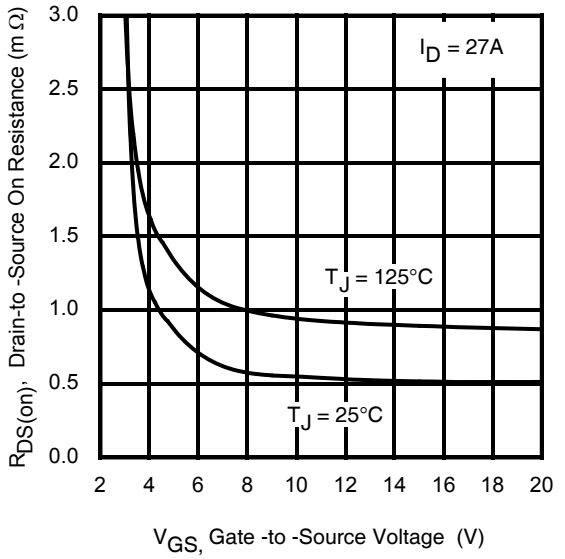


Fig 18. Typical On-Resistance vs. Gate Voltage

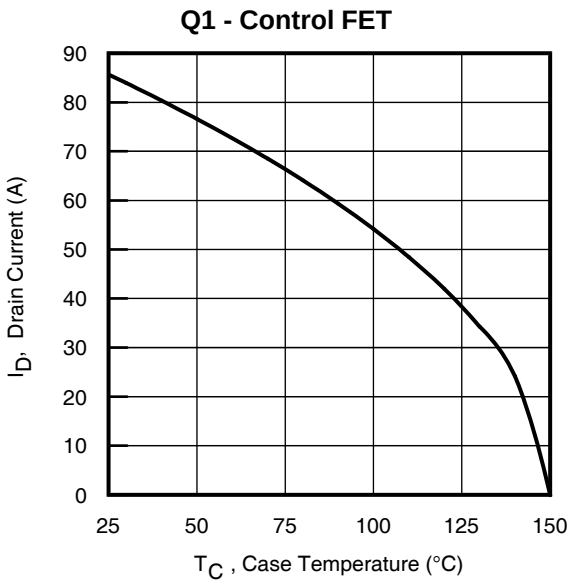


Fig 19. Maximum Drain Current vs. Case Temperature

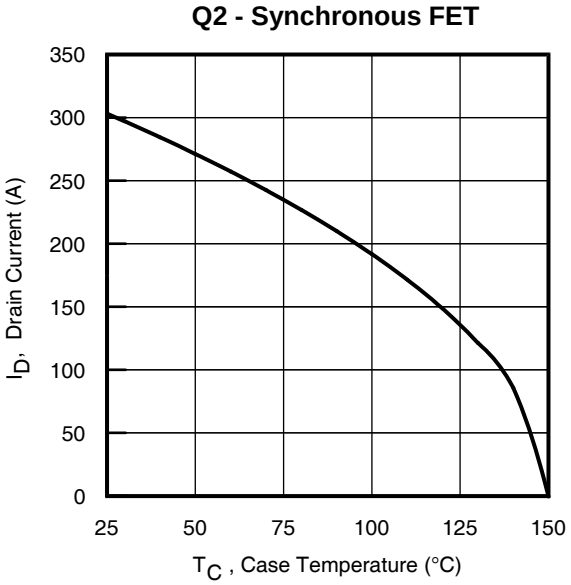


Fig 20. Maximum Drain Current vs. Case Temperature

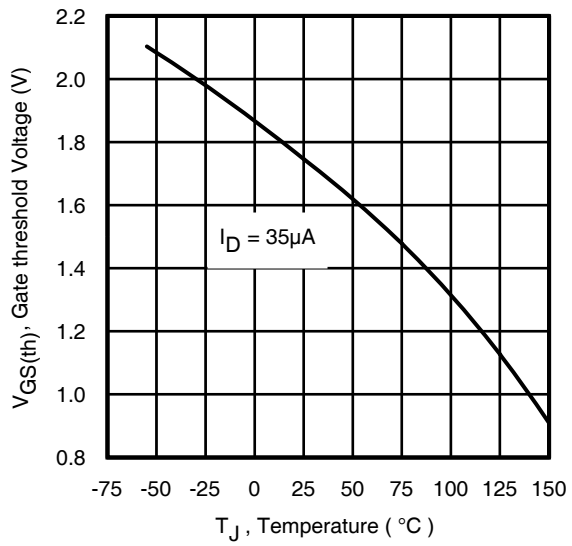


Fig 21. Threshold Voltage vs. Temperature

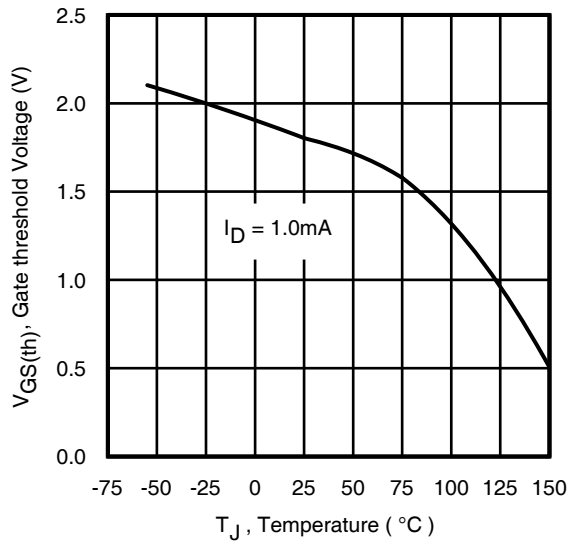


Fig 22. Threshold Voltage vs. Temperature

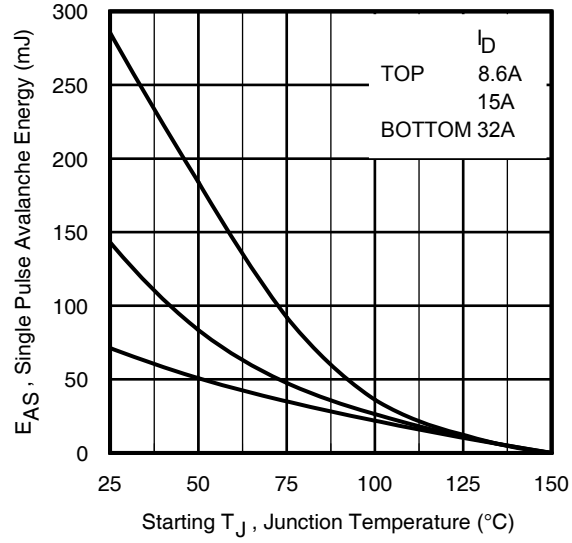


Fig 23. Maximum Avalanche Energy vs. Drain Current

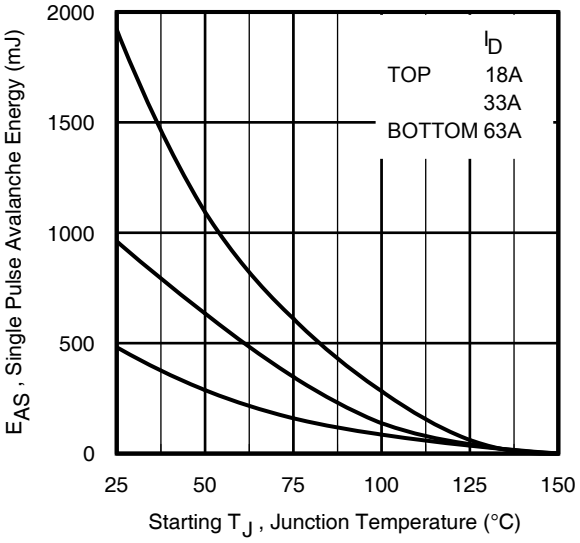


Fig 24. Maximum Avalanche Energy vs. Drain Current

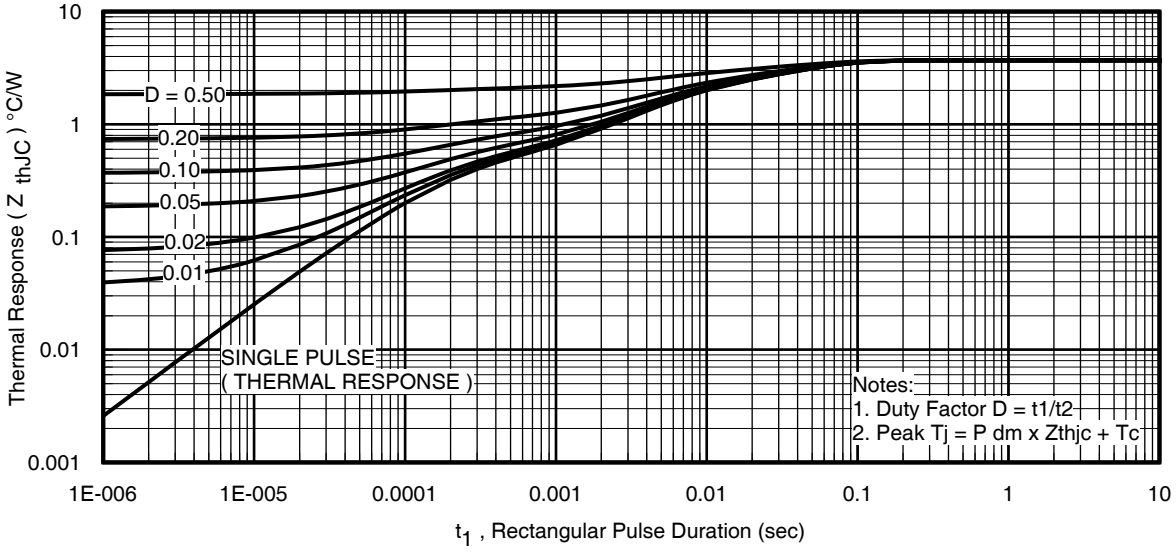


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)

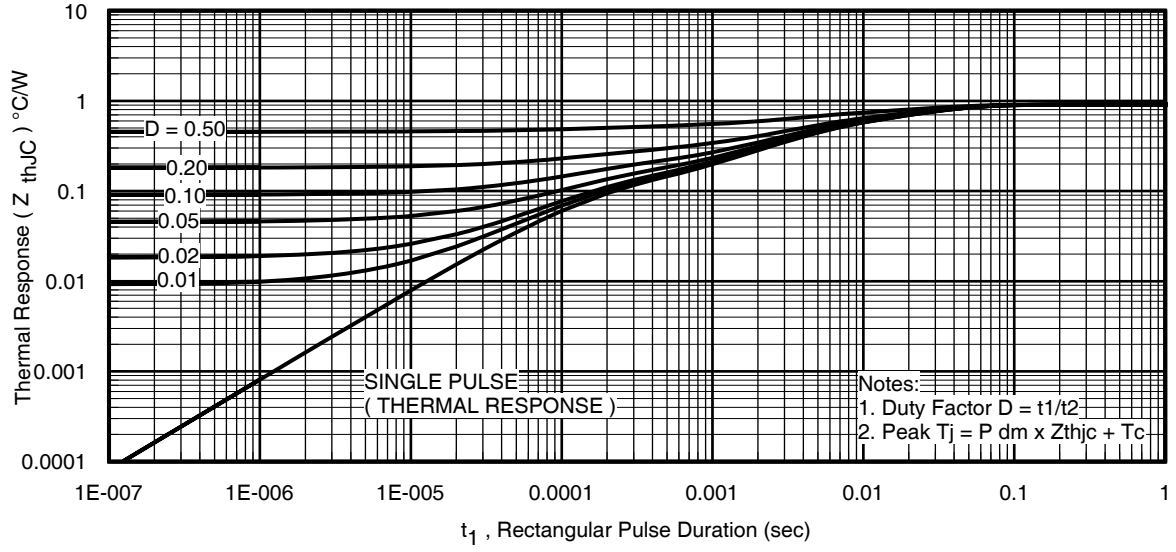


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)

MARKING INFORMATION

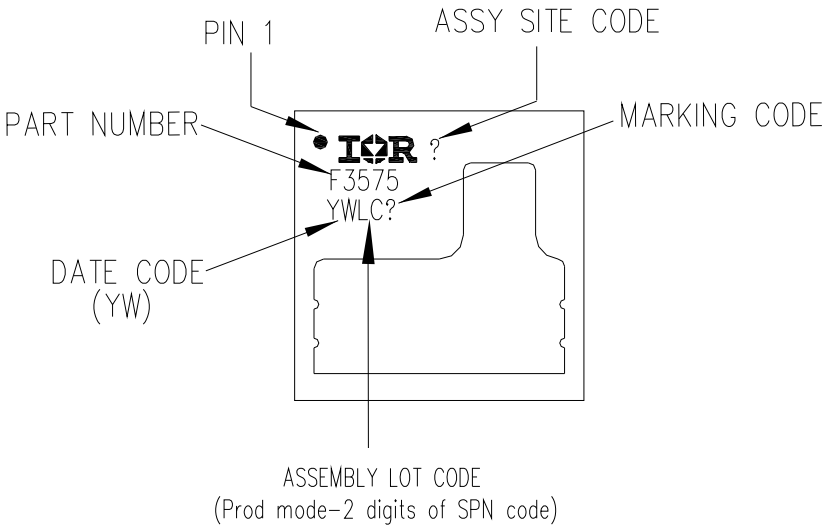
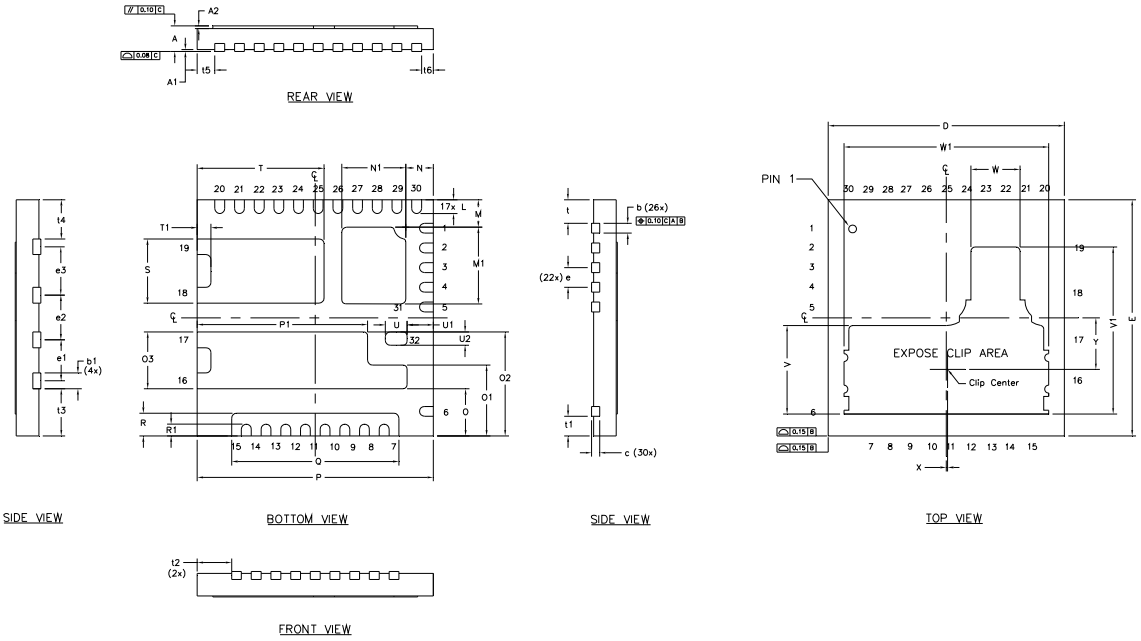


Figure 6: PQFN 6mm x 6mm

PACKAGE INFORMATION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.55	0.75	.0217	.0295
A1	0.000	0.050	.0000	.0020
A2	0.000	0.070	.0000	.0028
b	0.20	0.30	.0079	.0118
b1	0.350	0.450	.0138	.0177
c	0.203 REF.		.0080 REF.	
D	6.000 BASIC		.2362 BASIC	
E	6.000 BASIC		.2362 BASIC	
e	0.500 BASIC		.0197 BASIC	
e1	1.041 BASIC		.0410 BASIC	
e2	1.134 BASIC		.0446 BASIC	
e3	1.230 BASIC		.0484 BASIC	
t	0.600 BASIC		.0236 BASIC	
t1	0.500 BASIC		.0197 BASIC	
t2	0.875 BASIC		.0344 BASIC	
t3	1.200 BASIC		.0472 BASIC	
t4	0.996 BASIC		.0392 BASIC	
t5	0.450 BASIC		.0177 BASIC	
t6	0.300 BASIC		.0118 BASIC	
L	0.300	0.400	.0118	.0157
M	0.650	0.750	.0256	.0295
M1	1.896	1.996	.0747	.0786
N	0.650	0.750	.0256	.0296
N1	1.577	1.677	.0621	.0660

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
O	1.150	1.250	.0453	.0492
O1	1.750	1.850	.0689	.0728
O2	2.591	2.691	.1020	.1060
O3	1.391	1.491	.0548	.0587
P	5.281	5.381	.2079	.2119
P1	4.281	4.381	.1685	.1725
Q	4.200	4.300	.1654	.1693
R	0.525	0.625	.0207	.0246
R1	0.250	0.350	.0098	.0138
S	1.580	1.680	.0622	.0661
T	3.173	3.273	.1249	.1289
T1	0.300	0.400	.0118	.0157
U	0.500	0.600	.0197	.0236
U1	0.619	0.719	.0244	.0283
U2	0.287	0.387	.0130	.0152
V	2.147	2.347	.0845	.0924
V1	4.140	4.340	.1630	.1709
W	1.148	1.348	.0452	.0531
W1	5.100	5.300	.0200	.0208
X	0.1317	−0.0683	.0052	−0.0027
Y	1.207	1.407	.0475	.0554

Figure 6: PQFN 6mm x 6mm

GENERAL DESCRIPTION

The IRF3575DPbF contains integrated high and low side N-channel MOSFETs. It is suitable for high switching frequency up to 1MHz.

APPLICATION INFORMATION

SUPPLY DECOUPLING CAPACITOR

At least two 10uF 1206 ceramic capacitors and one 0.1uF 0402 ceramic capacitor are recommended for decoupling the VIN to PGND connection. The 0.1uF 0402 capacitor should be on the same side of the PCB as the IRF3546 and next to the VIN and PGND pins. Adding additional capacitance and use of capacitors with lower ESR and mounted with low inductance routing will improve efficiency and reduce overall system noise, especially in high current applications.

PCB LAYOUT CONSIDERATIONS

PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching.

- Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.
- Input supply decoupling and bootstrap capacitors should be physically located close to their respective IC pins.
- High current paths like the gate driver traces should be as wide and short as practically possible.
- GATEL interconnect trace inductances should be minimized to prevent Cdv/dt turn-on of the low side MOSFET.
- The ground connection of the IC should be as close as possible to the low-side MOSFET source.
- Use of a copper plane under and around the IC and thermal vias to connect to buried copper layers improves the thermal performance substantially.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length +0.15 - 0.3 mm outboard extension and 0 to + 0.05mm inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only 0.30mm diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect on the IC and to improve thermal performance.

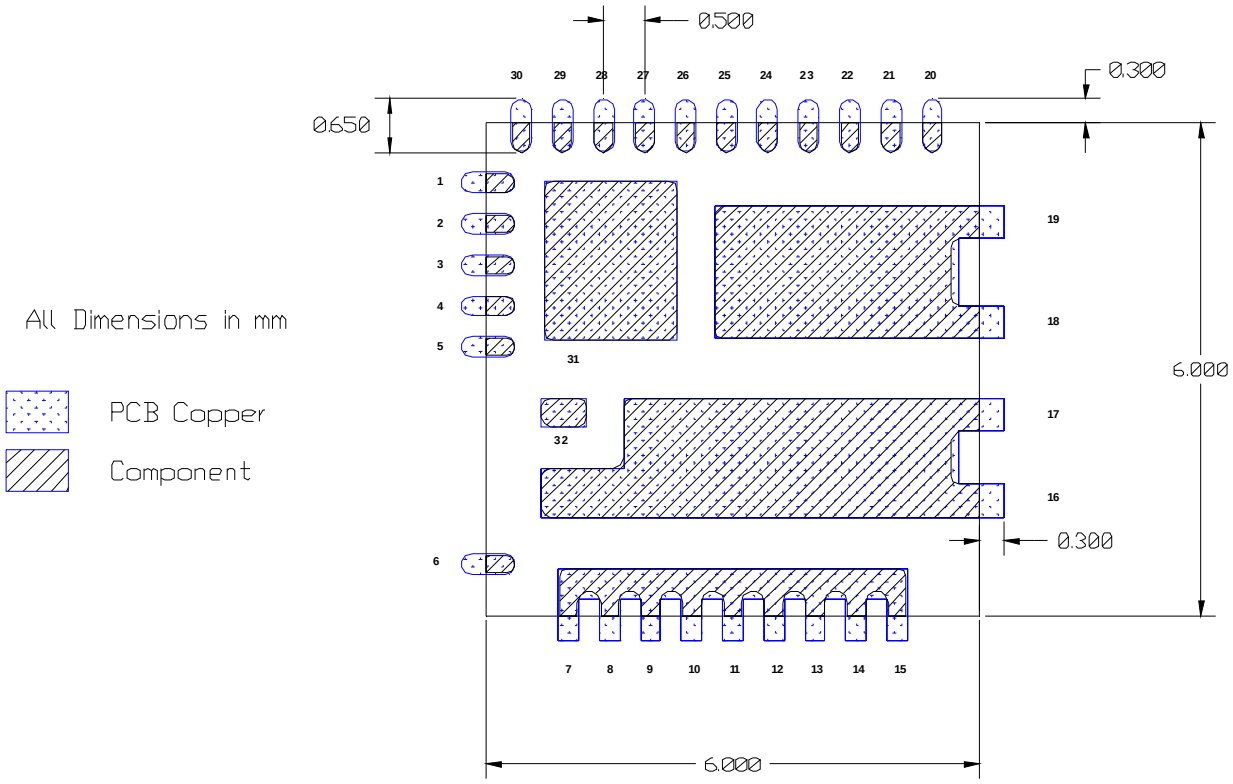


Figure 3: Metal and component placement

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm typical.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The power land pads VIN, PGND and SW should be Solder Mask Defined (SMD).
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

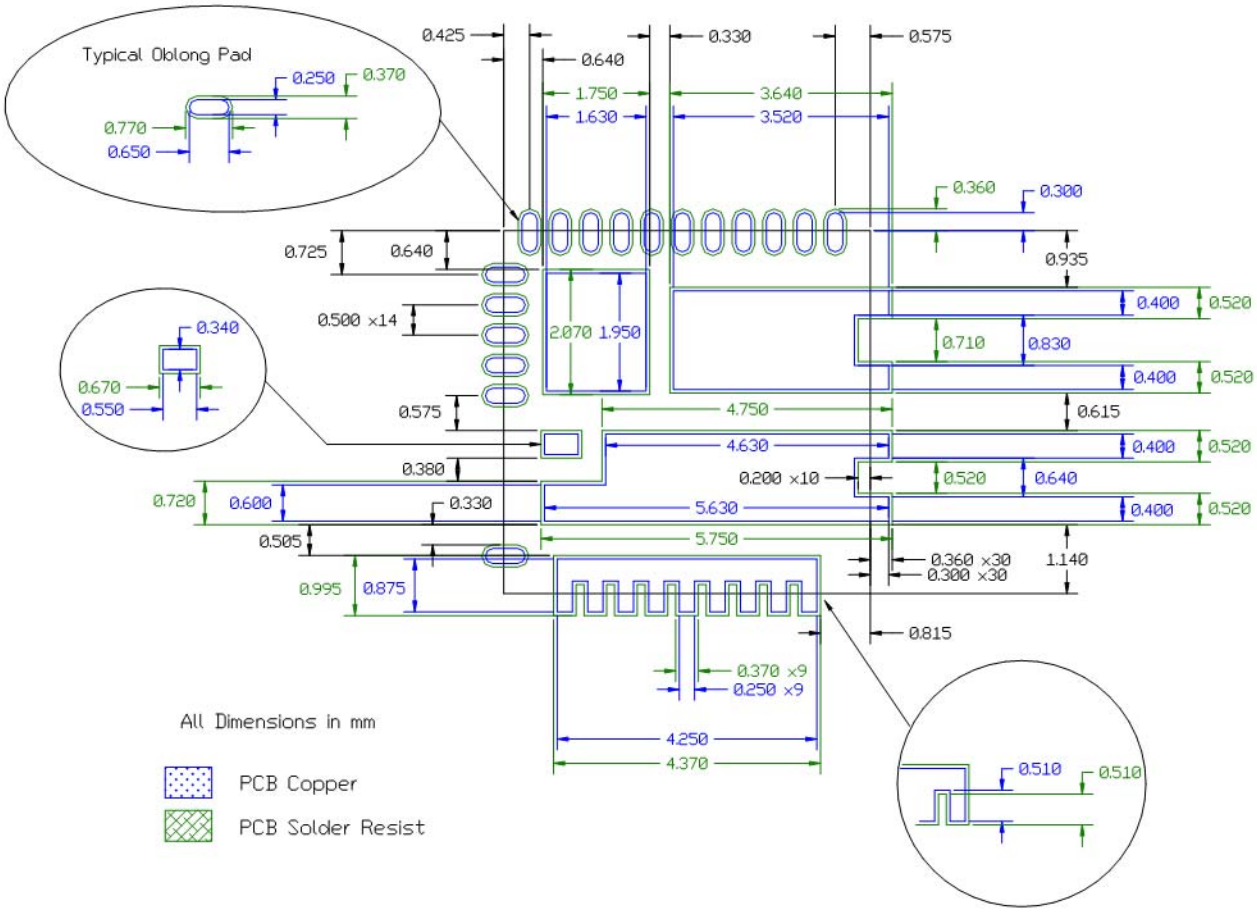


Figure 4: Solder resist

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN, PGND and SW, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

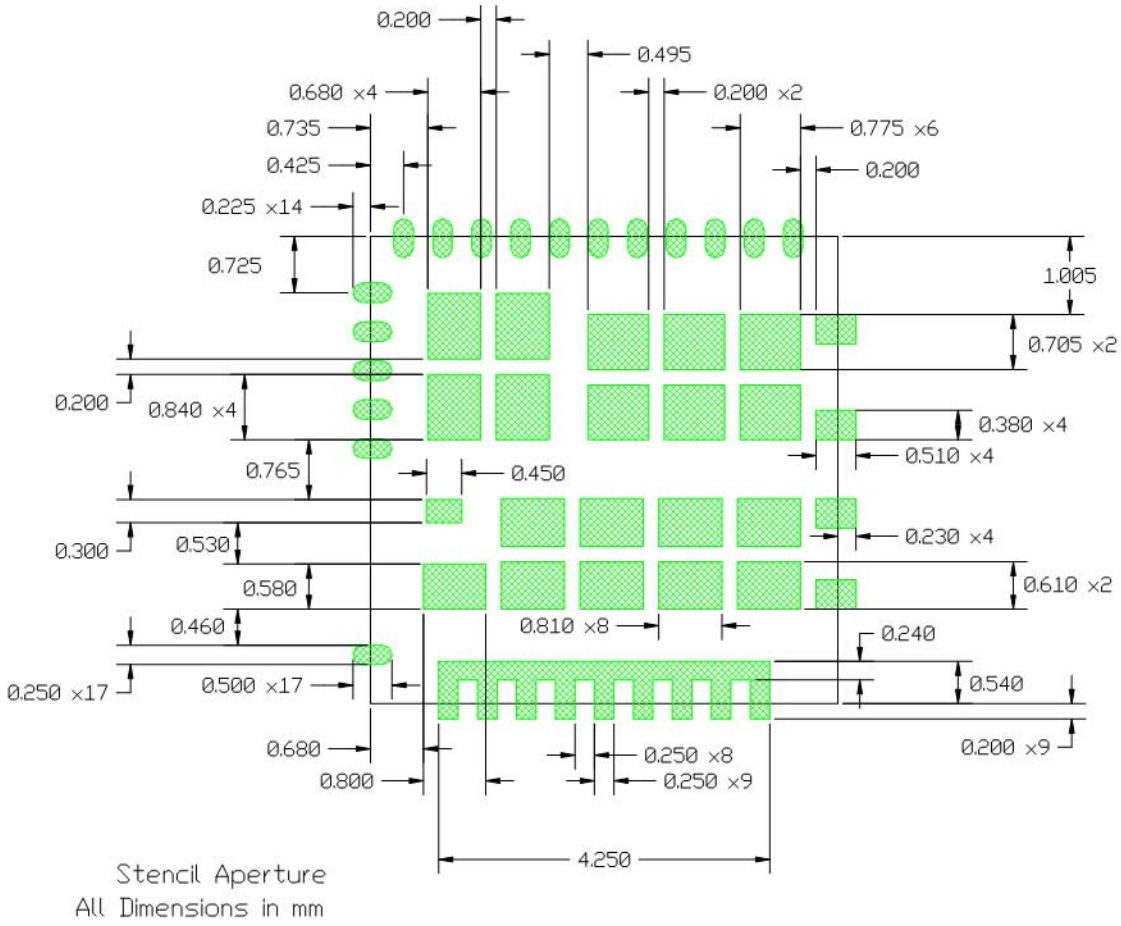


Figure 5: Stencil Design

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

Qualification Information†

Qualification level	Industrial (per JEDEC JESD47F †† guidelines)	
Moisture Sensitivity Level	DUAL PQFN 6mm x 6mm	MSL3 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

International
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To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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