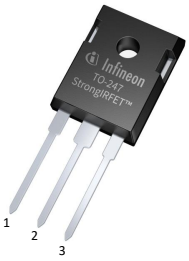
MOSFET

StrongIRFET™

PG-TO247-3



Features

- Very low $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ (FOM)
- Optimized Q_{rr}
- 175°C operating temperature
- Product validation according to JEDEC standard
- Optimized for broadest availability from distribution partners

Benefits

- Reduced conduction losses
- Ideal for high switching frequency
- Lower overshoot voltage
- Increased reliability versus 150°C rated parts
- Halogen-free according to IEC61249-2-21

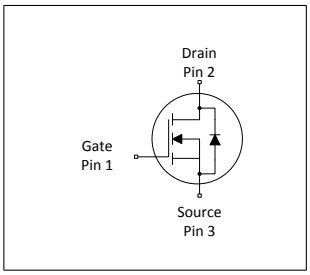


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),typ}$	3.6	mΩ
$R_{DS(on),max}$	4.5	mΩ
$I_{D(Silicon\ Limited)}$	186	A
Q_G(0V..10V)	80	nC

Type / Ordering Code	Package	Marking	Related Links
IRF150P221	PG-TO247-3	IRF150P221	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	186 132	A	V_{GS}=10 V, T_C=25 °C (silicon limited) V_{GS}=10 V, T_C=100 °C (silicon limited)[1]
Pulsed drain current[1]	$I_{D,pulse}$	-	-	507	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	420	mJ	I_D=100 A, R_{GS}=50 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	341 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W[3]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case[4]	R_{thJC}	-	-	0.44	°C/W	-
Thermal resistance, junction -Ambient	R_{thJA}	-	-	40	°C/W	-
Case-to-Sink, Flat Greased Surface	R_{thCS}	-	0.24	-	°C/W	-

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[4] R_{thJC} is measured at T_J approximately 90°C.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	60	-	mV/°C	I_D=2 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	3	-	4.6	V	V_{DS}=V_{GS}, I_D=264 µA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	3.6	4.5	mΩ	V_{GS}=10 V, I_D=100 A
Gate resistance[1]	R_G	-	1.1	-	Ω	-
Transconductance	g_{fs}	-	150	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	6000	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	1500	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	34	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=2.7 Ω
Rise time	t_r	-	90	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=2.7 Ω
Turn-off delay time	$t_{d(off)}$	-	29	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=2.7 Ω
Fall time	t_f	-	62	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=2.7 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	35	-	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	23	-	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	16	-	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	28	-	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	80	100	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	64	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[2]	Q_{oss}	-	225	-	nC	V_{DD}=75 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

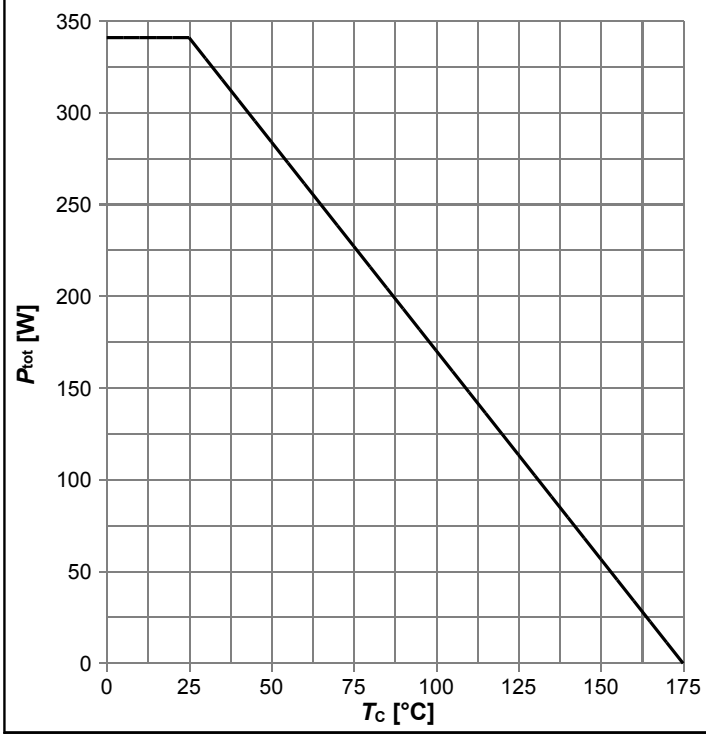
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	186	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	507	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-	1.1	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	57	-	ns	V_R=128 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	74	-	nC	V_R=128 V, I_F=100 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

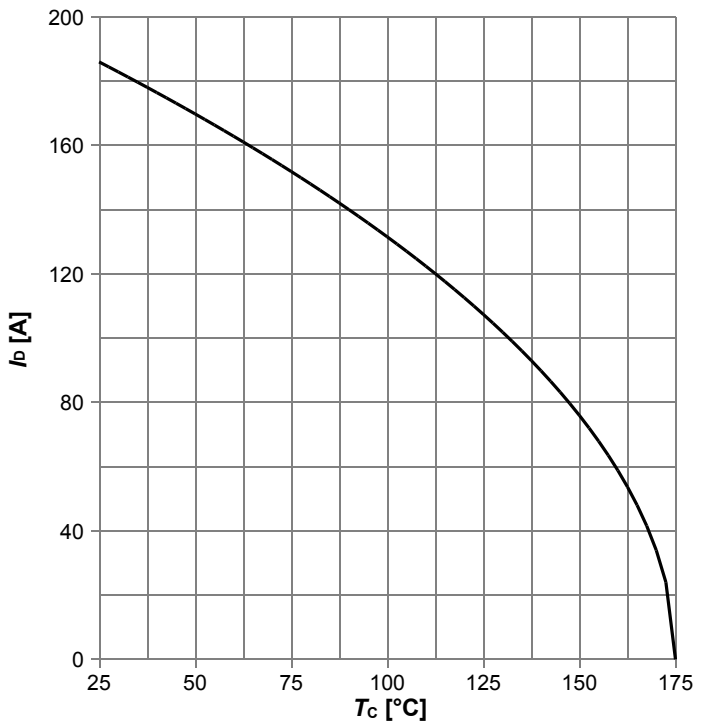
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



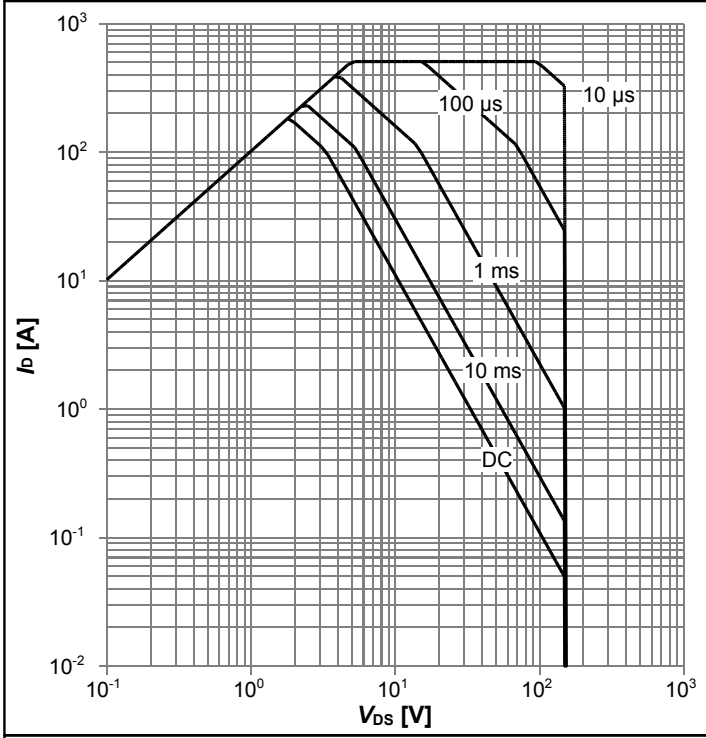
$P_{tot}=f(T_C)$

Diagram 2: Drain current



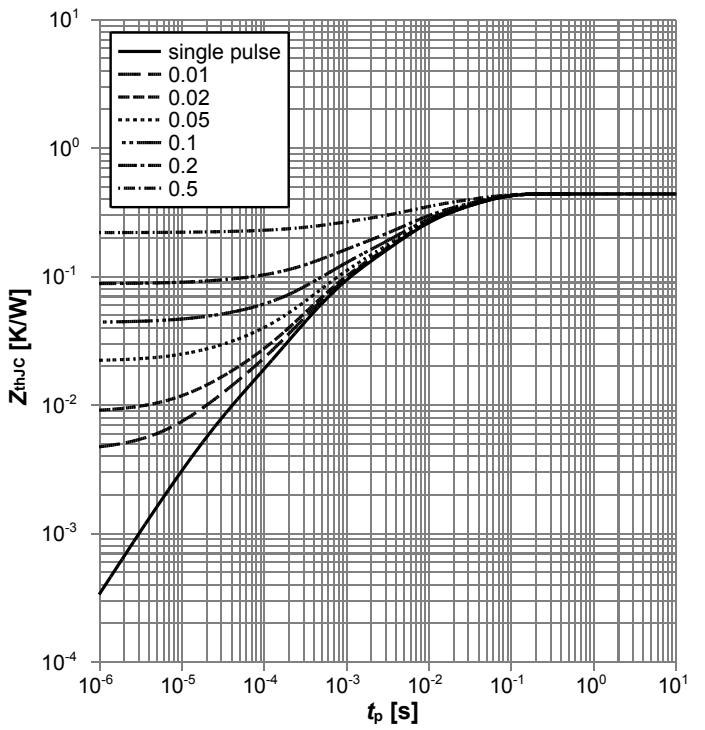
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



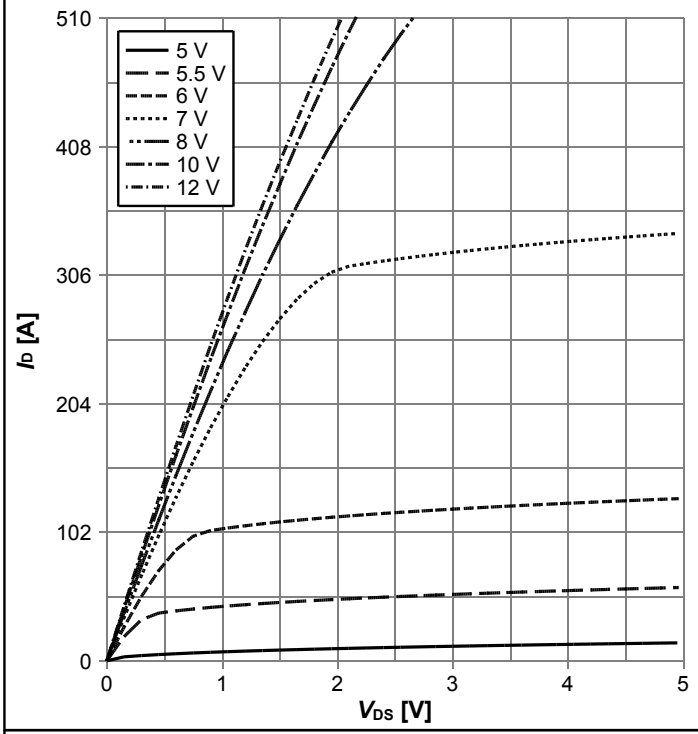
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



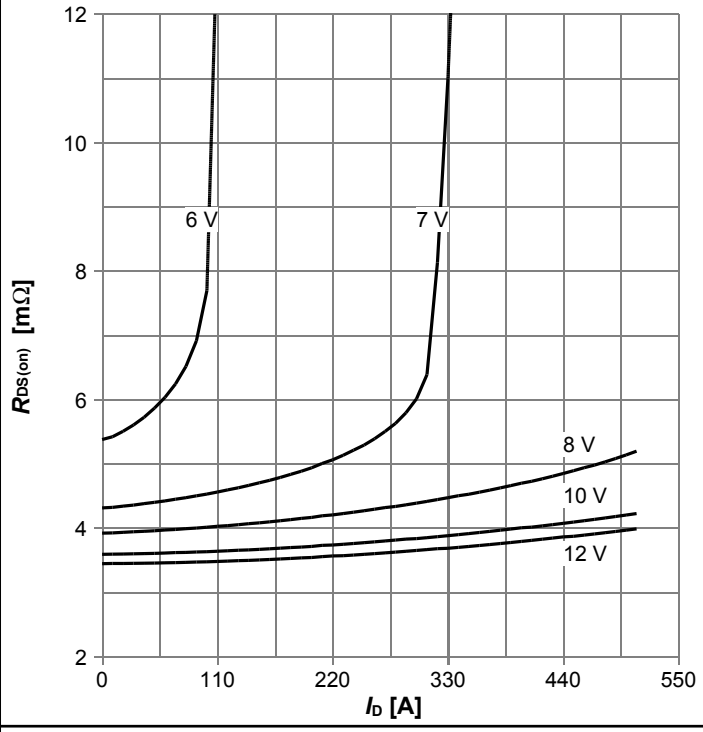
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



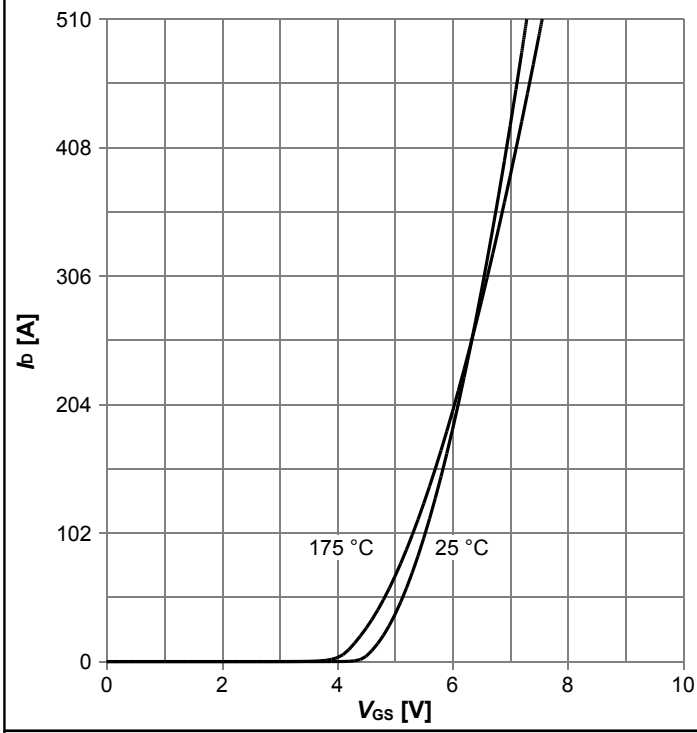
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



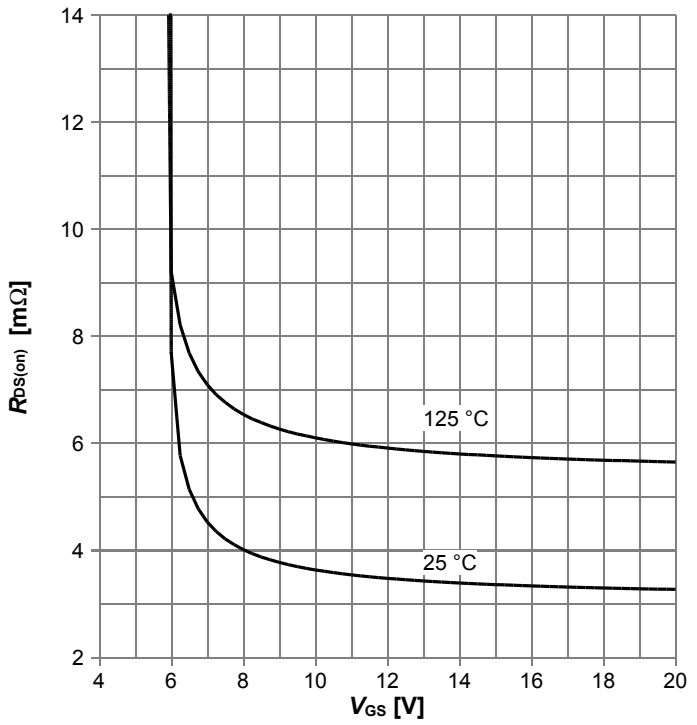
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



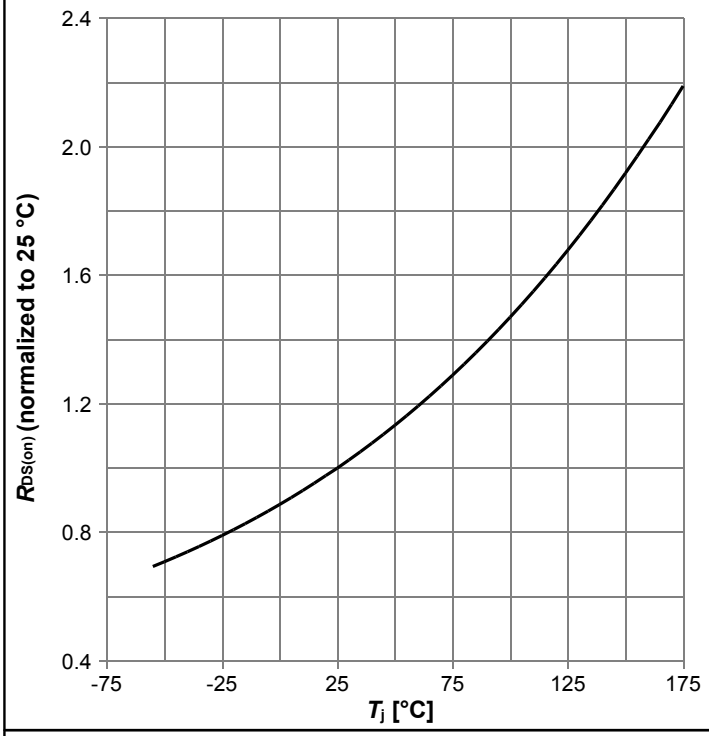
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



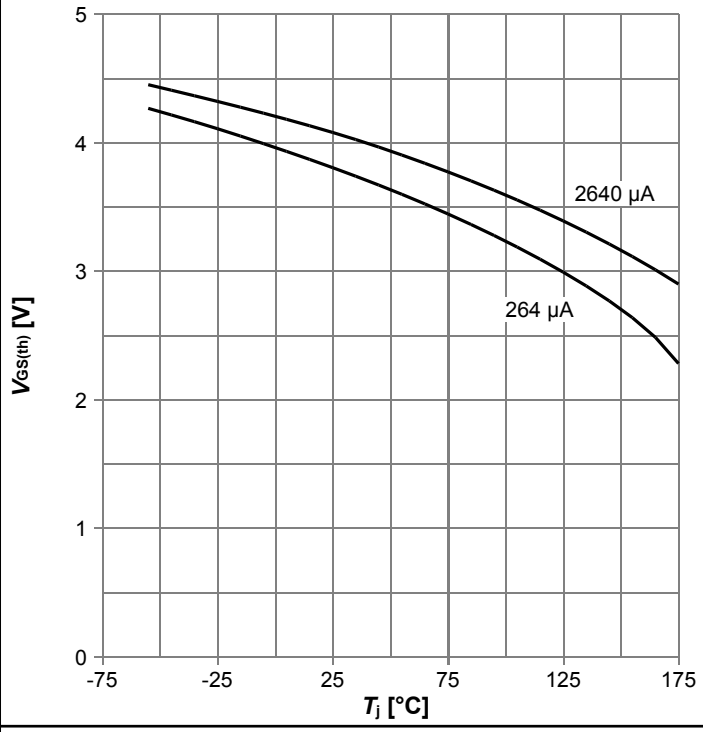
$R_{DS(on)}=f(V_{GS})$, $I_D=100$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



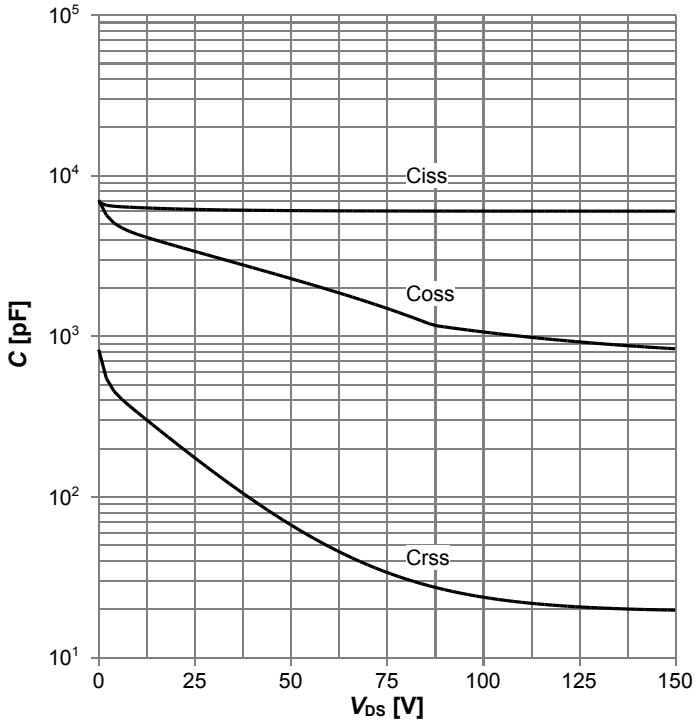
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



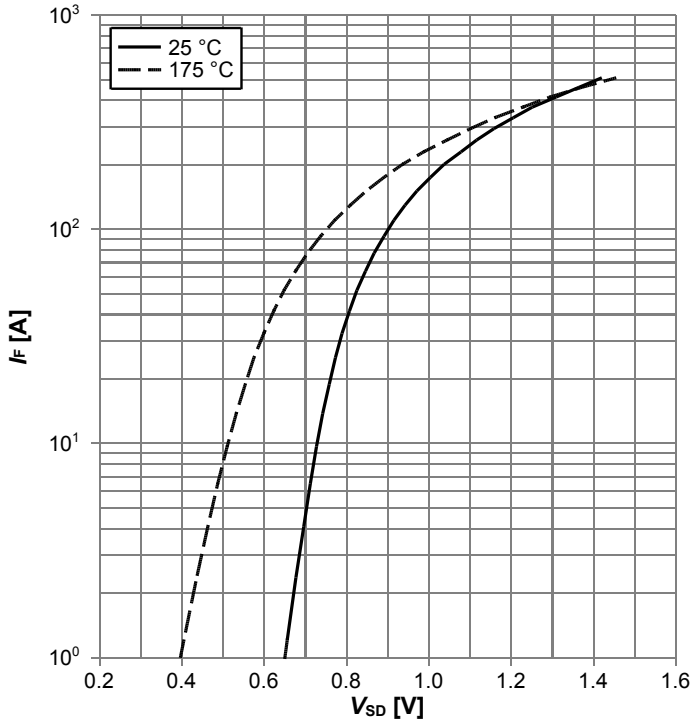
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



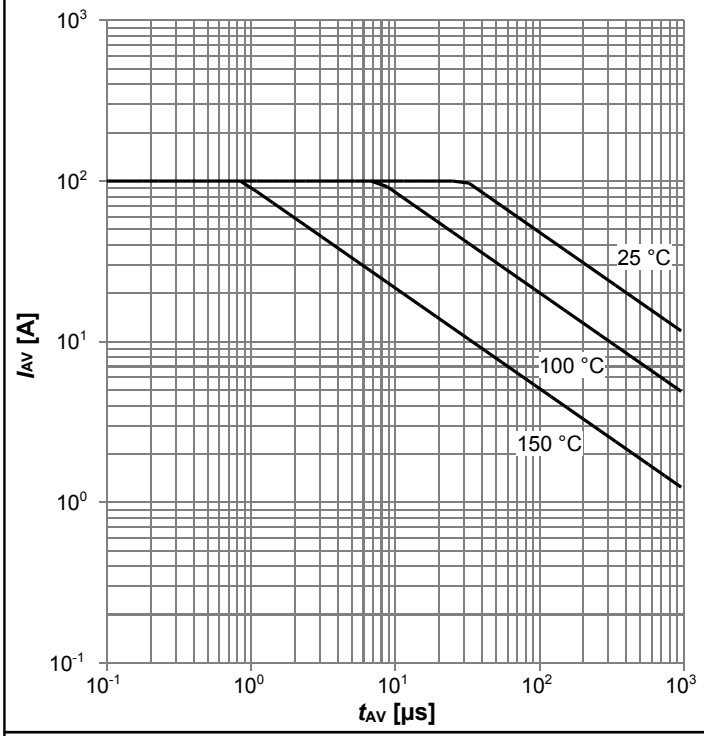
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



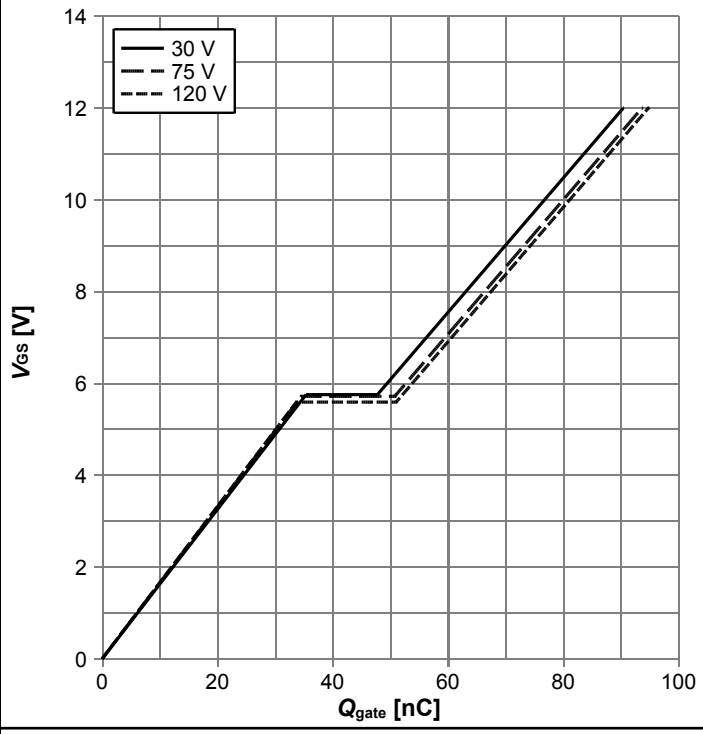
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



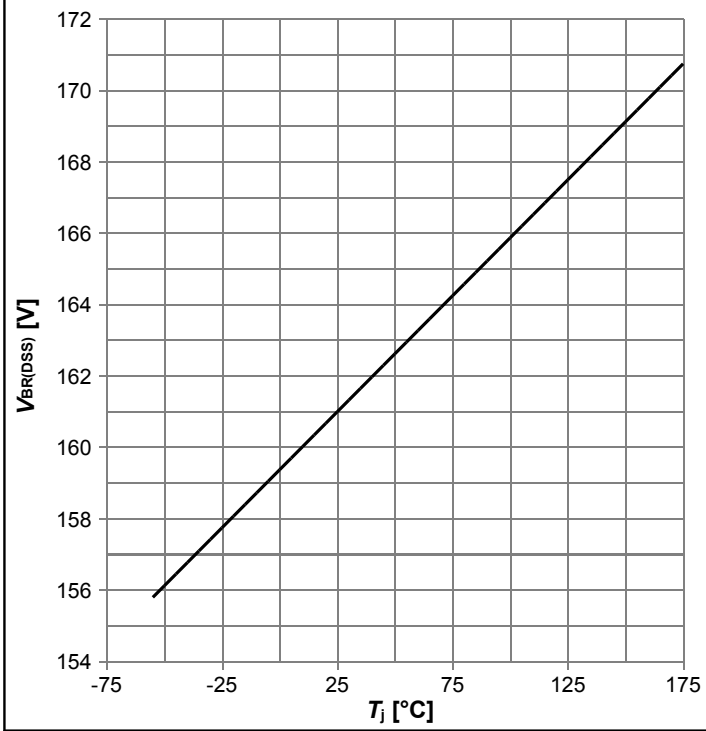
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



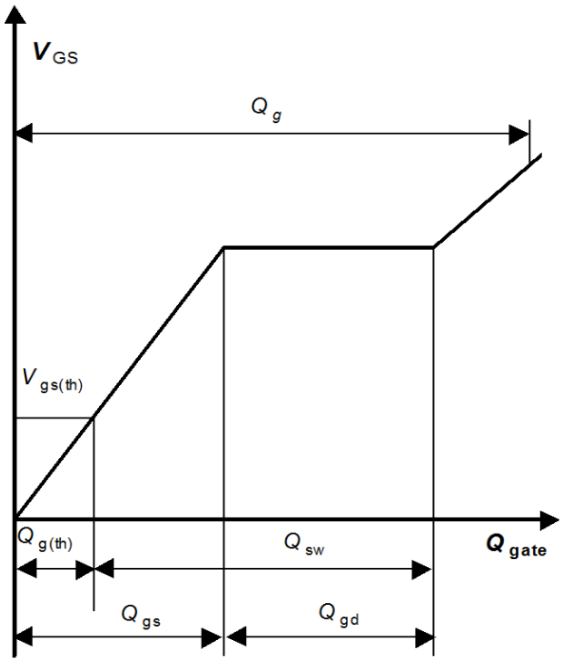
$V_{GS}=f(Q_{gate})$, $I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

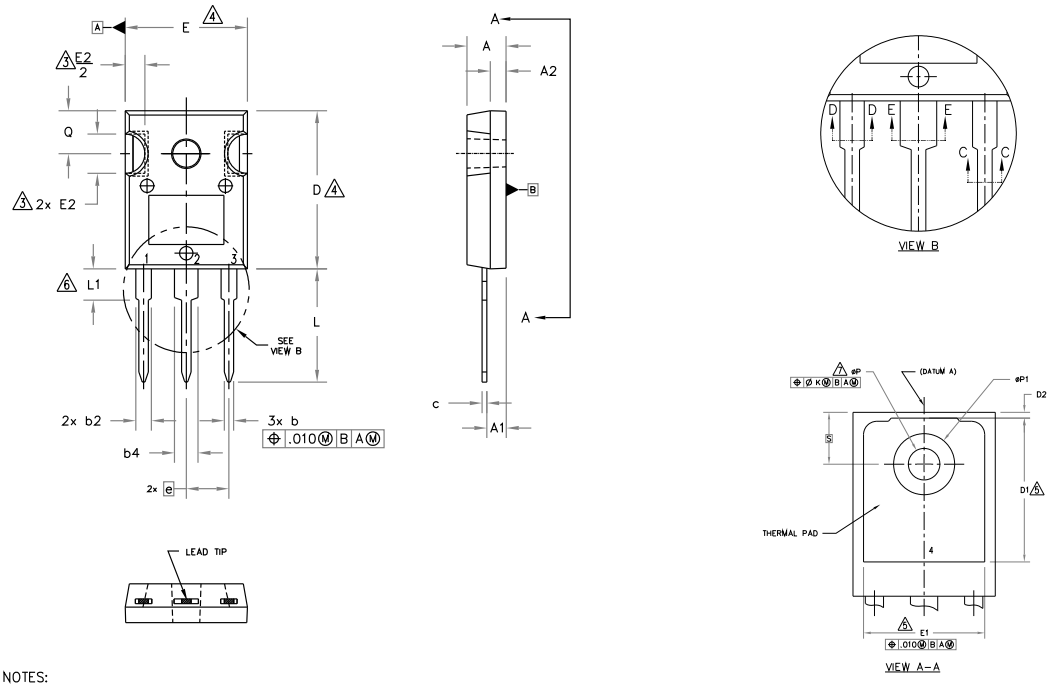


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms

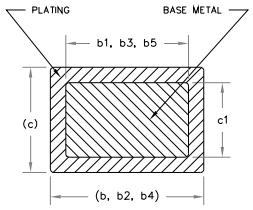


5 Package Outlines



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .



SECTION C–C, D–D, E–E

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

Figure 1 Outline PG-TO247-3, dimensions in mm/inches

Revision History

IRF150P221

Revision: 2023-04-14, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2018-09-21	Release of final version
2.1	2020-02-03	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™
2.2	2023-04-14	Update SOA diagram

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.
In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.
The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:
IRF150P221AKMA1