

MOSFET

OptiMOS™ 5, 150 V

Features

- Lead free, ultra thin double sided cooling package
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on -resistance $R_{DS(on)}$
- N-channel normal level
- 100% avalanche tested

Applications

- Brushed Motor drive, Synchronous rectifier and BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Product validation

Fully qualified according to JEDEC for Industrial Applications

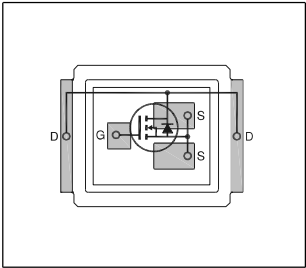
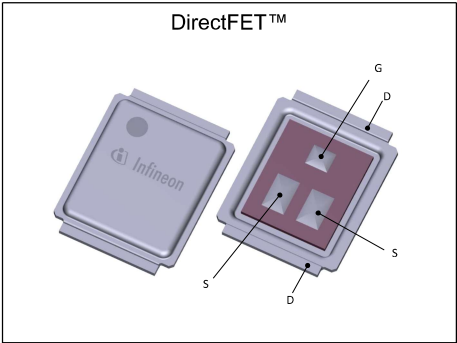


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	11.3	mΩ
I_D	60	A
Q_{oss}	87	nC
$Q_G(0V..10V)$	33	nC

Type / Ordering Code	Package	Marking	Related Links
IRF150DM115	MG-WDSO5-5	M115	-

Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 3

Electrical characteristics 4

Electrical characteristics diagrams 6

Test Circuits 10

Package Outlines 11

Revision History 14

Trademarks 14

Disclaimer 14

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	60 38 11	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=45\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	240	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	72	mJ	$I_D=45\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	78 2.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=45\text{ °C/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-40	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - ambient, double sided cooling	$R_{thJA}^{5)}$	-	12.5	-	°C/W	-
Thermal resistance, junction - ambient, mounted on minimum foot print	$R_{thJA}^{6)}$	-	20	-	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}^{2)}$	-	-	45	°C/W	-
Device on PCB	$R_{thJ-PCB}$	-	0.75	-	°C/W	-
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL3

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

⁵⁾ Used double sided cooling, mounting pad with large heat sink

⁶⁾ Mounted on minimum footprint full size board with metalized back with small clip heat sink

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3	3.8	4.6	V	$V_{DS}=V_{GS}$, $I_D=106\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	8.5	11.3	m Ω	$V_{GS}=10\text{ V}$, $I_D=45\text{ A}$
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance ¹⁾	g_{fs}	33	66	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=45\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	2300	3000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	580	780	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	41	70	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=45\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	21	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=45\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=45\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	14	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=45\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	13.2	-	nC	$V_{DD}=75\text{ V}$, $I_D=45\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	8.7	-	nC	$V_{DD}=75\text{ V}$, $I_D=45\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	8.0	12	nC	$V_{DD}=75\text{ V}$, $I_D=45\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	12.5	-	nC	$V_{DD}=75\text{ V}$, $I_D=45\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	33	50	nC	$V_{DD}=75\text{ V}$, $I_D=45\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=75\text{ V}$, $I_D=45\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	87	115	nC	$V_{DS}=75\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	60	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	240	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=45\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	39	78	ns	$V_R=75\text{ V}$, $I_F=45\text{ A}$, $di_F/dt=100\text{ A/}\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	47	94	nC	$V_R=75\text{ V}$, $I_F=45\text{ A}$, $di_F/dt=100\text{ A/}\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

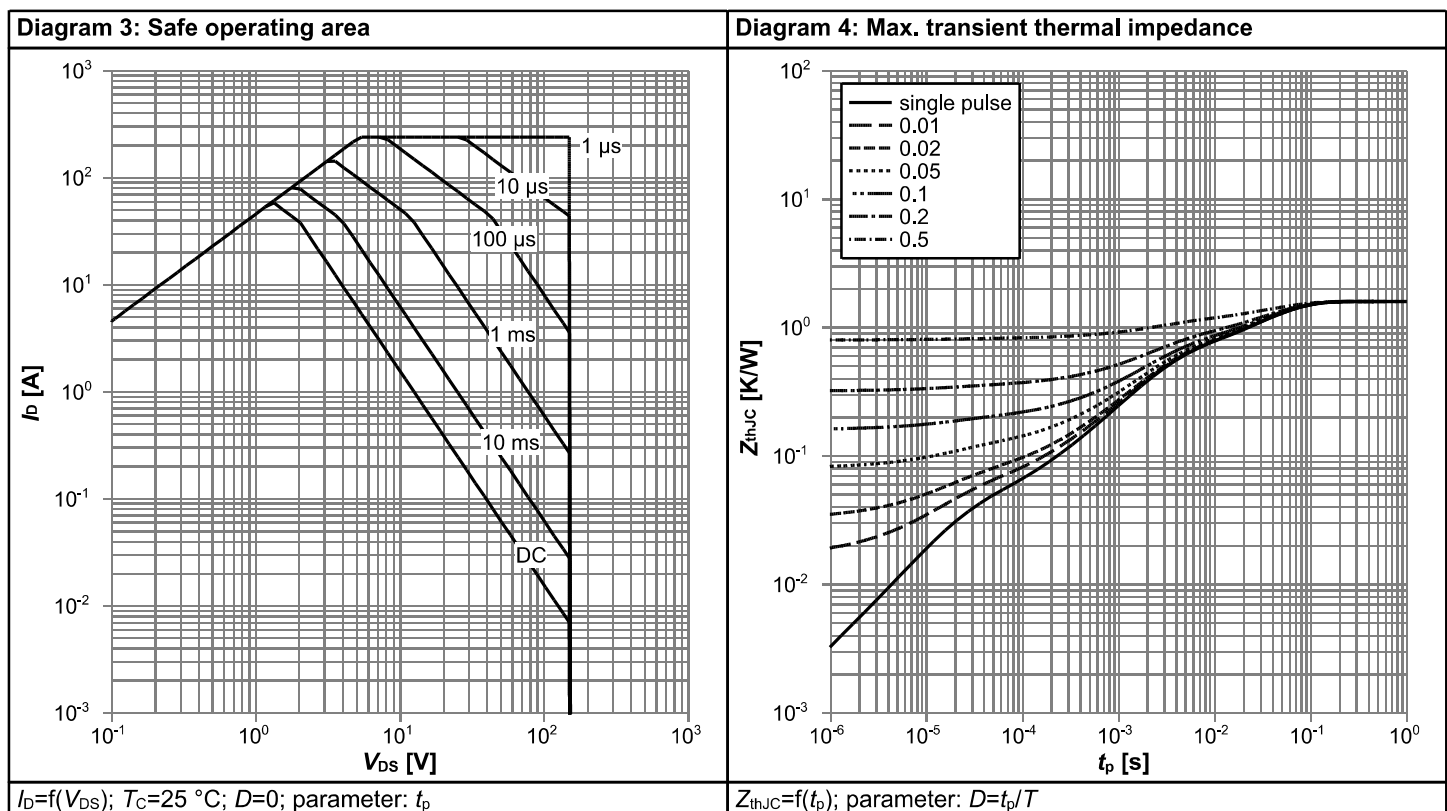
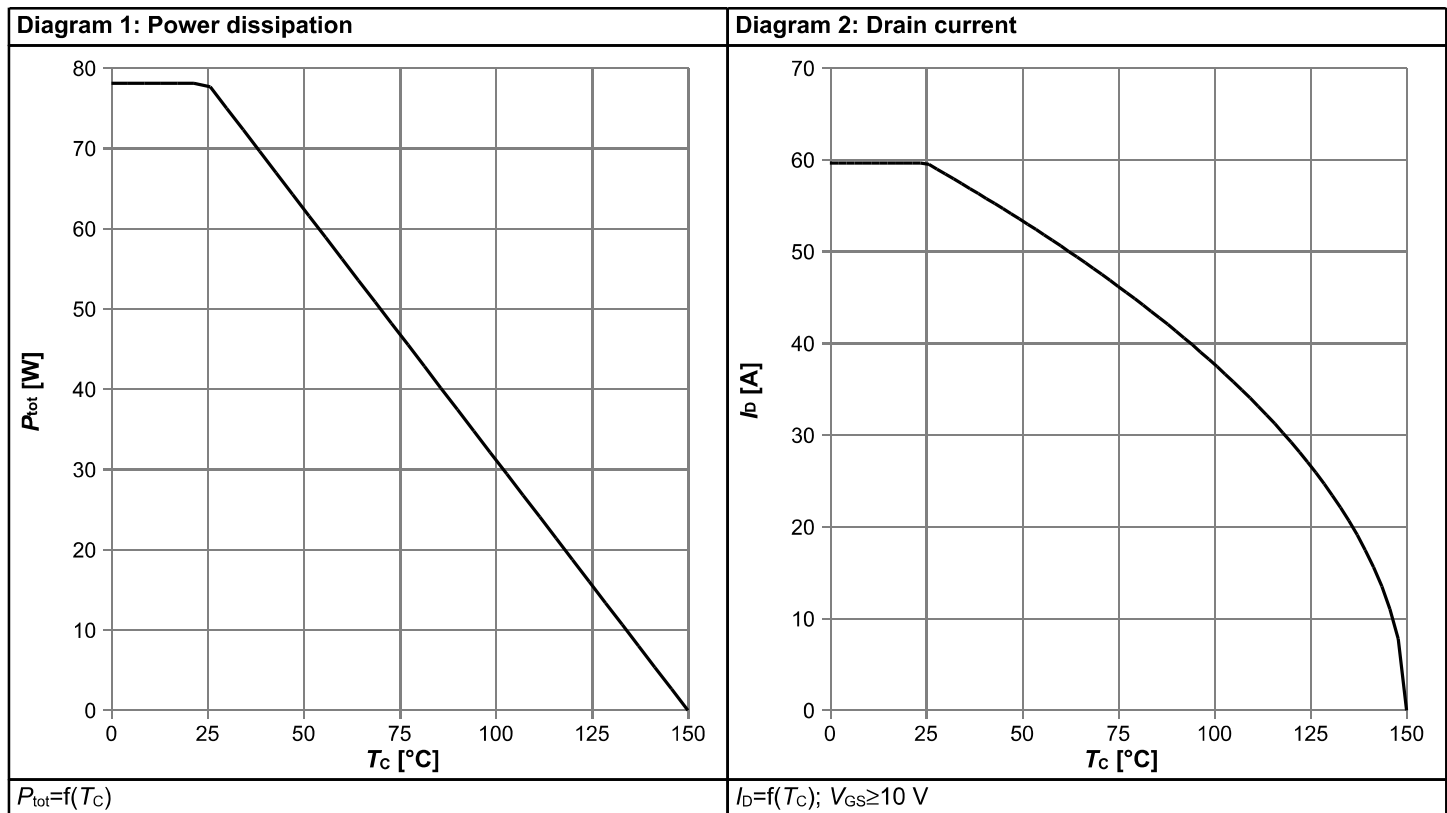
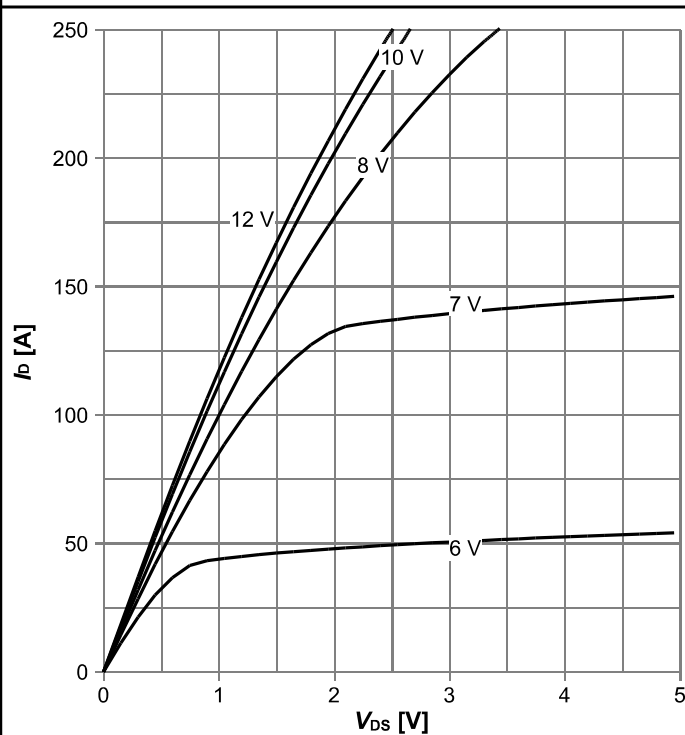
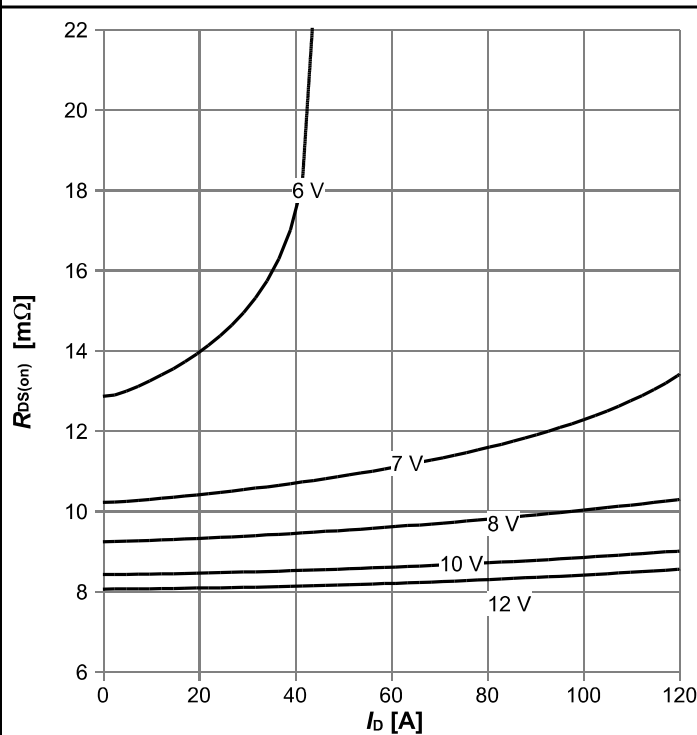


Diagram 5: Typ. output characteristics



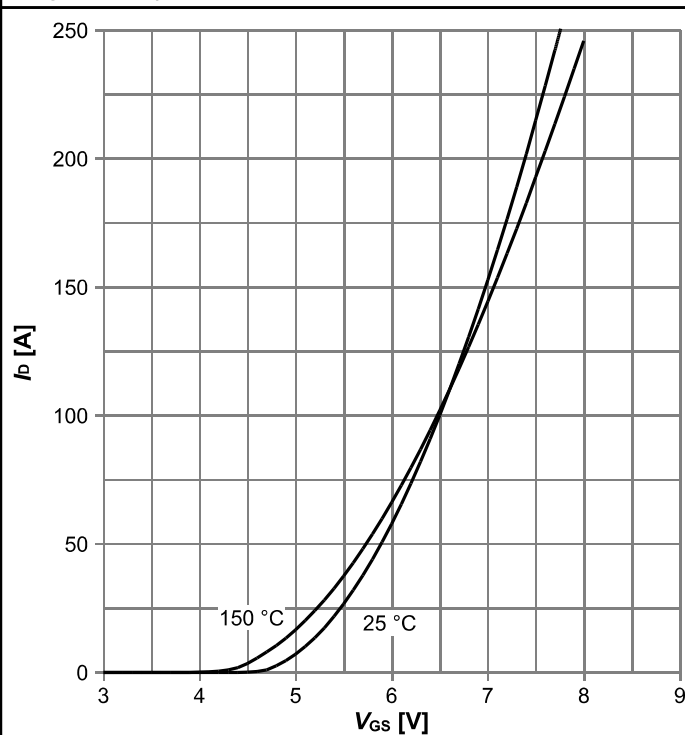
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



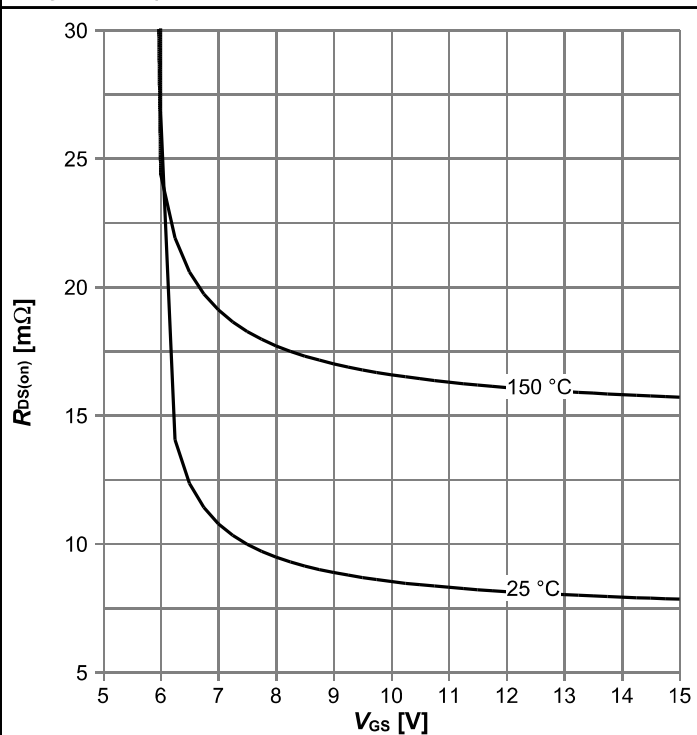
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



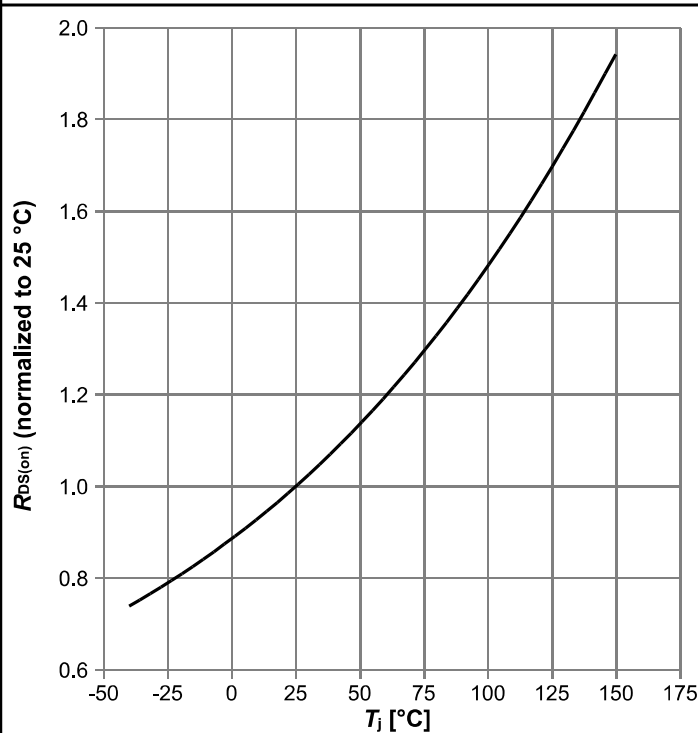
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



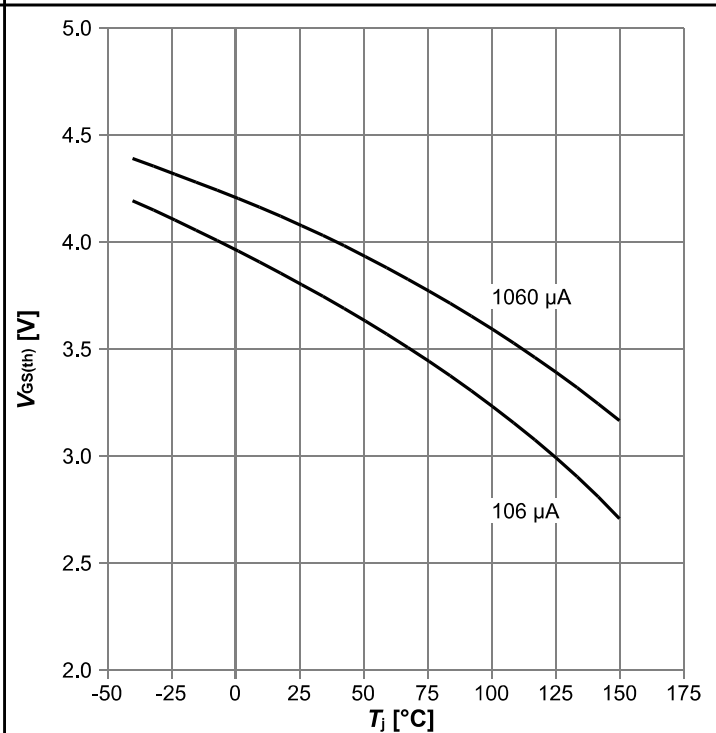
$R_{DS(on)} = f(V_{GS})$, $I_D = 45\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



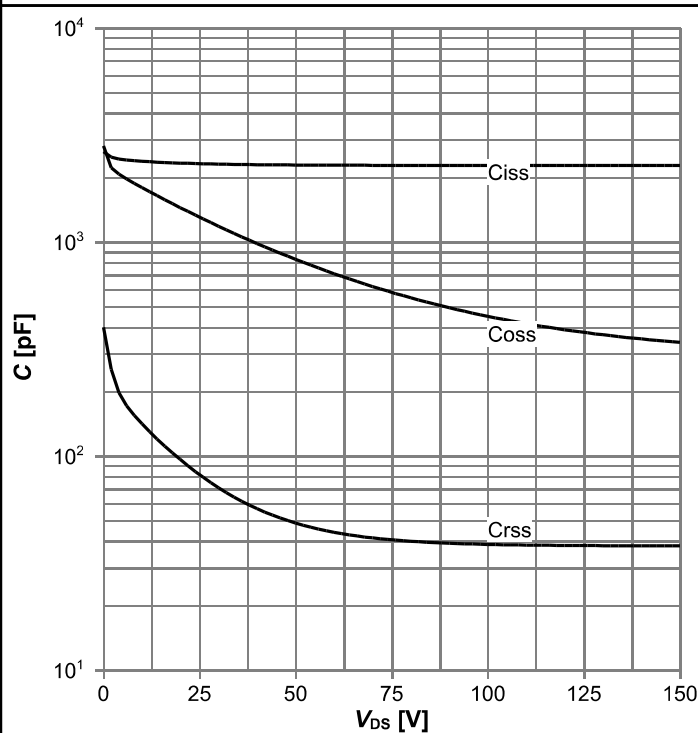
$R_{DS(on)} = f(T_j)$, $I_D = 45$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



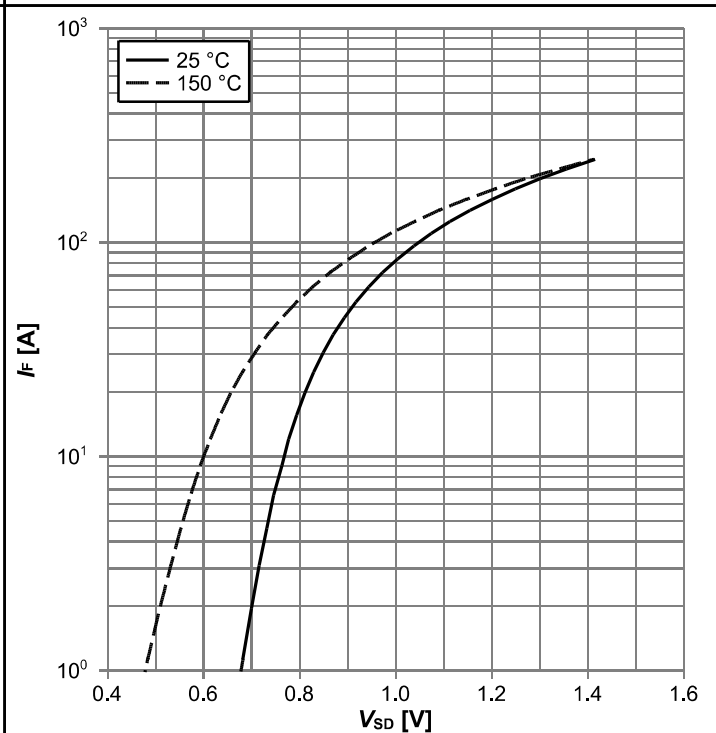
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



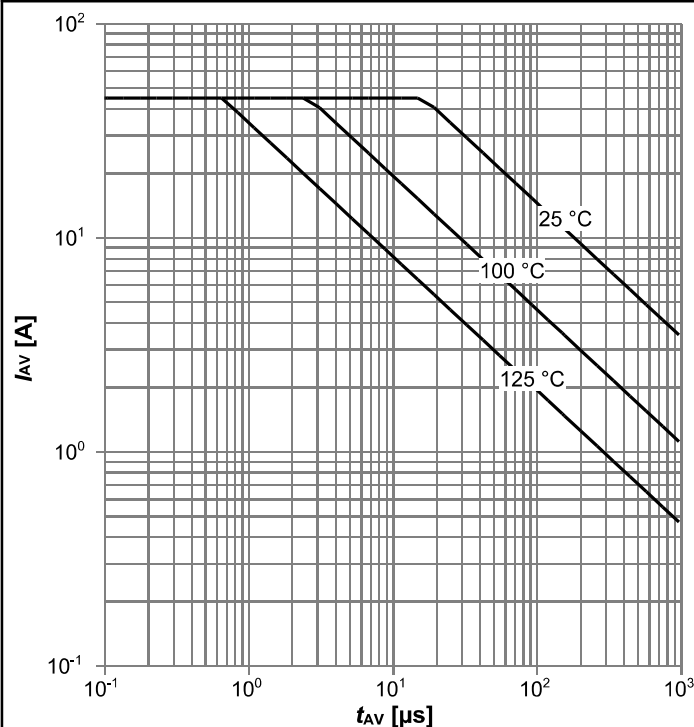
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Typ. forward characteristics of reverse diode



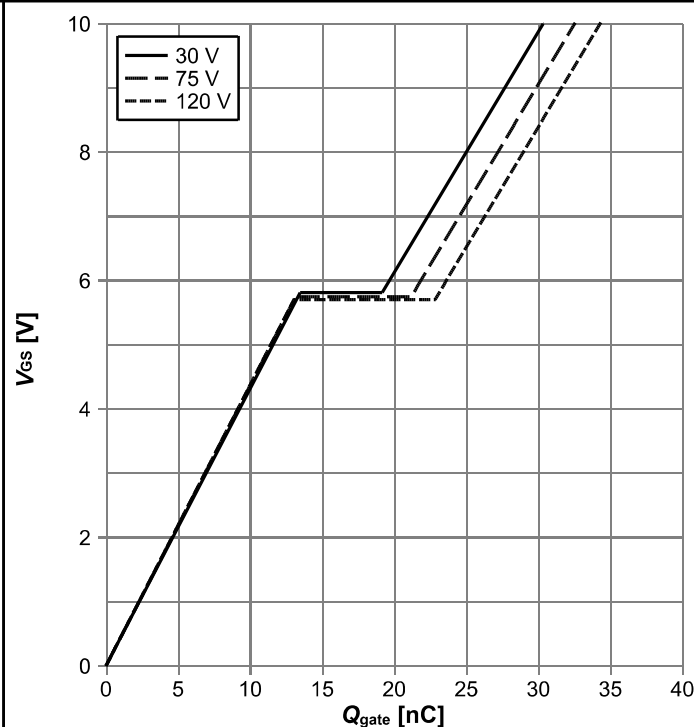
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



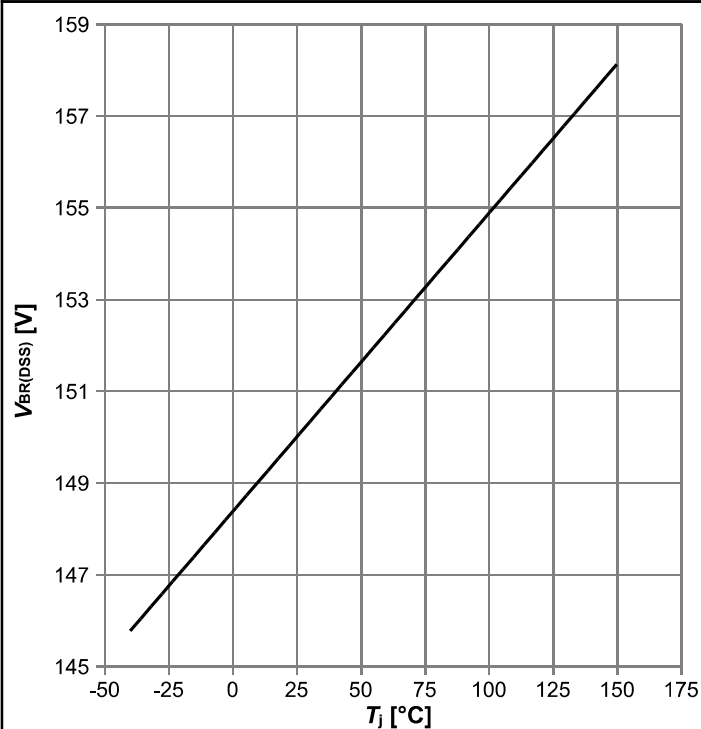
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



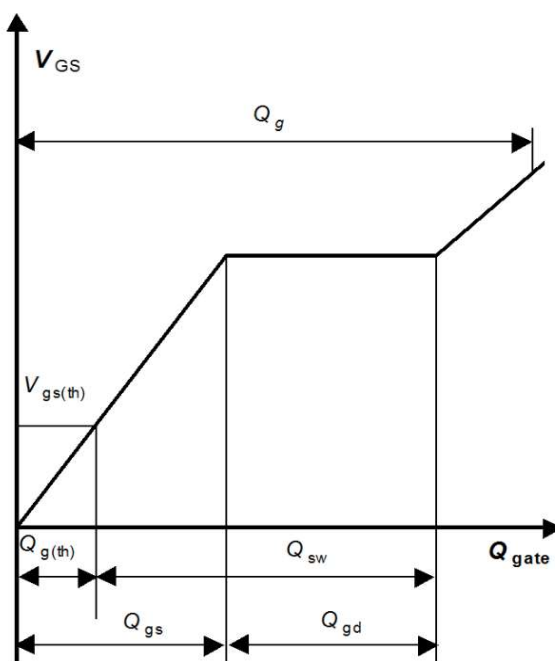
$V_{GS}=f(Q_{gate})$, $I_D=45\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



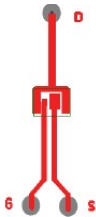
$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 Test Circuits

Table 8 Rth/Zth measurement diagrams

		
²⁾ Surface mounted on 1 in. square Cu board (still air).	⁶⁾ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)	

6 Package Outlines

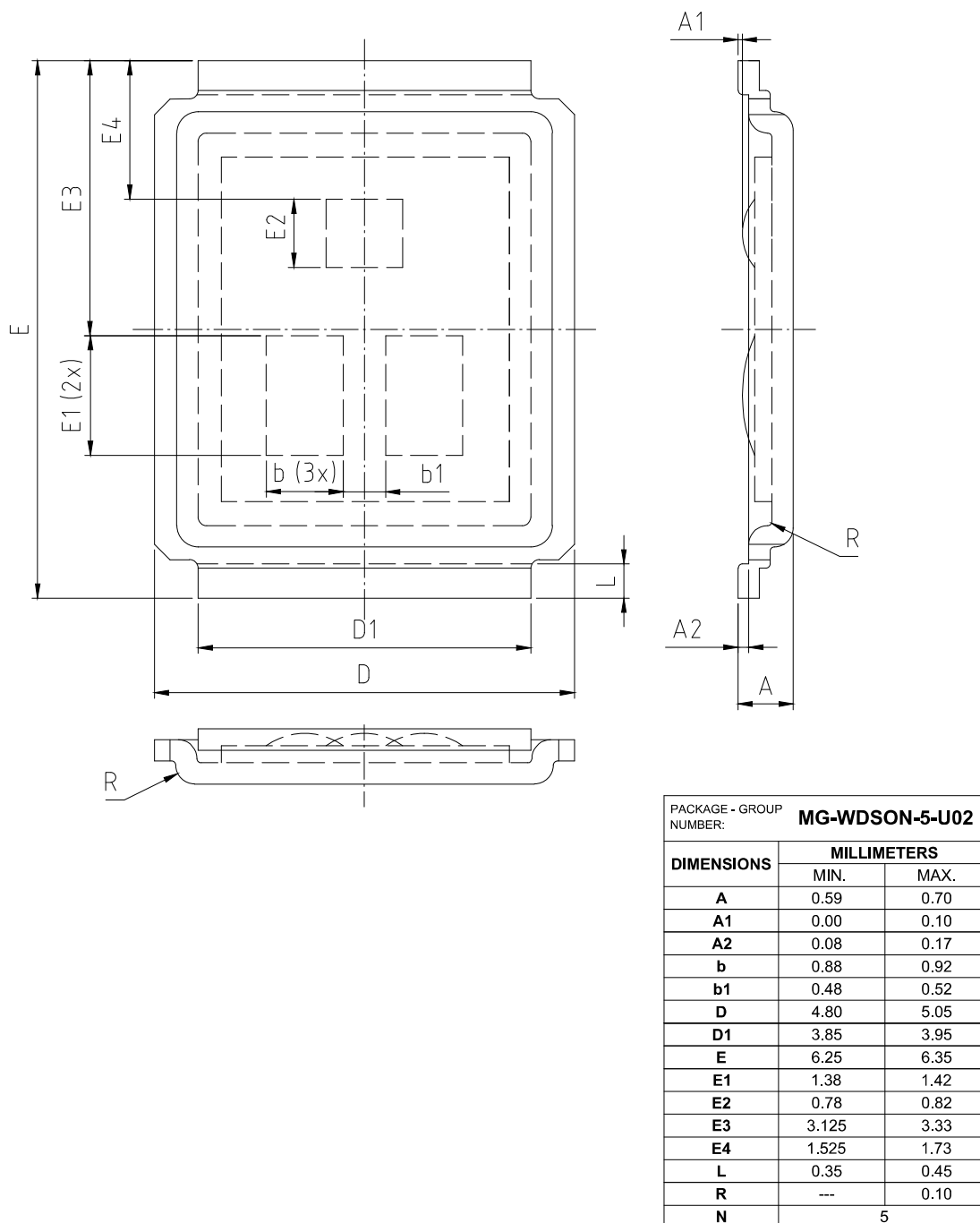
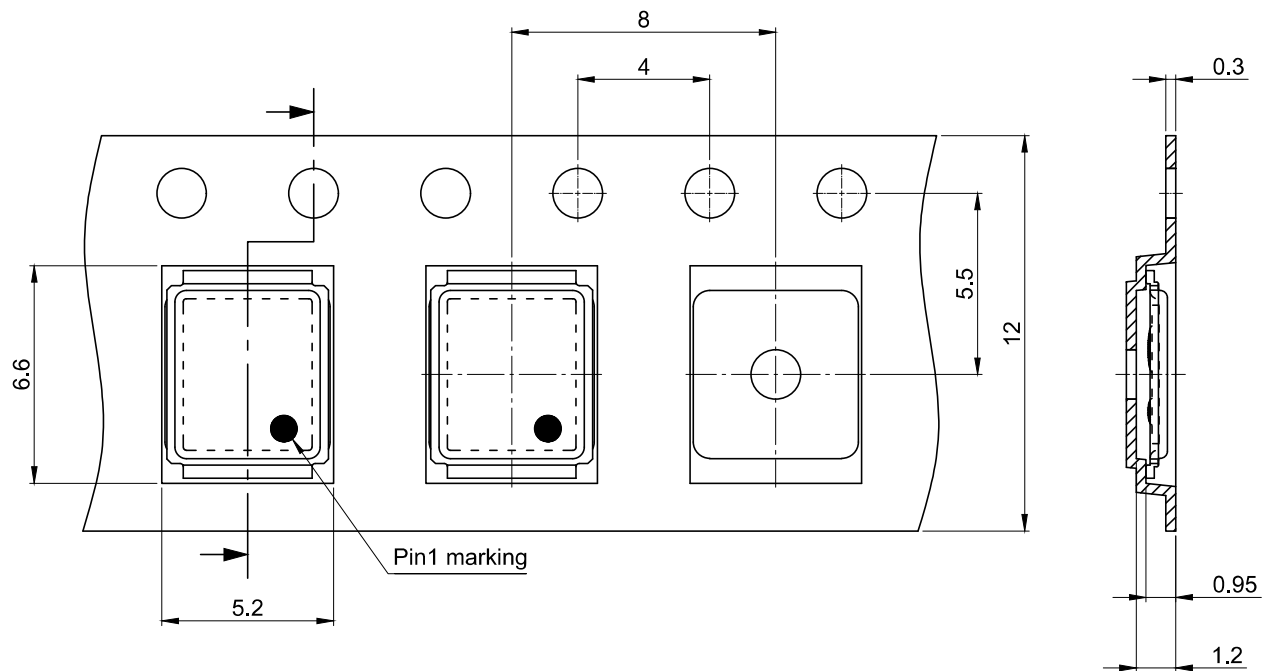
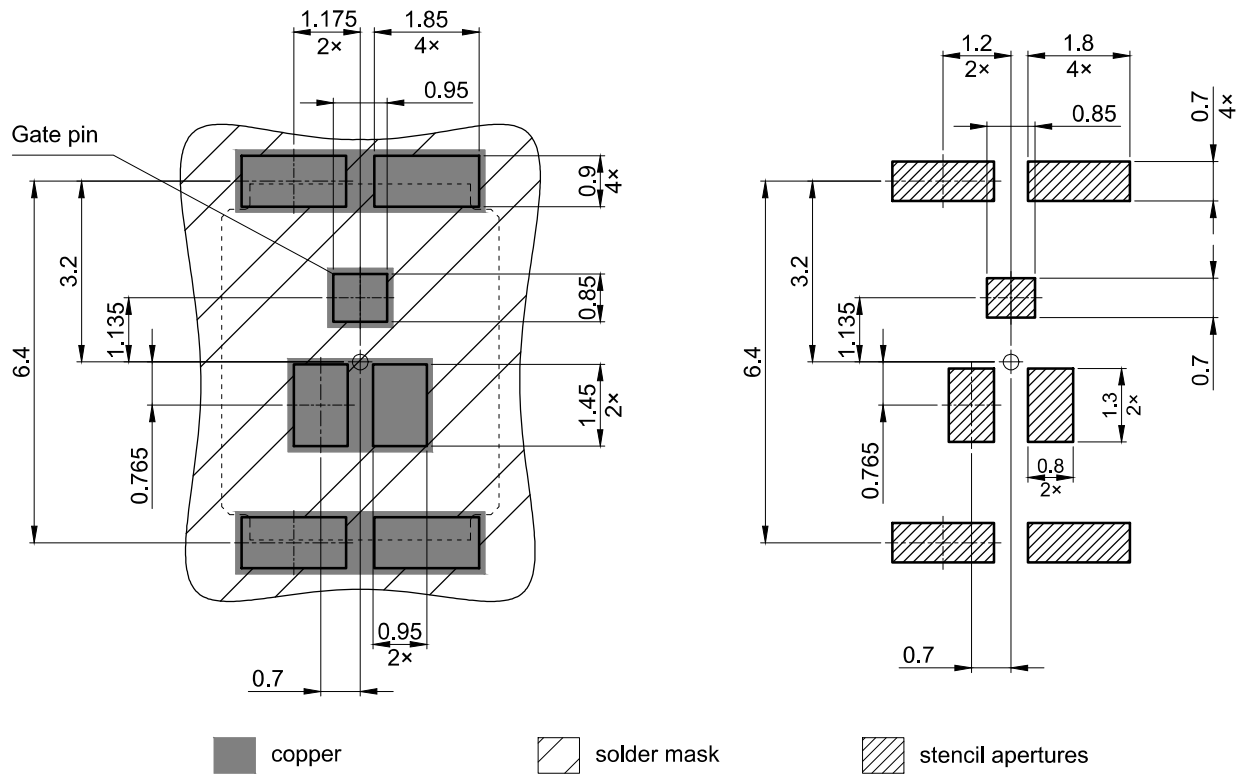


Figure 1 Outline MG-WDSO-5, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 2 Outline Tape (MG-WDSO5-5), dimensions in mm



All dimensions are in units mm
All pads are solder mask defined

Figure 3 Outline Footprint (MG-WDSO-5), dimensions in mm

Revision History

IRF150DM115

Revision: 2023-08-29, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-04-08	Release of final version
2.1	2023-08-29	Updated Rg, and outline_tape_footprint drawings

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