International
IOR Rectifier

Data Sheet No. PD60245

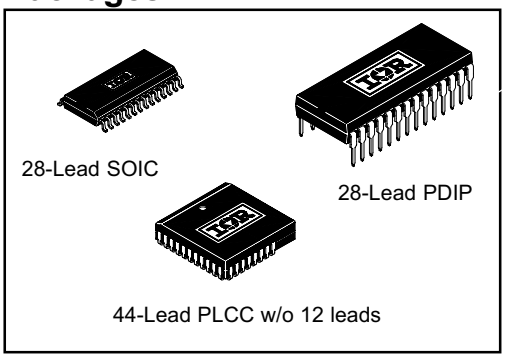
IR21363(J&S)PbF

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage - dV/dt immune
- Gate drive supply range from 12 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Lowside outputs out of phase with inputs. High side outputs out of phase
- 3.3V logic compatible
- Lower di/dt gate driver for better noise immunity
- Externally programmable delay for automatic fault clear

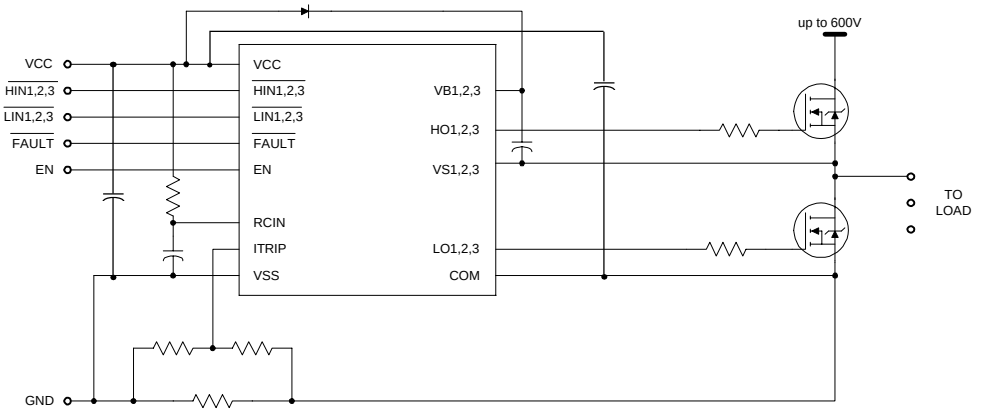
Packages



Description

The IR21363(J&S) are high votage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only.
Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	V
V_{BS}	High side floating supply voltage		-0.3	625	
V_{HO}	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN,HIN,ITRIP, EN, RCIN		V_{SS} - 0.3	lower of (V_{SS} + 15) or V_{CC} + 0.3)	
V_{FLT}	FAULT output voltage		V_{SS} - 0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ +12	$V_{S1,2,3}$ +20	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 1	600	
$V_{HO1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	12	20	
V_{SS}	Logic ground	-5	5	
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} +5	
V_{IN}	Logic input voltage $\overline{LIN}$, $\overline{HIN}$	V_{SS}	V_{SS} +5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5V to COM +600V. Logic state held for V_S of COM -5V to COM -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS}1,2,3$) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_S1,2,3$ and $L_S1,2,3$). The V_O and I_O parameters are referenced to COM and $V_S1,2,3$ and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$	3.0	—	—		
V_{IL}	Logic "1" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$	—	—	0.8		
$V_{EN,TH+}$	EN positive going threshold	—	—	3		
$V_{EN,TH-}$	EN negative going threshold	0.8	—	—		
$V_{IT,TH+}$	ITRIP positive going threshold	0.37	0.46	0.55		
$V_{IT,HYS}$	ITRIP input hysteresis	—	0.07	—		
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—		
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.9	1.4	V	I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.4	0.6		I_O = 20 mA
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	10.6	11.1	11.6		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	10.4	10.9	11.4		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	—	0.2	—		
I_{LK}	Offset supply leakage current	—	—	50	µA	$V_{B1,2,3}$=$V_{S1,2,3}$=600V
I_{QBS}	Quiescent V_{BS} supply current	—	70	120		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	3.3	—	mA	
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.9	5.2	5.5	V	I_{IN} = 100µA
I_{LIN+}	Input bias current (LOUT = HI)	—	200	300		V_{LIN} = 5V
I_{LIN-}	Input bias current (LOUT = LO)	—	100	220		V_{LIN} = 0V
I_{HIN+}	Input bias current (HOUT = HI)	—	200	300		V_{HIN} = 5V
I_{HIN-}	Input bias current (HOUT = LO)	—	100	220	µA	V_{HIN} = 0V
I_{ITRIP+}	"high" ITRIP input bias current	—	30	100		V_{ITRIP} = 5V
I_{ITRIP-}	"low" ITRIP input bias current	—	0	1		V_{ITRIP} = 0V
I_{EN+}	"high" ENABLE input bias current	—	30	100		V_{ENABLE} = 5V
I_{EN-}	"low" ENABLE input bias current	—	0	1		V_{ENABLE} = 0V
I_{RCIN}	RCIN input bias current	—	0	1		V_{RCIN} = 0V or 15V
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O=0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O=15V, PW ≤10 µs
$R_{ON,RCIN}$	RCIN low on resistance	—	50	100	Ω	
$R_{ON,FLT}$	FAULT low on resistance	—	50	100		

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 15V, $V_{S1,2,3}$ = V_{SS} = COM, TA = 25°C and C_L = 1000 pF unless otherwise specified.

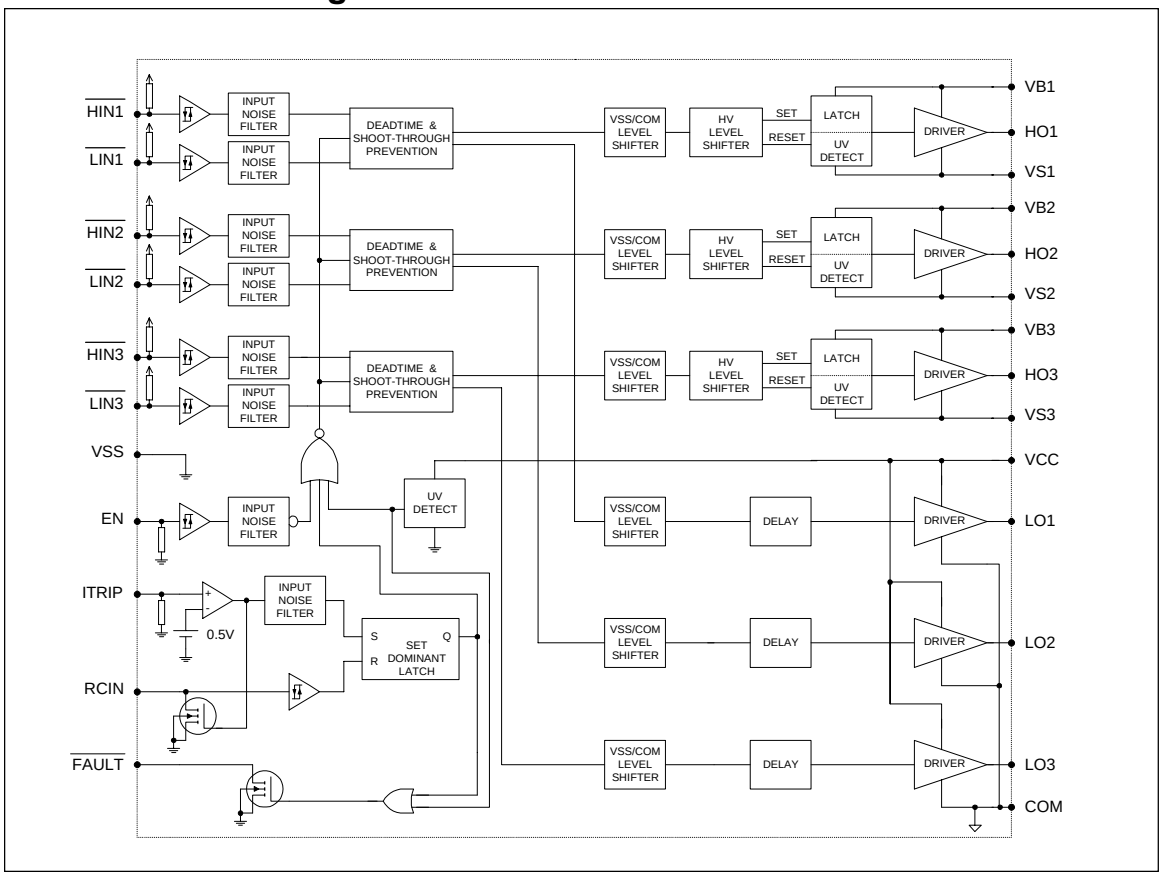
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	370	525	680	nS	V_{IN} = 0 & 5V
t_{off}	Turn-off propagation delay	310	500	690		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{EN}	ENABLE low to output shutdown propagation delay	300	450	600		V_{IN}, V_{EN} = 0V or 5V
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1000		V_{ITRIP} = 5V
t_{bl}	ITRIP blanking time	100	150	—		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	800		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FILIN}	Input filter time (HIN, LIN) (EN)	— 100	310 200	— —		V_{IN} = 0 & 5V
t_{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	1.3	1.65	2	mS	V_{IN} = 0V or 5V V_{ITRIP} = 0V
DT	Deadtime	220	290	360	nS	V_{IN} = 0 & 5V
MT	Matching delay ON and OFF	—	40	75		External dead time >400nsec
MDT	Matching delay, max (t_{on},t_{off}) - min (t_{on},t_{off}), (ton,toff are applicable to all 3 channels)	—	25	70		
PM	Output pulse width matching, PWin -PWout (fig.2)	—	40	75		

NOTE: For high side PWM, HIN pulse width must be ≥ 1μsec

VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1,2,3	0
15V	15V	0V	5V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>V_{ITRIP}	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 1: UVCC is not latched, when VCC>UVCC, FAULT returns to high impedance.
Note 2: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

Functional Block Diagram

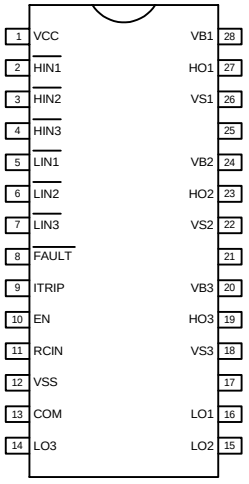


Lead Definitions

Symbol	Description
V_{CC}	Low side and logic fixed supply
VSS	Logic Ground
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occured. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
V_B1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply returns
LO1,2,3	Low side gate driver output

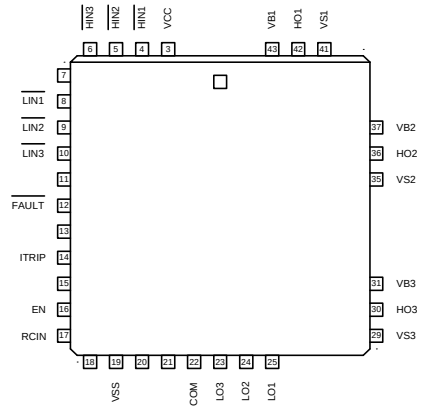
Note: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Lead Assignments



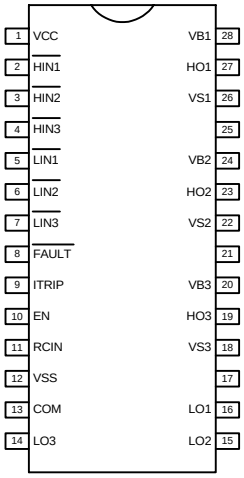
28 Lead PDIP

IR21363



44 Lead PLCC w/o 12 leads

IR21363(J)



28 lead SOIC (wide body)

IR21363(S)

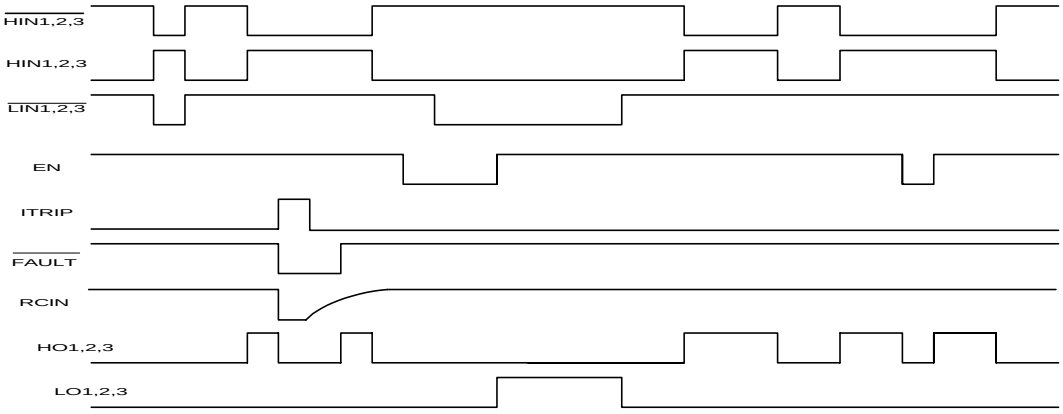


Figure 1. Input/Output Timing Diagram

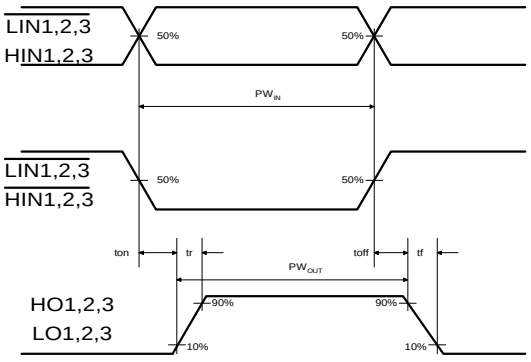


Figure 2. Switching Time Waveforms

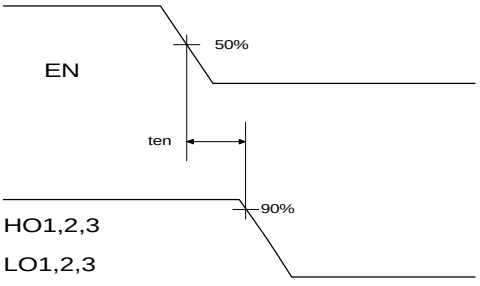


Figure 3. Output Enable Timing Waveform

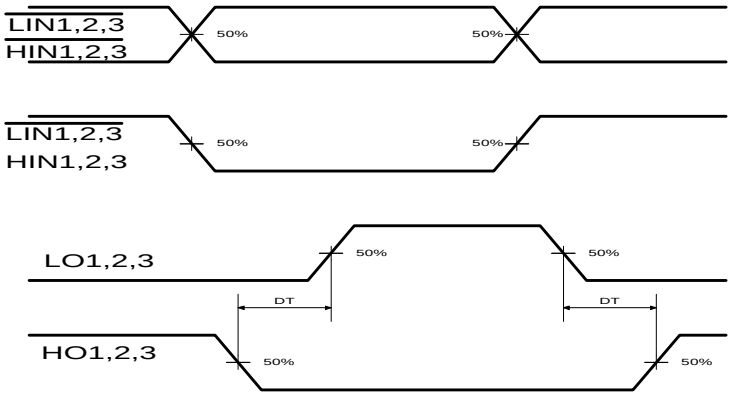


Figure 4. Internal Deadtime Timing Waveforms

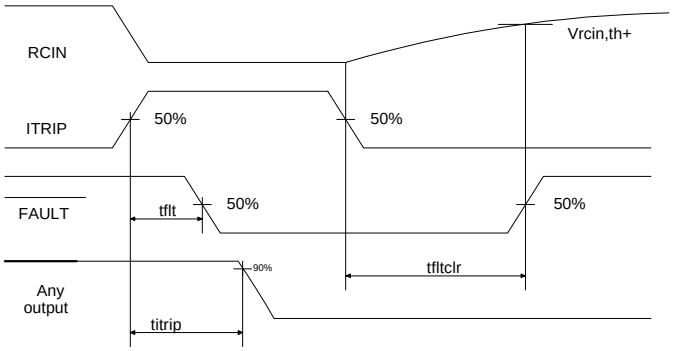


Figure 5. ITRIP/RCIN Timing Waveforms

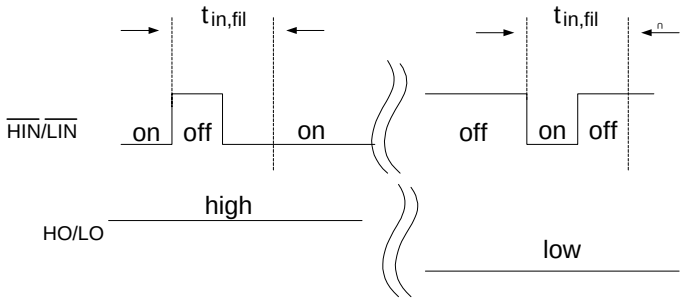


Figure 5.5 Input Filter Function

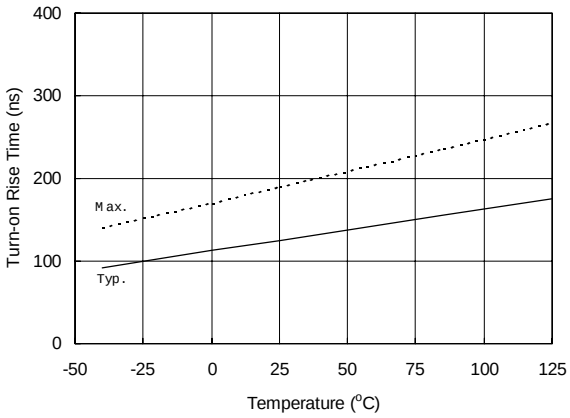


Figure 6A. Turn-on Rise Time vs. Temperature

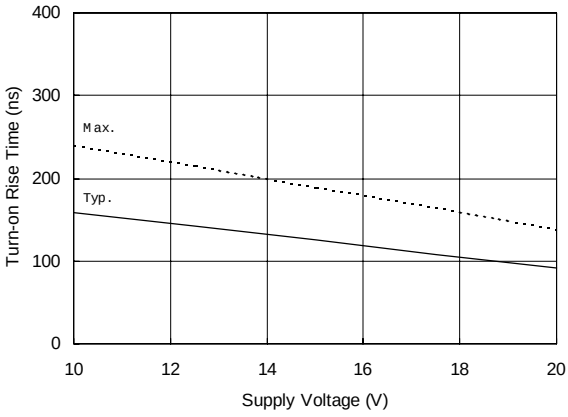


Figure 6B. Turn-on Rise Time vs. Supply Voltage

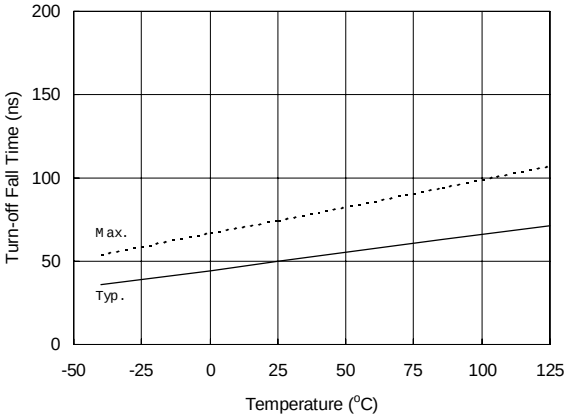


Figure 7A. Turn-off Fall Time vs. Temperature

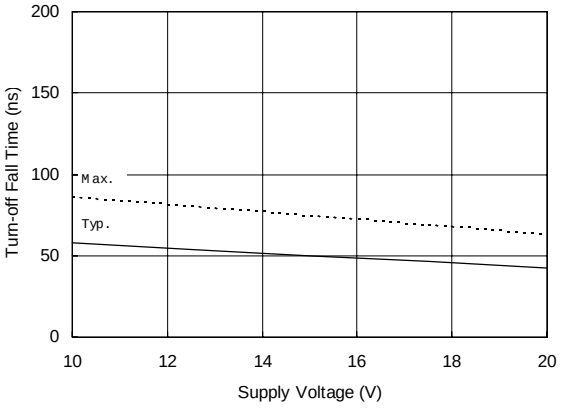


Figure 7B. Turn-off Fall Time vs. Supply Voltage

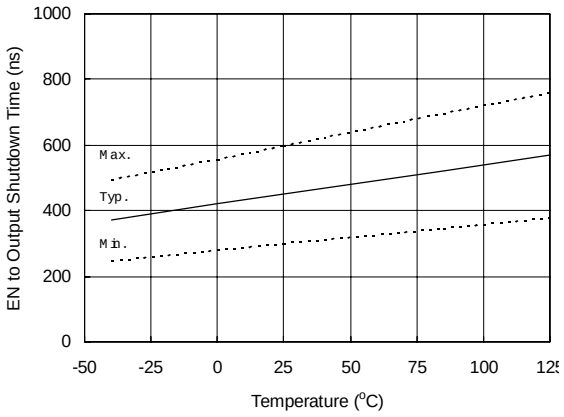


Figure 8A. EN to Output Shutdown Time vs. Temperature

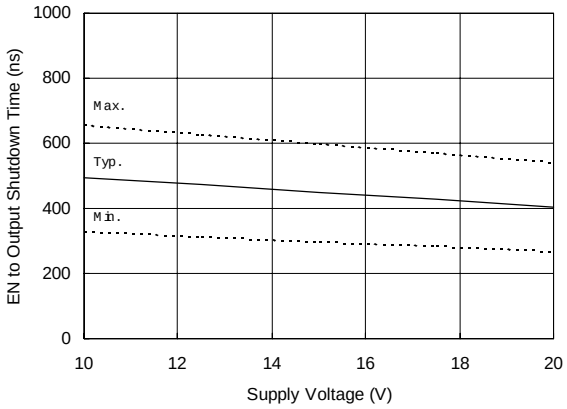


Figure 8B. EN to Output Shutdown Time vs. Supply Voltage

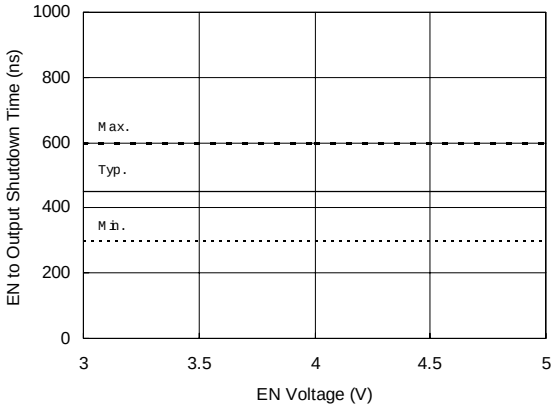


Figure 8C. EN to Output Shutdown Time vs. EN Voltage

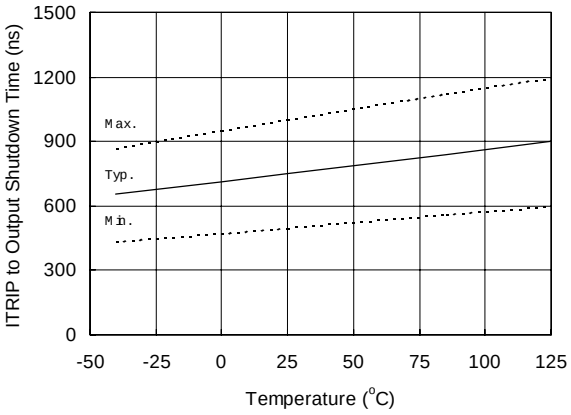


Figure 9A. ITRIP to Output Shutdown Time vs. Temperature

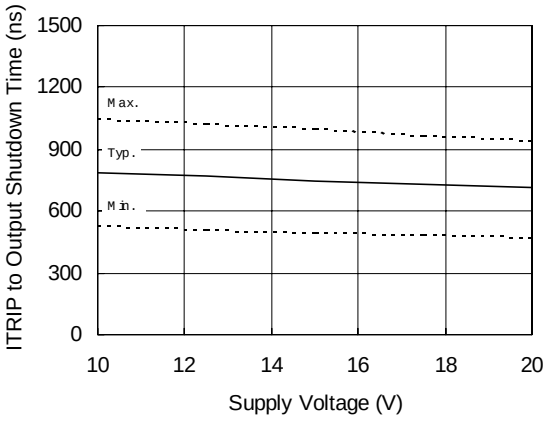


Figure 9B. ITRIP to Output Shutdown Time vs. Supply Voltage

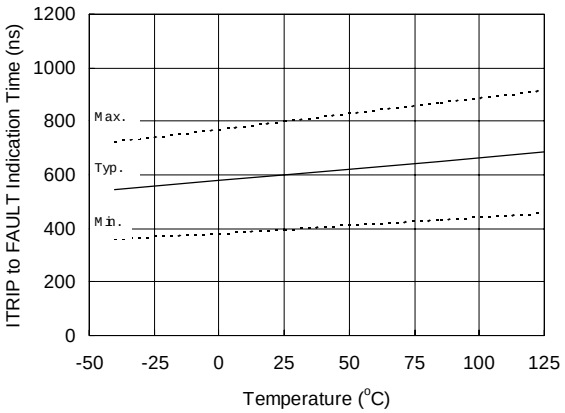


Figure 10A. ITRIP to FAULT Indication Time vs. Temperature

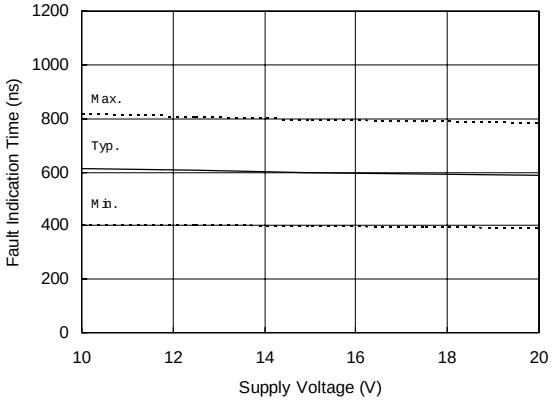


Figure 10B. ITRIP to FAULT Indication Time vs. Supply Voltage

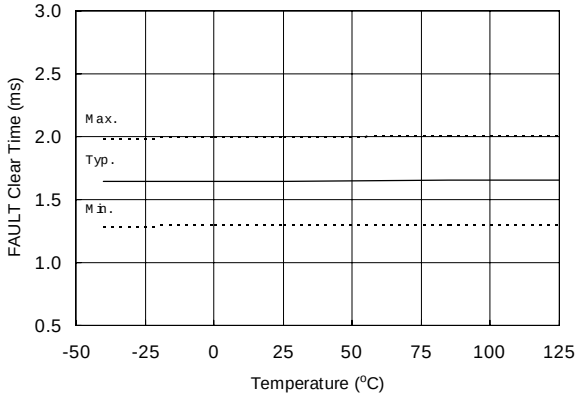


Figure 11A. FAULT Clear Time vs. Temperature

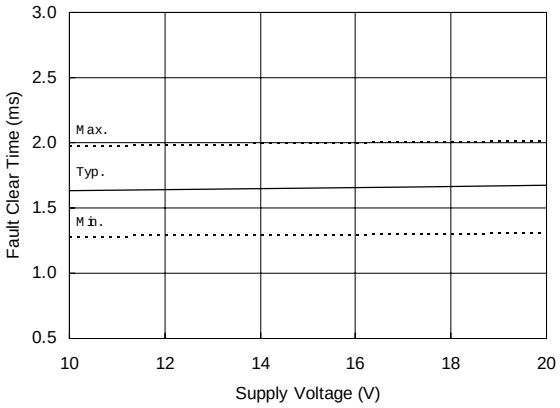


Figure 11B. FAULT Clear Time vs. Supply Voltage

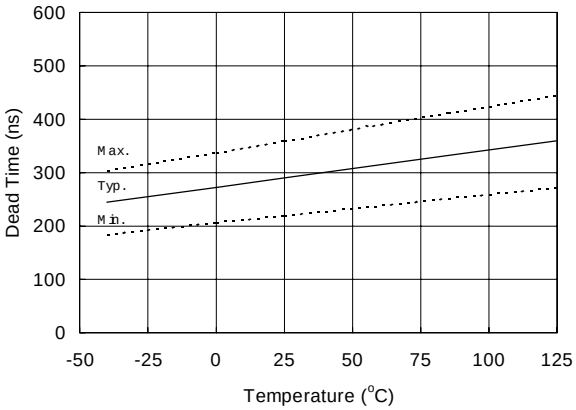


Figure 12A. Dead Time vs. Temperature

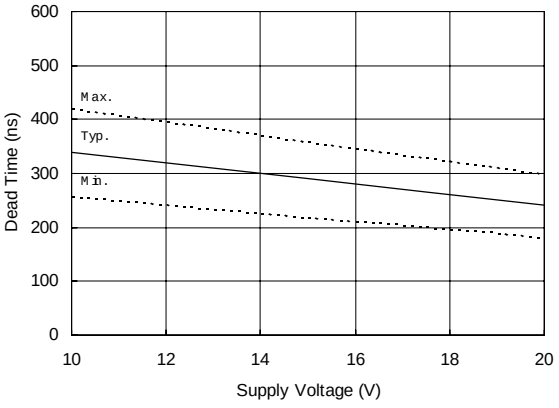


Figure 12B. Dead Time vs. Supply Voltage

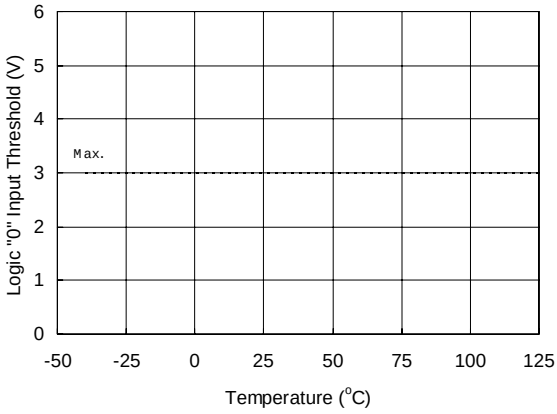


Figure 13A. Logic "0" Input Threshold vs. Temperature

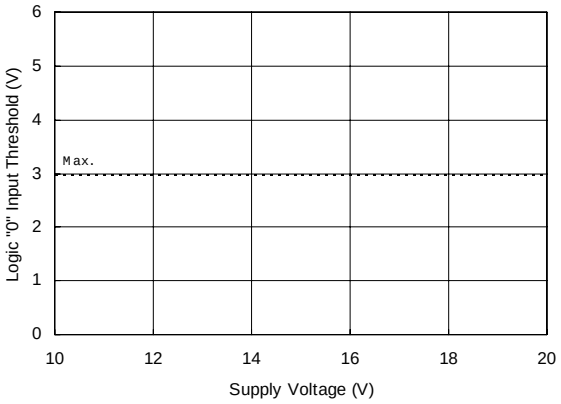


Figure 13B. Logic "0" Input Threshold vs. Supply Voltage

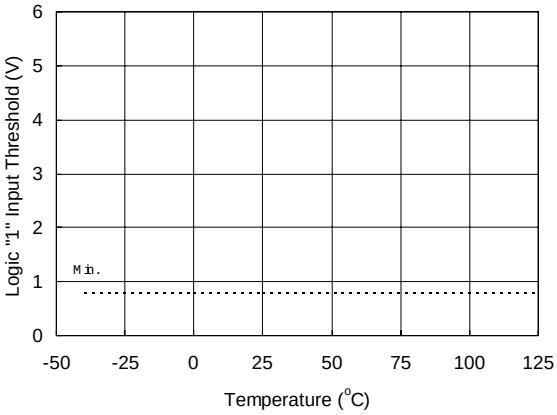


Figure 14A. Logic "1" Input Threshold vs. Temperature

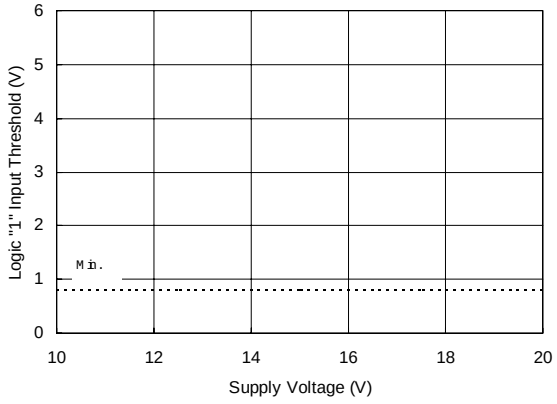


Figure 14B. Logic "1" Input Threshold vs. Supply Voltage

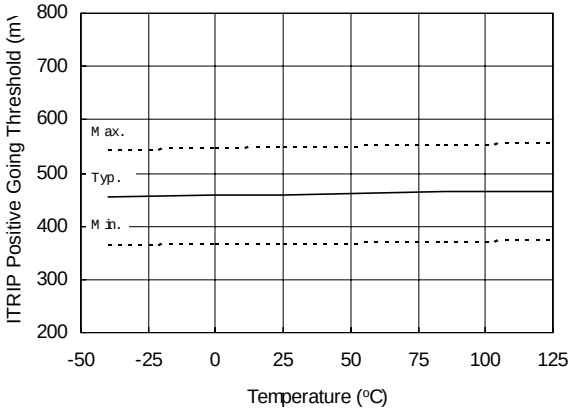


Figure 15A. ITRIP Positive Going Threshold vs. Temperature

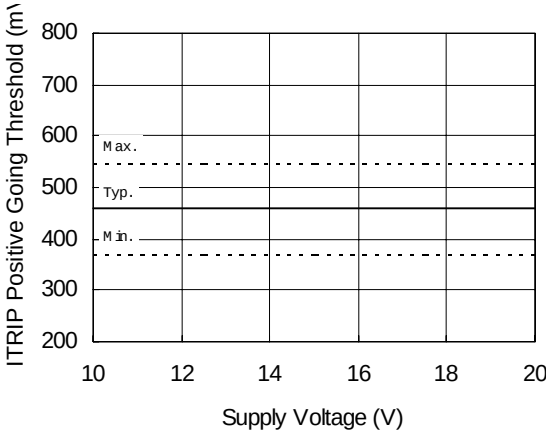


Figure 15B. ITRIP Positive Going Threshold vs. Supply Voltage

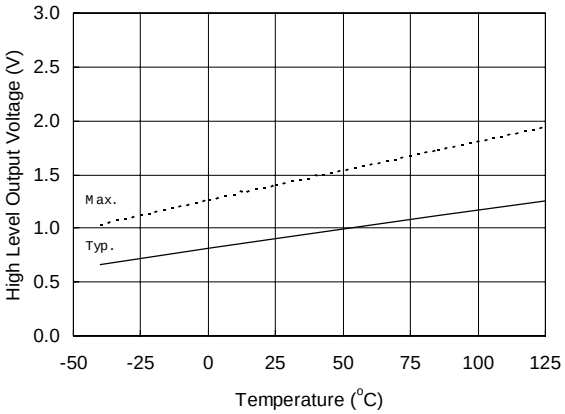


Figure 16A. High Level Output vs. Temperature

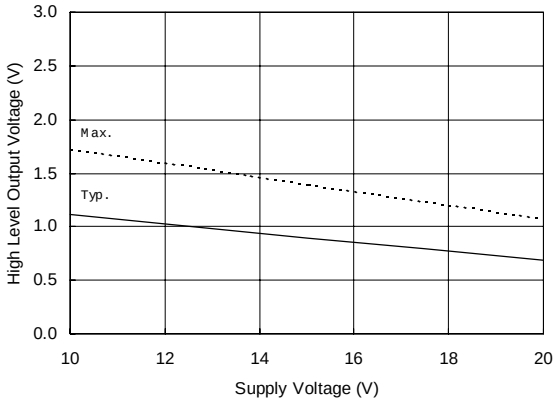


Figure 16B. High Level Output vs. Supply Voltage

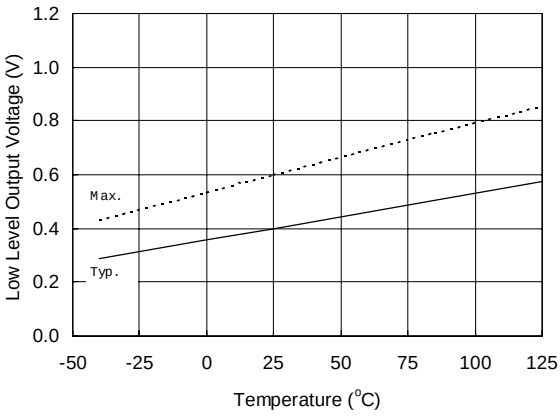


Figure 17A. Low Level Output vs. Temperature

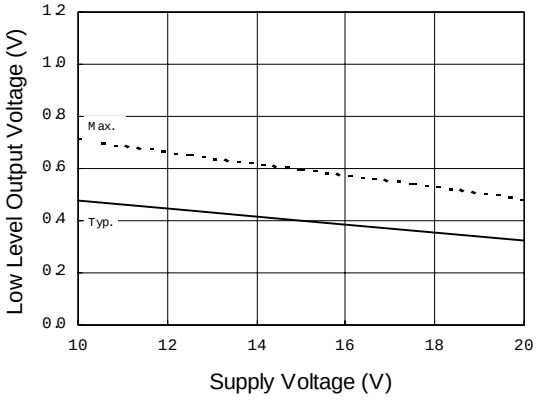


Figure 17B. Low Level Output vs. Supply Voltage

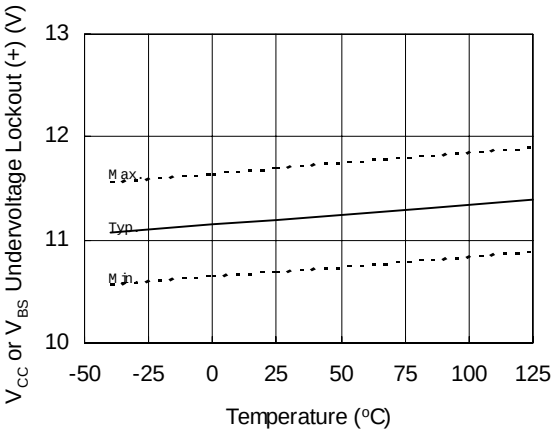


Figure 18. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature

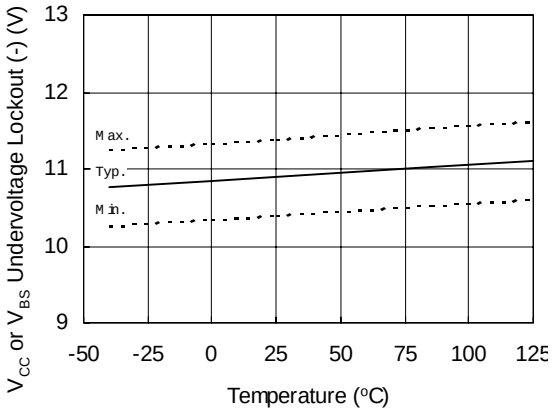


Figure 19. V_{CC} or V_{BS} Undervoltage (-) vs. Temperature

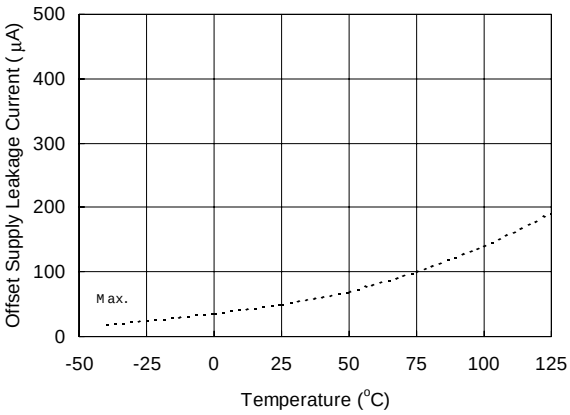


Figure 20A. Offset Supply Leakage Current vs. Temperature

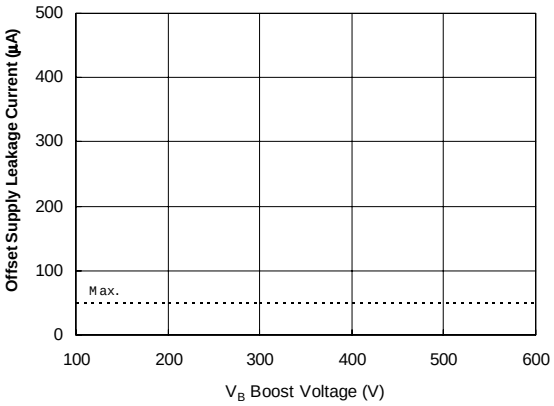


Figure 20B. Offset Supply Leakage Current vs. V_B Boost Voltage

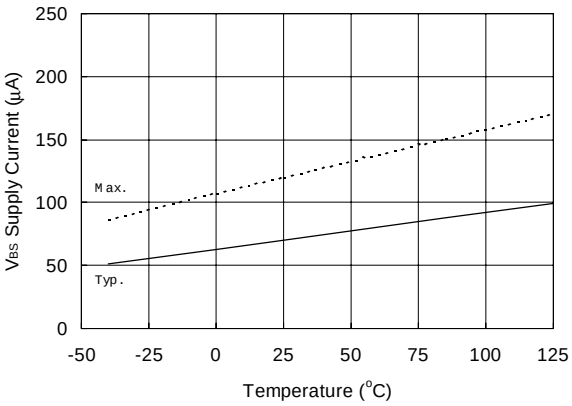


Figure 21A. V_B Supply Current vs. Temperature

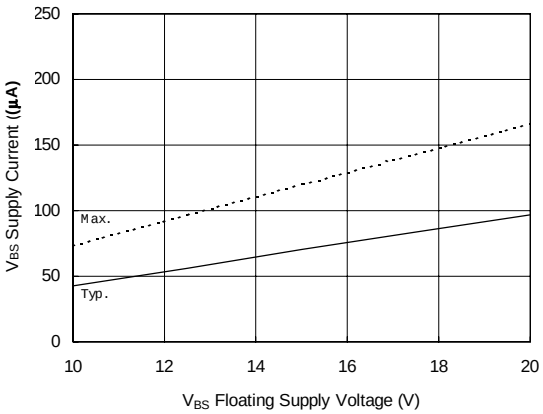


Figure 21B. V_{BS} Supply Current vs. V_{BS} Floating Supply Voltage

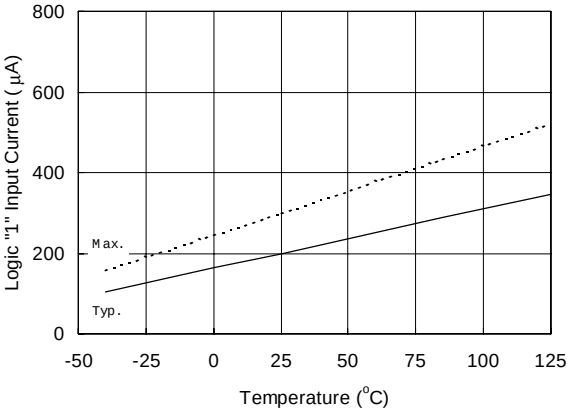


Figure 22A. Input Current vs. Temperature

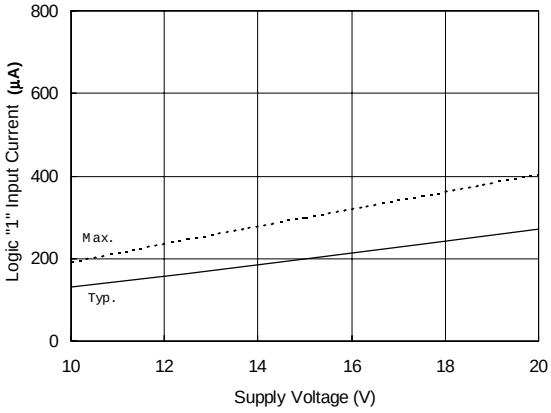


Figure 22B. Logic "1" Input Current vs. Supply Voltage

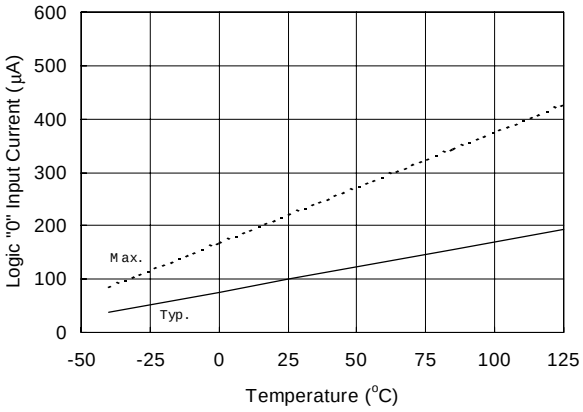


Figure 23A. Logic "0" Input Current vs. Temperature

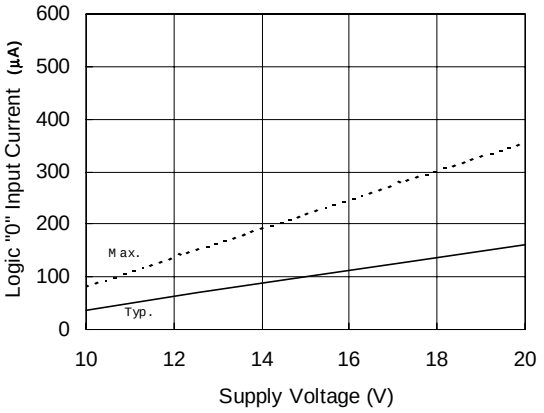


Figure 23B. Logic "0" Input Current vs. Supply Voltage

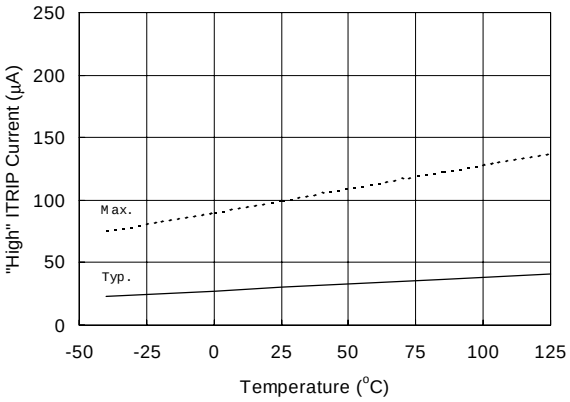


Figure 24A. High ITRIP Current vs. Temperature

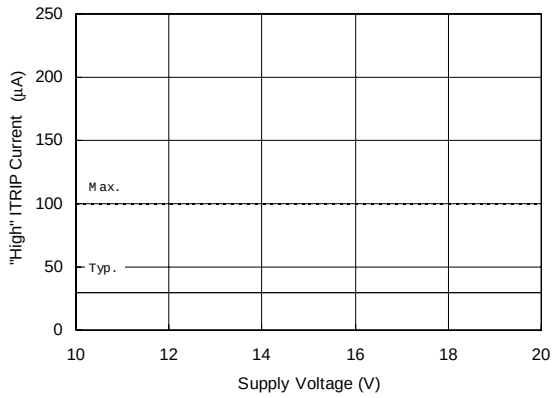


Figure 24B. "High" ITRIP Current vs. Supply Voltage

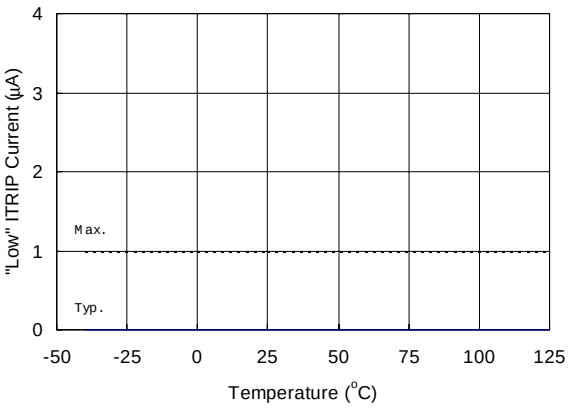


Figure 25A. "Low" ITRIP Current vs. Temperature

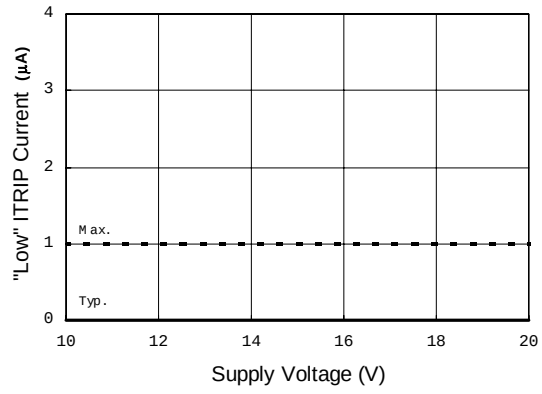


Figure 25B. ITRIP Current vs. Supply Voltage

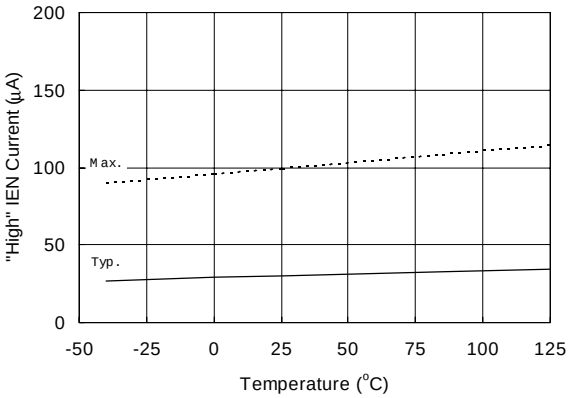


Figure 26A. "High" IEN Current vs. Temperature

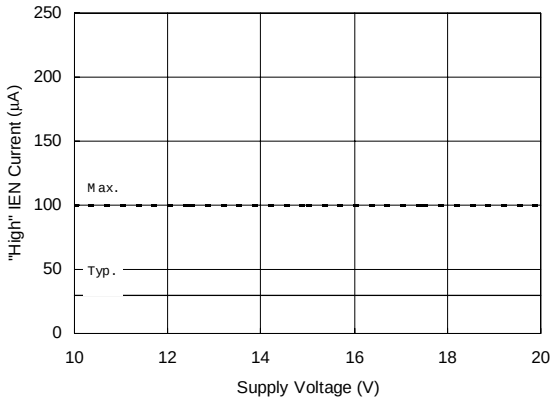


Figure 26B. "High" IEN Current vs. Supply Voltage

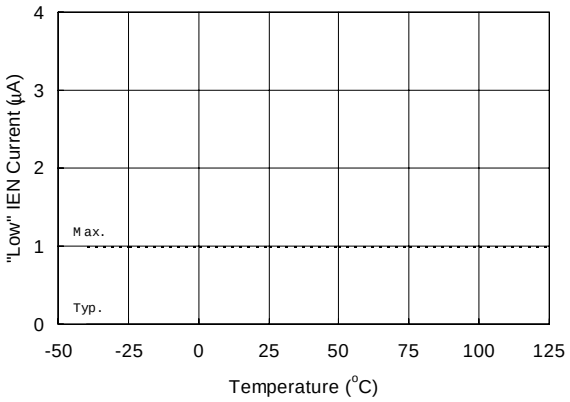


Figure 27A. "Low" IEN Current vs. Temperature

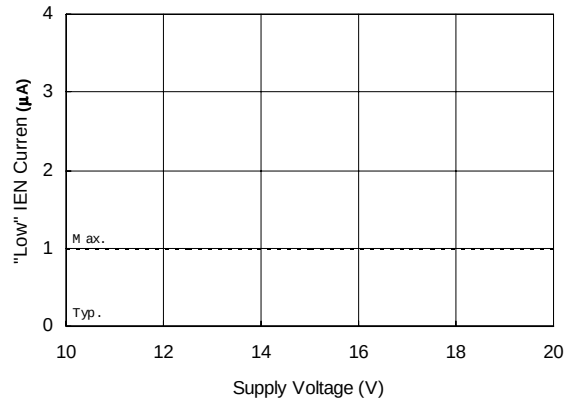


Figure 27B. IEN Current vs. Supply Voltage

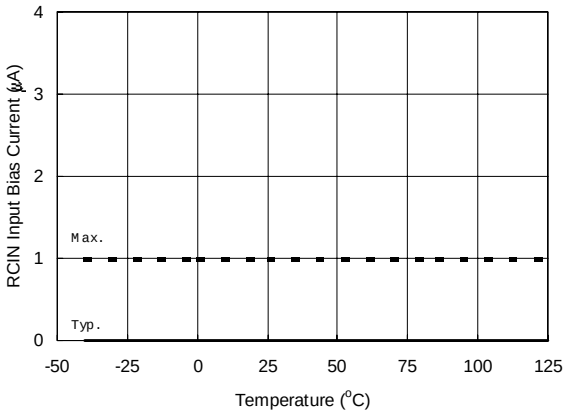


Figure 28A. RCIN Input Bias Current vs. Temperature

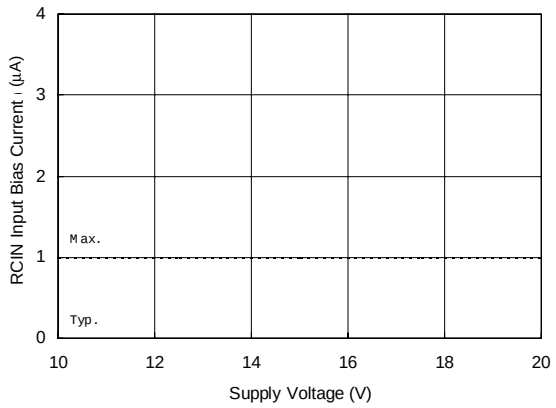


Figure 28B. RCIN Input Bias Current vs. Supply Voltage

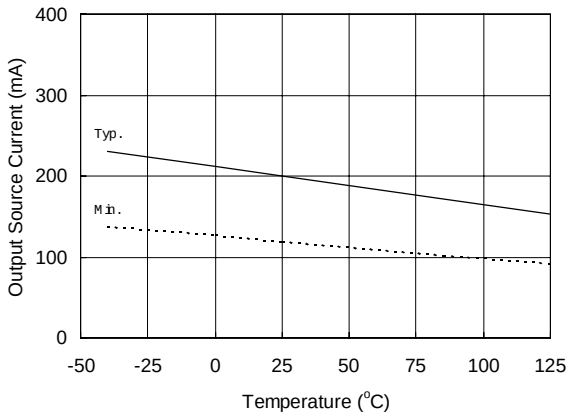


Figure 29A. Output Source Current vs. Temperature

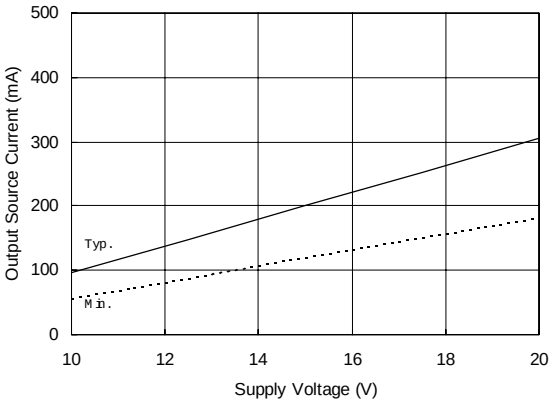


Figure 29B. Output Source Current vs. Supply Voltage

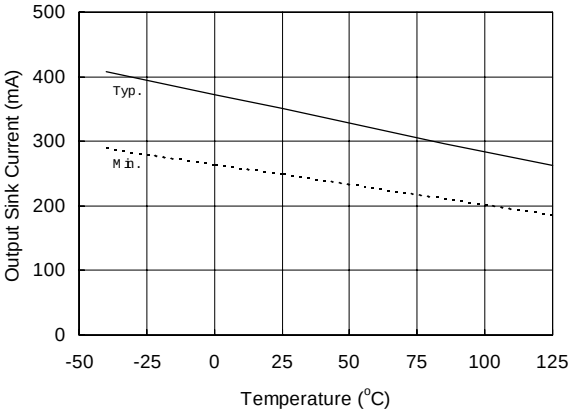


Figure 30A. Output Sink Current vs. Temperature

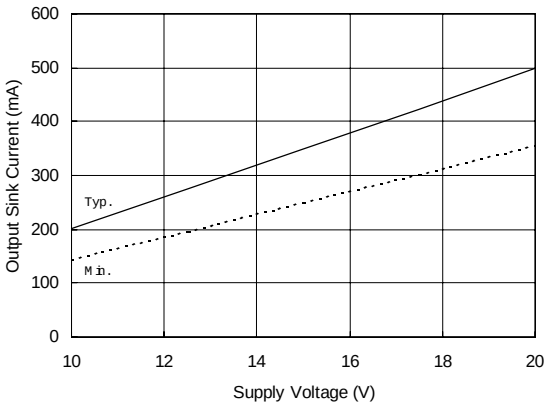


Figure 30B. Output Sink Current vs. Supply Voltage

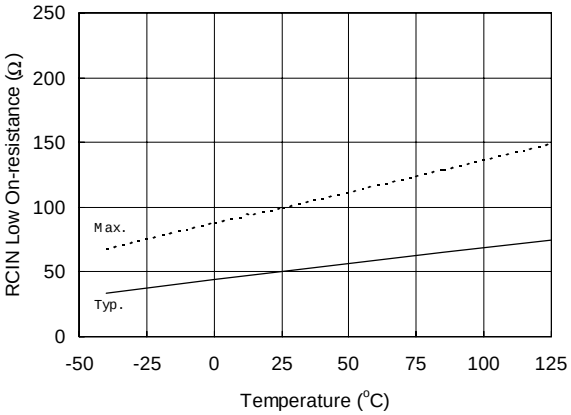


Figure 31A. RCIN Low On-resistance vs. Temperature

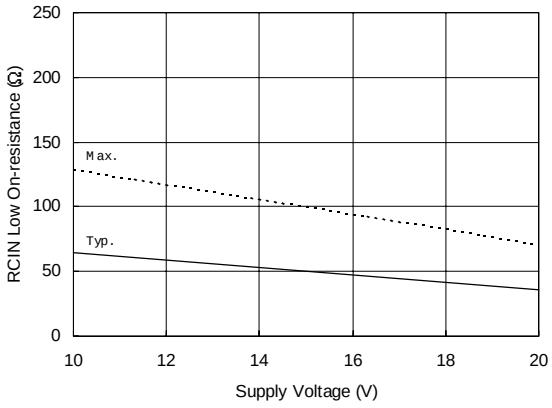


Figure 31B. RCIN Low On-resistance vs. Supply Voltage

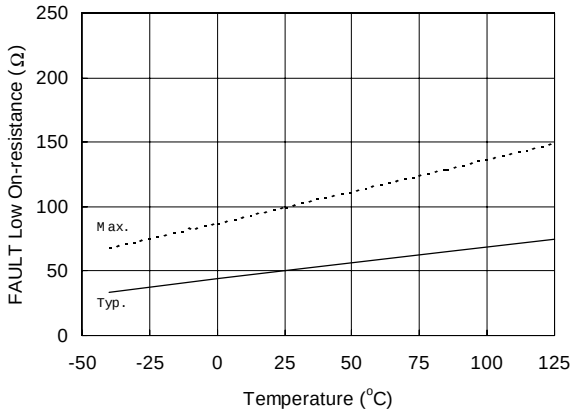


Figure 32A. FAULT Low On-resistance vs. Temperature

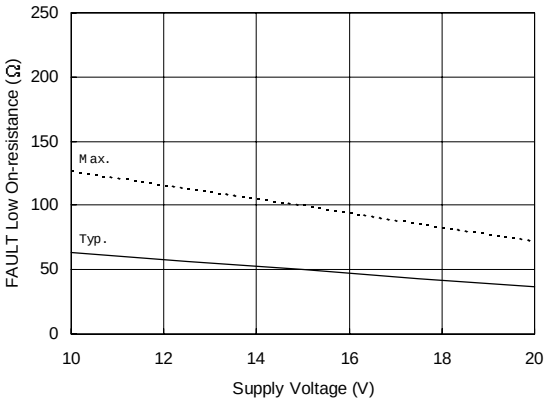


Figure 32B. FAULT Low On-resistance vs. Supply Voltage

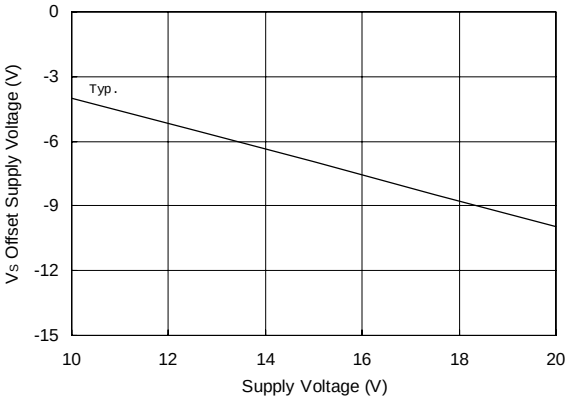


Figure 33. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

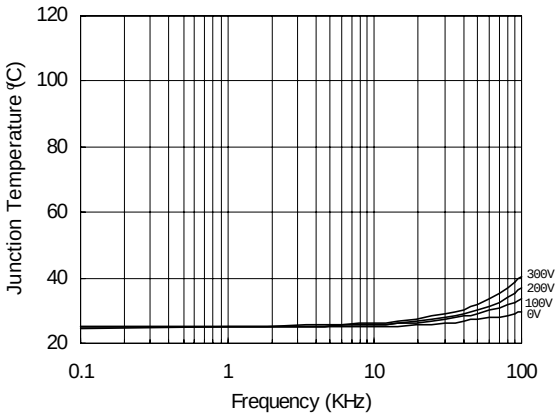


Figure 34. IR21363 vs. Frequency (IRG4BC20W), R_{gate}=33Ω, Vcc=15V

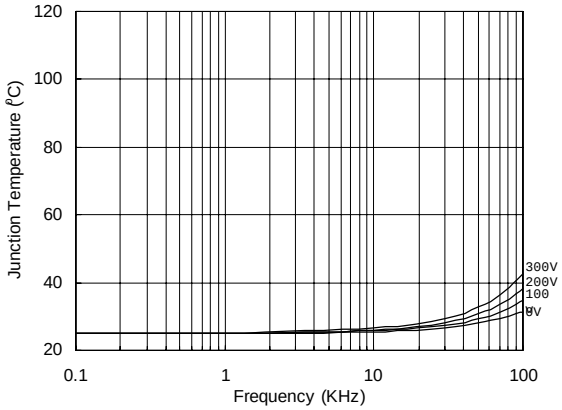


Figure 35. IR21363 vs. Frequency (IRG4BC30W), R_{gate}=15Ω, Vcc=15V

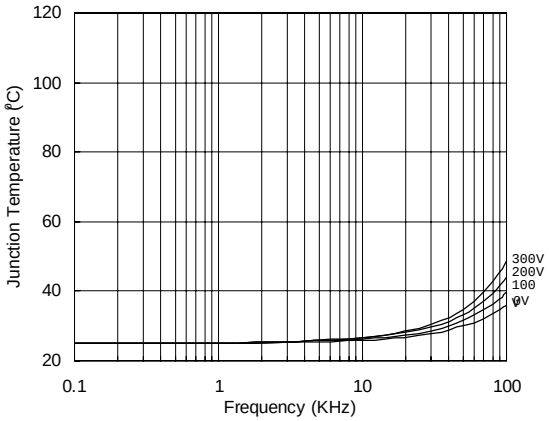


Figure 36. IR21363 vs. Frequency (IRG4BC40W), R_{gate}=10Ω, Vcc=15V

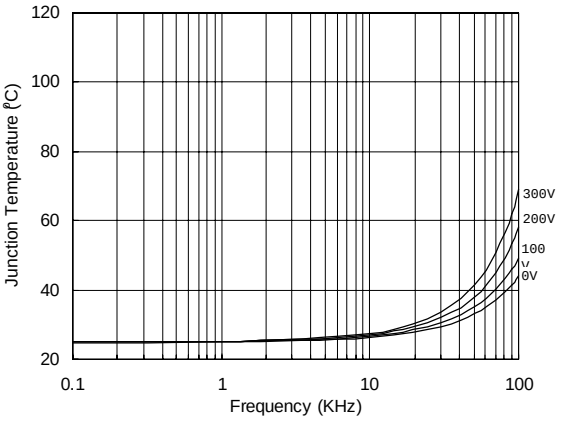


Figure 37. IR21363 vs. Frequency (IRG4PC50W), R_{gate}=5Ω, Vcc=15V

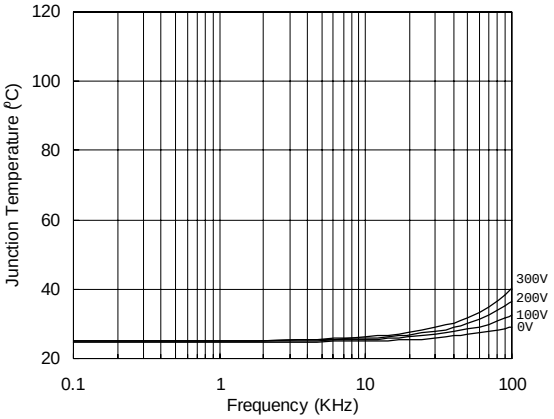


Figure 38. IR21363 (J) vs. Frequency (IRG4BC20W), R_{gate}=33Ω, Vcc=15V

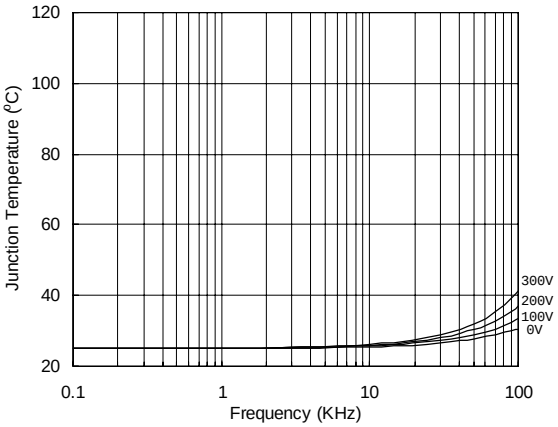


Figure 39. IR21363 (J) vs. Frequency (IRG4BC30W), R_{gate}=15Ω, Vcc=15V

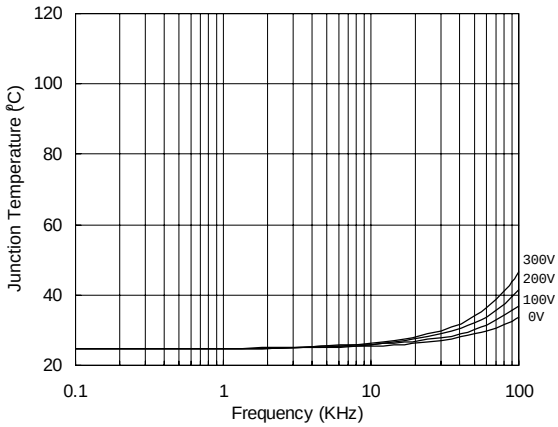


Figure 40. IR21363 (J) vs. Frequency (IRG4BC40W), R_{gate}=10Ω, Vcc=15V

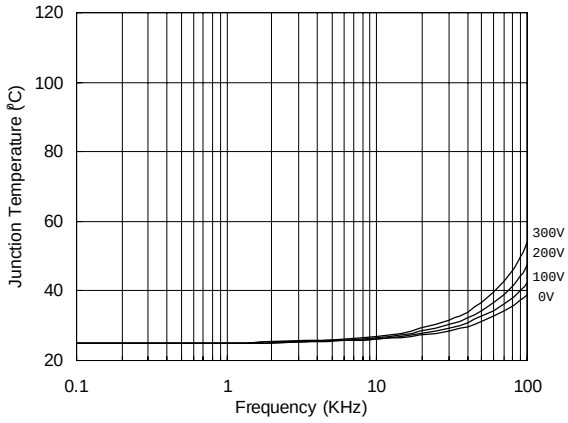


Figure 41. IR21363 (J) vs. Frequency (IRG4PC50W), R_{gate}=5Ω, Vcc=15V

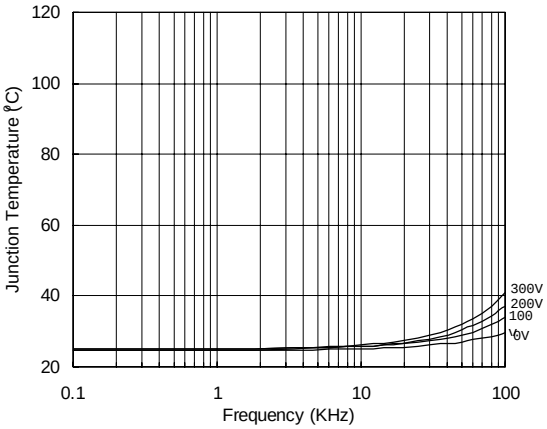


Figure 42. IR21363 (S) vs. vs. Frequency (IRG4BC20W), R_{gate}=33Ω, Vcc=15V

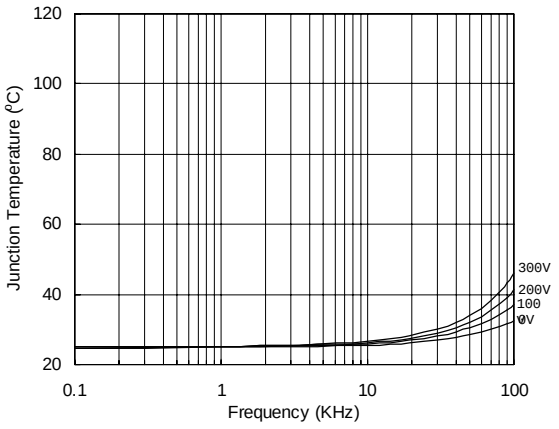


Figure 43. IR21363 (S) vs. vs. Frequency (IRG4BC30W), R_{gate}=15Ω, Vcc=15V

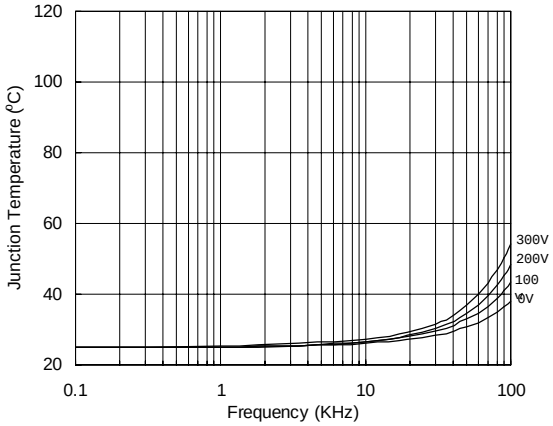


Figure 44. IR21363 (S) vs. vs. Frequency (IRG4BC40W), R_{gate}=10Ω, Vcc=15V

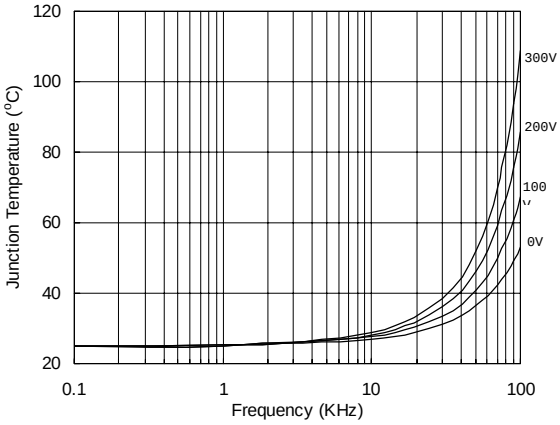
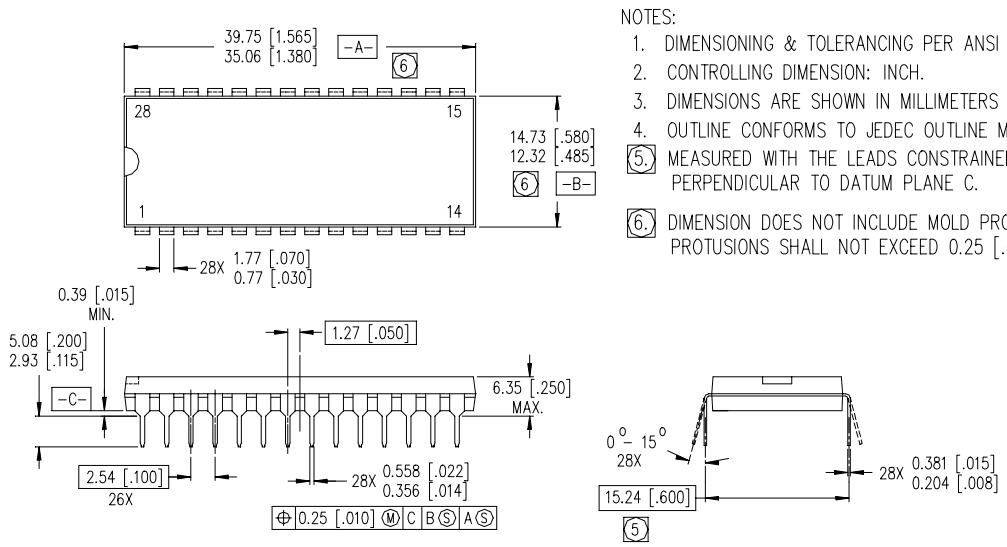


Figure 45. IR21363 (S) vs. vs. Frequency (IRG4PC50W), R_{gate}=5Ω, Vcc=15V

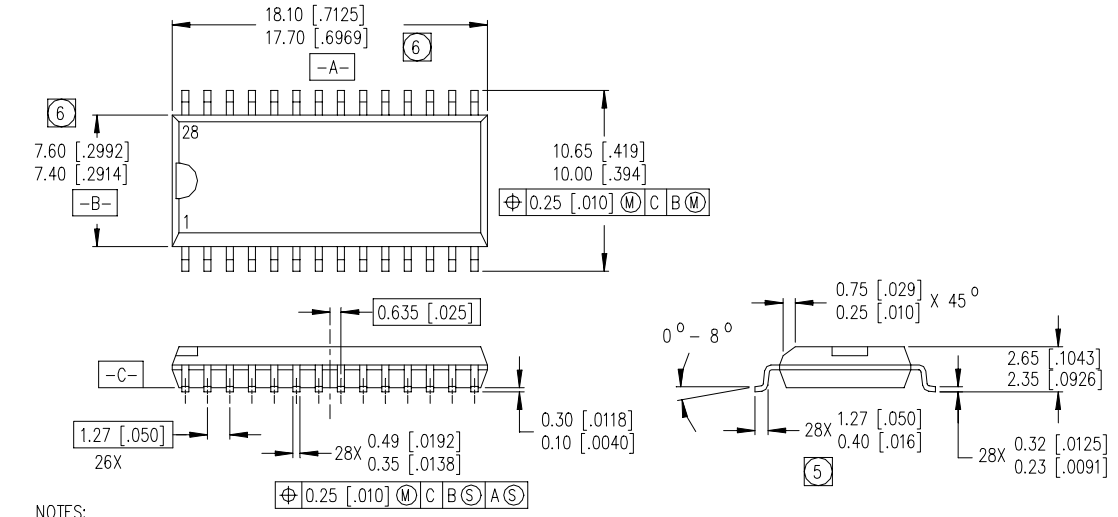
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

28-Lead PDIP (wide body)

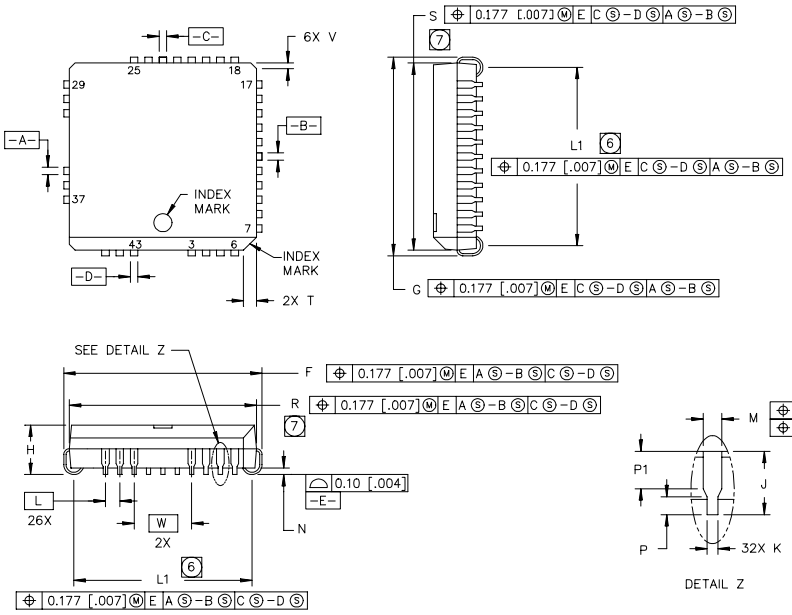
01-6011
01-3024 02 (MS-011AB)



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–013AE.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

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