

MOSFET

OptiMOS™ 7 Power-Transistor, 15 V

Features

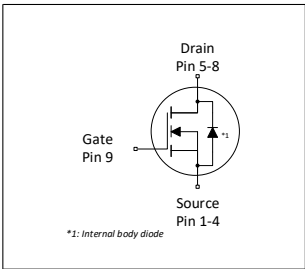
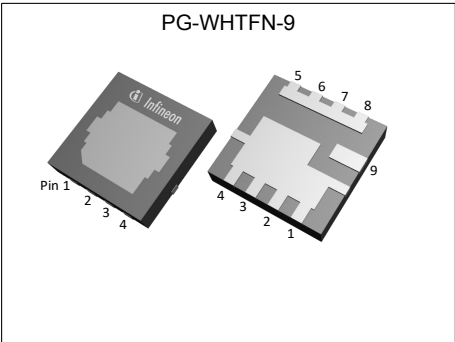
- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Optimized for high performance SMPS, e.g. synchronous rectification

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	15	V
$R_{DS(on),max}$	0.45	mΩ
I_D	379	A
Q_{oss}	27	nC
Q_G	29	nC



Type / Ordering Code	Package	Marking	Related Links
IQE004NE1LM7CGSC	PG-WHTFN-9	H	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	379 240 58	A	$V_{GS}=7\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=7\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=7\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1516	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	859	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Recommended gate source voltage	V_{GS}	-7	-	7	V	-
Gate source voltage, transient	$V_{GS,AC}$	-8	-	8	V	$t_{pulse}<20\text{ ns}$
Power dissipation	P_{tot}	-	-	89 2.1	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.4	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	0.7	-	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	60	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for source connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	15	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	$V_{DS}=V_{GS}$, $I_D=432\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=7\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.37 0.47	0.45 0.57	m Ω	$V_{GS}=7\text{ V}$, $I_D=30\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
Gate resistance	R_G	-	0.4	-	Ω	-
Transconductance	g_{fs}	85	170	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=30\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4800	6240	pF	$V_{GS}=0\text{ V}$, $V_{DS}=7.5\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	2600	3380	pF	$V_{GS}=0\text{ V}$, $V_{DS}=7.5\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	260	455	pF	$V_{GS}=0\text{ V}$, $V_{DS}=7.5\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	2	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	21	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	4	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge ¹⁾	Q_{gs}	-	13	18.8	nC	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold ¹⁾	$Q_{g(th)}$	-	7.6	11	nC	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	5.7	5.5	nC	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	11.1	-	nC	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	29	36	nC	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.7	-	V	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	44	55	nC	$V_{DD}=7.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }7\text{ V}$
Output charge ¹⁾	Q_{oss}	-	27	36	nC	$V_{DS}=7.5\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	87	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1516	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.76	1.0	V	$V_{GS}=0\text{ V}$, $I_F=30\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	31	62	ns	$V_R=7.5\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	24	48	nC	$V_R=7.5\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time ¹⁾	t_{rr}	-	25	50	ns	$V_R=7.5\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=300\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	49	98	nC	$V_R=7.5\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=300\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

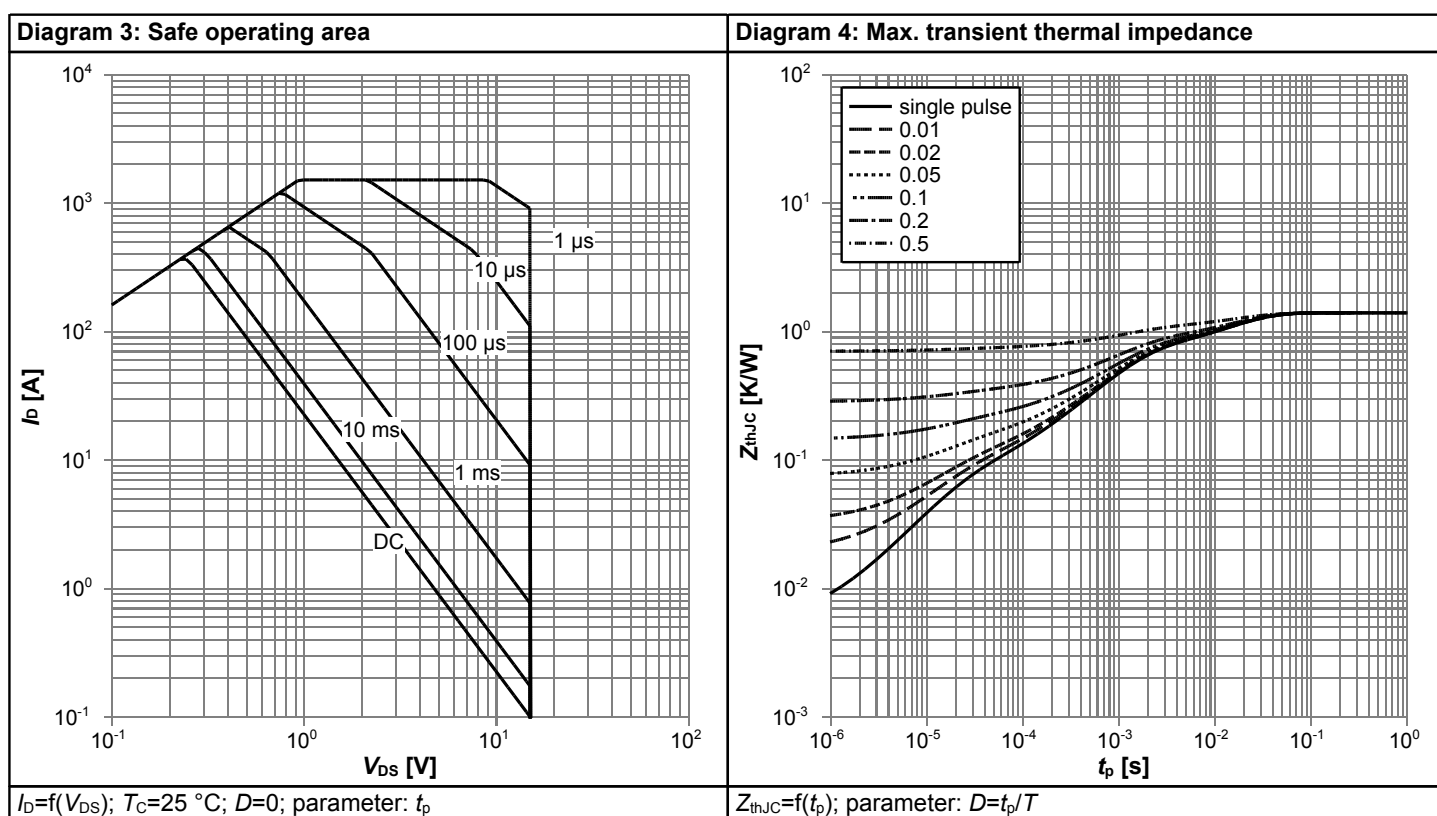
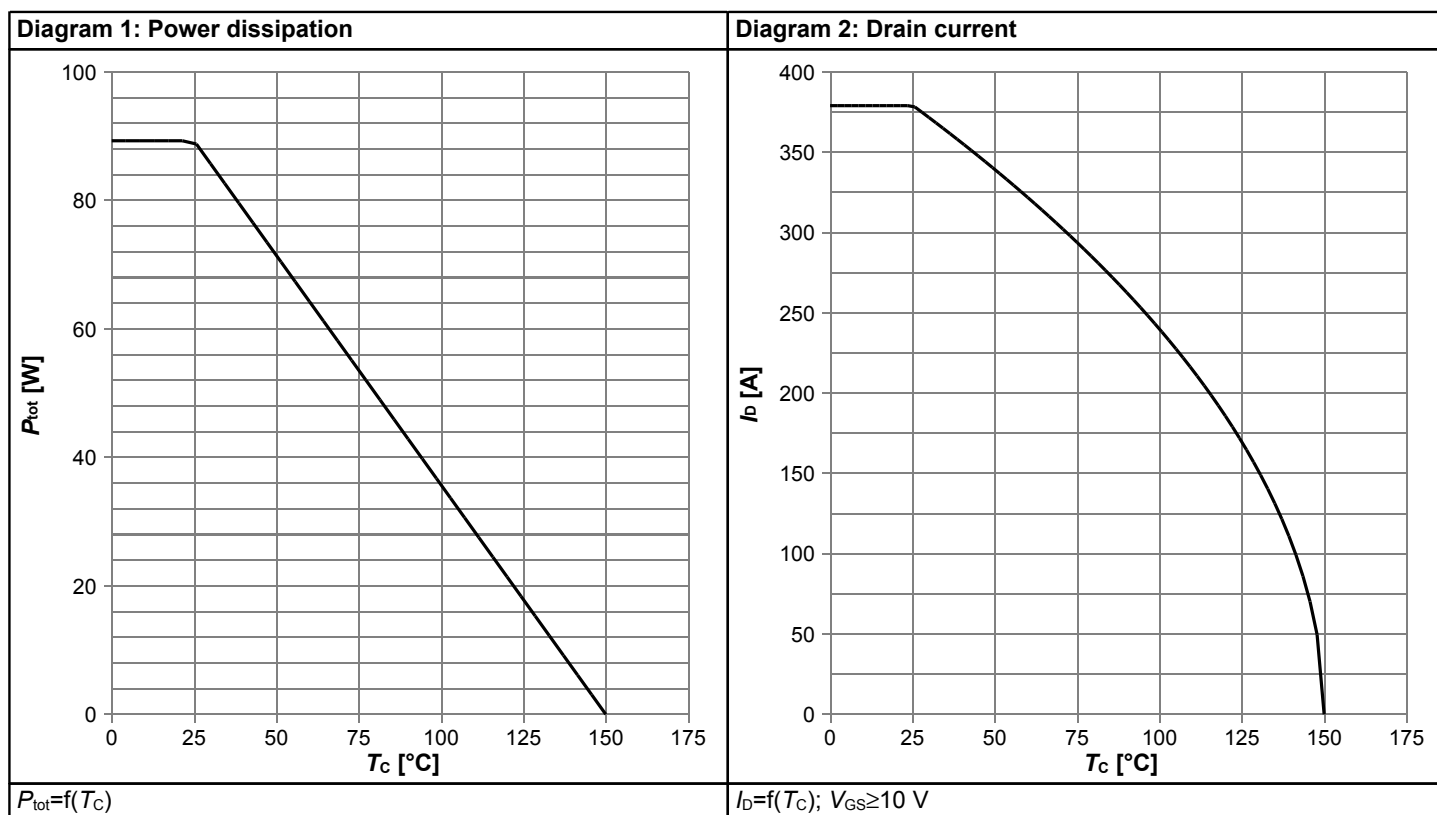
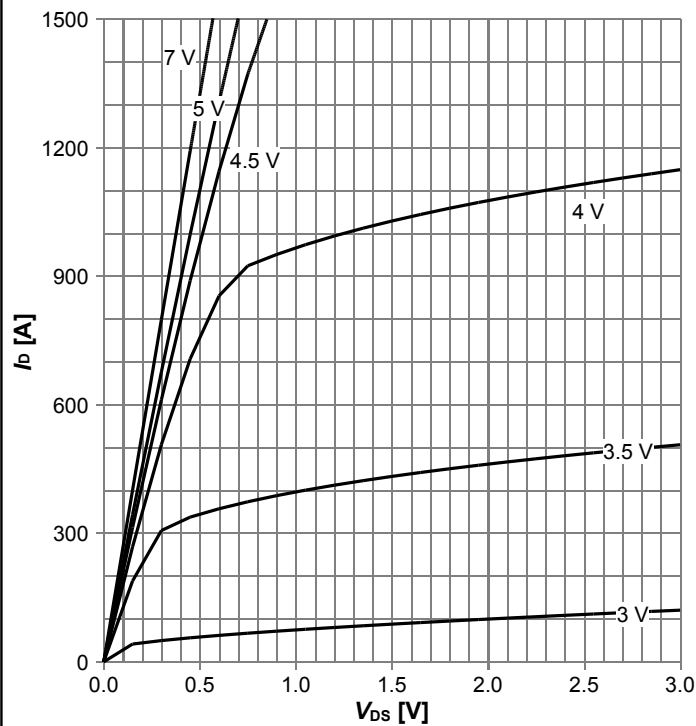
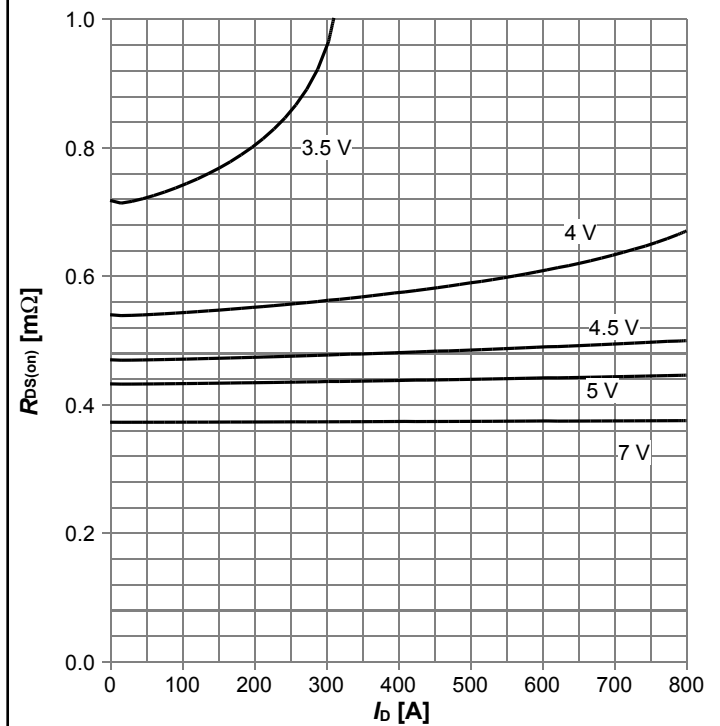


Diagram 5: Typ. output characteristics



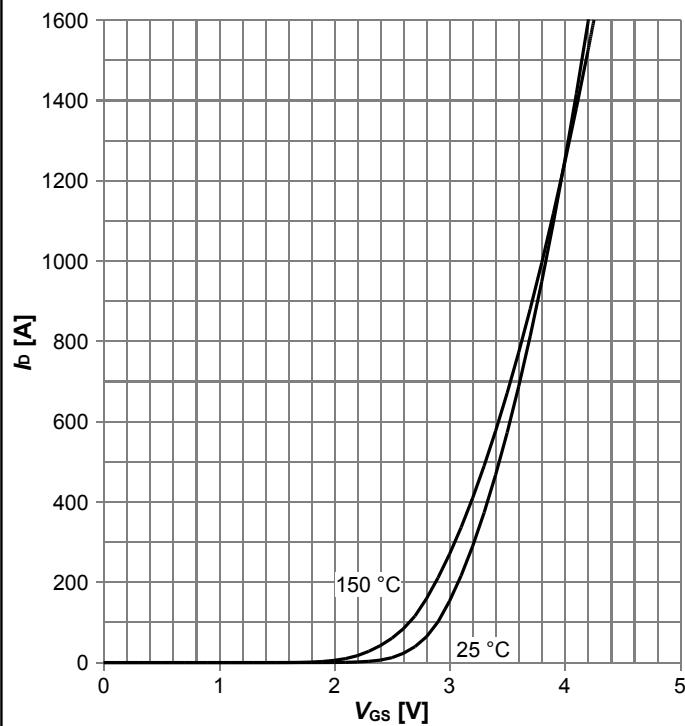
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



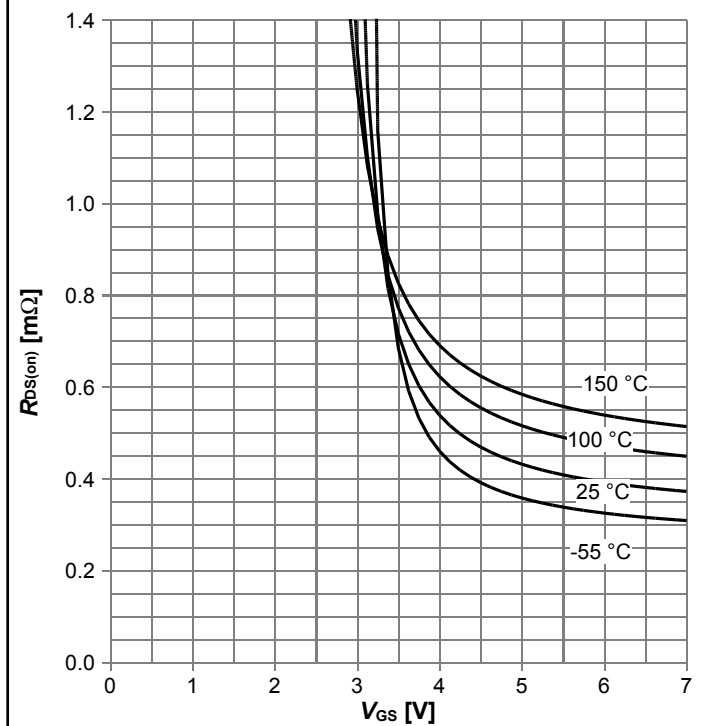
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



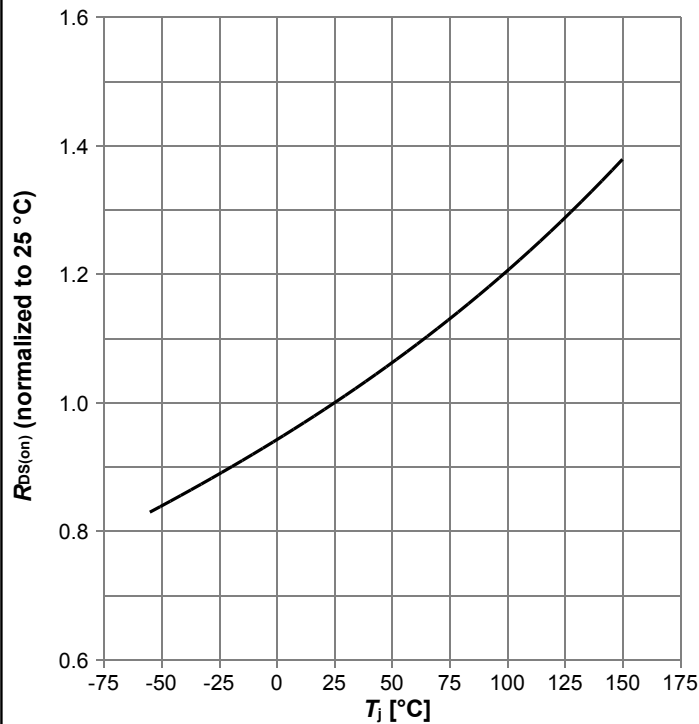
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



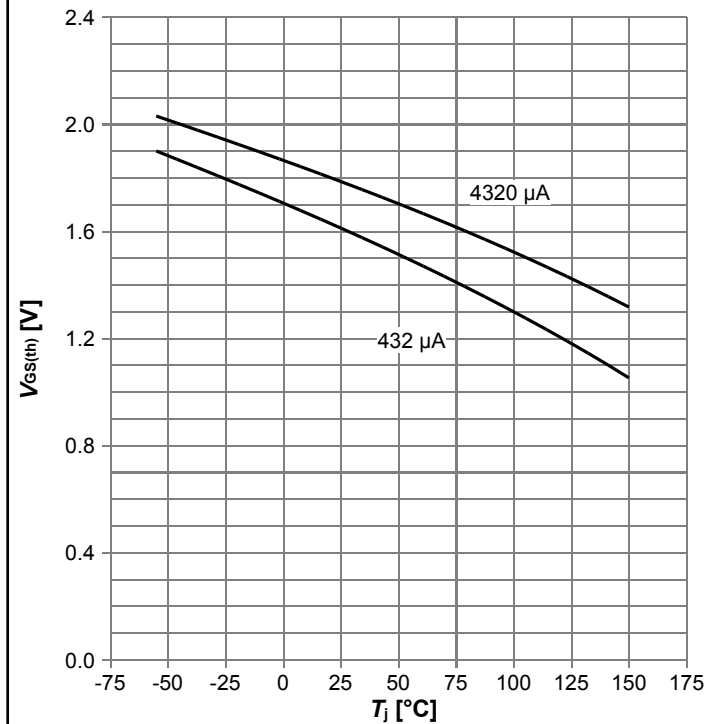
$R_{DS(on)} = f(V_{GS})$, $I_D = 30\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



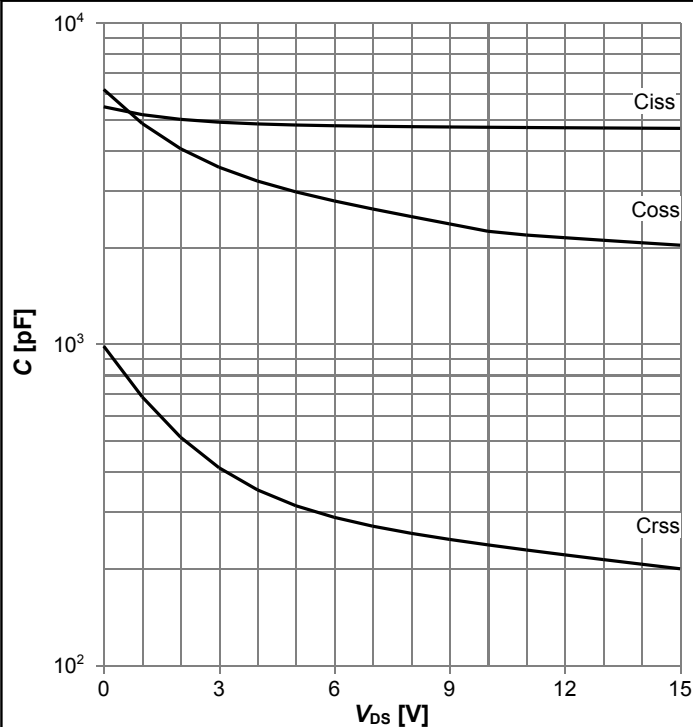
$R_{DS(on)}=f(T_j)$, $I_D=30$ A; parameter: V_{GS}

Diagram 10: Typ. gate threshold voltage



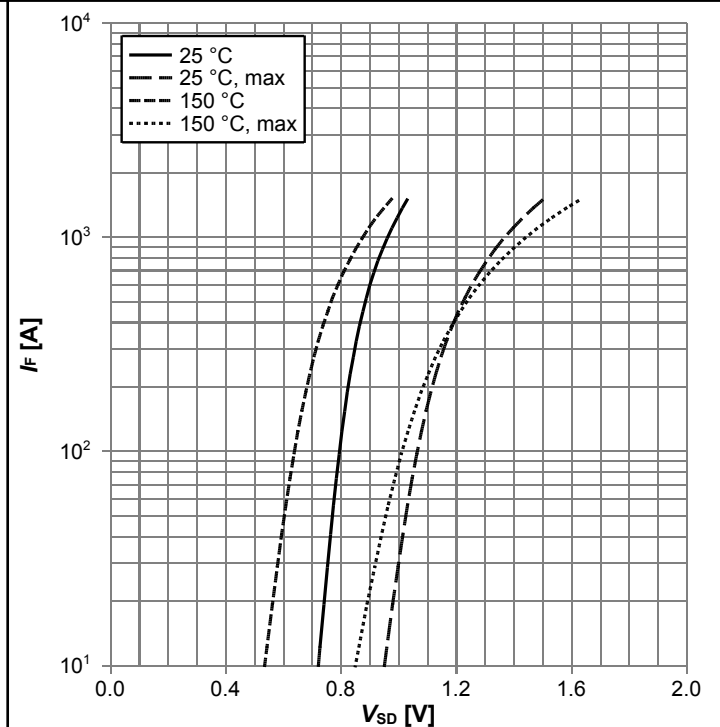
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode

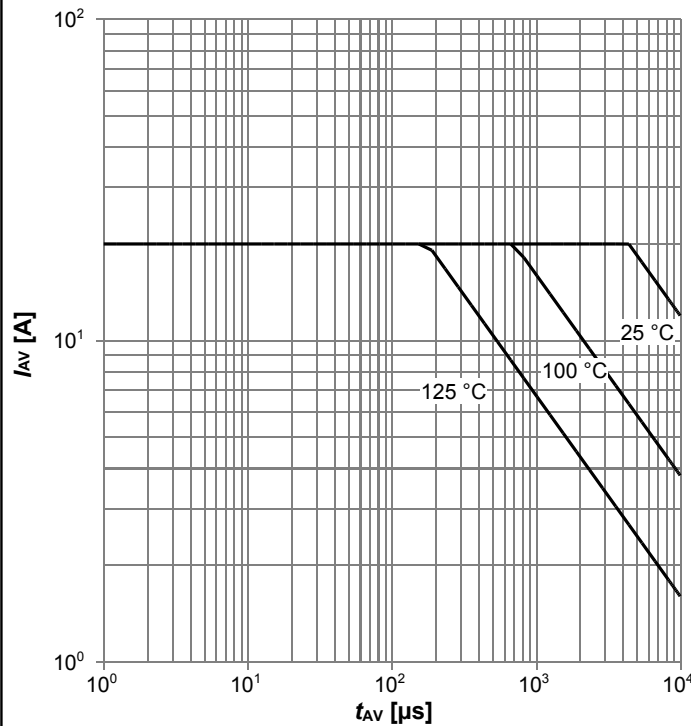


$I_F=f(V_{SD})$; parameter: T_j

OptiMOS™ 7 Power-Transistor, 15 V

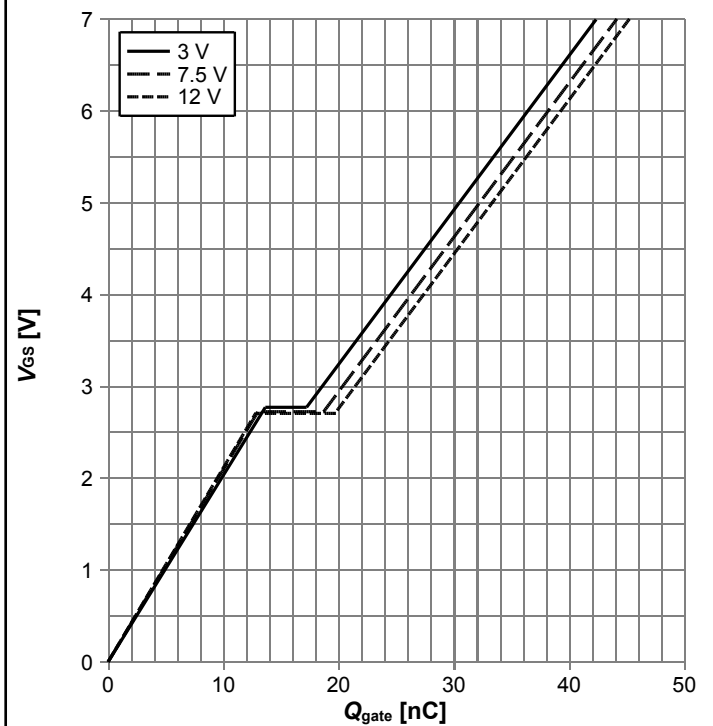
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Diagram 13: Avalanche characteristics



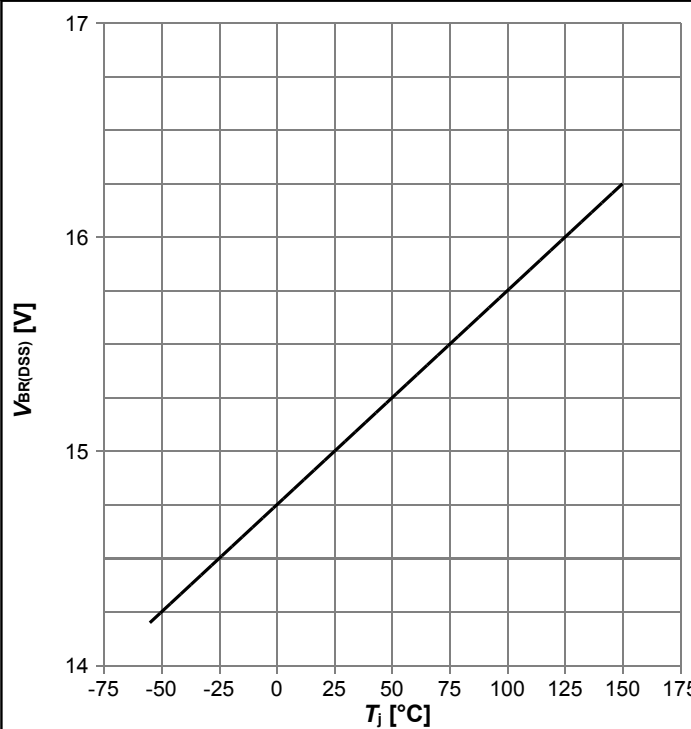
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



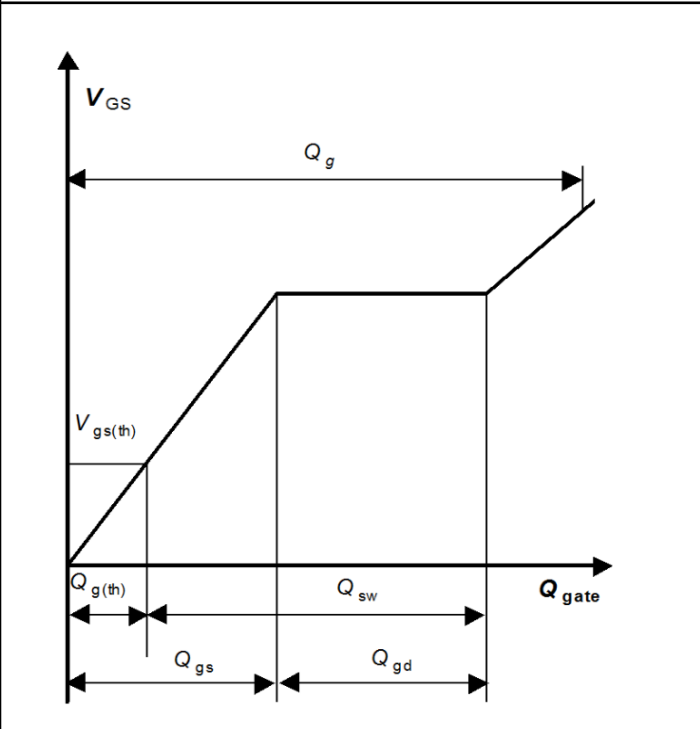
$V_{GS}=f(Q_{gate})$, $I_D=30\ A$ pulsed, $T_j=25\ ^\circ C$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\ mA$

Diagram Gate charge waveforms



5 Package Outlines

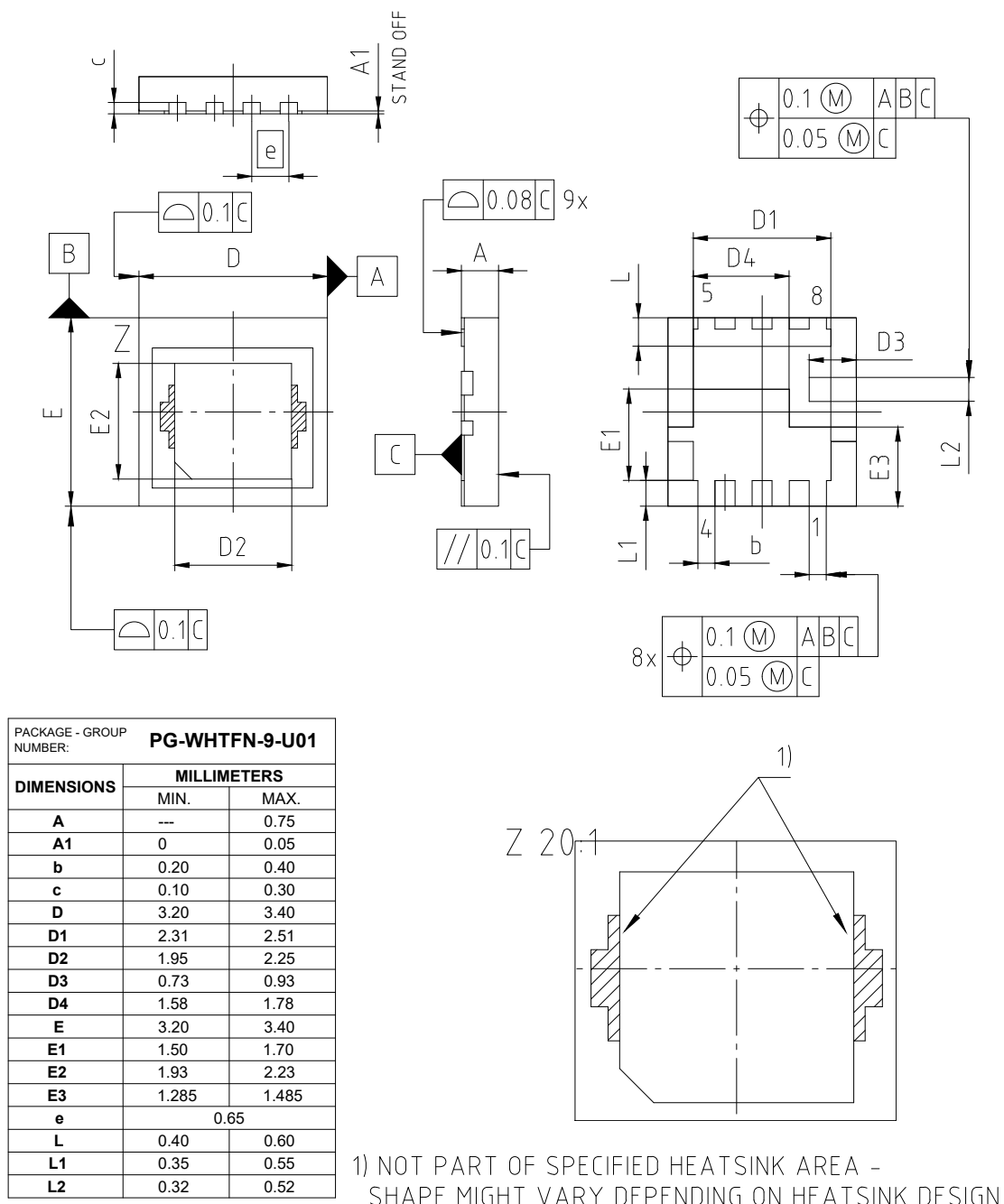


Figure 1 Outline PG-WHTFN-9, dimensions in mm

Revision History

IQE004NE1LM7CGSC

Revision: 2023-07-25, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-07-25	Release of final version

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Published by

Infineon Technologies AG

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