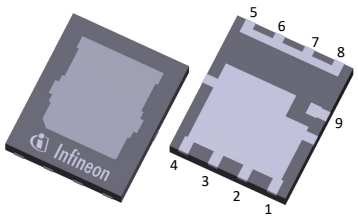
MOSFET

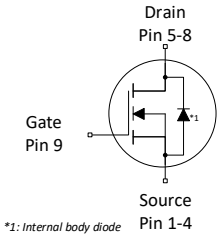
OptiMOS™ 5 Power-Transistor, 25 V

PG-WHTFN-9



Features

- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- Optimized design for double side cooling
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

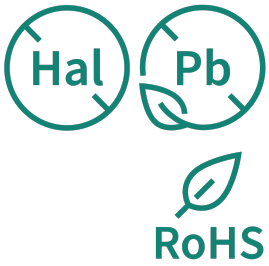


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	0.29	mΩ
I_D	789	A
Q_{oss}	127	nC
Q_G	88	nC



Type/Ordering Code	Package	Marking	Related Links
IQDH29NE2LM5CGSC	PG-WHTFN-9	KA	-

Table of Contents

1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	789 499 454 75	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	3156	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	1200	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	-	-	278 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for source connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.45	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	0.56	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}	-	-	50	°C/W	-

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for source connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	V_{DS}=V_{GS}, I_D=1448 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=20 V, V_{GS}=0 V, T_j=25 °C V_{DS}=20 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=16 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.2 0.3	0.29 0.35	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=50 A
Gate resistance	R_G	-	0.46	-	Ω	-
Transconductance	g_{fs}	305	610	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	13000	17000	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Output capacitance [6]	C_{oss}	-	5400	7000	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Reverse transfer capacitance [6]	C_{rss}	-	380	660	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	6	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	77	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	19	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

[6] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	28	-	nC	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	20	-	nC	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate to drain charge [8]	Q_{gd}	-	17	25	nC	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	25	-	nC	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total [8]	Q_g	-	88	110	nC	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.2	-	V	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total [8]	Q_g	-	191	254	nC	V_{DD}=12 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	84	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge [8]	Q_{oss}	-	127	169	nC	V_{DS}=12 V, V_{GS}=0 V

[7] See "Gate charge waveforms" for parameter definition

[8] Defined by design. Not subject to production test.

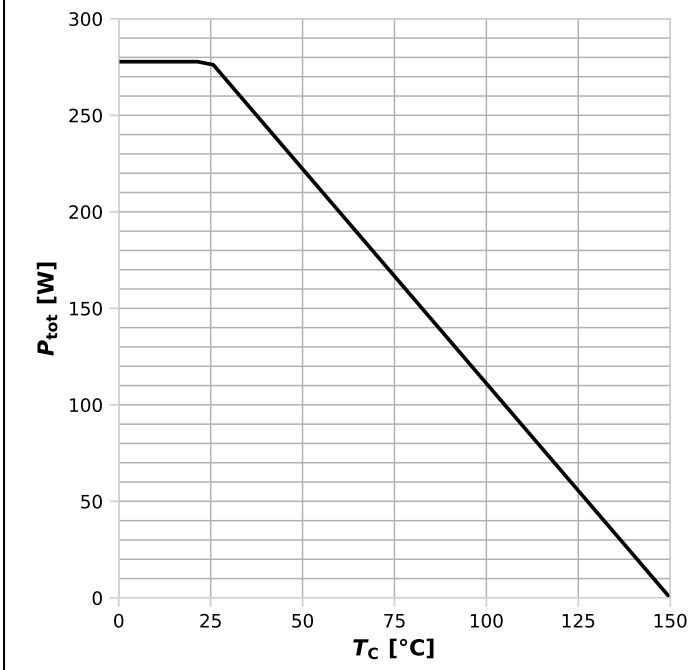
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	244	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	3156	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.74	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [9]	t_{rr}	-	59	118	ns	V_R=12 V, I_F=25 A, di_F/dt=100 A/µs
Reverse recovery charge [9]	Q_{rr}	-	120	240	nC	V_R=12 V, I_F=25 A, di_F/dt=100 A/µs
Reverse recovery time [9]	t_{rr}	-	39	78	ns	V_R=12 V, I_F=50 A, di_F/dt=500 A/µs
Reverse recovery charge [9]	Q_{rr}	-	203	406	nC	V_R=12 V, I_F=50 A, di_F/dt=500 A/µs

[9] Defined by design. Not subject to production test.

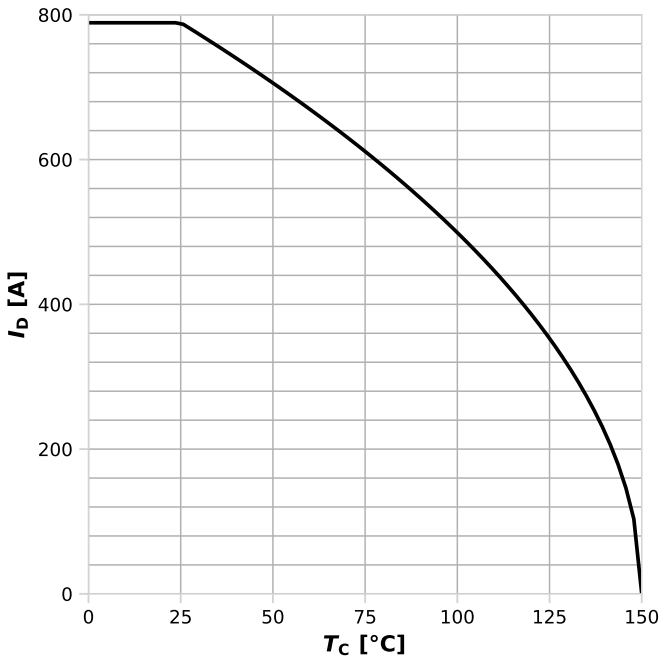
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



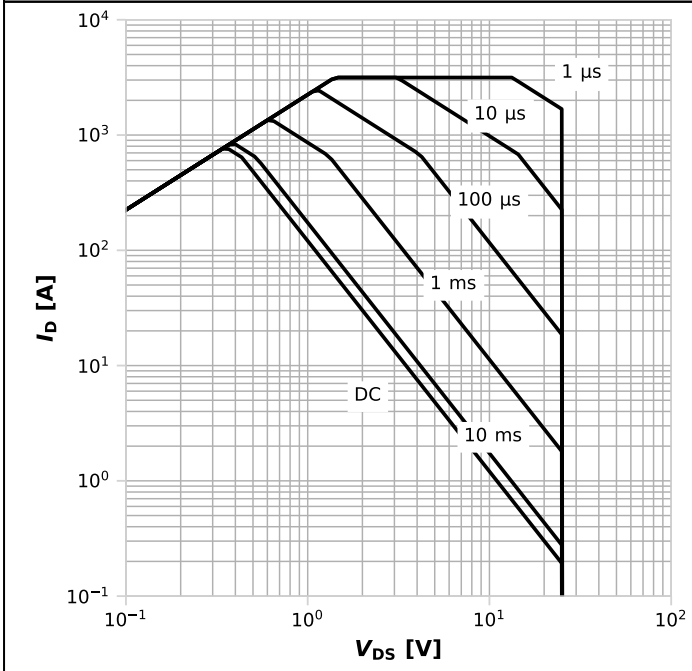
P_{tot}=f(T_C)

Diagram 2: Drain current



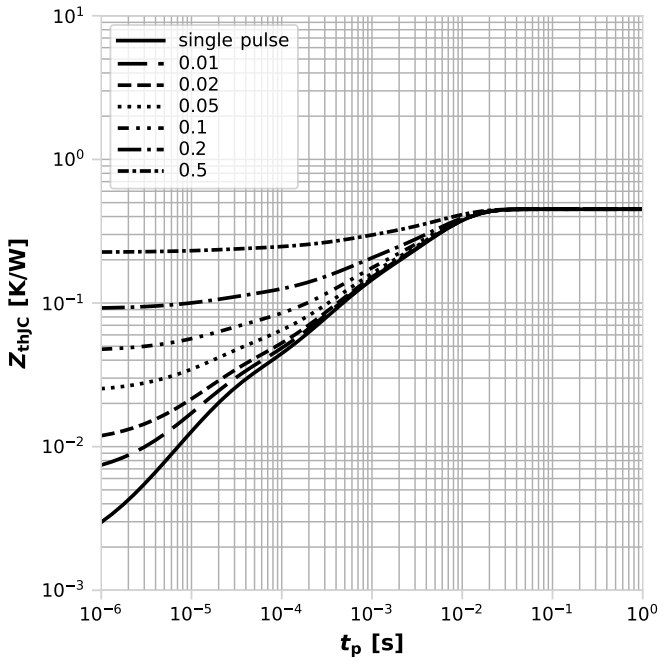
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



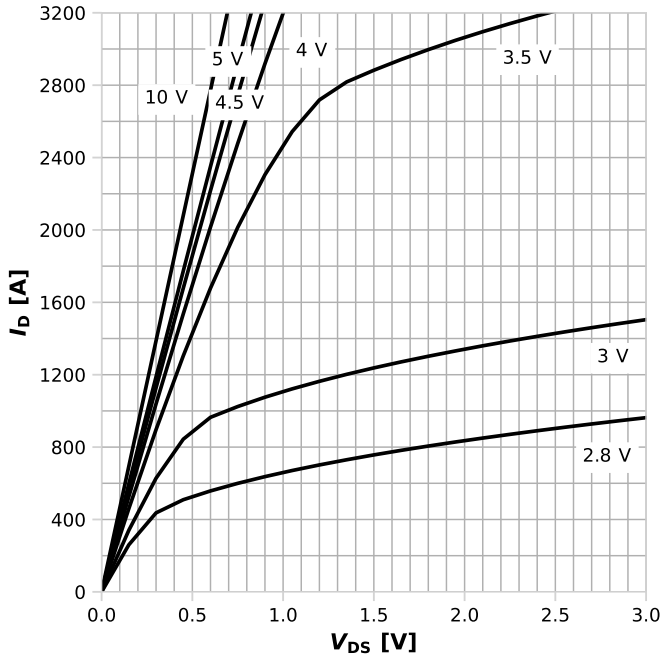
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



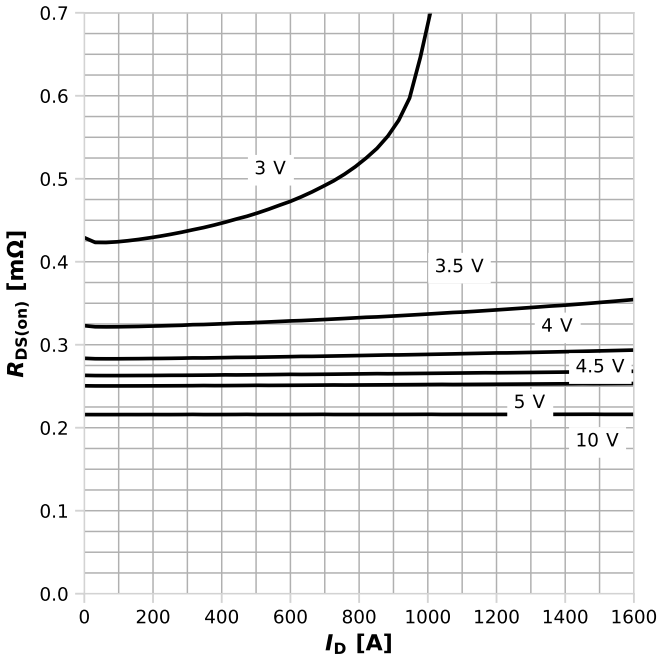
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



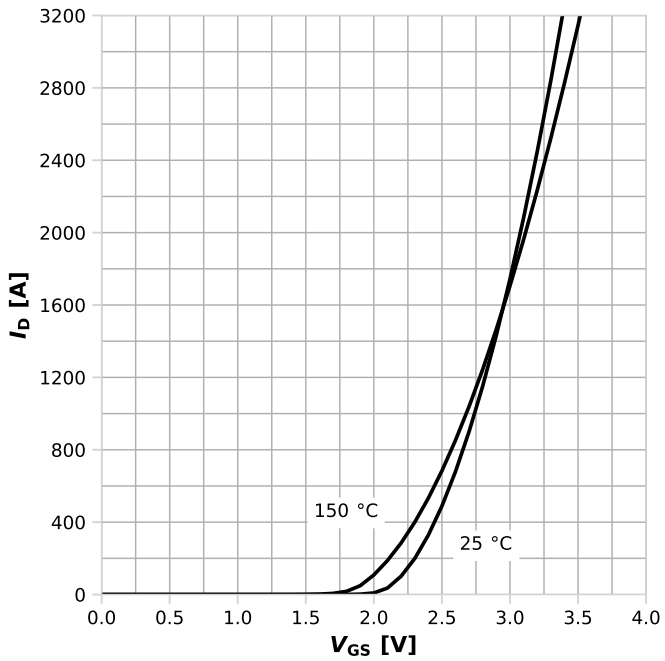
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



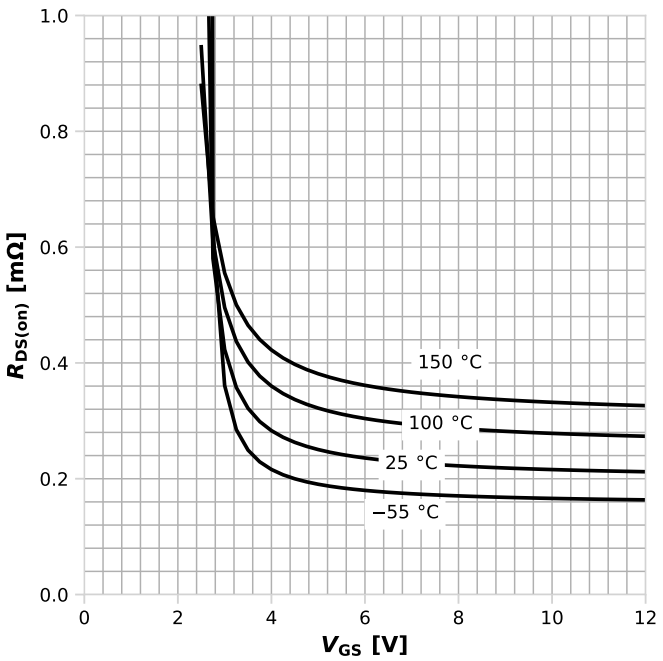
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

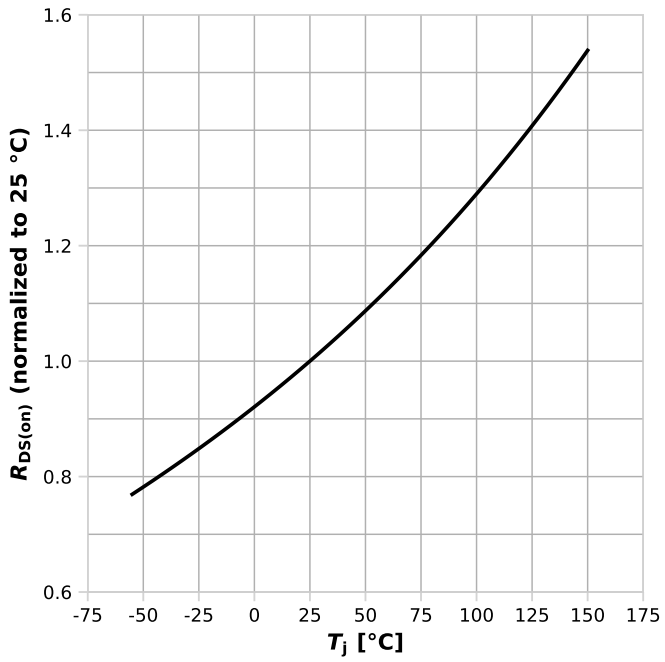
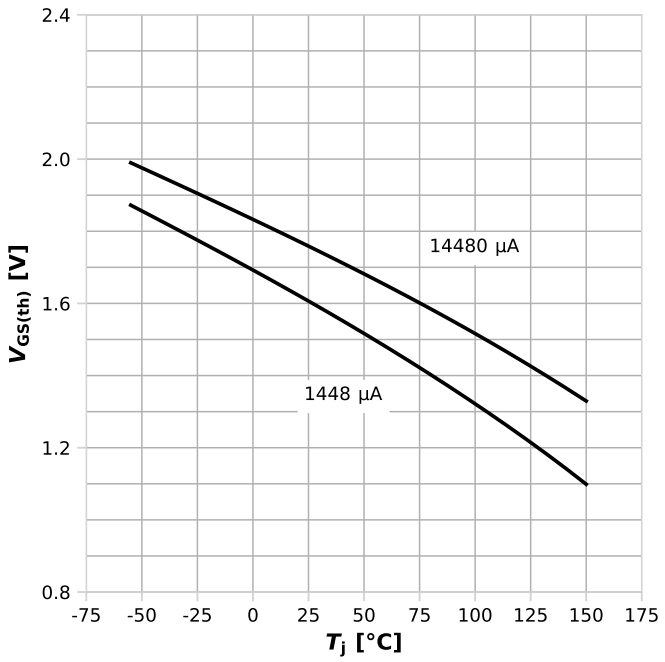
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

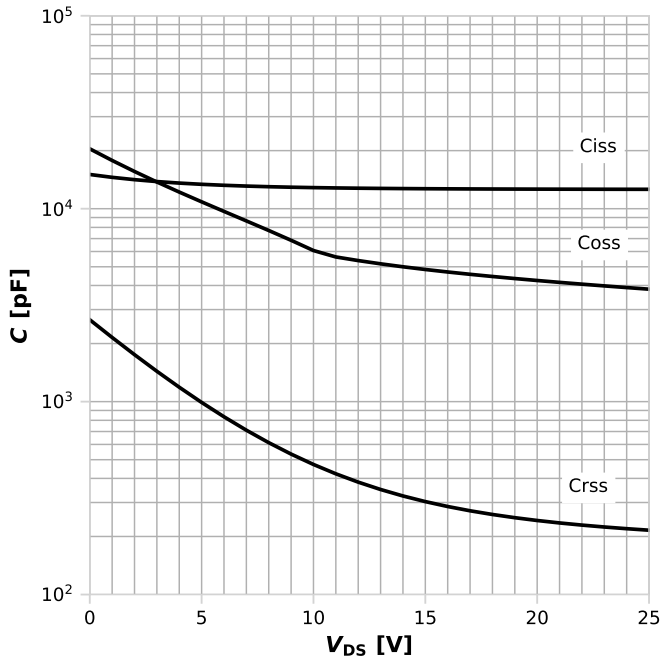
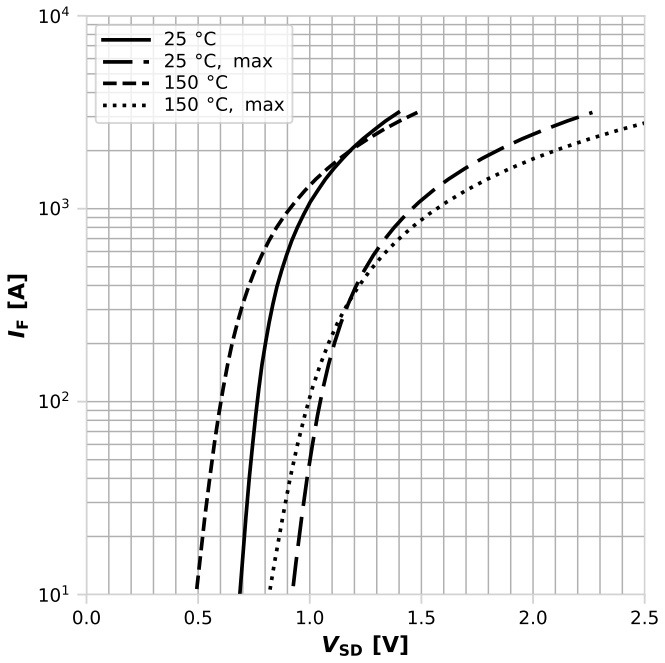
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

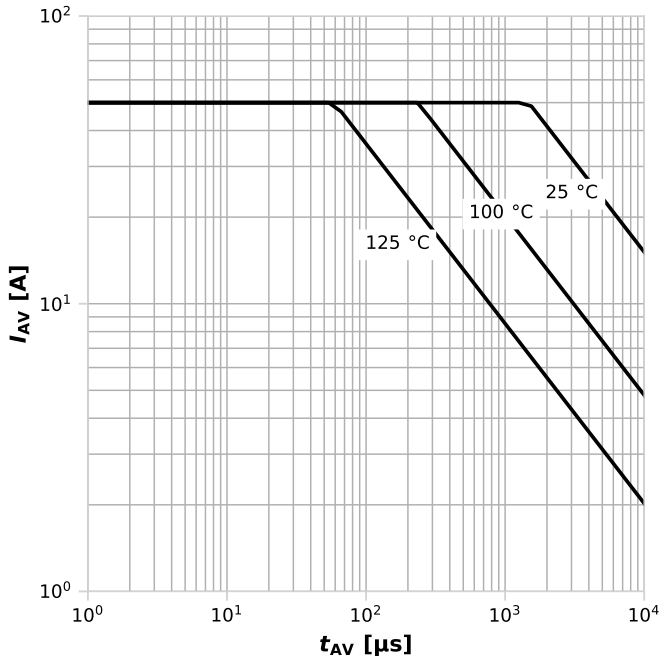
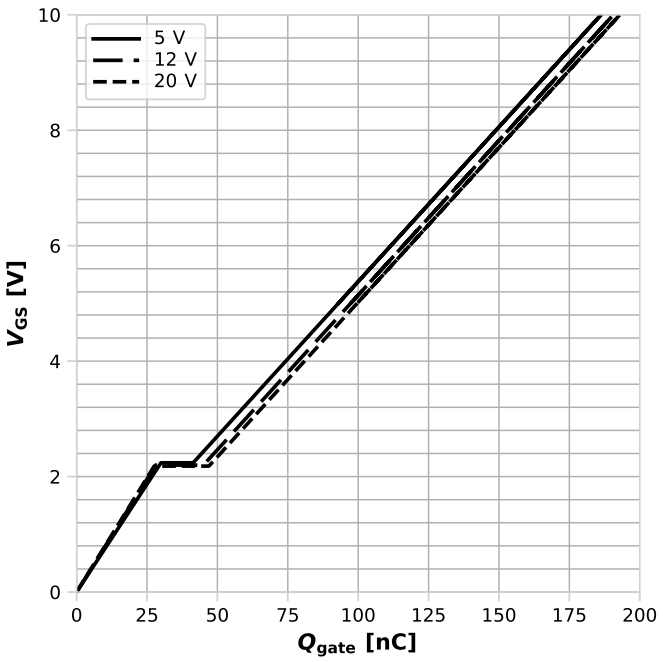
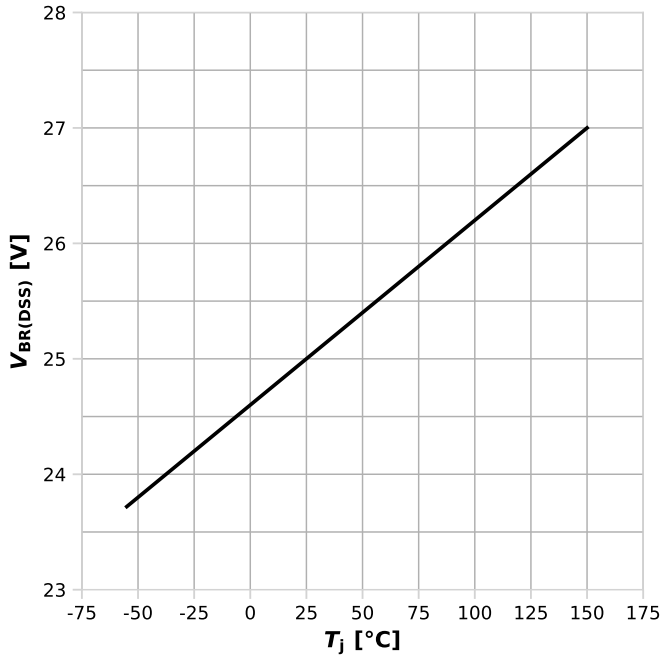
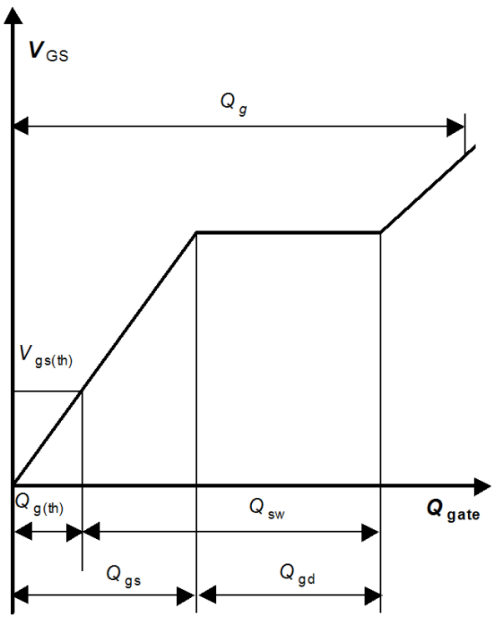
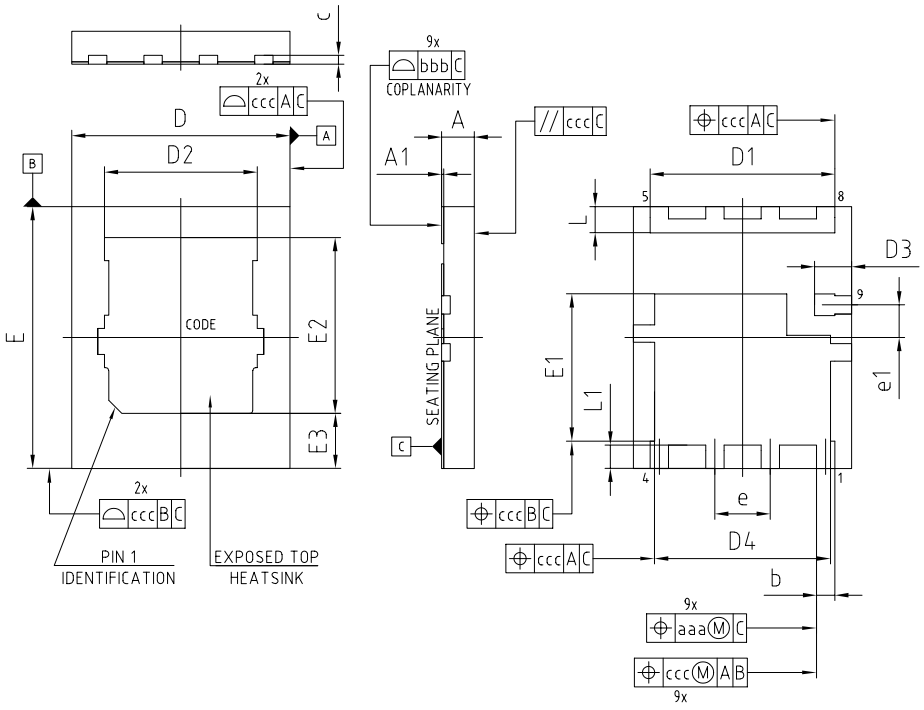
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-WHTFN-9-U02				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.55	0.75	e	1.27	
A1	0.00	0.05	e1	0.75	
b	0.32	0.52	L	0.50	0.70
c	0.10	0.30	L1	0.44	0.64
D	5.00		aaa	0.05	
D1	4.13	4.33	bbb	0.08	
D2	3.40	3.60	ccc	0.10	
D3	0.75	0.95			
D4	3.93	4.13			
E	6.00				
E1	3.28	3.48			
E2	3.93	4.13			
E3	1.16	1.36			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-WHTFN-9, dimensions in mm

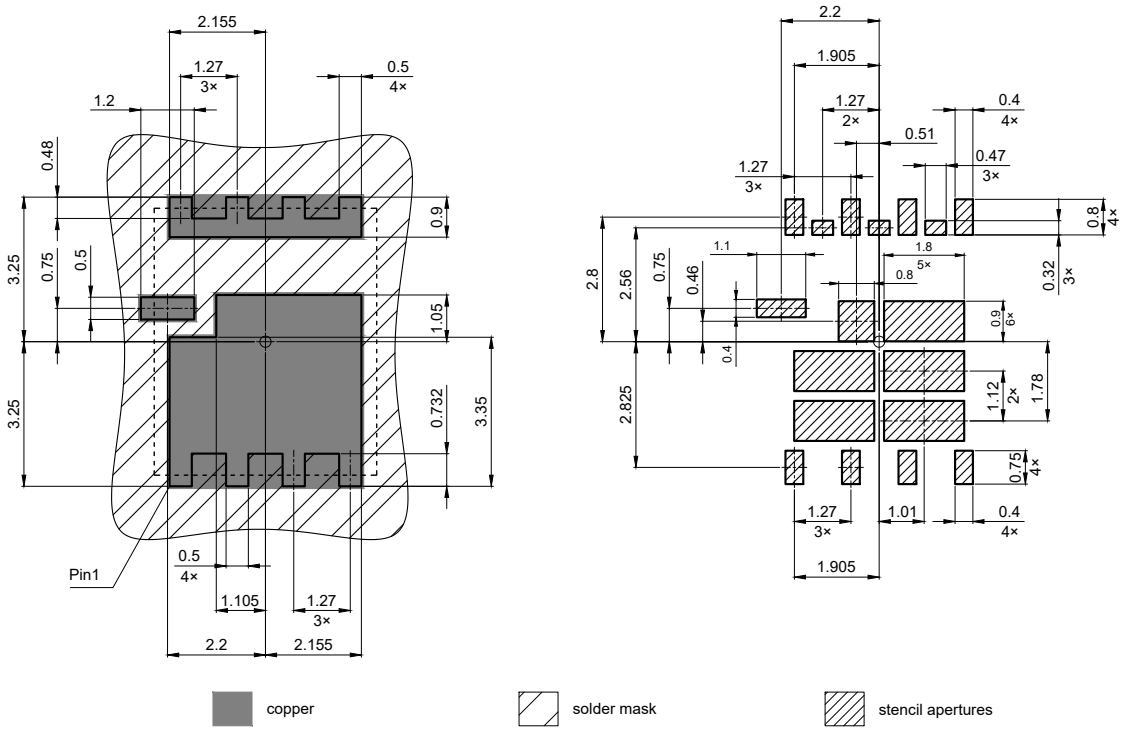


Figure 2 Outline PG-WHTFN-9, dimensions in mm

Revision History

IQDH29NE2LM5CGSC

Revision 2024-06-17, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-06-17	Release of final

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