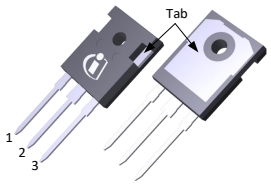
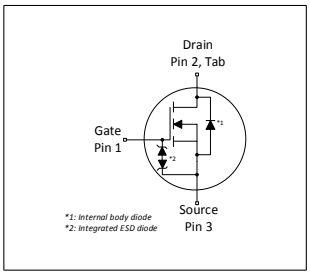
MOSFET

650V CoolMOS™ CFD7 SJ Power Device

PG-TO 247-3



The latest 650 V CoolMOS™ CFD7 extends the voltage class offering of the CFD7 family and is a successor to the 650 V CoolMOS™ CFD2. Resulting from improved switching performance and excellent thermal behavior, 650 V CooMOS™ CFD7 offers highest efficiency in resonant switching topologies, such as LLC and phase-shift-full-bridge (ZVS). As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions.



Features

- Ultra-fast body diode
- 650V break down voltage
- Best-in-class $R_{DS(on)}$
- Reduced switching losses
- Low $R_{DS(on)}$ dependency over temperature

Benefits

- Excellent hard commutation ruggedness
- Extra safety margin for designs with increased bus voltage
- Enabling increased power density solutions
- Outstanding light load efficiency in industrial SMPS applications
- Improved full load efficiency in industrial SMPS applications
- Price competitiveness over previous CoolMOS™ families

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging, Solar

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	110	mΩ
$Q_{g,typ}$	41	nC
$I_{D,pulse}$	82	A
E_{oss} @ 400V	5.8	µJ
Body diode di_F/dt	1300	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPW65R110CFD7	PG-TO247-3	65R110F7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	22 14	A	T_C=25°C T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	82	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	97	mJ	I_D=4.7A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.48	mJ	I_D=4.7A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	4.7	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	114	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current[1)]	I_S	-	-	22	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	82	A	T_C=25°C
Reverse diode dv/dt[3)]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}<=9.7A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	1300	A/µs	V_{DS}=0...400V, I_{SD}<=9.7A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1)] Limited by $T_{j\,max}$.
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.1	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=0.48mA
Zero gate voltage drain current[1]	I_{DSS}	- -	- 8	1 37	µA	V_{DS}=650V, V_{GS}=0V, T_j=25°C V_{DS}=650V, V_{GS}=0V, T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	1000	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.087 0.194	0.110 -	Ω	V_{GS}=10V, I_D=9.7A, T_j=25°C V_{GS}=10V, I_D=9.7A, T_j=150°C
Gate resistance	R_G	-	6.0	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1942	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	32	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	-	73	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[3]	$C_{o(tr)}$	-	751	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8Ω; see table 9
Rise time	t_r	-	9	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	71	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8Ω; see table 9
Fall time	t_f	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=9.7A, R_G=1.8Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	11	-	nC	V_{DD}=400V, I_D=9.7A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	13	-	nC	V_{DD}=400V, I_D=9.7A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	41	-	nC	V_{DD}=400V, I_D=9.7A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=400V, I_D=9.7A, V_{GS}=0 to 10V

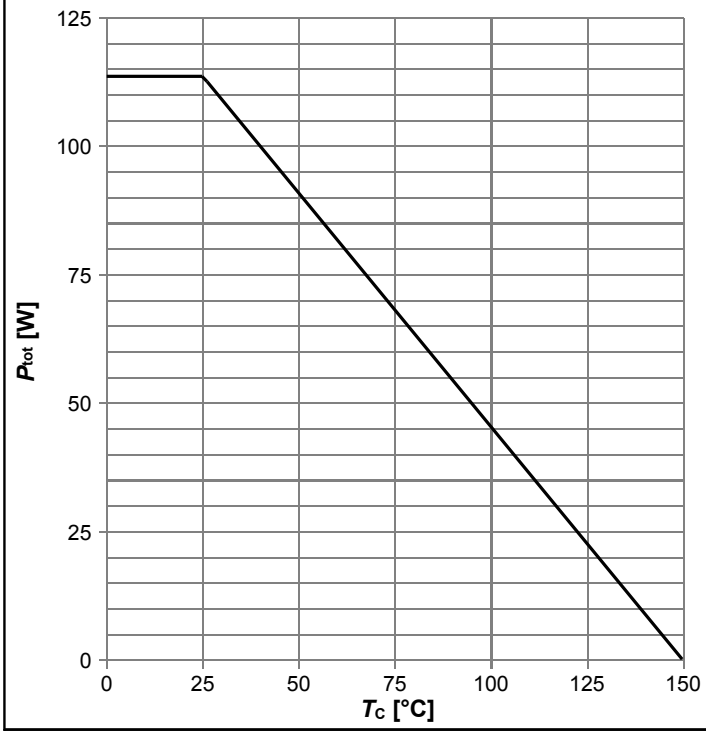
[1] Maximum specification is defined by calculated six sigma upper confidence bound
[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	V_{GS}=0V, I_F=9.7A, T_j=25°C
Reverse recovery time	t_{rr}	-	110	165	ns	V_R=400V, I_F=9.7A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	0.56	1.12	µC	V_R=400V, I_F=9.7A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	8.7	-	A	V_R=400V, I_F=9.7A, di_F/dt=100A/µs; see table 8

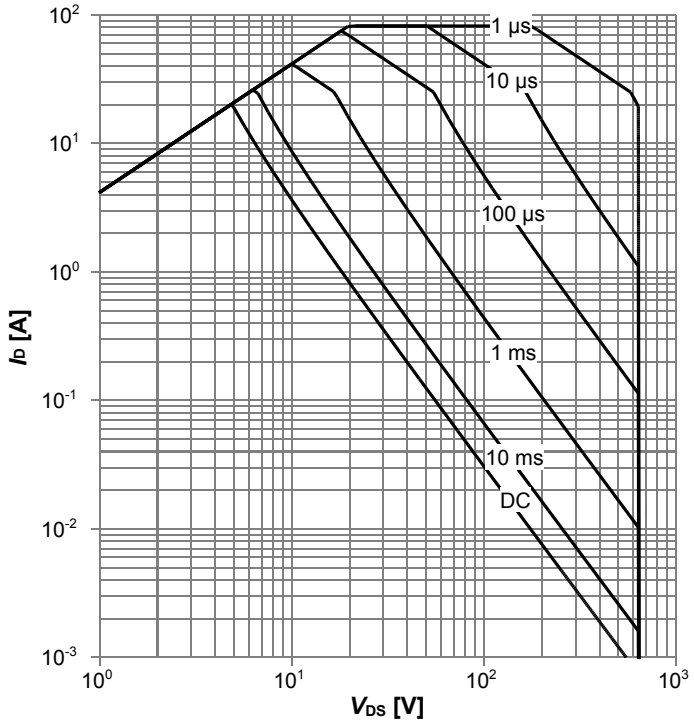
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



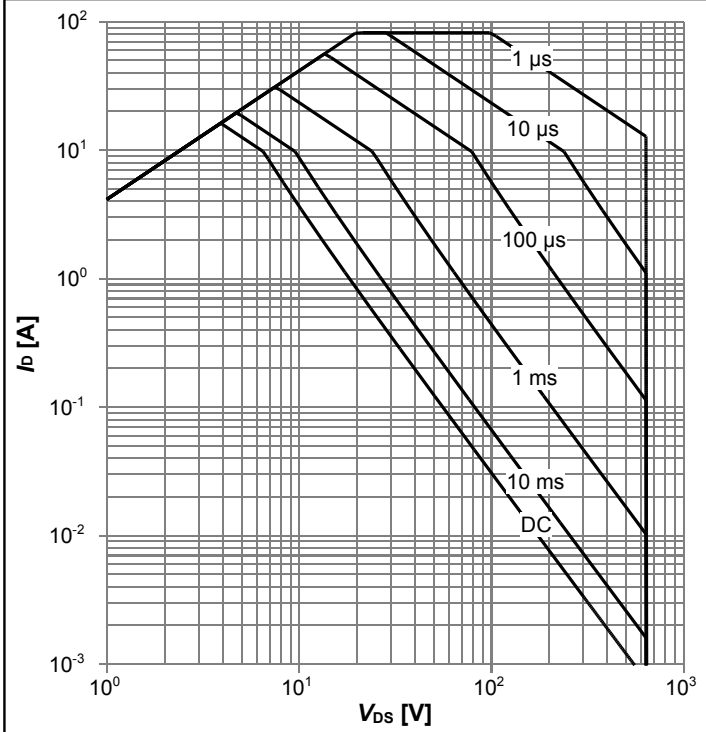
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



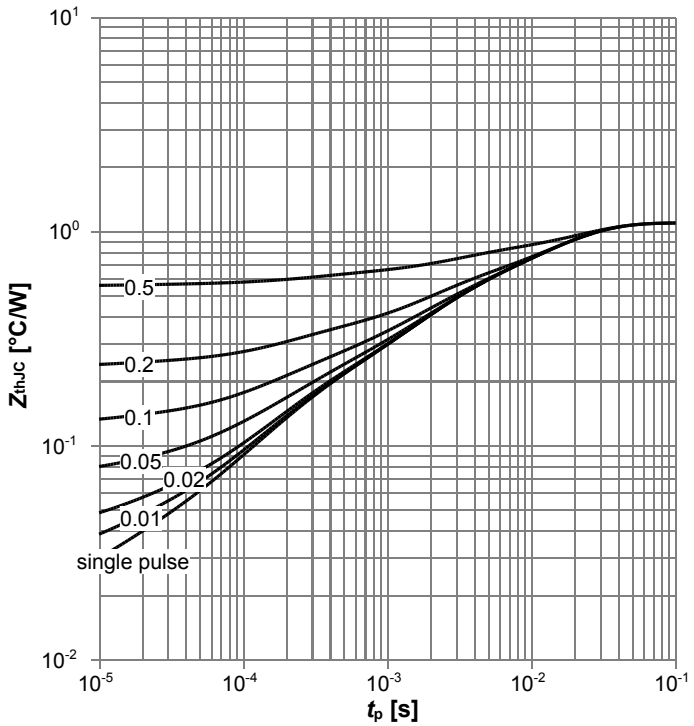
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



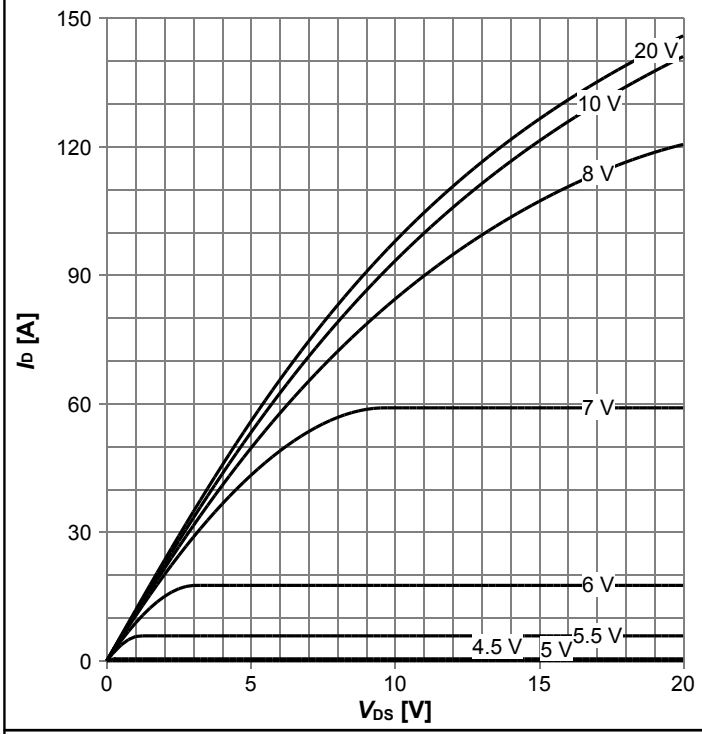
$I_D=f(V_{DS})$; T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



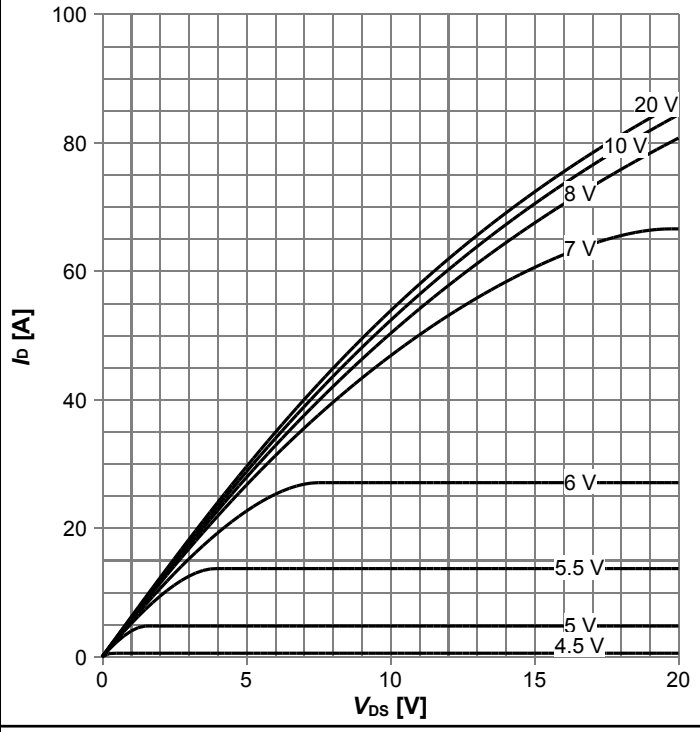
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



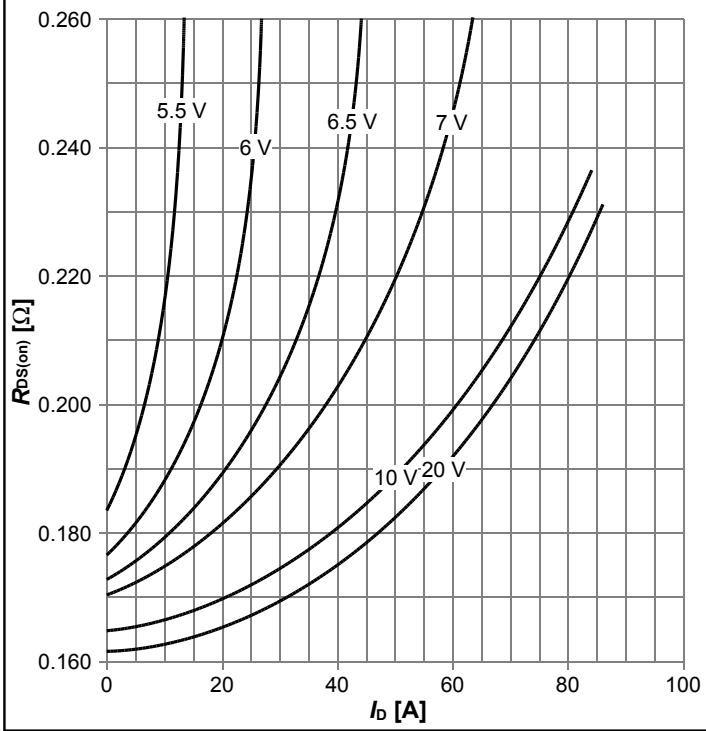
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



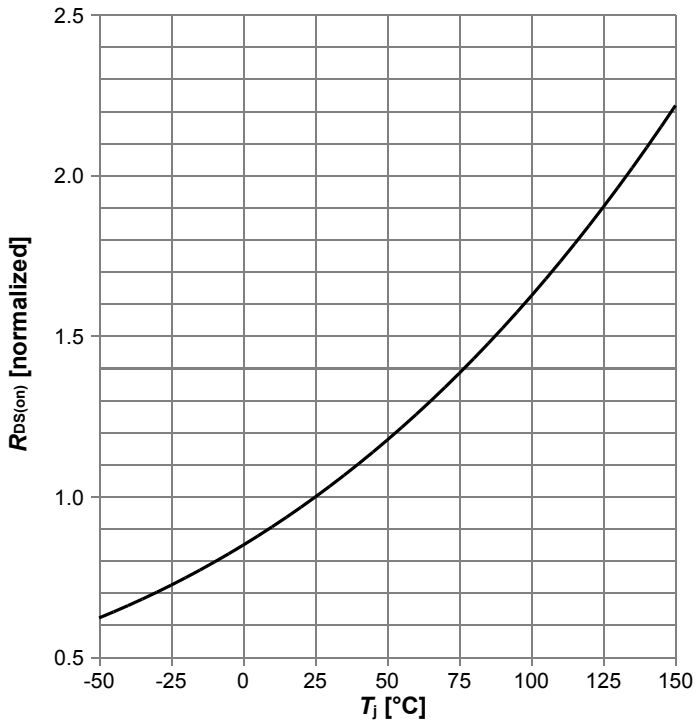
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



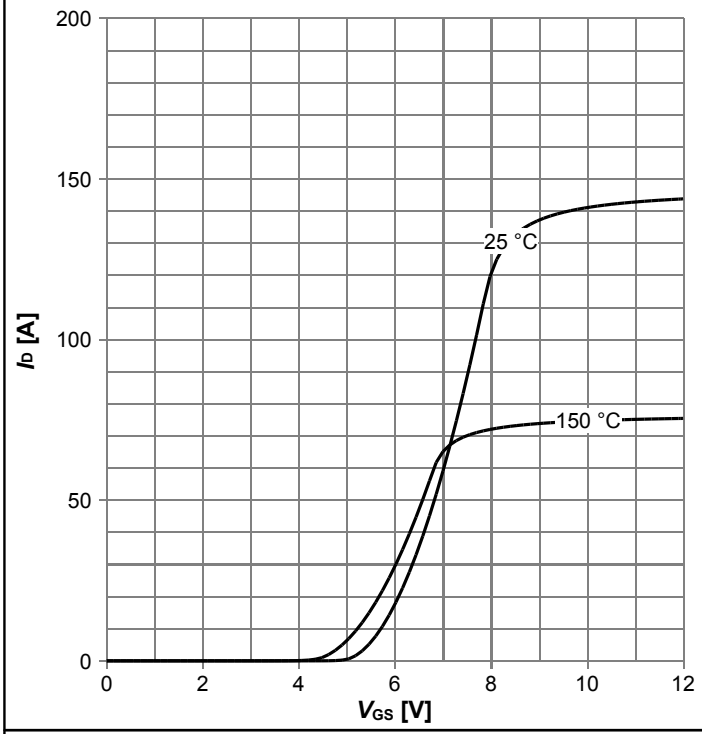
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



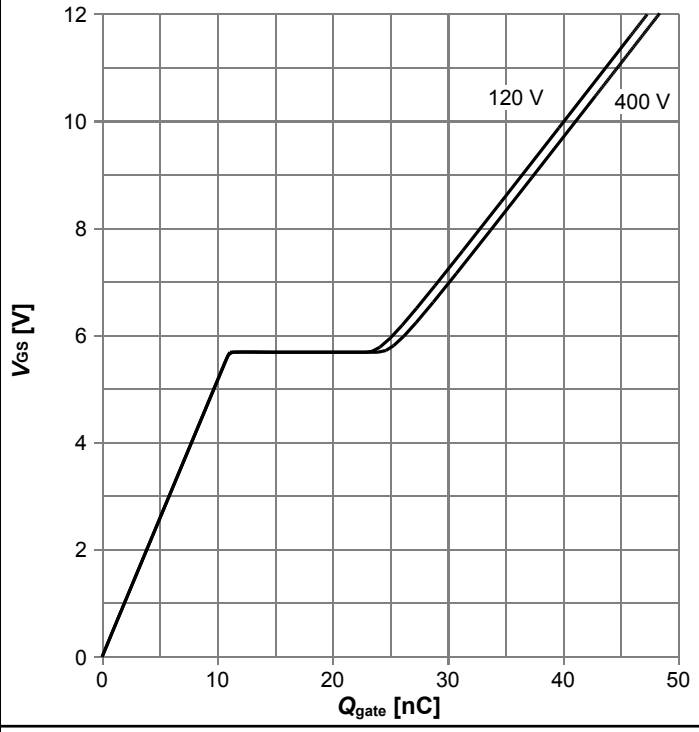
$R_{DS(on)}=f(T_j)$; $I_D=9.7$ A; $V_{GS}=10$ V

Diagram 9: Typ. transfer characteristics



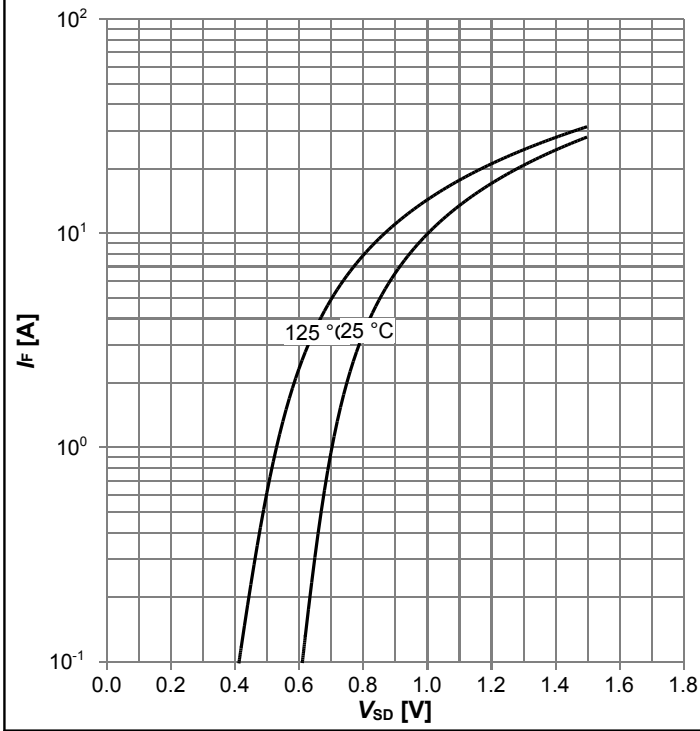
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



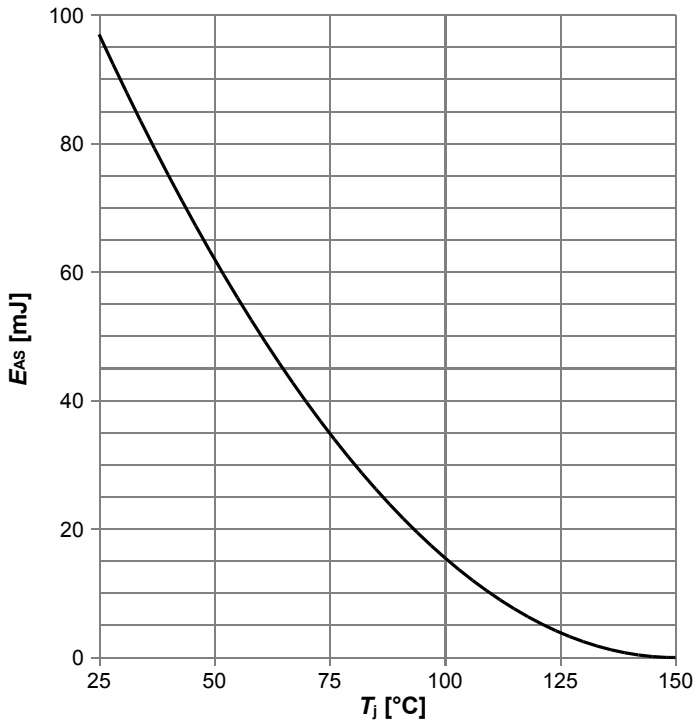
V_{GS}=f(Q_{gate}); I_D=9.7 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



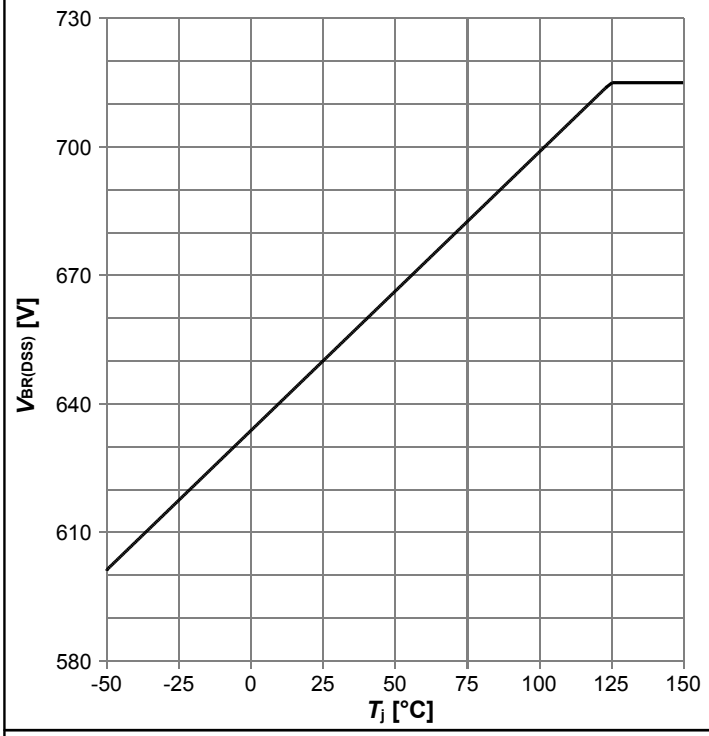
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



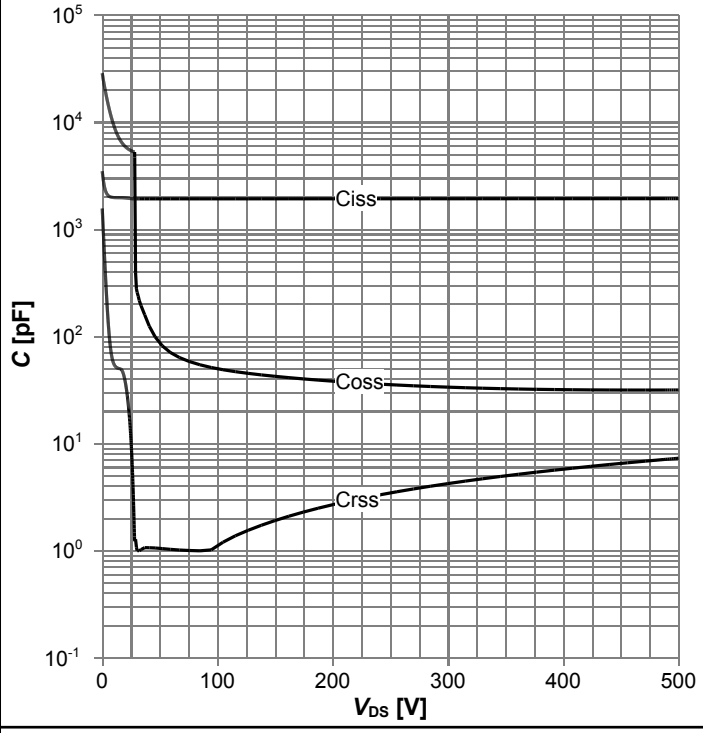
E_{AS}=f(T_j); I_D=4.7 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



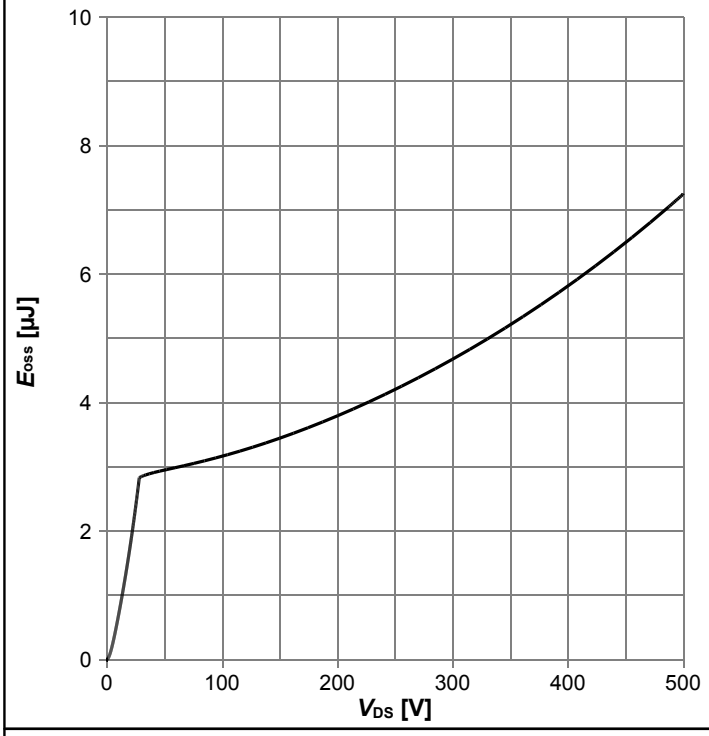
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

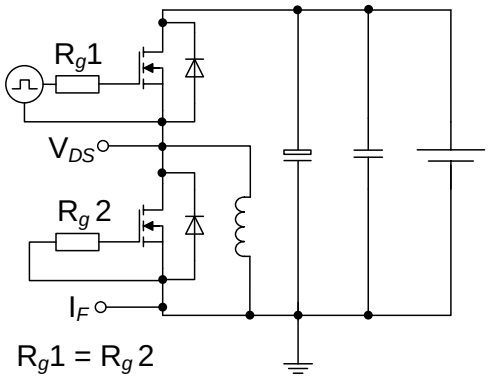
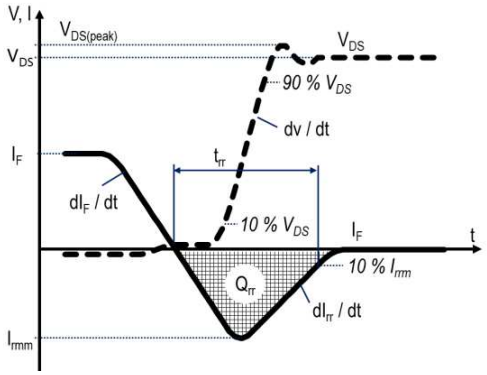
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

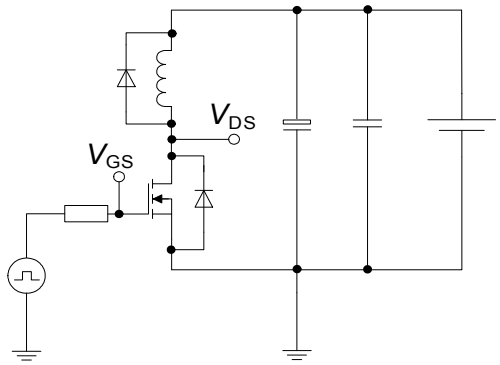
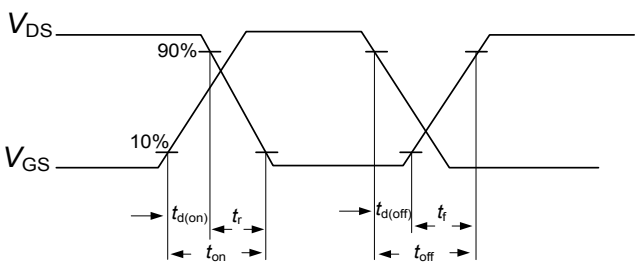
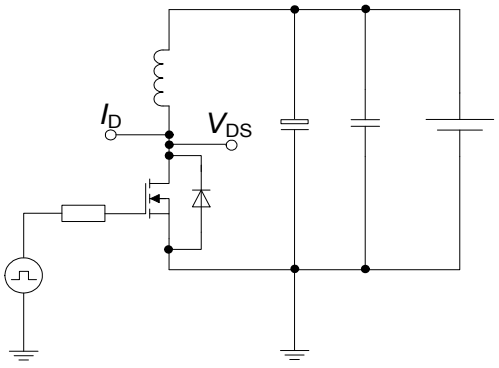
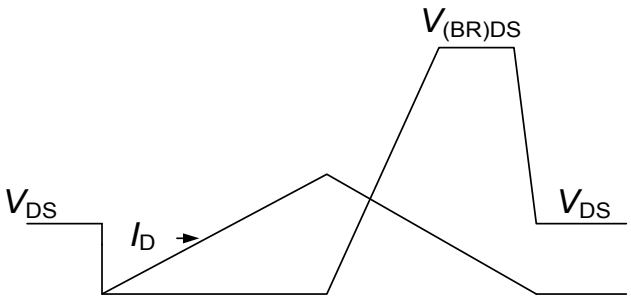
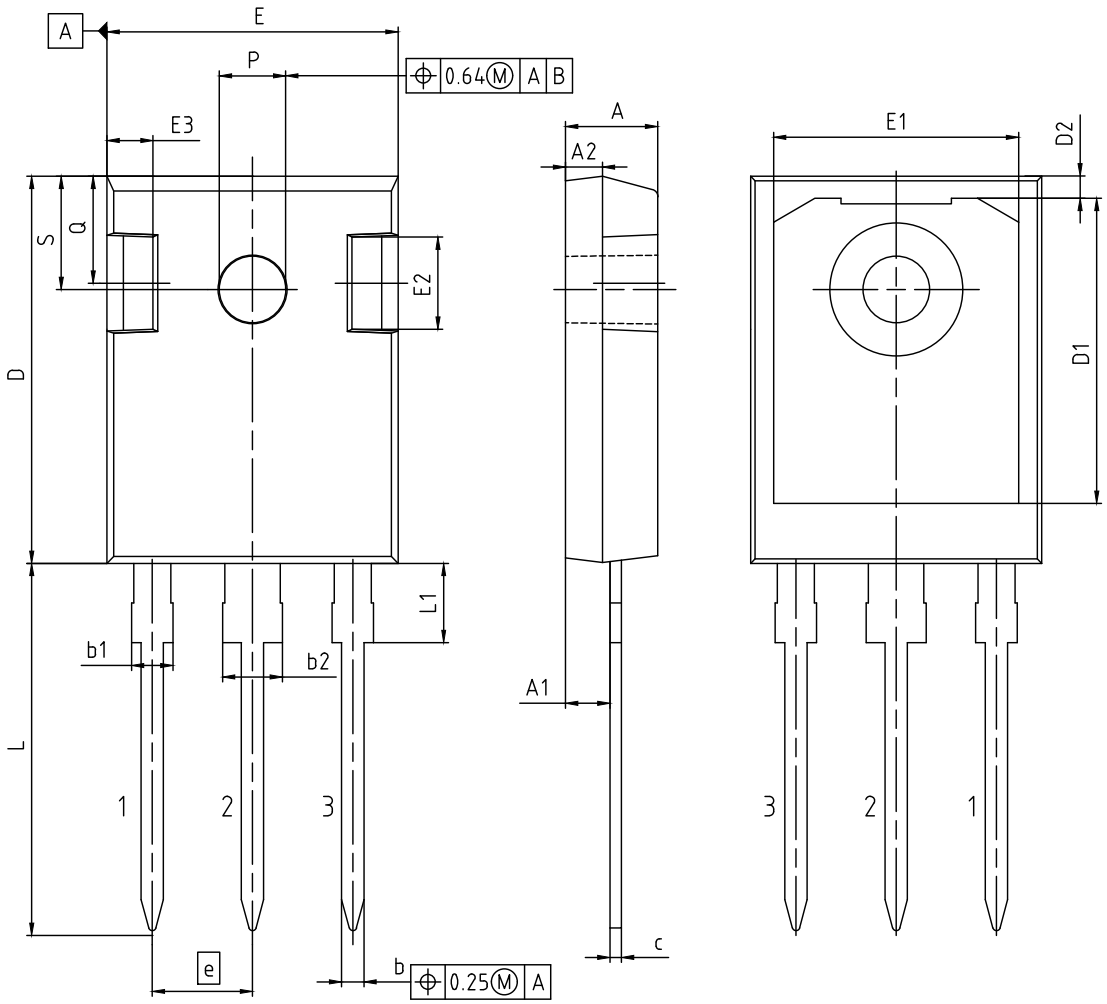
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.70	5.30
A1	2.20	2.60
A2	1.50	2.50
b	1.00	1.40
b1	1.60	2.41
b2	2.57	3.43
c	0.38	0.89
D	20.70	21.50
D1	13.08	17.65
D2	0.51	1.35
E	15.50	16.30
E1	12.38	14.15
E2	3.40	5.10
E3	1.00	2.60
e	5.44	
L	19.80	20.40
L1	3.85	4.50
P	3.50	3.70
Q	5.35	6.25
S	6.04	6.30

DOCUMENT NO.	Z8B00003327
REVISION	06
SCALE 3:1	0 1 2 3 4 5mm
EUROPEAN PROJECTION	
ISSUE DATE	25.07.2018

Figure 1 Outline PG-TO247-3, dimensions in mm

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 650V Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 650V application note:** www.infineon.com
- **IFX CoolMOS CFD7 650V simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPW65R110CFD7

Revision: 2020-10-28, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2020-10-28	Release of final version

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