OptiMOS™3 Power-Transistor

Features

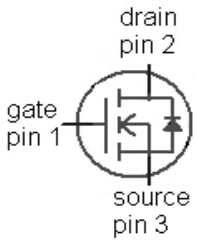
- Optimized technology for synchronous rectification
- Ideal for high frequency switching and DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant, halogen free
- Qualified according to JEDEC[1] for target applications

Product Summary

V_{DS}	75	V
$R_{DS(on),max}$	5.2	mΩ
I_D	80	A

RoHS

Type	IPP052NE7N3 G	IPI052NE7N3 G
		
Package	PG-TO220-3	PG-TO262-3
Marking	052NE7N	052NE7N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	80	A
		T_C=100 °C	80	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	320	
Avalanche energy, single pulse[3]	E_{AS}	I_D=56 A, R_{GS}=25 Ω	370	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	150	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[4)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	75	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=91 µA	2.3	3.1	3.8	
Zero gate voltage drain current	I_{DSS}	V_{DS}=75 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=75 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=80 A	-	4.7	5.2	mΩ
Gate resistance	R_G		-	2.2	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=80 A	52	103	-	S

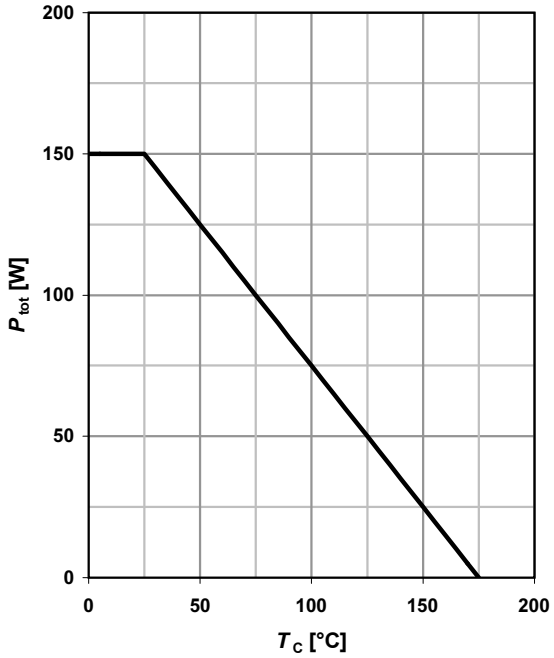
[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=37.5 V, f=1 MHz	-	3570	4750	pF
Output capacitance	C_{oss}		-	805	1070	
Reverse transfer capacitance	C_{rss}		-	40	60	
Turn-on delay time	$t_{d(on)}$	V_{DD}=37.5 V, V_{GS}=10 V, I_D=80 A, R_G=1.6 Ω	-	14	-	ns
Rise time	t_r		-	11	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	8	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=37.5 V, I_D=80 A, V_{GS}=0 to 10 V	-	20	-	nC
Gate to drain charge	Q_{gd}		-	11	-	
Switching charge	Q_{sw}		-	19	-	
Gate charge total	Q_g		-	51	68	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V
Output charge	Q_{oss}	V_{DD}=37.5 V, V_{GS}=0 V	-	53	71	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	80	A
Diode pulse current	$I_{S,pulse}$		-	-	320	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=80 A, T_j=25 °C	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_R=37.5 V, I_F=I_S, di_F/dt=100 A/µs	-	48	-	ns
Reverse recovery charge	Q_{rr}		-	87	-	nC

[5)] See figure 16 for gate charge parameter definition

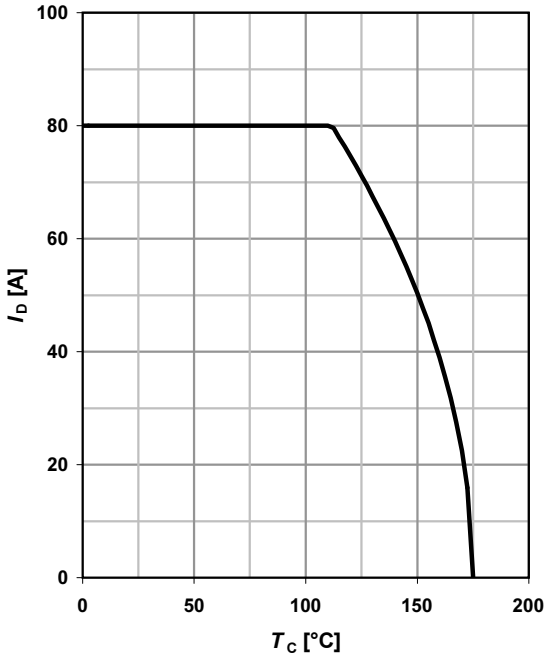
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

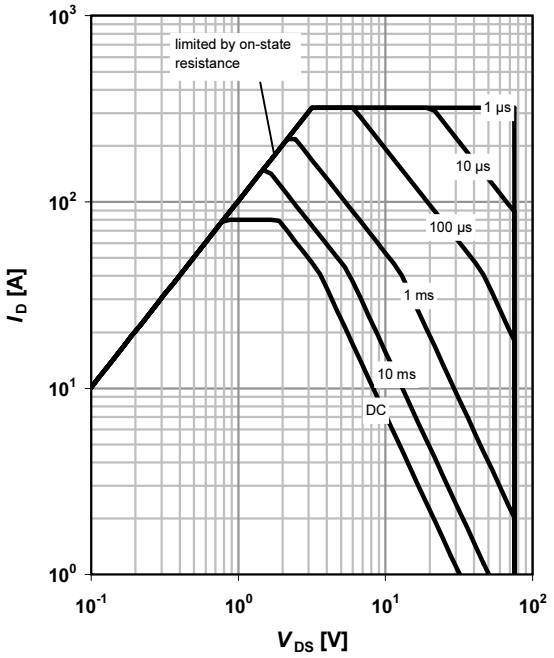
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

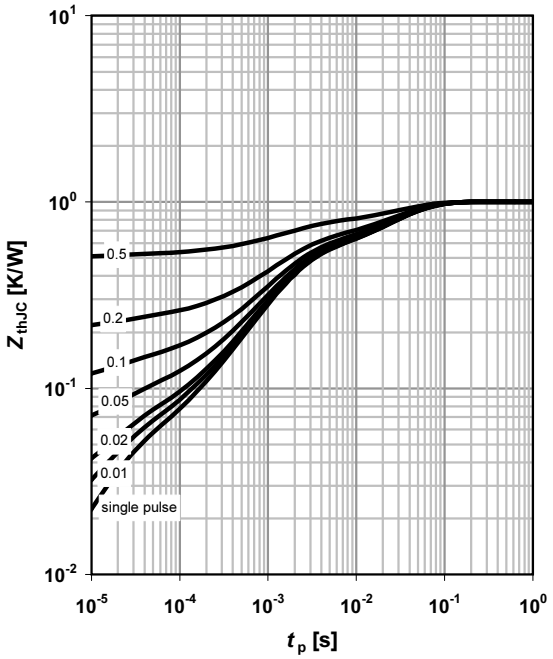
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

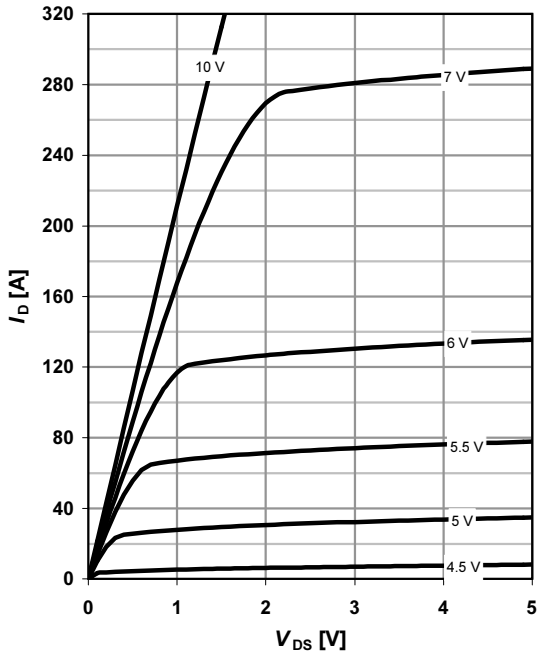
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

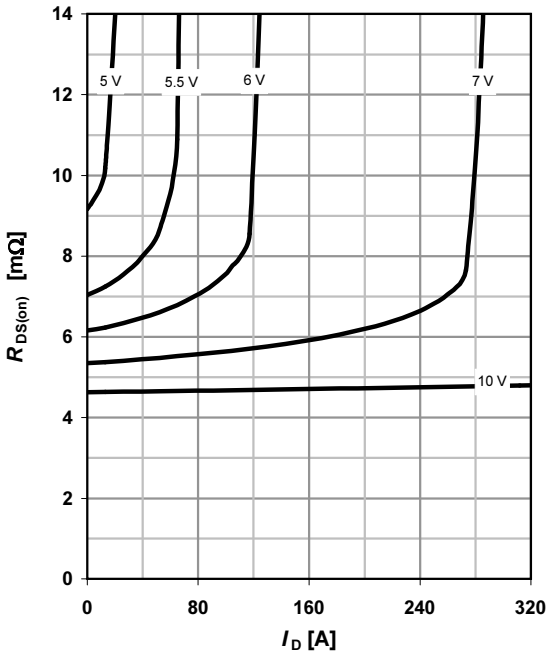
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

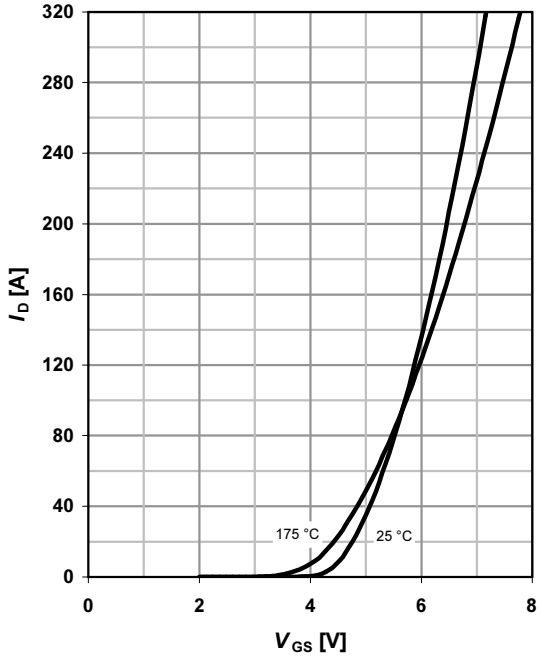
parameter: V_{GS}



7 Typ. transfer characteristics

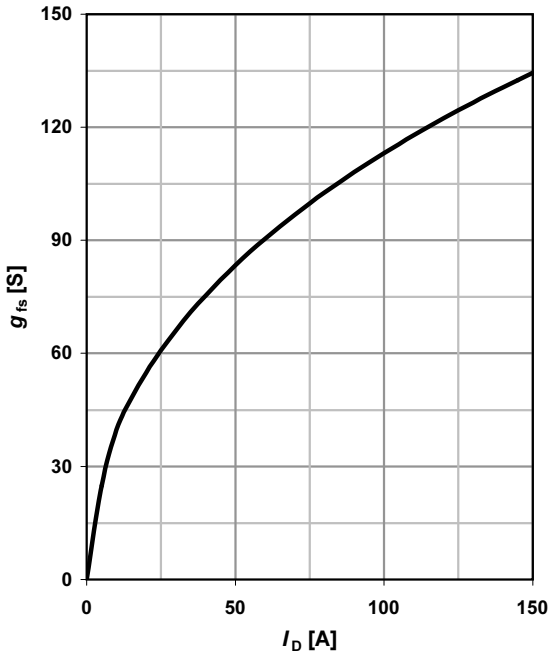
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

parameter: T_j



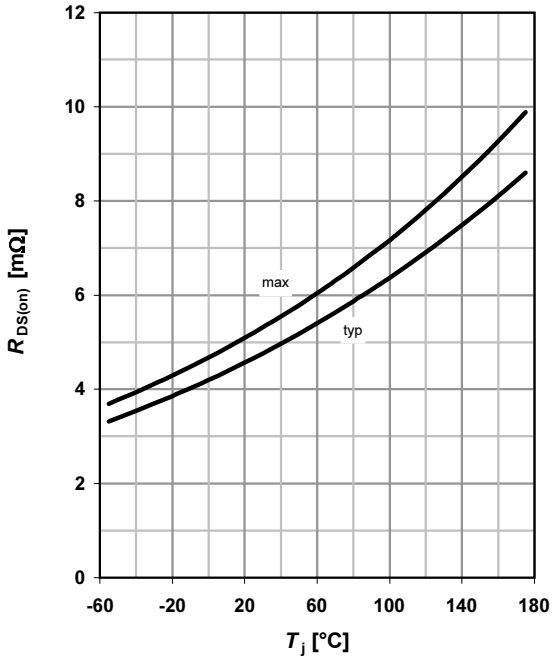
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

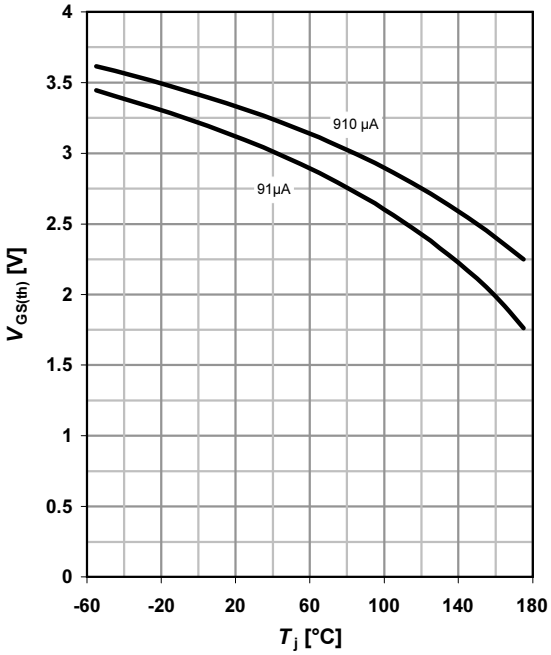
$R_{DS(on)}$=f(T_j); I_D=80 A; V_{GS}=10 V



10 Typ. gate threshold voltage

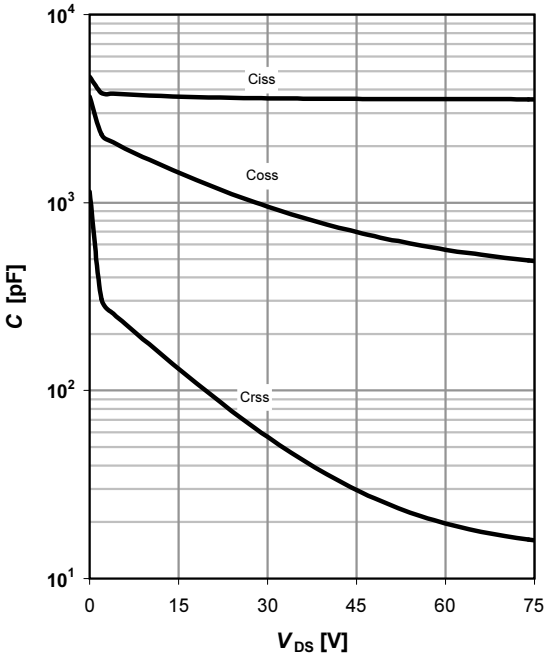
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

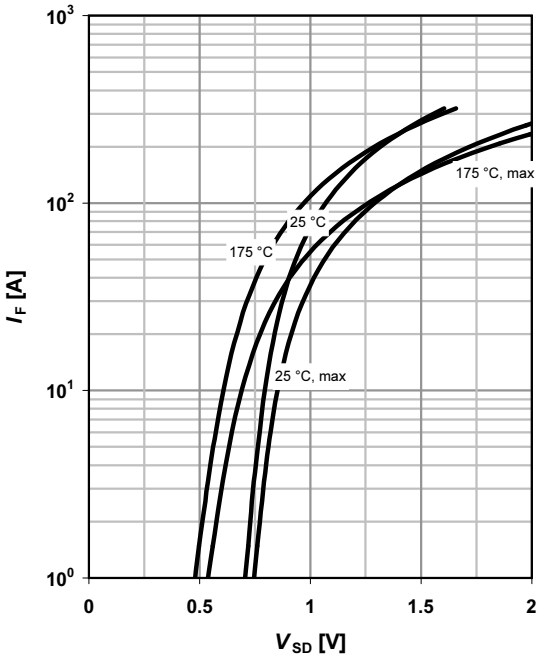
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

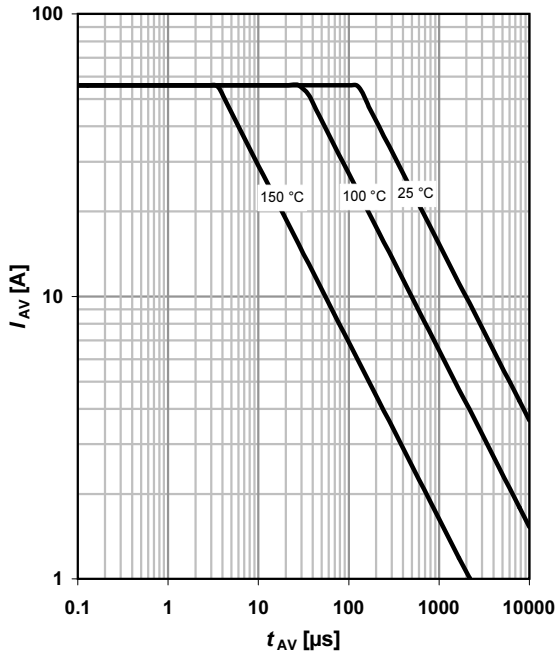
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

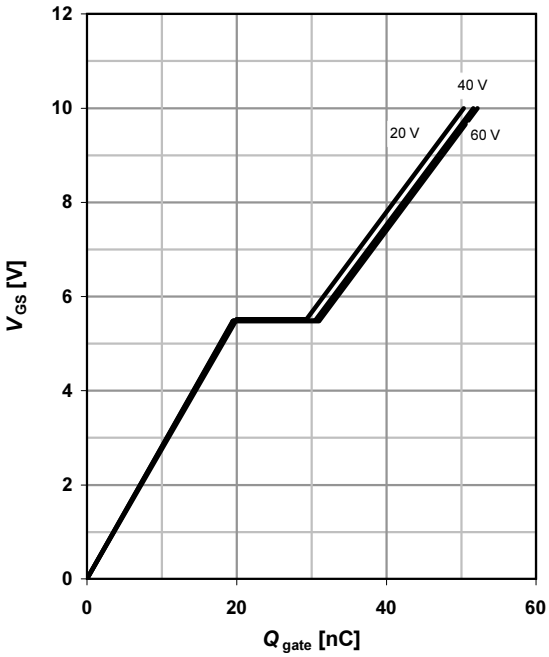
parameter: $T_{j(start)}$



14 Typ. gate charge

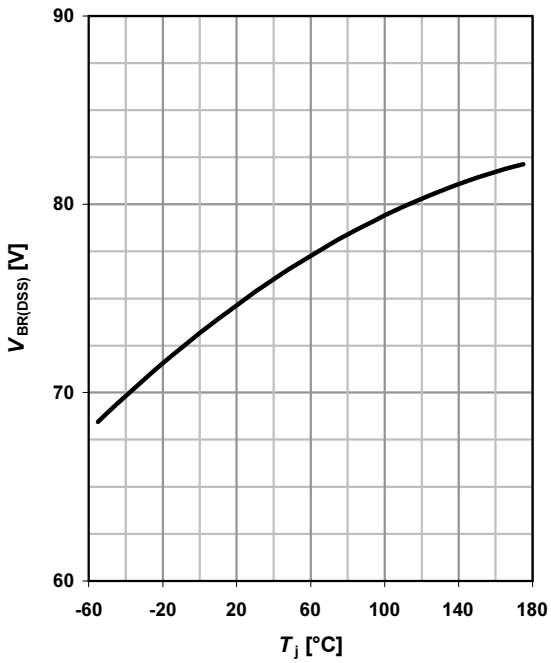
V_{GS}=f(Q_{gate}); I_D=80 A pulsed

parameter: V_{DD}

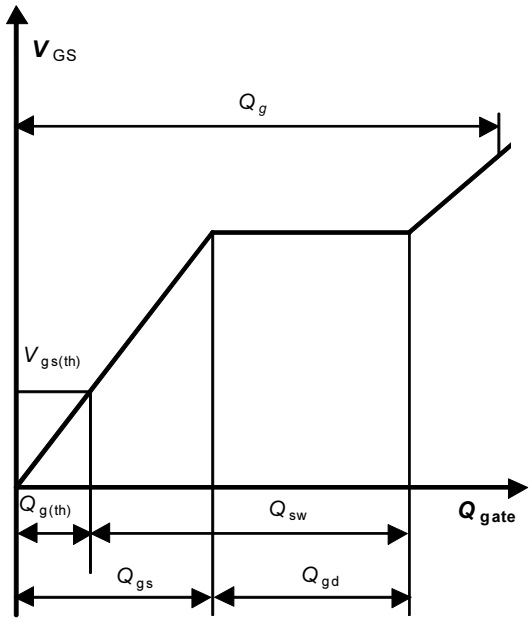


15 Drain-source breakdown voltage

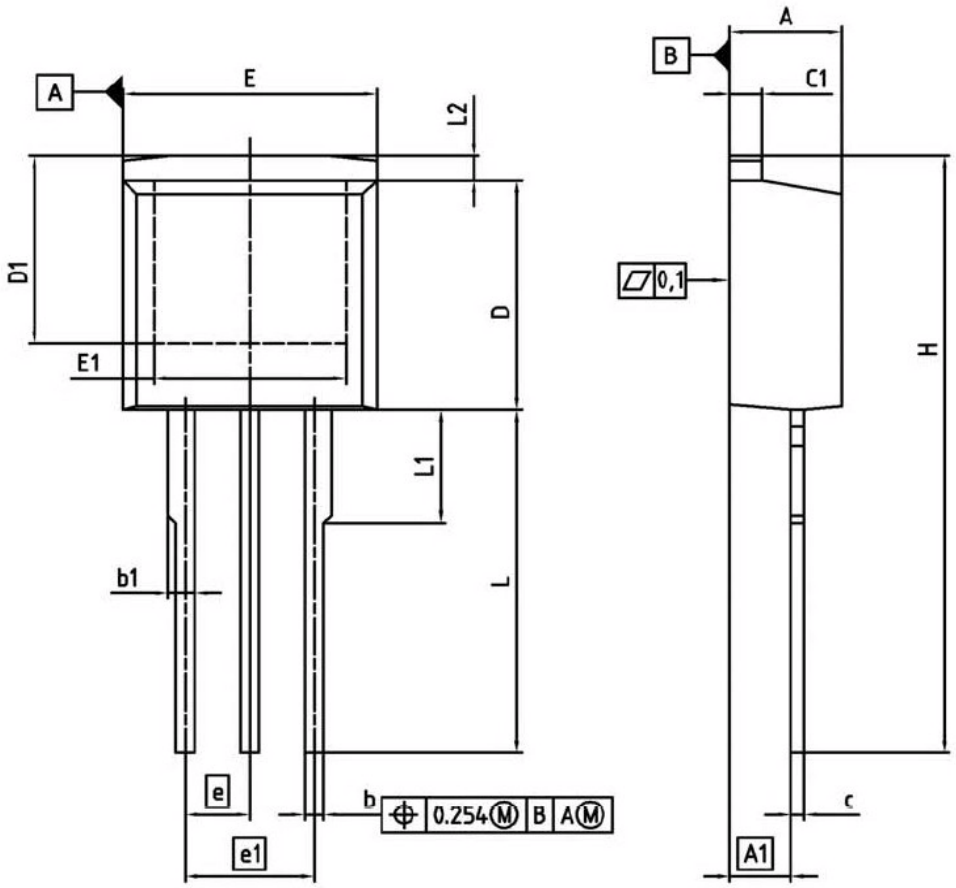
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



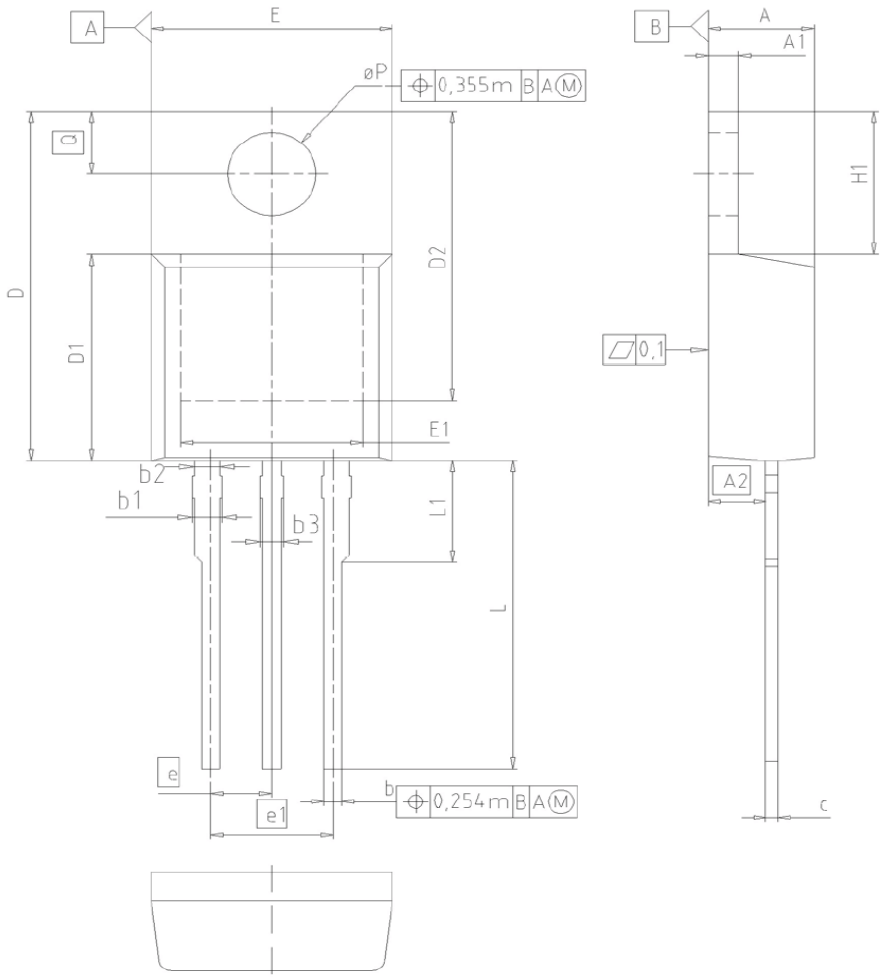
PG-TO262-3 (I²-Pak)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.635	1.400	0.025	0.055
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE	JEDEC TO262
	0 2.5 5mm
EUROPEAN PROJECTION	
ISSUE DATE	05-05-2006
FILE	TO262_1

PG-TO220-3



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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