

## OptiMOS®-T2 Power-Transistor



### Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

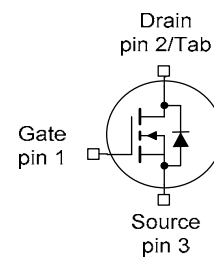
### Product Summary

|                  |     |    |
|------------------|-----|----|
| $V_{DS}$         | 40  | V  |
| $R_{DS(on),max}$ | 2.4 | mΩ |
| $I_D$            | 90  | A  |

### PG-TO252-3-313



| Type          | Package        | Marking |
|---------------|----------------|---------|
| IPD90N04S4-02 | PG-TO252-3-313 | 4N0402  |



**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

| Parameter                                    | Symbol            | Conditions                                      | Value        | Unit |
|----------------------------------------------|-------------------|-------------------------------------------------|--------------|------|
| Continuous drain current <sup>1)</sup>       | $I_D$             | $T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}$       | 90           | A    |
|                                              |                   | $T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}^{2)}$ | 90           |      |
| Pulsed drain current <sup>2)</sup>           | $I_{D,pulse}$     | $T_C=25\text{ °C}$                              | 360          |      |
| Avalanche energy, single pulse <sup>2)</sup> | $E_{AS}$          | $I_D=45\text{ A}$                               | 475          | mJ   |
| Avalanche current, single pulse              | $I_{AS}$          | -                                               | 90           | A    |
| Gate source voltage                          | $V_{GS}$          | -                                               | ±20          | V    |
| Power dissipation                            | $P_{tot}$         | $T_C=25\text{ °C}$                              | 150          | W    |
| Operating and storage temperature            | $T_j$ , $T_{stg}$ | -                                               | -55 ... +175 | °C   |
| IEC climatic category; DIN IEC 68-1          | -                 | -                                               | 55/175/56    |      |

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

### Thermal characteristics<sup>2)</sup>

|                                                |            |                                              |   |   |     |     |
|------------------------------------------------|------------|----------------------------------------------|---|---|-----|-----|
| Thermal resistance, junction - case            | $R_{thJC}$ | -                                            | - | - | 1.0 | K/W |
| Thermal resistance, junction - ambient, leaded | $R_{thJA}$ | -                                            | - | - | 62  |     |
| SMD version, device on PCB                     | $R_{thJA}$ | minimal footprint                            | - | - | 62  |     |
|                                                |            | 6 cm <sup>2</sup> cooling area <sup>3)</sup> | - | - | 40  |     |

### Electrical characteristics, at $T_j=25^\circ\text{C}$ , unless otherwise specified

#### Static characteristics

|                                  |               |                                                    |     |      |     |            |
|----------------------------------|---------------|----------------------------------------------------|-----|------|-----|------------|
| Drain-source breakdown voltage   | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=1mA$                               | 40  | -    | -   | V          |
| Gate threshold voltage           | $V_{GS(th)}$  | $V_{DS}=V_{GS}, I_D=95\mu A$                       | 2.0 | 3.0  | 4.0 |            |
| Zero gate voltage drain current  | $I_{DSS}$     | $V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$      | -   | 0.04 | 1   | $\mu A$    |
|                                  |               | $V_{DS}=18V, V_{GS}=0V, T_j=85^\circ\text{C}^{2)}$ | -   | 1    | 20  |            |
| Gate-source leakage current      | $I_{GSS}$     | $V_{GS}=20V, V_{DS}=0V$                            | -   | -    | 100 | nA         |
| Drain-source on-state resistance | $R_{DS(on)}$  | $V_{GS}=10V, I_D=90A$                              | -   | 2.0  | 2.4 | m $\Omega$ |

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

### Dynamic characteristics<sup>2)</sup>

|                              |              |                                                                       |   |      |      |    |
|------------------------------|--------------|-----------------------------------------------------------------------|---|------|------|----|
| Input capacitance            | $C_{iss}$    | $V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$               | - | 7250 | 9430 | pF |
| Output capacitance           | $C_{oss}$    |                                                                       | - | 1630 | 2120 |    |
| Reverse transfer capacitance | $C_{rss}$    |                                                                       | - | 55   | 127  |    |
| Turn-on delay time           | $t_{d(on)}$  | $V_{DD}=20\text{V}, V_{GS}=10\text{V}, I_D=90\text{A}, R_G=3.5\Omega$ | - | 23   | -    | ns |
| Rise time                    | $t_r$        |                                                                       | - | 10   | -    |    |
| Turn-off delay time          | $t_{d(off)}$ |                                                                       | - | 27   | -    |    |
| Fall time                    | $t_f$        |                                                                       | - | 23   | -    |    |

### Gate Charge Characteristics<sup>2)</sup>

|                       |               |                                                                    |   |     |     |    |
|-----------------------|---------------|--------------------------------------------------------------------|---|-----|-----|----|
| Gate to source charge | $Q_{gs}$      | $V_{DD}=32\text{V}, I_D=90\text{A}, V_{GS}=0\text{ to }10\text{V}$ | - | 39  | 51  | nC |
| Gate to drain charge  | $Q_{gd}$      |                                                                    | - | 12  | 28  |    |
| Gate charge total     | $Q_g$         |                                                                    | - | 91  | 118 |    |
| Gate plateau voltage  | $V_{plateau}$ |                                                                    | - | 5.8 | -   | V  |

### Reverse Diode

|                                                |               |                                                                   |   |     |     |    |
|------------------------------------------------|---------------|-------------------------------------------------------------------|---|-----|-----|----|
| Diode continuous forward current <sup>2)</sup> | $I_S$         | $T_C=25^\circ\text{C}$                                            | - | -   | 90  | A  |
| Diode pulse current <sup>2)</sup>              | $I_{S,pulse}$ |                                                                   | - | -   | 360 |    |
| Diode forward voltage                          | $V_{SD}$      | $V_{GS}=0\text{V}, I_F=90\text{A}, T_j=25^\circ\text{C}$          | - | 0.9 | 1.3 | V  |
| Reverse recovery time <sup>2)</sup>            | $t_{rr}$      | $V_R=20\text{V}, I_F=50\text{A}, di_F/dt=100\text{A}/\mu\text{s}$ | - | 53  | -   | ns |
| Reverse recovery charge <sup>2)</sup>          | $Q_{rr}$      |                                                                   | - | 65  | -   | nC |

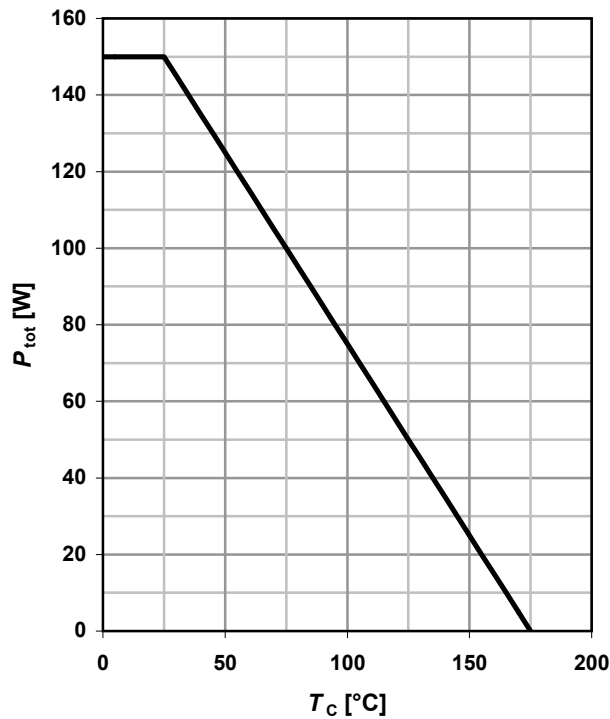
<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 1.0\text{K/W}$  the chip is able to carry 188A at 25°C.

<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

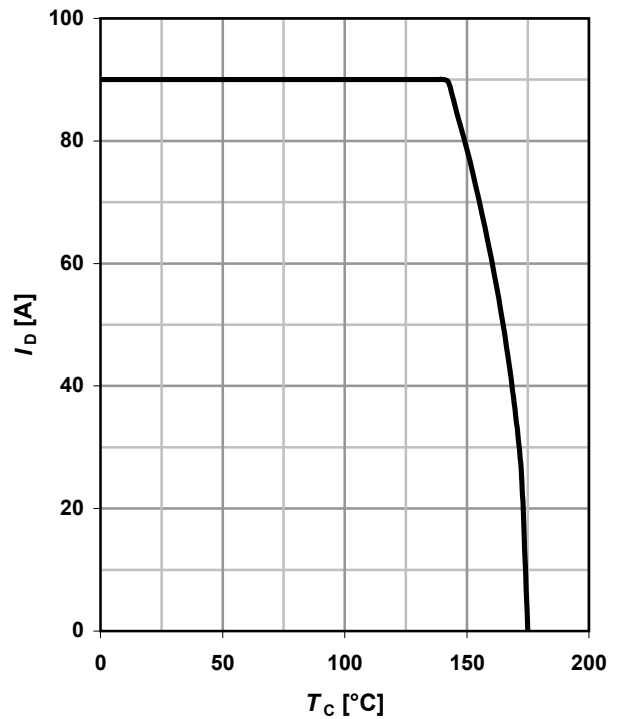
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



### 2 Drain current

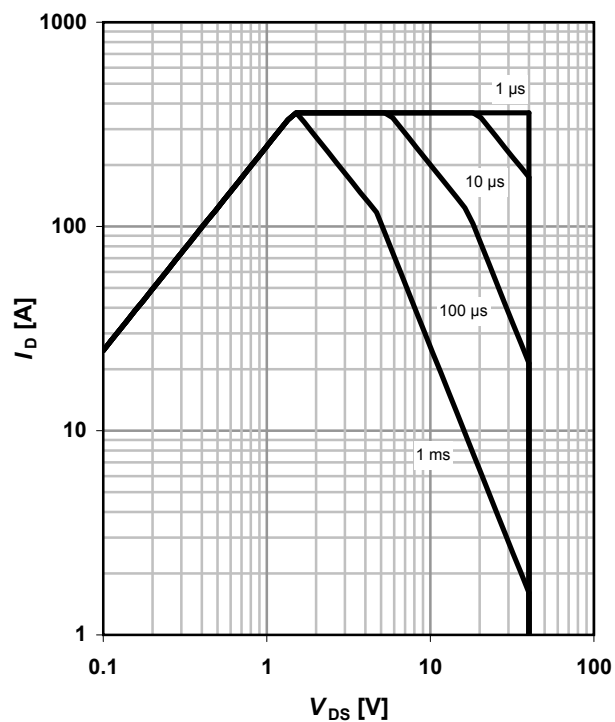
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

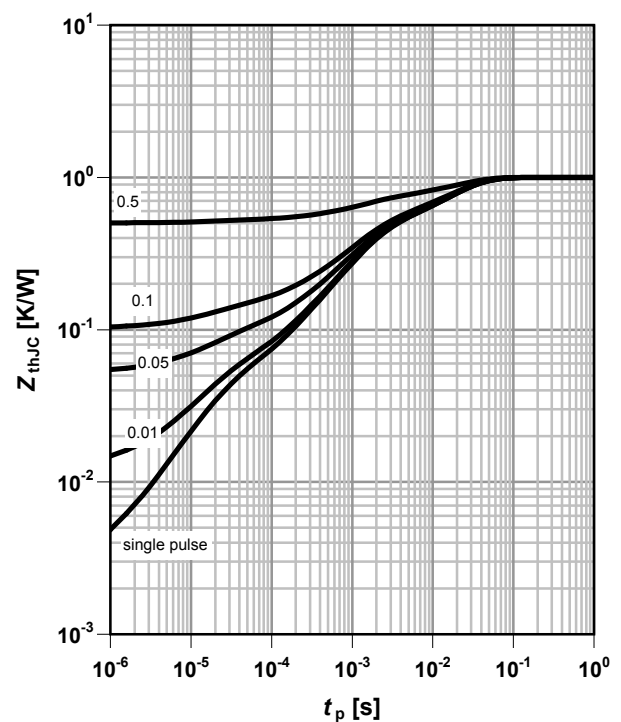
parameter:  $t_p$



### 4 Max. transient thermal impedance

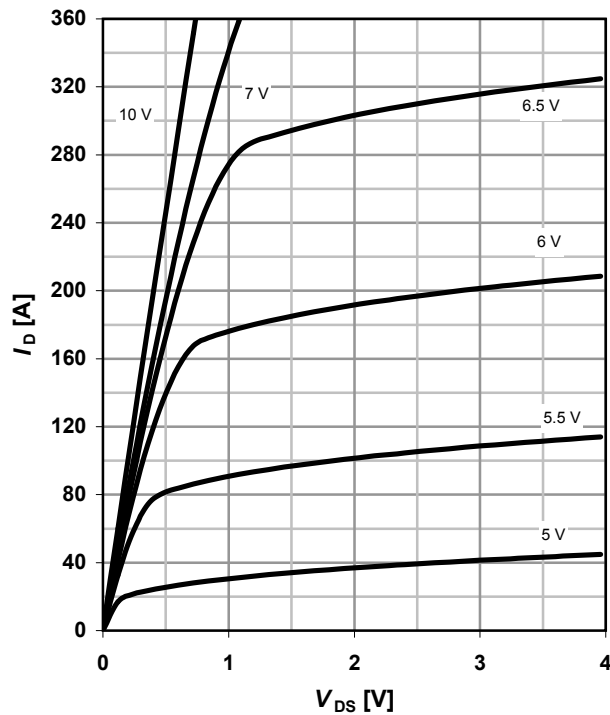
$$Z_{\text{thJC}} = f(t_p)$$

parameter:  $D = t_p/T$



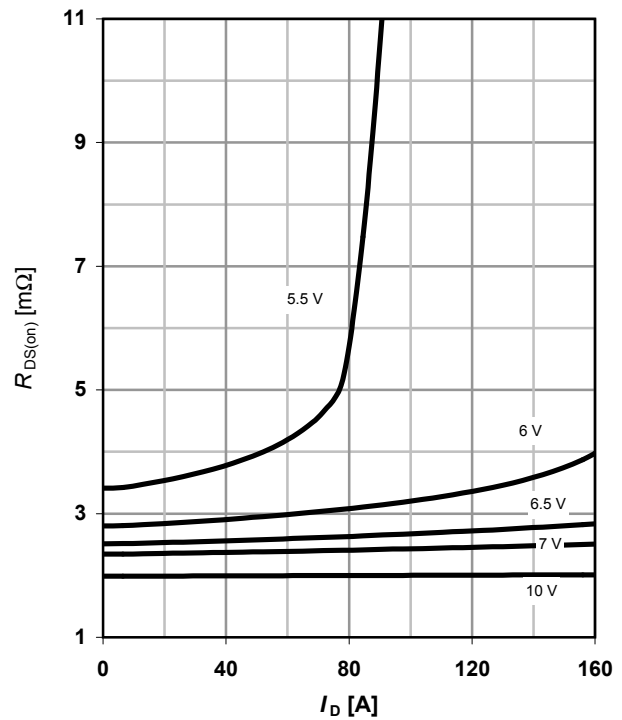
### 5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$ 

parameter:  $V_{GS}$ 


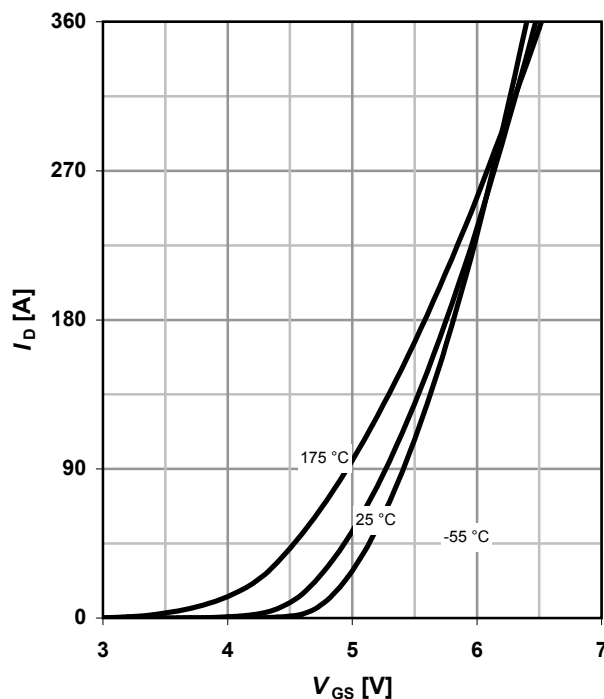
### 6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$ 

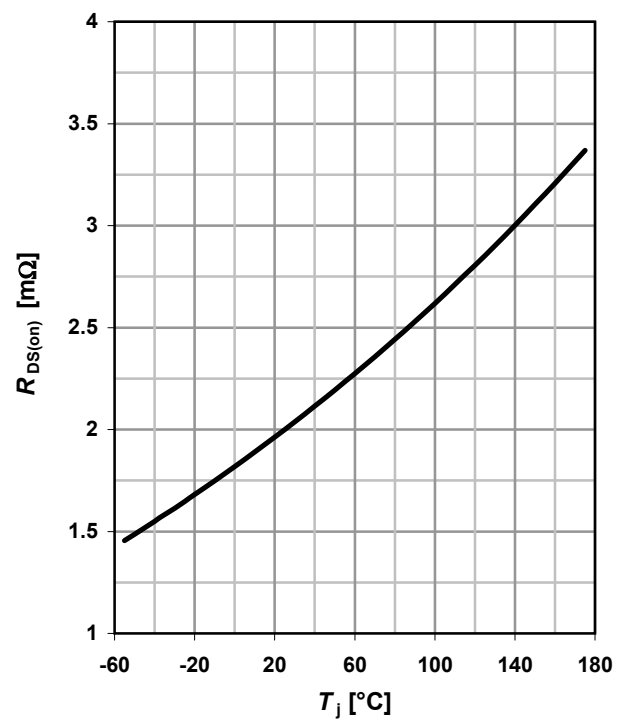
parameter:  $V_{GS}$ 


### 7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$ 

parameter:  $T_j$ 


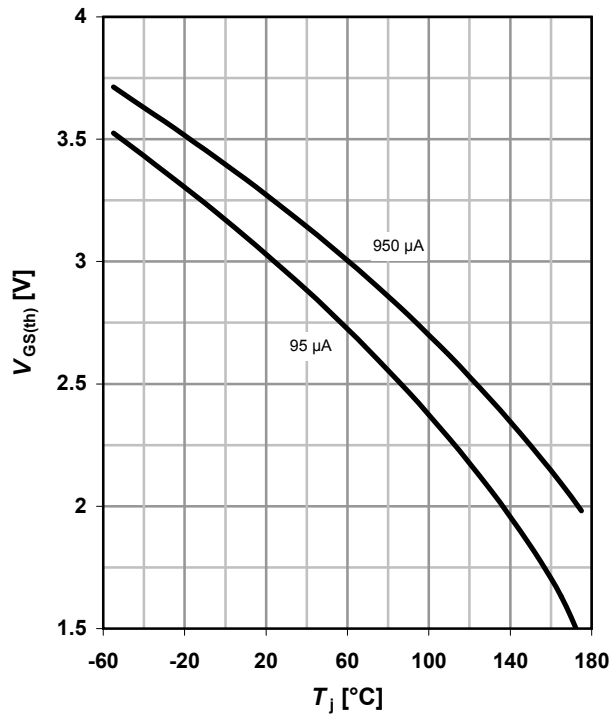
### 8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 90\text{ A}; V_{GS} = 10\text{ V}$ 


## 9 Typ. gate threshold voltage

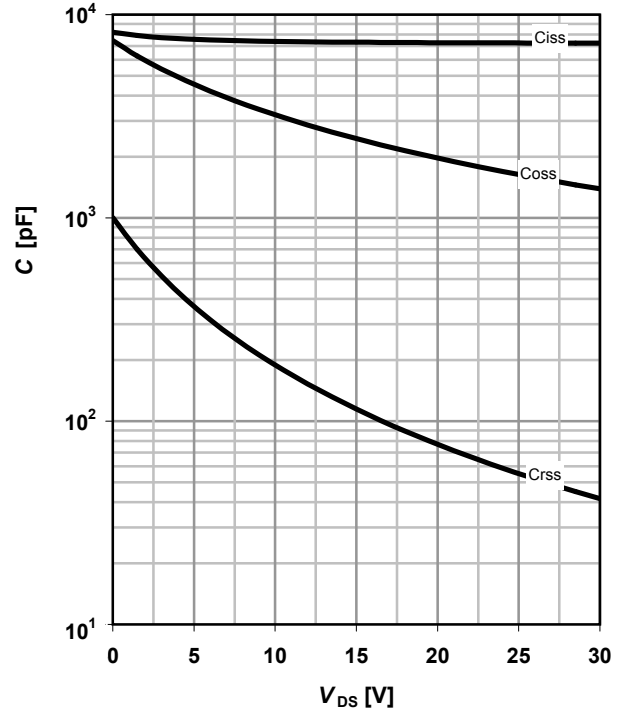
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $I_D$



## 10 Typ. capacitances

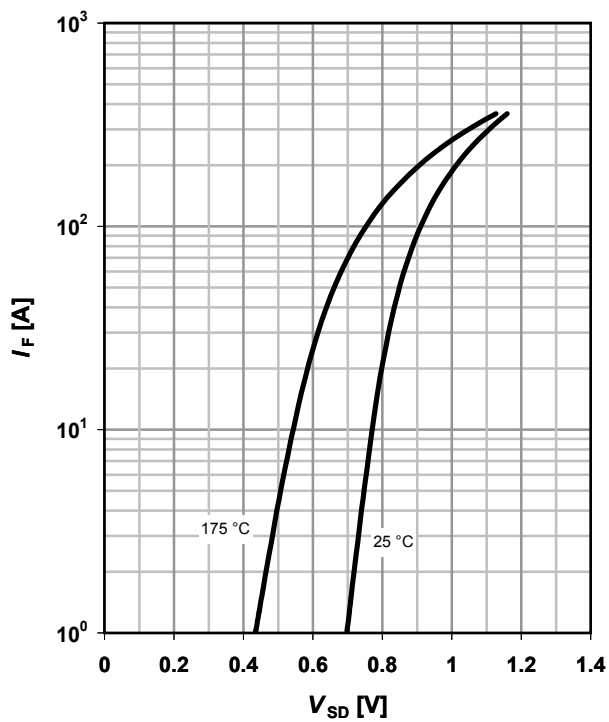
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



## 11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

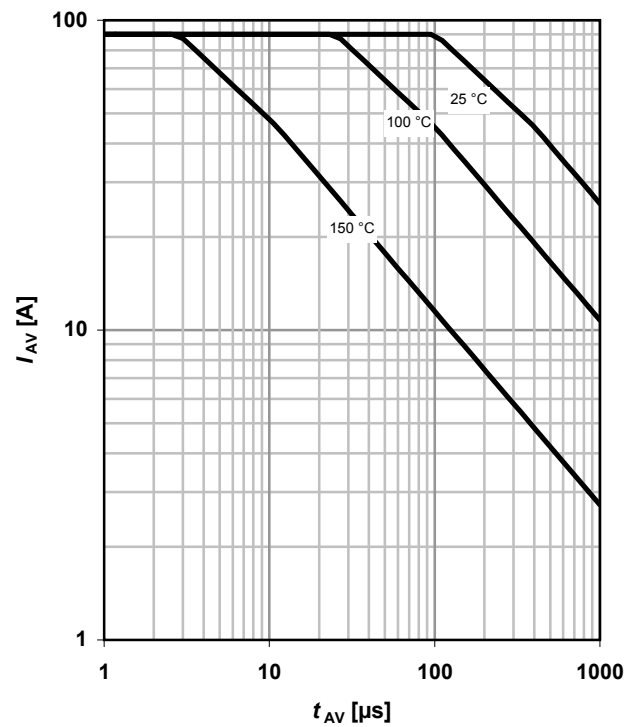
parameter:  $T_j$



## 12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

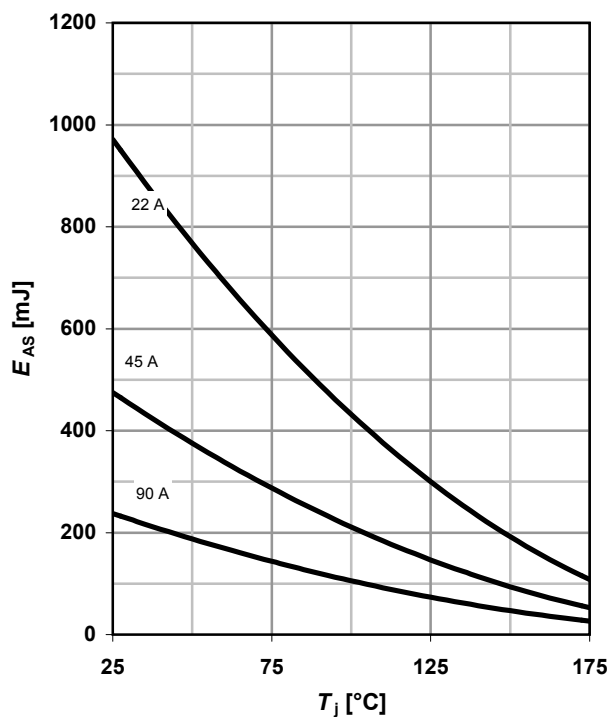
parameter:  $T_{j(start)}$



### 13 Avalanche energy

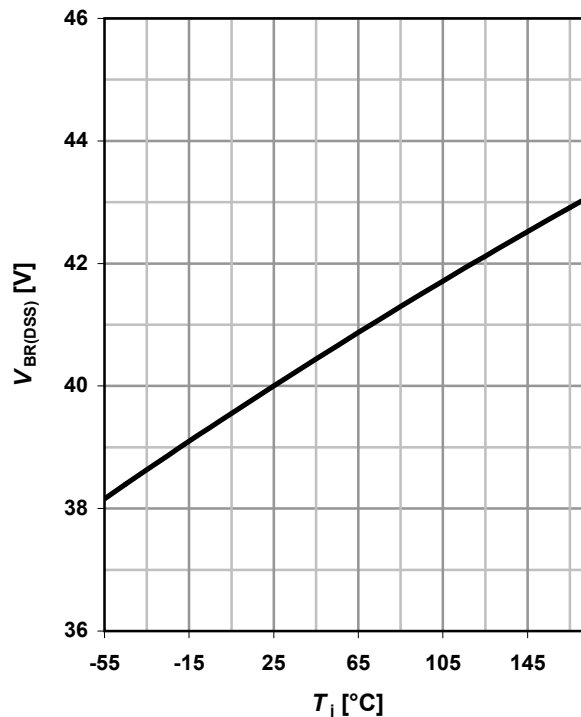
$$E_{AS} = f(T_j)$$

parameter:  $I_D$



### 14 Drain-source breakdown voltage

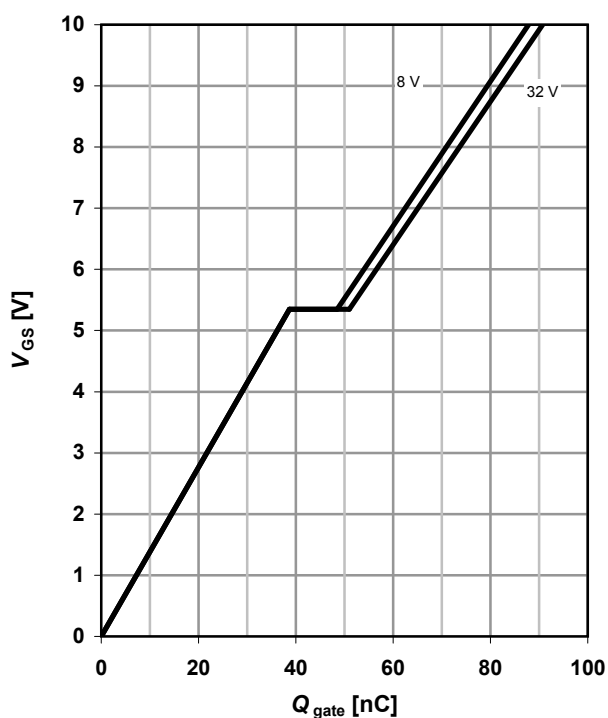
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



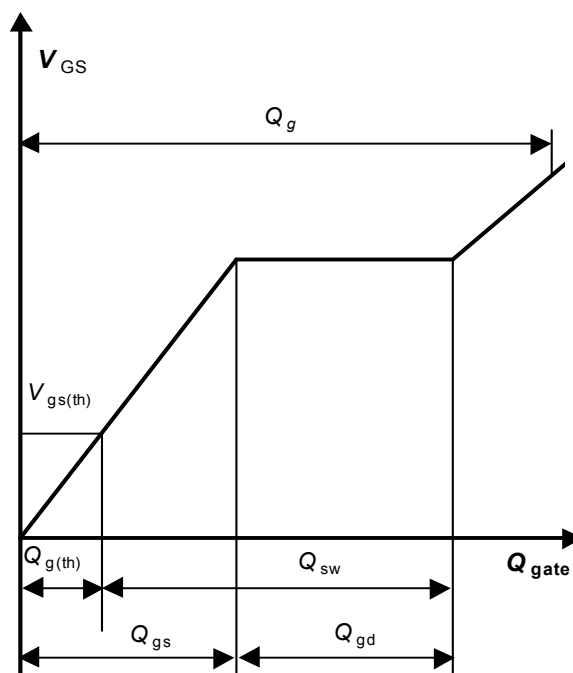
### 15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 90 \text{ A pulsed}$$

parameter:  $V_{DD}$



### 16 Gate charge waveforms



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Revision History

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| Version      | Date       | Changes          |
|--------------|------------|------------------|
| Revision 1.0 | 13.04.2010 | Final Data Sheet |
|              |            |                  |
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