

OptiMOS® -P2 Power-Transistor



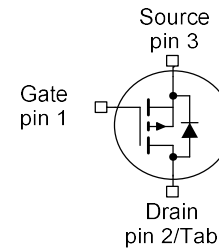
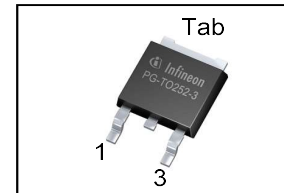
Features

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested
- Intended for reverse battery protection

Product Summary

V_{DS}	-30	V
$R_{DS(on)}$	6.8	mΩ
I_D	-80	A

PG-TO252-3-11



Type	Package	Marking
IPD80P03P4L-07	PG-TO252-3-11	4P03L07

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=-10\text{ V}^{(1)}$	-80	A
		$T_C=100\text{ °C}$, $V_{GS}=-10\text{ V}^{(2)}$	-65	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	-320	
Avalanche energy, single pulse	E_{AS}	$I_D=-40\text{ A}$	135	mJ
Avalanche current, single pulse	I_{AS}	-	-80	A
Gate source voltage	V_{GS}	-	+5/-16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	88	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	1.7	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-1mA$	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-130\mu A$	-1.0	-1.5	-2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-0.03	-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-16V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-40A$	-	8.7	12	m Ω
		$V_{GS}=-10V, I_D=-80A$	-	5.6	6.8	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	4400	5700	pF
Output capacitance	C_{oss}		-	1220	1600	
Reverse transfer capacitance	C_{rss}		-	48	96	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15V,$ $V_{GS}=-10V, I_D=-80A,$ $R_G=3.5\Omega$	-	8	-	ns
Rise time	t_r		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	15	-	
Fall time	t_f		-	60	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-24V, I_D=-80A,$ $V_{GS}=0 \text{ to } -10V$	-	16	20	nC
Gate to drain charge	Q_{gd}		-	8	16	
Gate charge total	Q_g		-	63	80	
Gate plateau voltage	$V_{plateau}$		-	-3.7	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	-80	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	-320	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=-80A,$ $T_j=25^\circ C$	-	-	-1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-15V, I_F=-40A,$ $di_F/dt=-100A/\mu s$	-	50	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	40	-	nC

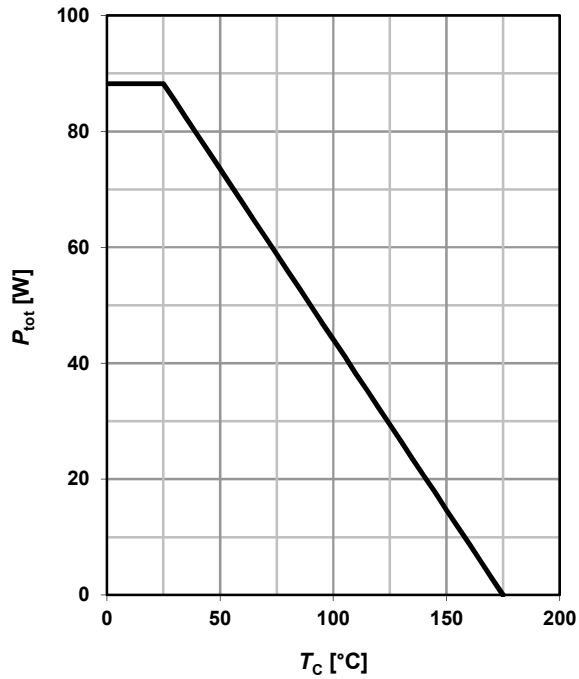
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 1.7K/W$ the chip is able to carry 92A at 25°C.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

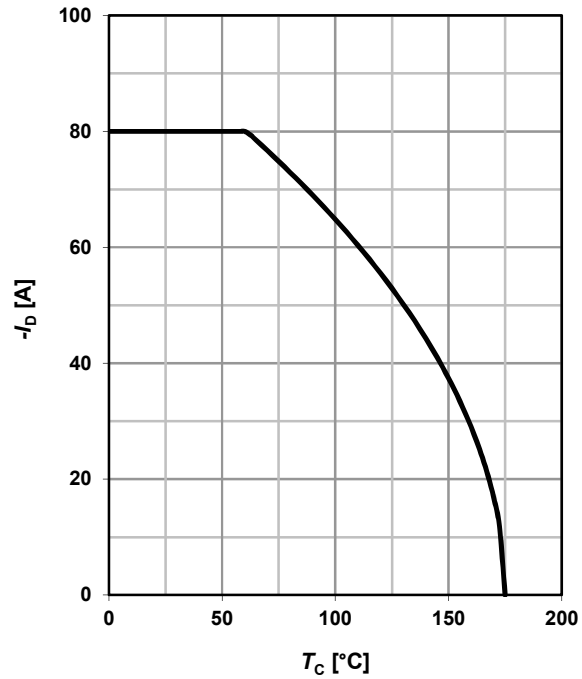
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \leq -6\text{V}$$



2 Drain current

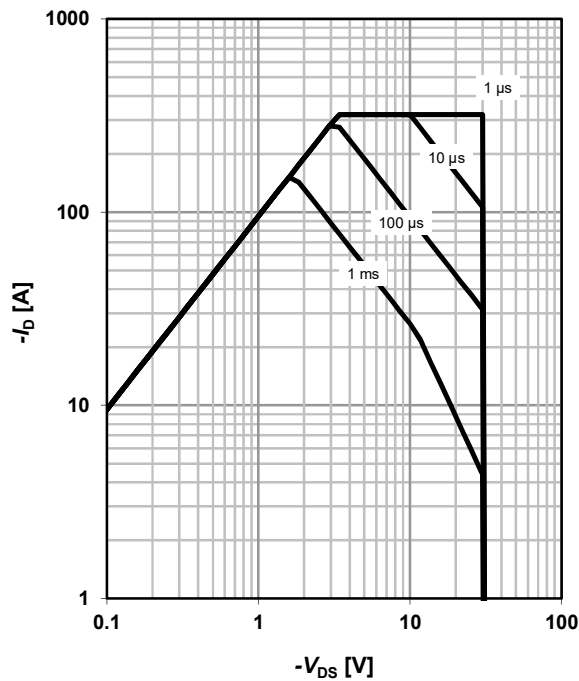
$$I_D = f(T_C); V_{\text{GS}} \leq -6\text{V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

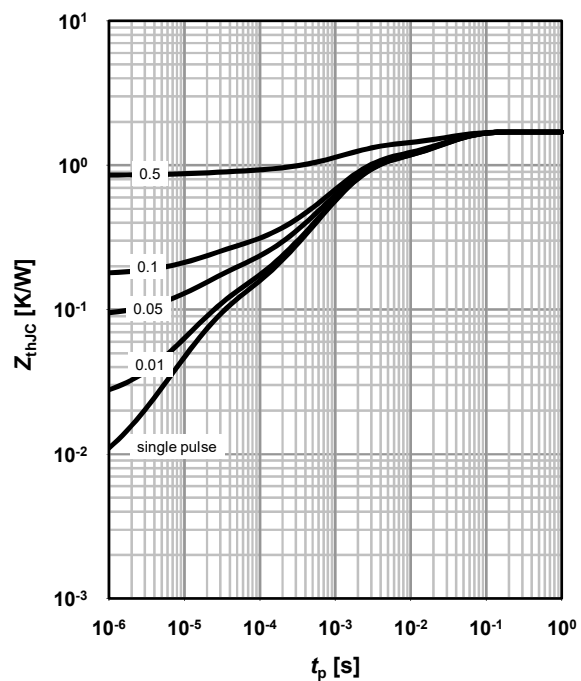
parameter: t_p



4 Max. transient thermal impedance

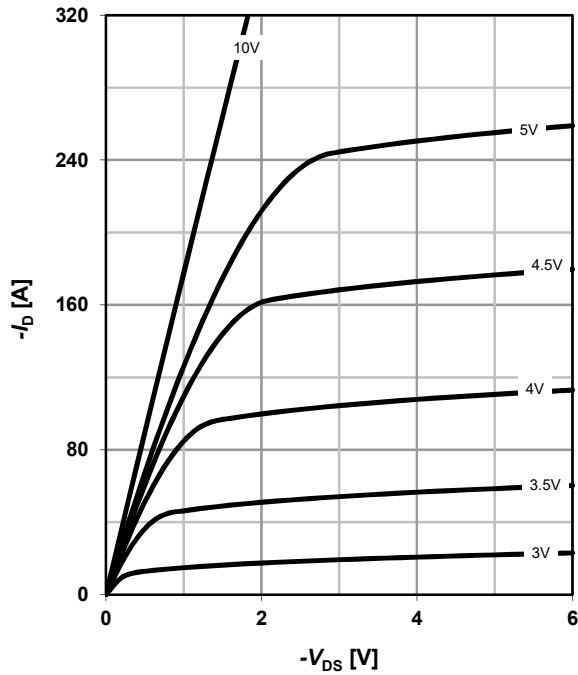
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



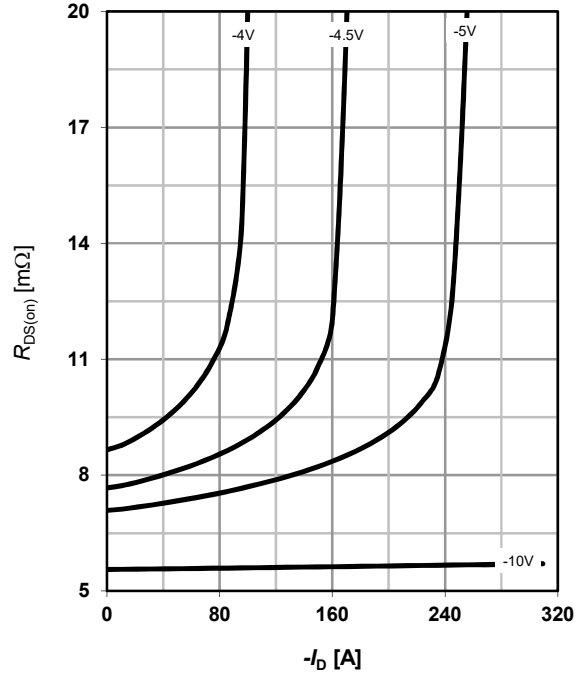
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


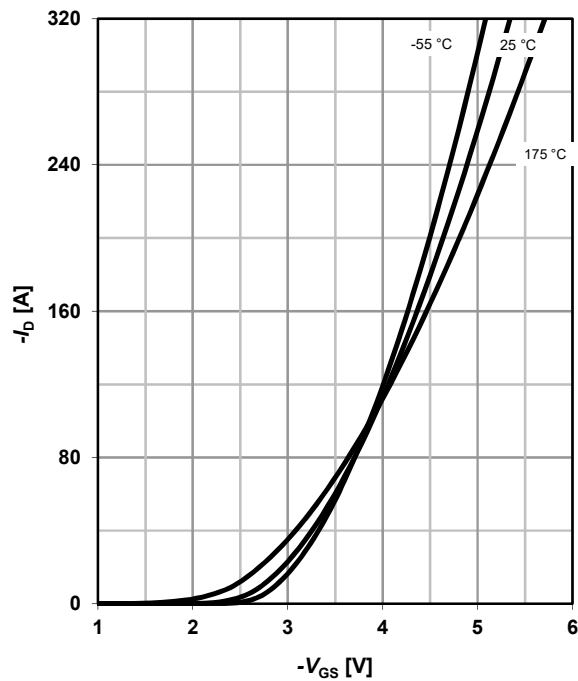
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

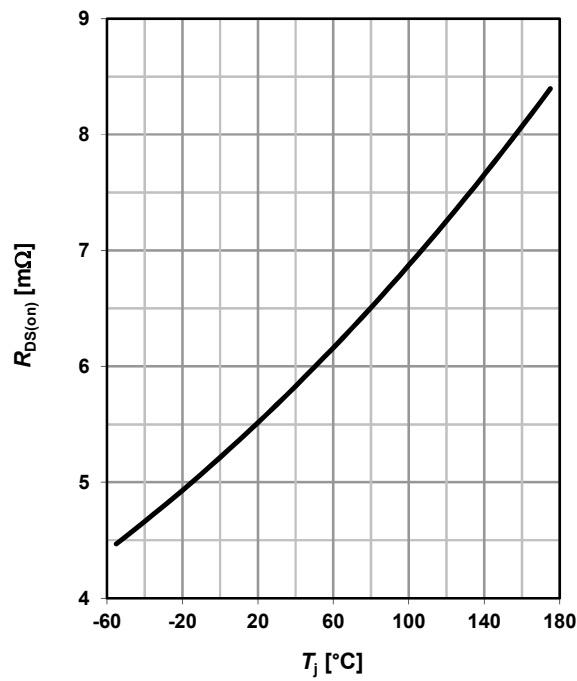
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = -6V$

parameter: T_j


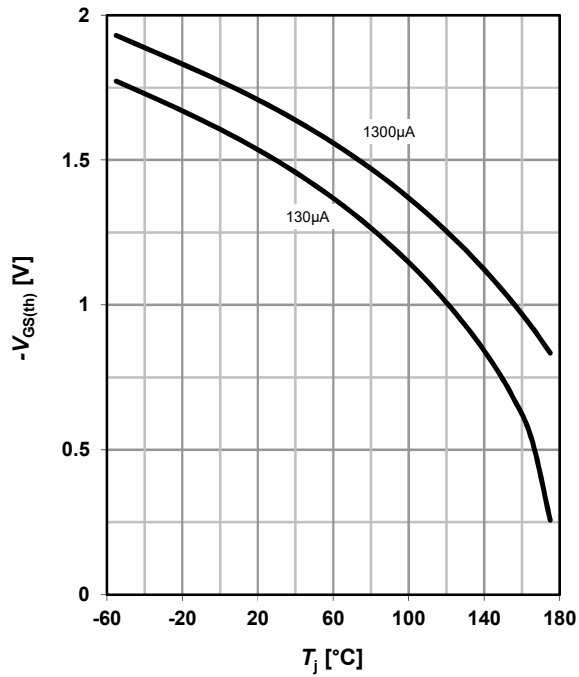
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = -80\text{ A}; V_{GS} = -10\text{ V}$


9 Typ. gate threshold voltage

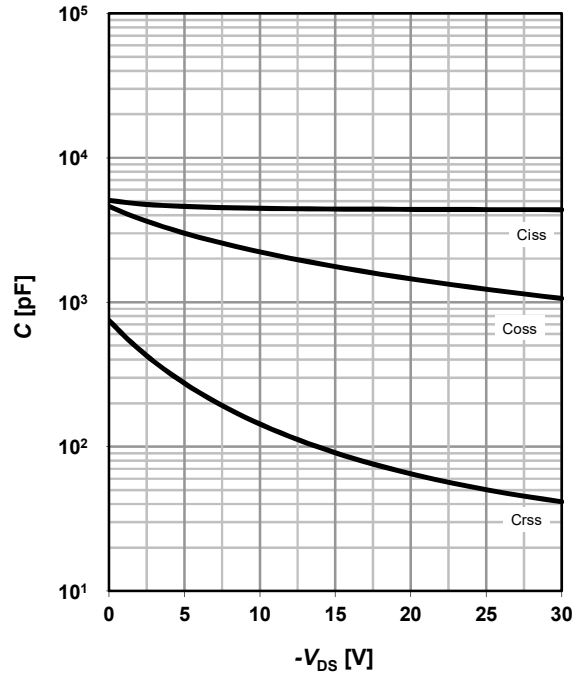
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: $-I_D$



10 Typ. capacitances

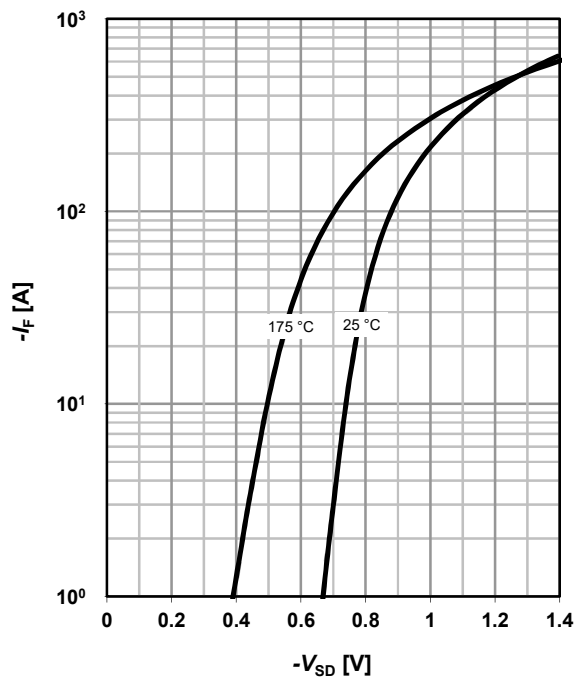
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

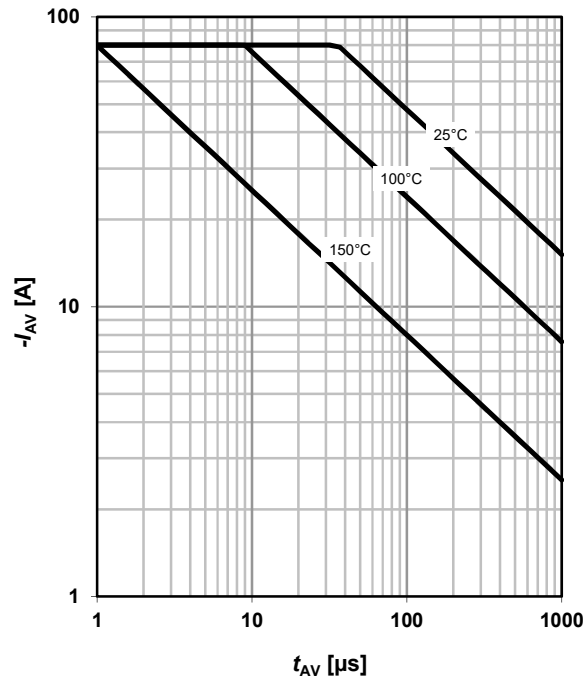
parameter: T_j



12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

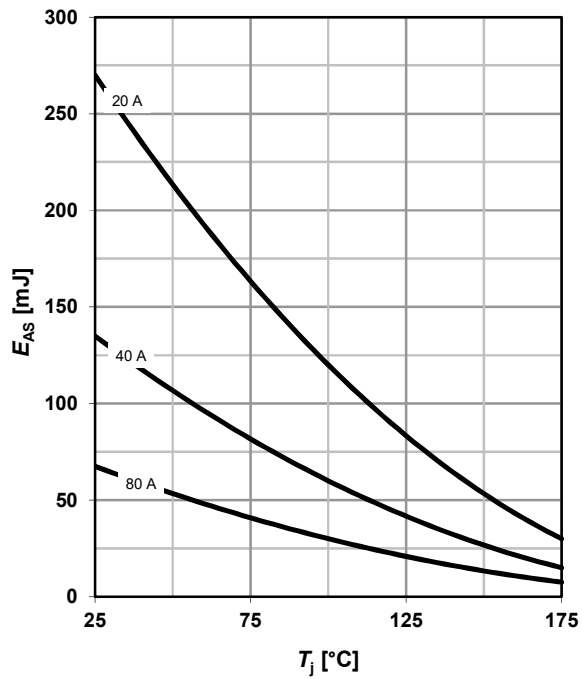
parameter: $T_{j(start)}$



13 Avalanche energy

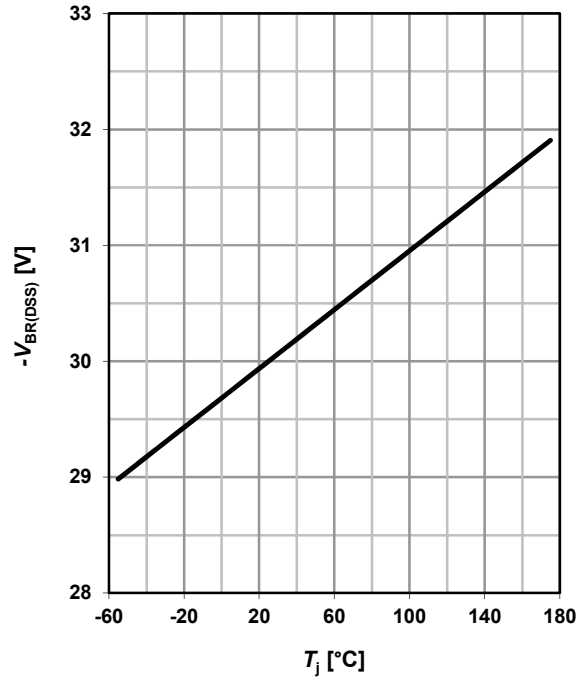
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

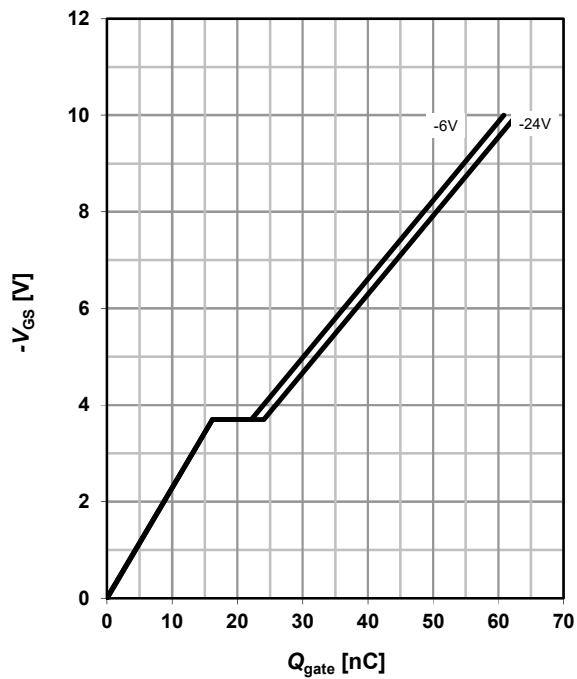
$$V_{BR(DSS)} = f(T_j); I_D = -1 \text{ mA}$$



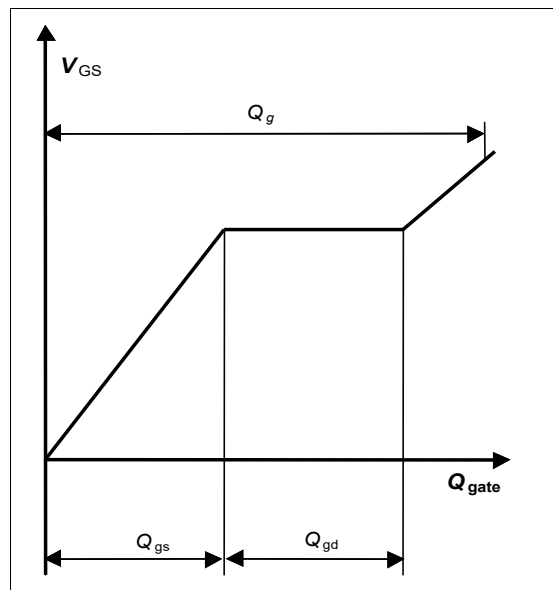
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = -80 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	2018-02-15	Final datasheet
Revision 2.0	2018-07-30	Typo corrected
Revision 2.1	2022-03-10	Corrected Crss

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