

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

800V CoolMOS™ CE Power Transistor
IPA80R650CE

Data Sheet

Rev. 2.1
Final

1 Description

CoolMOS™ CE is a revolutionary technology for high voltage power MOSFETs. The high voltage capability combines safety with performance and ruggedness to allow stable designs at highest efficiency level. CoolMOS™ 800V CE comes with selected package choice offering the benefit of reduced system costs and higher power density designs.

Features

- High voltage technology
- Extreme dv/dt rated
- High peak current capability
- Low gate charge
- Low effective capacitances
- Pb-free plating, RoHS Compliant, Halogen free mold compound
- Qualified for consumer grade applications

Applications

LED Lighting and Adapter in QR Flyback topology

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

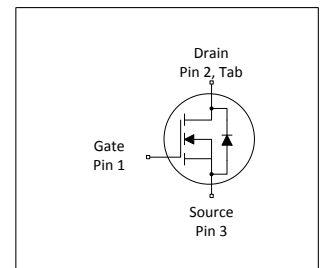


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_J=25^{\circ}C$	800	V
$R_{DS(on),max}$	650	mΩ
$Q_{g,typ}$	45	nC
$I_{D,pulse}$	24	A
$E_{oss}@400V$	3.3	μJ
Body diode di/dt	400	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPA80R650CE	PG-TO 220 FullPAK	8R650CE	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	8.0 5.1	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	24	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	340	mJ	$I_D=1.6\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.20	mJ	$I_D=1.6\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, repetitive	I_{AR}	-	-	1.60	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots640\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	33	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	8.0	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	24	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	4	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	400	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max} < 150^\circ\text{C}$.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 FullPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V$, $I_D=0.25mA$
Gate threshold voltage	$V_{(GS)th}$	2.1	3.0	3.9	V	$V_{DS}=V_{GS}$, $I_D=0.47mA$
Zero gate voltage drain current	I_{DSS}	-	-	20	μA	$V_{DS}=800$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=800$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.56	0.65	Ω	$V_{GS}=10V$, $I_D=5.1A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=5.1A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1.2	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1100	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Output capacitance	C_{oss}	-	46	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	36	-	pF	$V_{GS}=0V$, $V_{DS}=0...480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	99	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...480V$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=8A$, $R_G=10\Omega$; see table 9
Rise time	t_r	-	15	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=8A$, $R_G=10\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	72	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=8A$, $R_G=10\Omega$; see table 9
Fall time	t_f	-	10	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=8A$, $R_G=10\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6	-	nC	$V_{DD}=640V$, $I_D=8A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	22	-	nC	$V_{DD}=640V$, $I_D=8A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	45	-	nC	$V_{DD}=640V$, $I_D=8A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	$V_{DD}=640V$, $I_D=8A$, $V_{GS}=0$ to $10V$

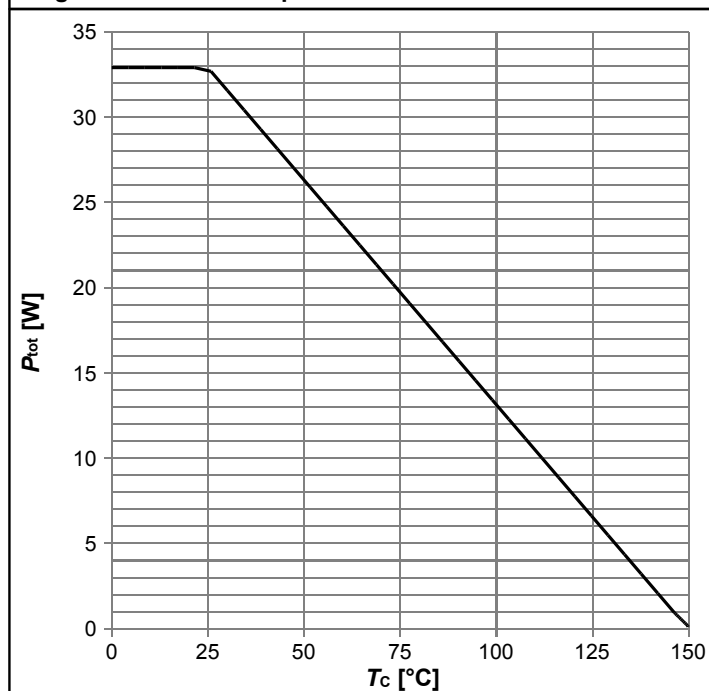
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 480V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 480V

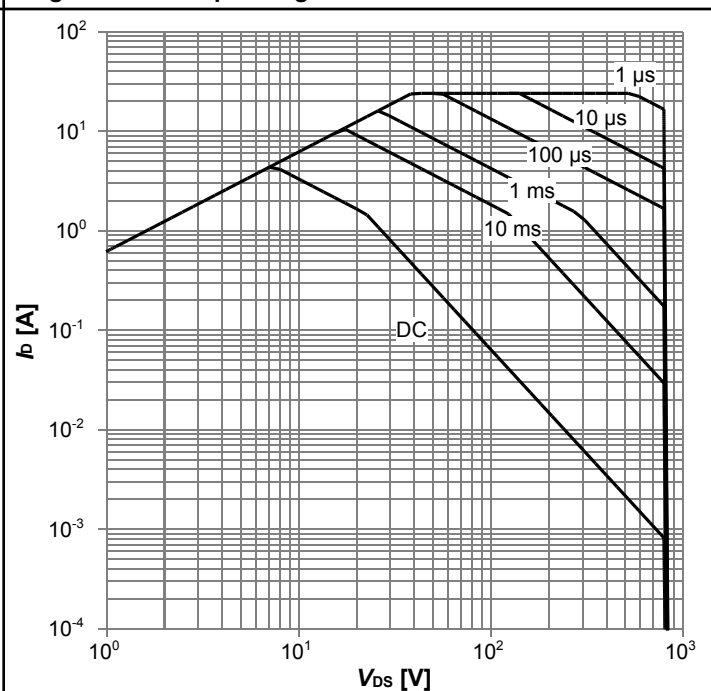
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1	-	V	$V_{GS}=0V$, $I_F=8A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	550	-	ns	$V_R=400V$, $I_F=8A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	7	-	μC	$V_R=400V$, $I_F=8A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	24	-	A	$V_R=400V$, $I_F=8A$, $di_F/dt=100A/\mu s$; see table 8

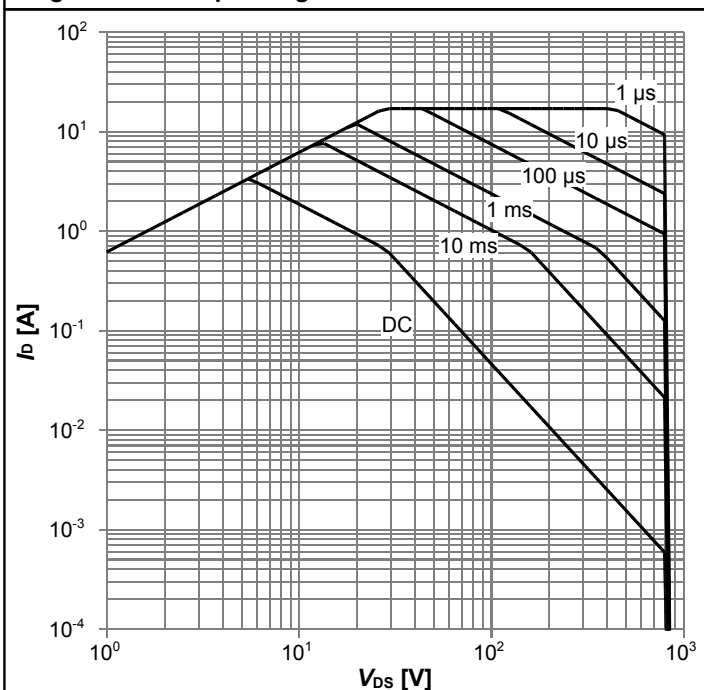
5 Electrical characteristics diagrams

Diagram 1: Power dissipation


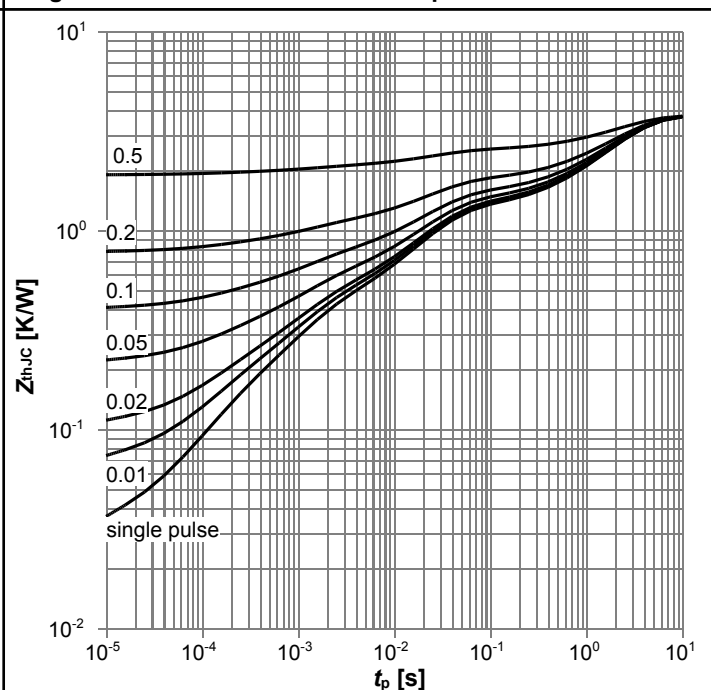
$$P_{tot}=f(T_c)$$

Diagram 2: Safe operating area


$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 3: Safe operating area


$$I_D=f(V_{DS}); T_c=80\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance


$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics

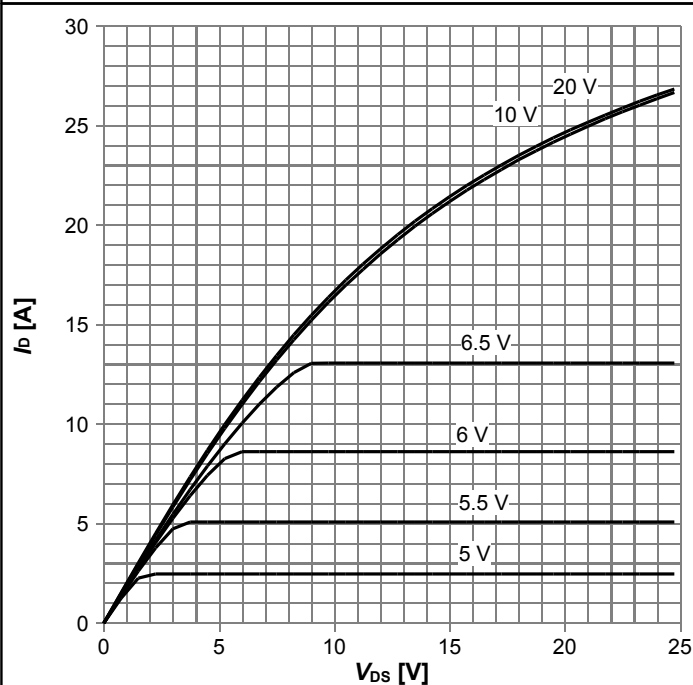

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; t_p = 10\ \mu\text{s}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics

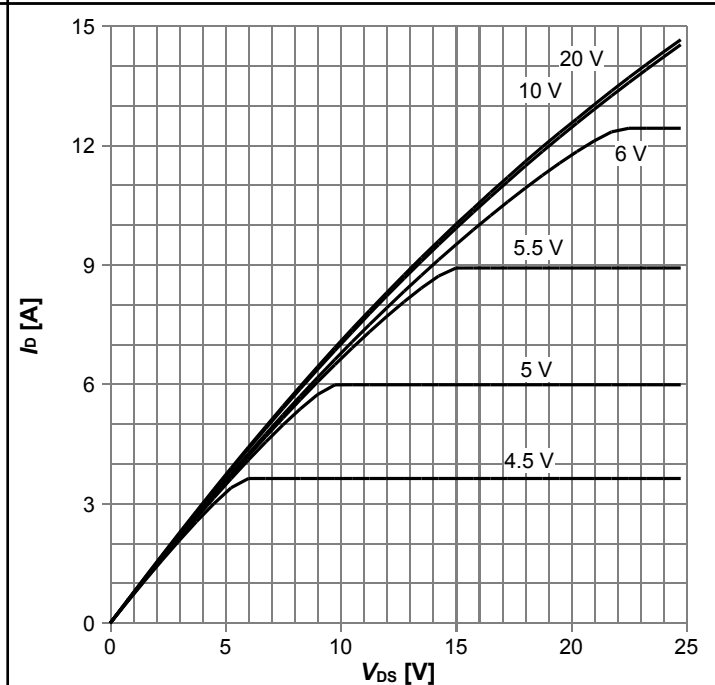

 $I_D = f(V_{DS}); T_J = 150^\circ\text{C}; t_p = 10\ \mu\text{s}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance

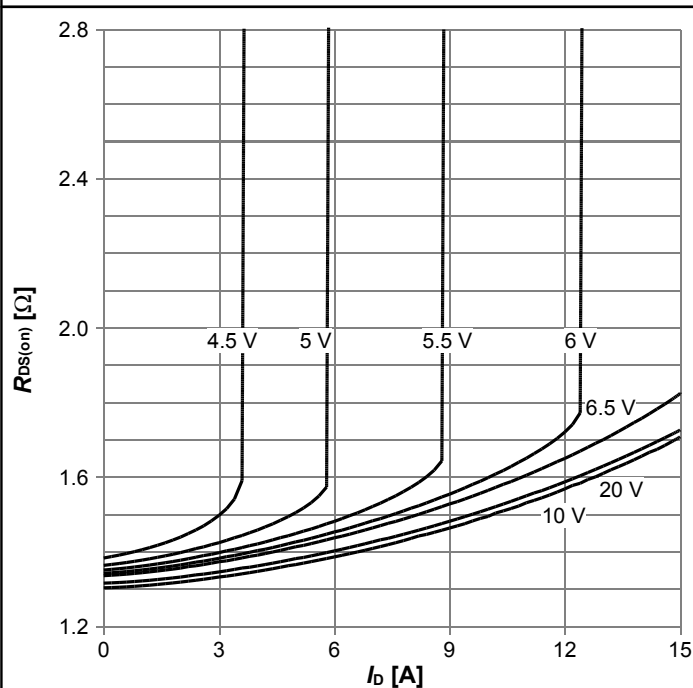

 $R_{DS(on)} = f(I_D); T_J = 150^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance

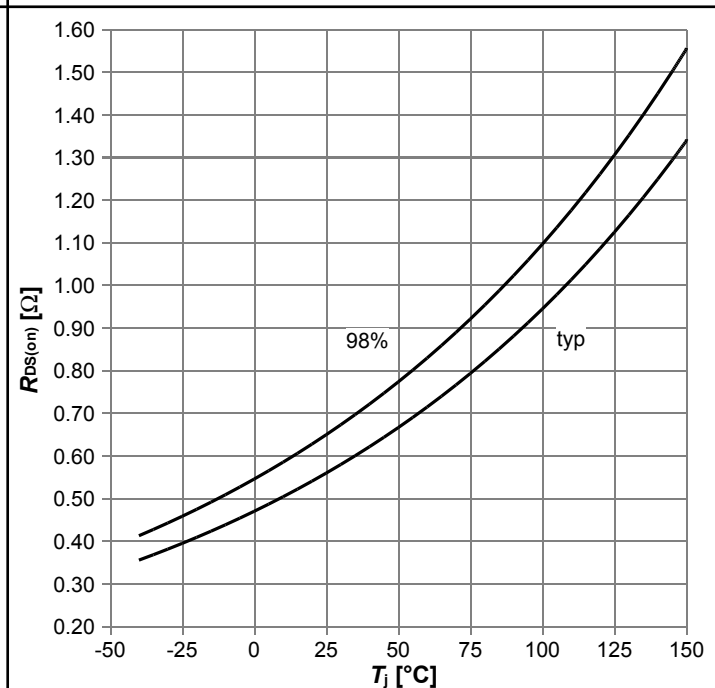

 $R_{DS(on)} = f(T_J); I_D = 5.1\ \text{A}; V_{GS} = 10\ \text{V}$

Diagram 9: Typ. transfer characteristics

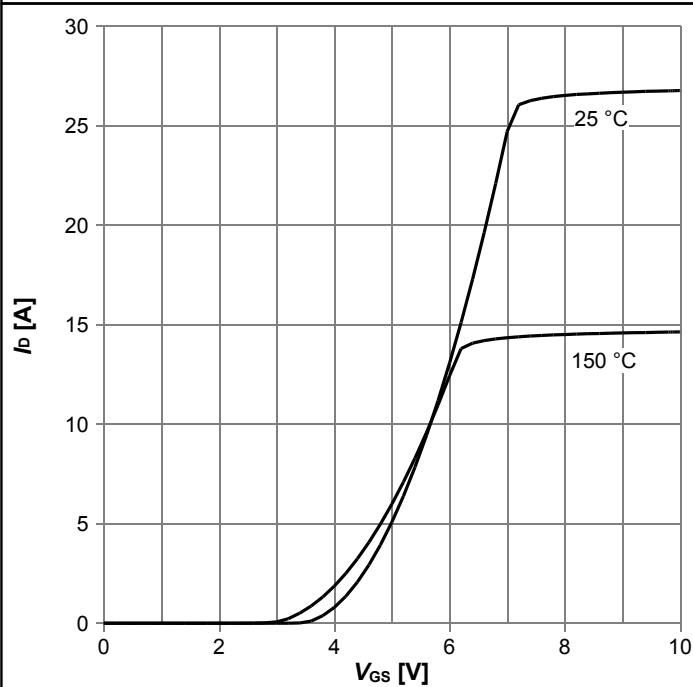

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; t_p = 10 \mu s; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

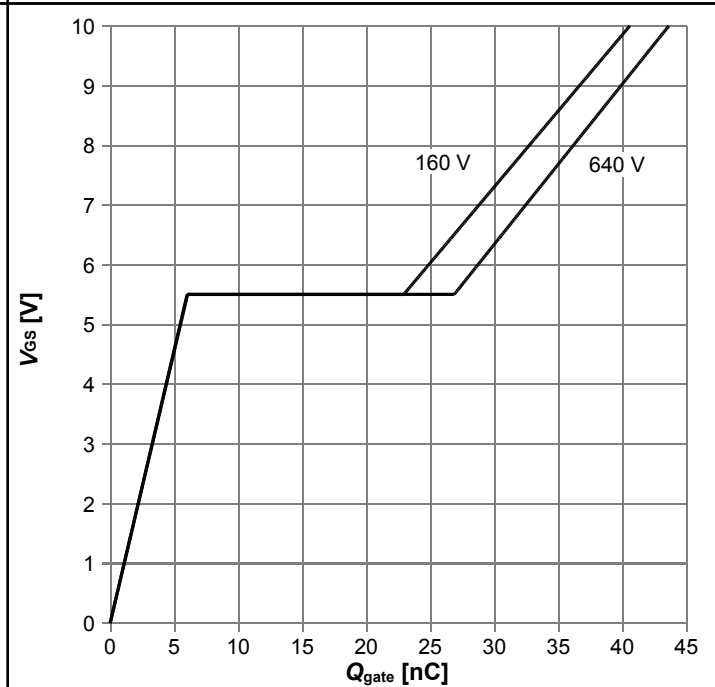

 $V_{GS} = f(Q_{gate}); I_D = 8.0 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode

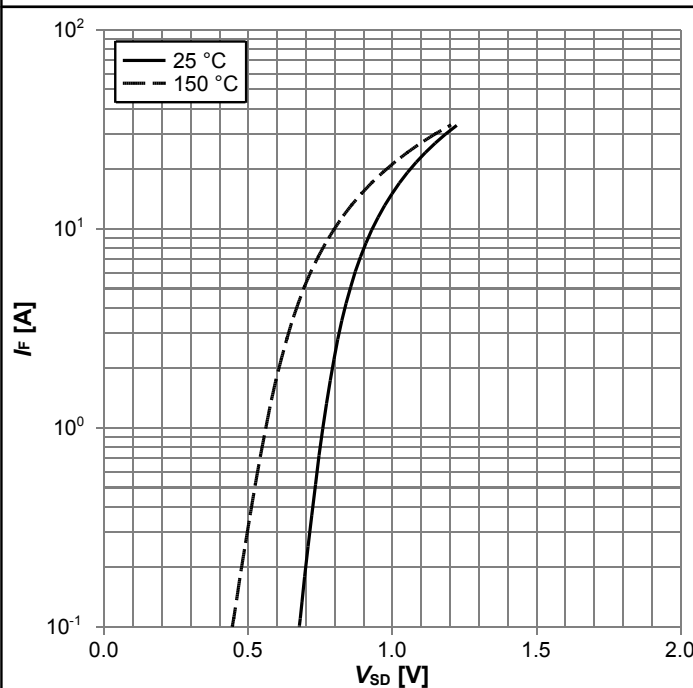

 $I_F = f(V_{SD}); t_p = 10 \mu s; \text{parameter: } T_j$

Diagram 12: Avalanche energy

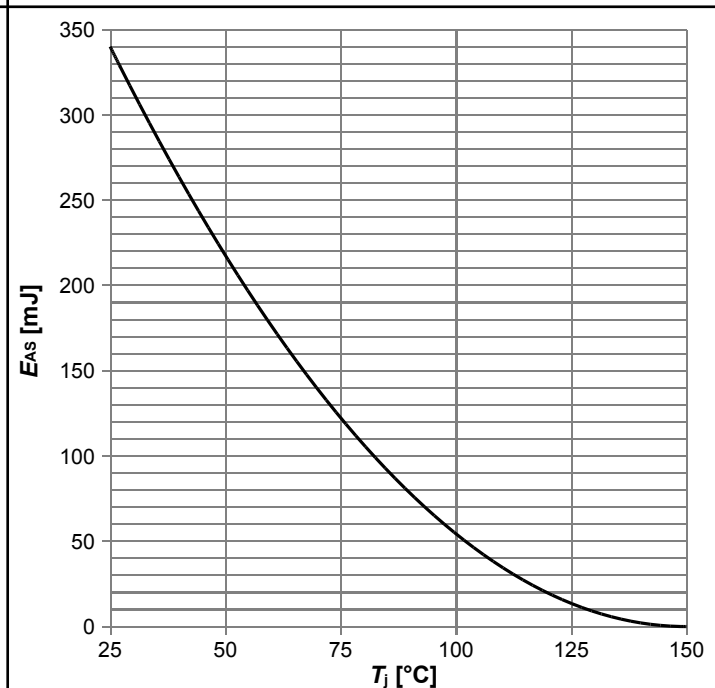
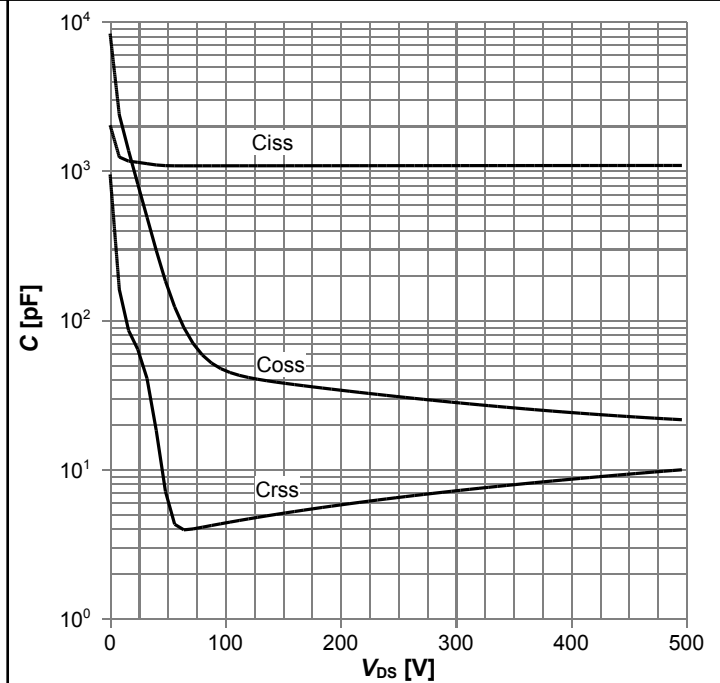

 $E_{AS} = f(T_j); I_D = 1.6 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



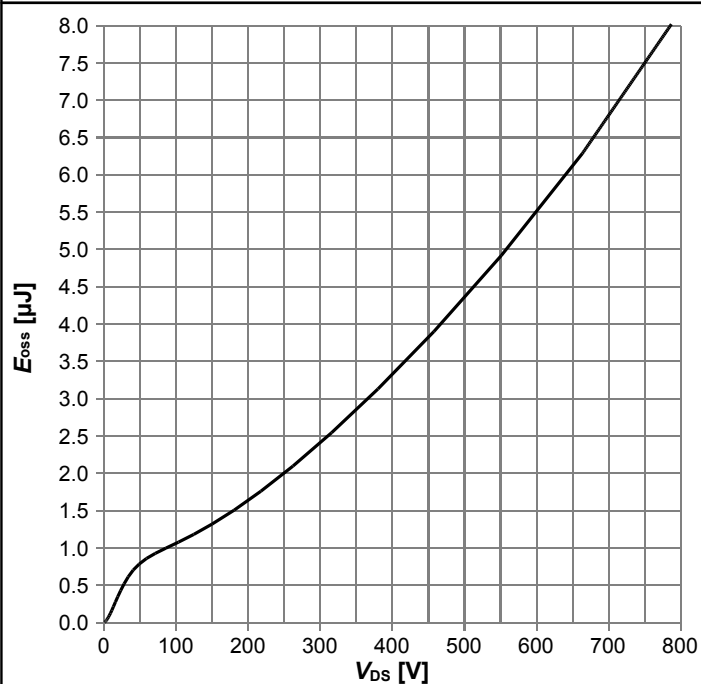
$$V_{BR(DSS)} = f(T_j); I_D = 0.25 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $t_{rr} = t_F + t_s$ $Q_{rr} = Q_F + Q_S$
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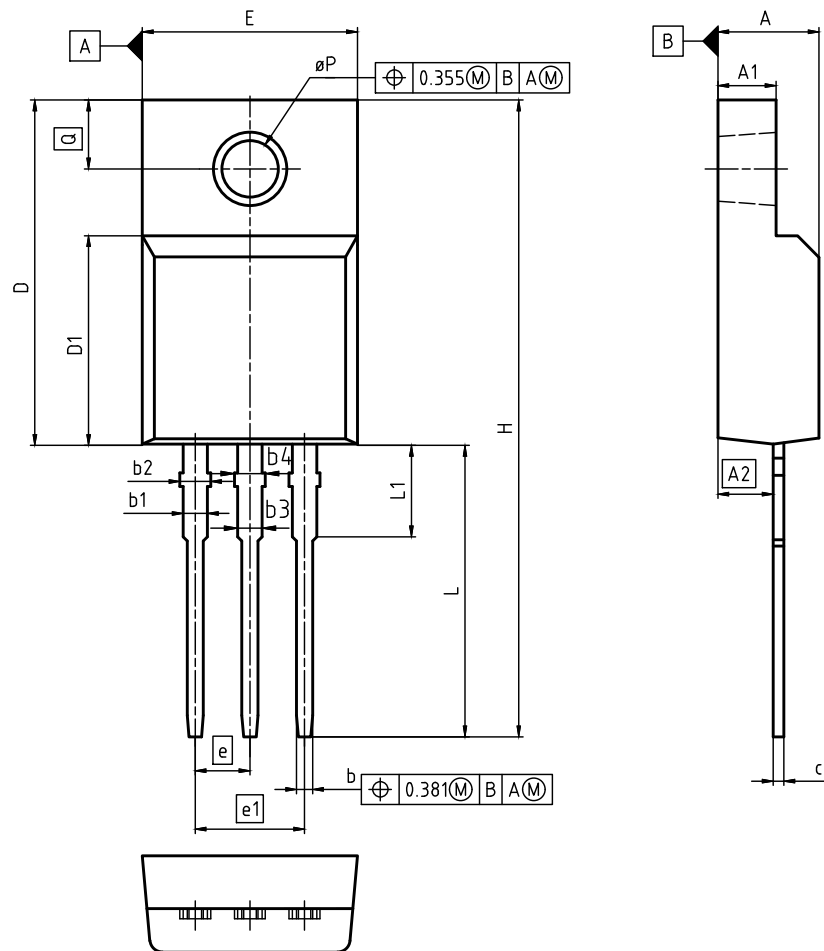
Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform
The circuit diagram illustrates a MOSFET switching an inductive load. A pulse generator is connected to the gate of the MOSFET through a resistor, with the gate voltage labeled V_{GS}. The MOSFET's drain is connected to a DC source and an inductive load (represented by an inductor and a diode in parallel). The drain voltage is labeled V_{DS}. The load is connected to ground.	The timing diagram shows the relationship between the drain-source voltage V_{DS} and the gate-source voltage V_{GS} during switching transitions. The V_{GS} signal is a square wave. The V_{DS} signal shows the voltage across the MOSFET during turn-on and turn-off. Key points on the V_{DS} waveform are marked at 90% and 10% of the supply voltage. The switching times are defined as follows: $t_{d(on)}$: Delay time from 10% V_{GS} to 90% V_{DS}. t_r: Rise time from 90% V_{DS} to 100% V_{DS}. t_{on}: Total turn-on time from 10% V_{GS} to 100% V_{DS}. $t_{d(off)}$: Delay time from 90% V_{DS} to 10% V_{GS}. t_f: Fall time from 10% V_{DS} to 0% V_{DS}. t_{off}: Total turn-off time from 90% V_{DS} to 0% V_{DS}.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

Dimensions do not include mold flash, protrusions or gate burrs

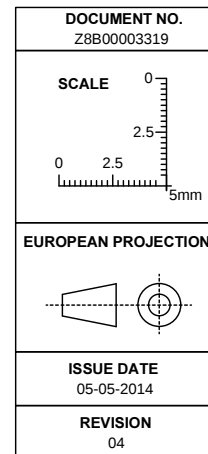


Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA80R650CE

Revision: 2015-06-23, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-09-25	Release of final version
2.1	2015-06-23	Continuous current Id update

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

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