

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ E6 600V

600V CoolMOS™ E6 Power Transistor
IPx60R600E6

Data Sheet

Rev. 2.4
Final

600V CoolMOS™ E6 Power Transistor

IPD60R600E6, IPP60R600E6
IPA60R600E6

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ E6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive, Pb-free plating, halogen free
- Fully qualified according to JEDEC for Industrial Applications

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

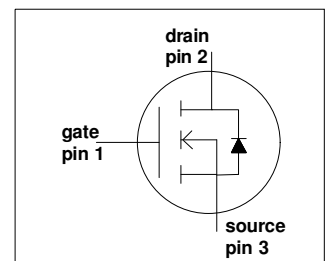
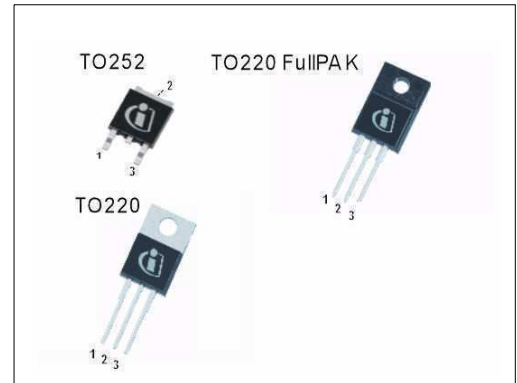


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.6	Ω
$Q_{g,typ}$	20.5	nC
$I_{D,pulse}$	19	A
$E_{oss} @ 400V$	1.9	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPD60R600E6	PG-TO252	6R600E6	IFX CoolMOS Webpage
IPP60R600E6	PG-TO220		IFX Design tools
IPA60R600E6	PG-TO220 FullPAK		

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7.3	A	$T_C = 25\text{ °C}$
				4.6		$T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	19	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	133	mJ	$I_D = 1.3\text{ A}, V_{DD} = 50\text{ V}$ (see table 21)
Avalanche energy, repetitive	E_{AR}	-	-	0.2		$I_D = 1.3\text{ A}, V_{DD} = 50\text{ V}$
Avalanche current, repetitive	I_{AR}	-	-	1.3	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation for TO-220, TO-252	P_{tot}	-	-	63	W	$T_C = 25\text{ °C}$
Power dissipation for TO-220 FullPAK	P_{tot}	-	-	28	W	$T_C = 25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220		-	-	60	Ncm	M3 and M3.5 screws
Mounting torque TO-220 FullPAK				50		M2.5 screws
Continuous diode forward current	I_S	-	-	6.3	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	19	A	$T_C = 25\text{ °C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{ V}, I_{SD} \leq I_D,$ $T_j = 25\text{ °C}$
Maximum diode commutation speed ³⁾	di/dt			500	A/μs	(see table 22)

1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 (IPP60R600E6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.0	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220FullPAK (IPA60R600E6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.5	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-252 (IPD60R600E6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.0	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
			35			
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Electrical characteristics, at $T_J=25\text{ °C}$, unless otherwise specified.

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{ V}$, $I_D=0.25\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}$, $I_D=0.20\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=25\text{ °C}$
		-	10	-		$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.54	0.60	Ω	$V_{GS}=10\text{ V}$, $I_D=2.4\text{ A}$, $T_J=25\text{ °C}$
		-	1.40	-		$V_{GS}=10\text{ V}$, $I_D=2.4\text{ A}$, $T_J=150\text{ °C}$
Gate resistance	R_G	-	10	-	Ω	$f=1\text{ MHz}$, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	440	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	30	-		
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	21	-		$V_{GS}=0\text{ V}$, $V_{DS}=0\ldots 480\text{ V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	88	-		$I_D=\text{constant}$, $V_{GS}=0\text{ V}$ $V_{DS}=0\ldots 480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=3\text{ A}$, $R_G=6.8\text{ }\Omega$ (see table 20)
Rise time	t_r	-	8	-		
Turn-off delay time	$t_{d(off)}$	-	58	-		
Fall time	t_f	-	11	-		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.5	-	nC	$V_{DD}=480\text{ V}$, $I_D=3.0\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	10.5	-		
Gate charge total	Q_g	-	20.5	-		
Gate plateau voltage	V_{plateau}	-	5.4	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=3.0\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	250	-	ns	$V_R=400\text{ V}$, $I_F=3.0\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ (see table 22)
Reverse recovery charge	Q_{rr}	-	2.1	-	μC	
Peak reverse recovery current	I_{rrm}	-	16	-	A	

5 Electrical characteristics diagrams

Table 10

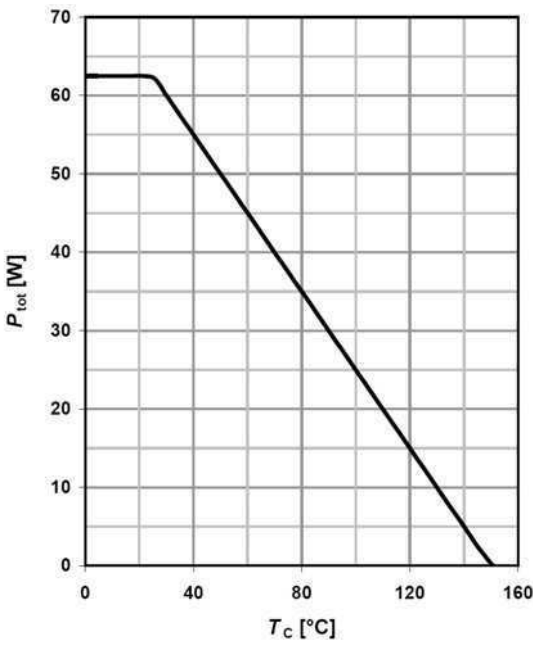
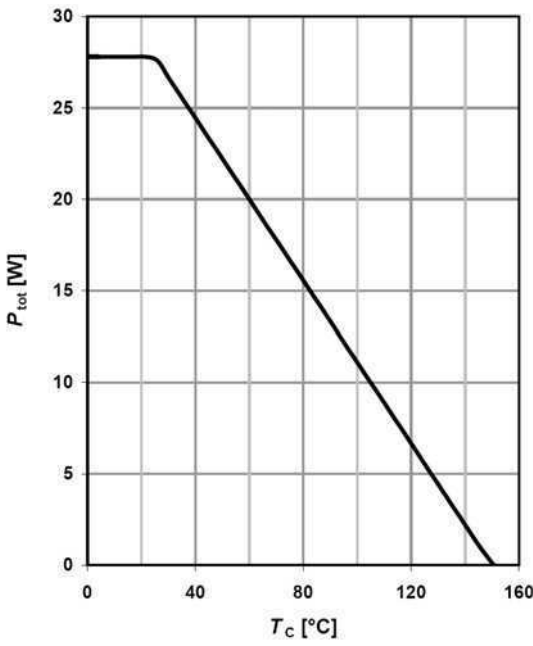
Power dissipation TO-220, TO-252	Power dissipation TO-220 FullPAK
	
$P_{\text{tot}} = f(T_c)$	$P_{\text{tot}} = f(T_c)$

Table 11

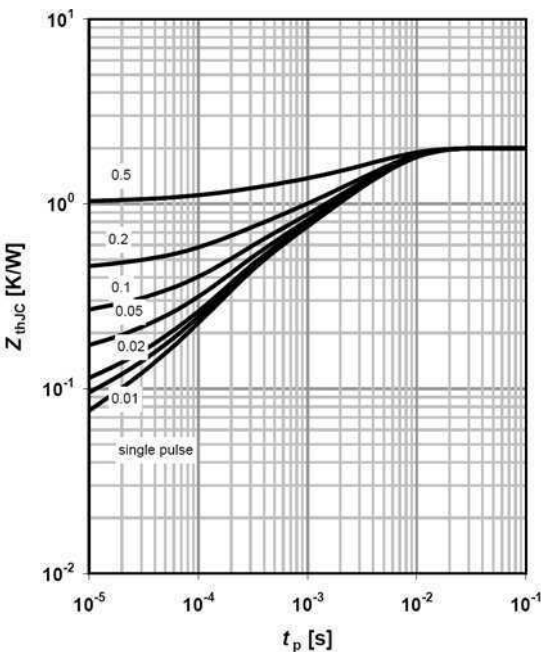
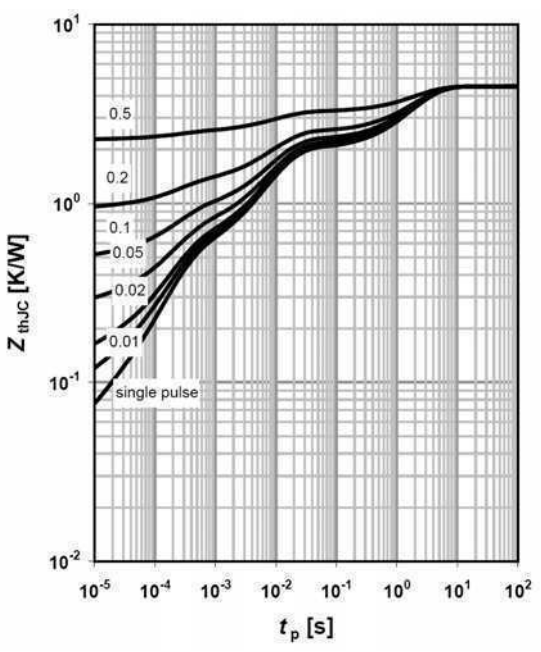
Max. transient thermal impedance TO-220, TO-252	Max. transient thermal impedance TO-220 FullPAK
	
$Z_{(\text{thJC})} = f(t_p)$; parameter: $D = t_p / T$	$Z_{(\text{thJC})} = f(t_p)$; parameter: $D = t_p / T$

Table 12

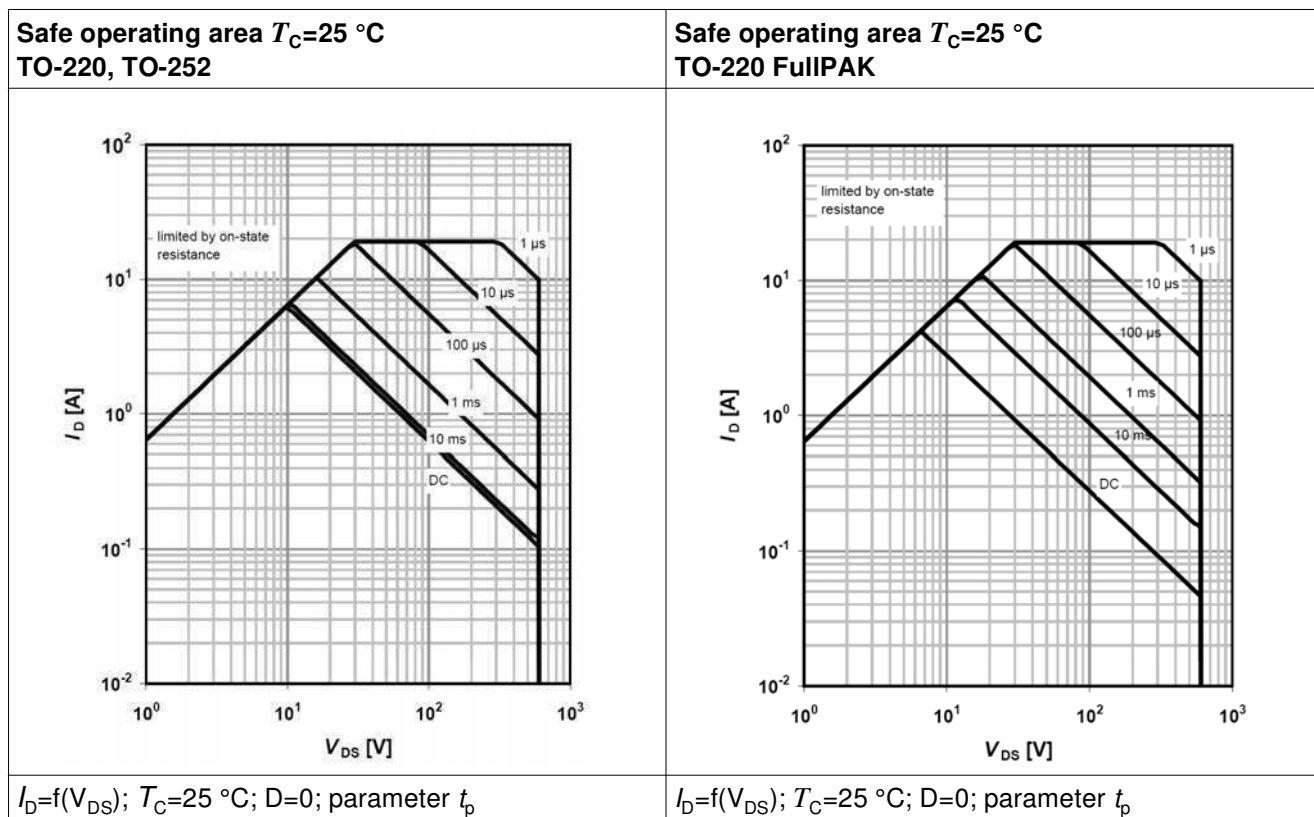
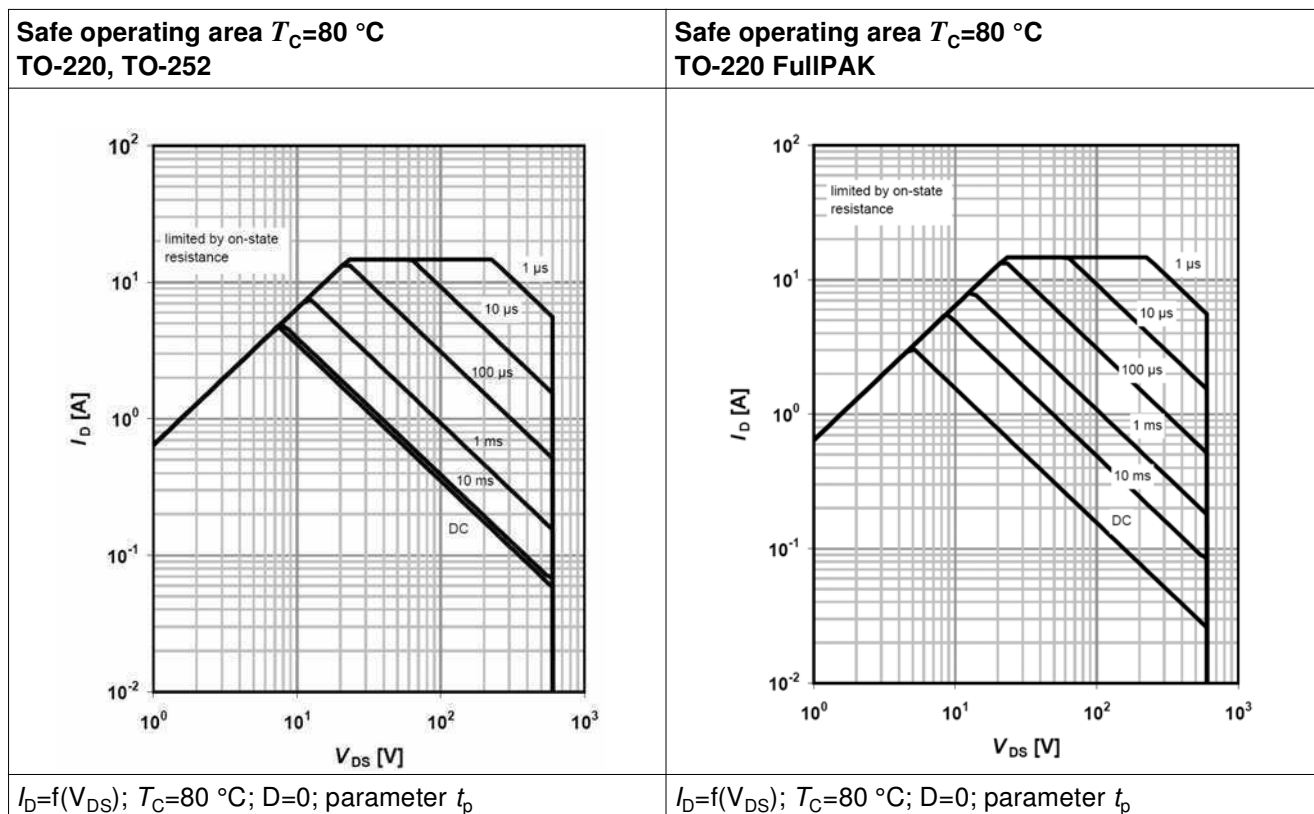


Table 13



Electrical characteristics diagrams

Table 14

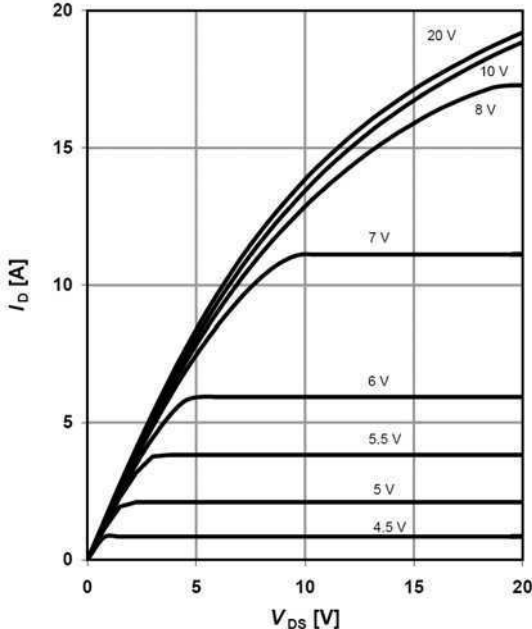
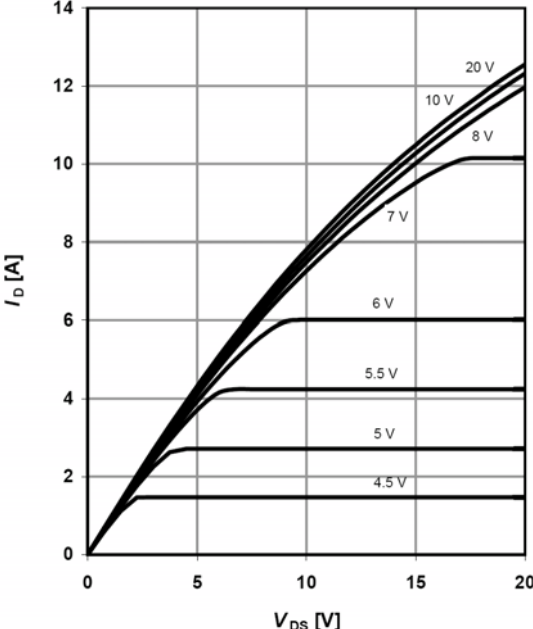
Typ. output characteristics $T_c=25\text{ °C}$	Typ. output characteristics $T_j=125\text{ °C}$
	
$I_D=f(V_{DS}); T_j=25\text{ °C}; \text{parameter: } V_{GS}$	$I_D=f(V_{DS}); T_j=125\text{ °C}; \text{parameter: } V_{GS}$

Table 15

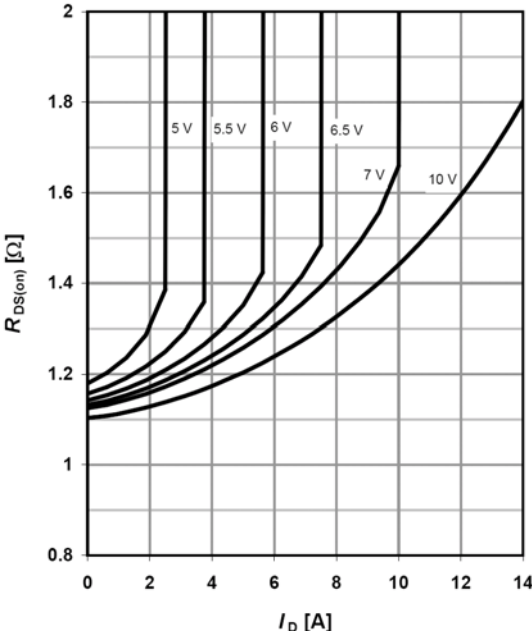
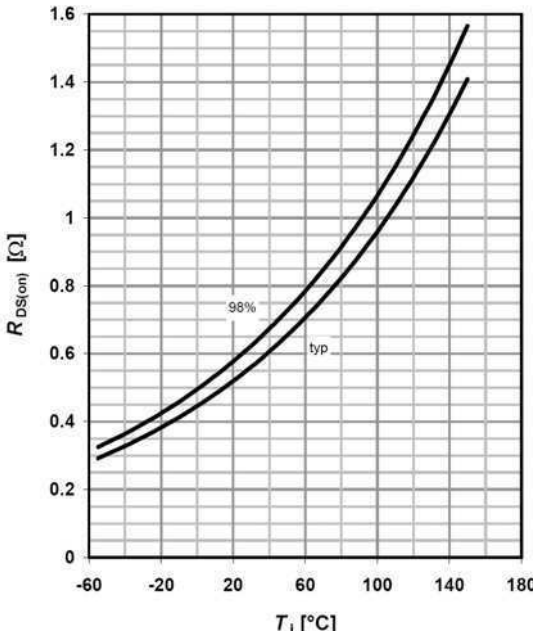
Typ. drain-source on-state resistance	Drain-source on-state resistance
	
$R_{DS(on)}=f(I_D); T_j=125\text{ °C}; \text{parameter: } V_{GS}$	$R_{DS(on)}=f(T_j); I_D=2.4\text{ A}; V_{GS}=10\text{ V}$

Table 16

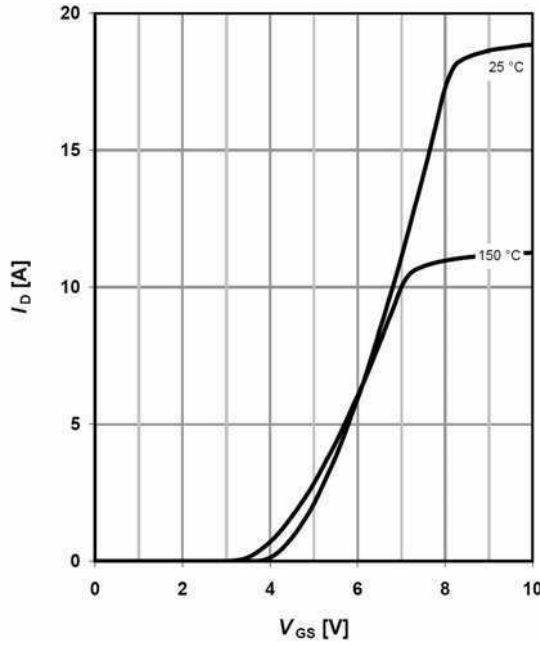
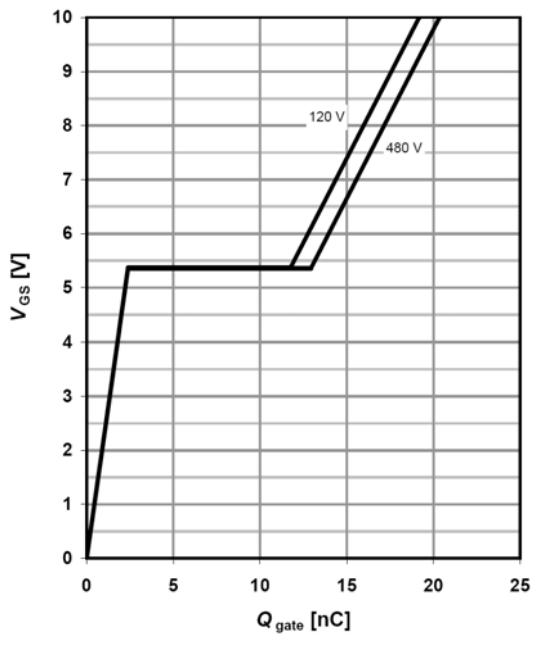
Typ. transfer characteristics	Typ. gate charge
 $I_D = f(V_{GS}); V_{DS} = 20V$	 $V_{GS} = f(Q_{gate}), I_D = 3.0A$ pulsed

Table 17

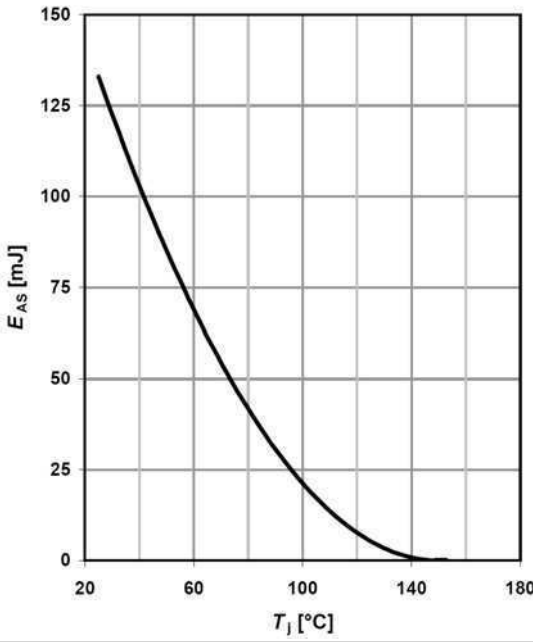
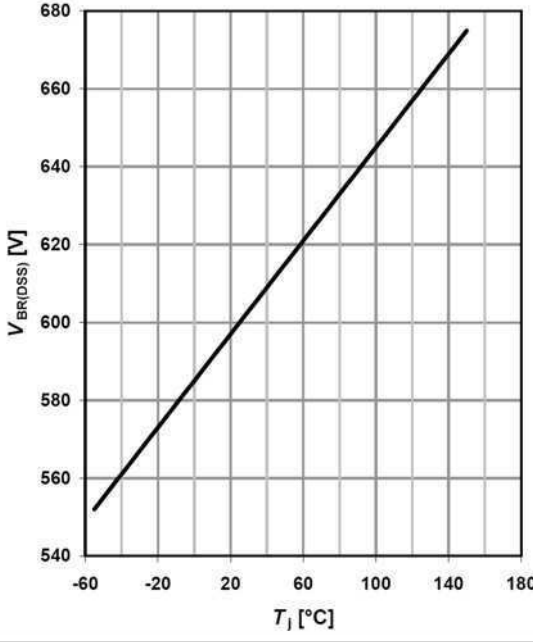
Avalanche energy	Drain-source breakdown voltage
 $E_{AS} = f(T_j); I_D = 1.3 A; V_{DD} = 50 V$	 $V_{BR(DSS)} = f(T_j); I_D = 0.25 mA$

Table 18

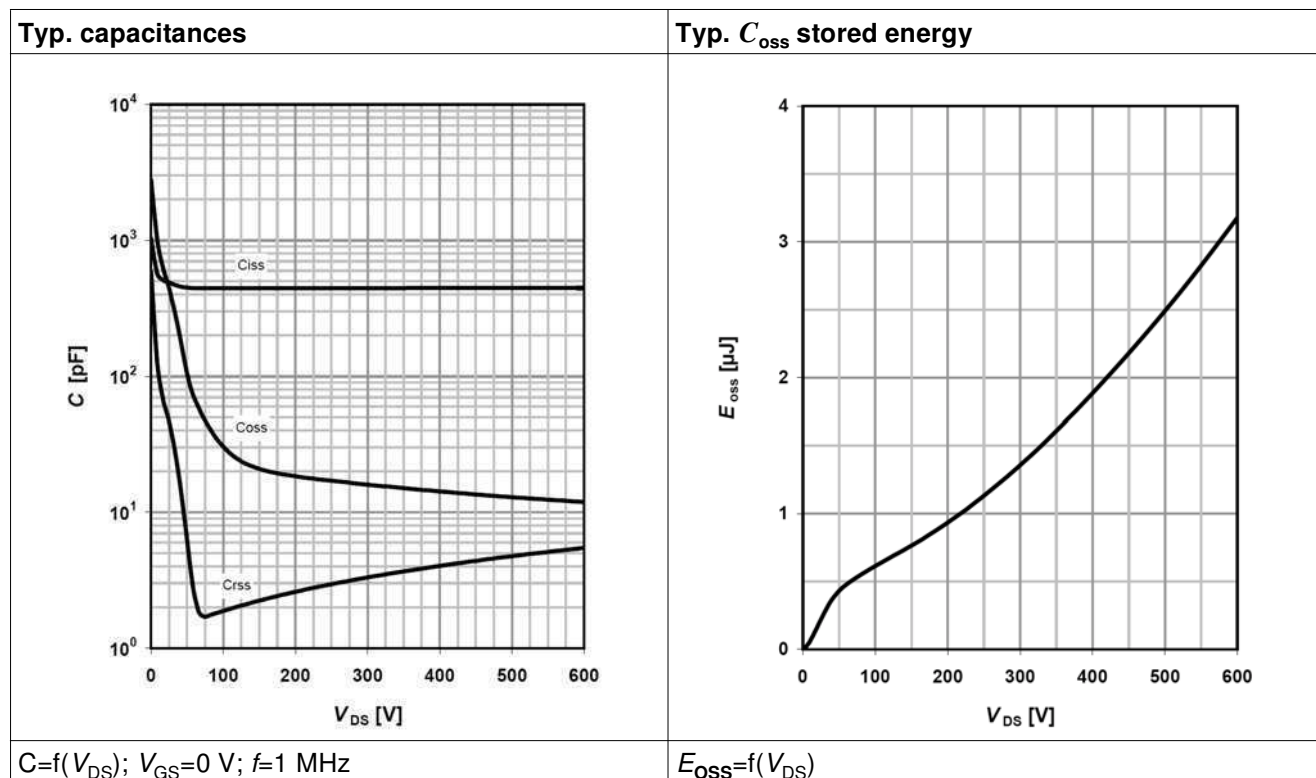
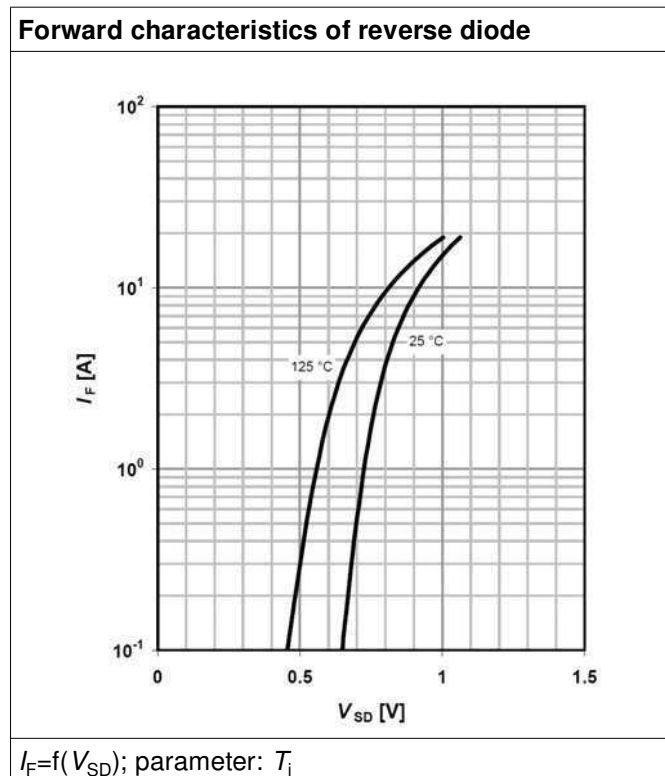


Table 19



6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

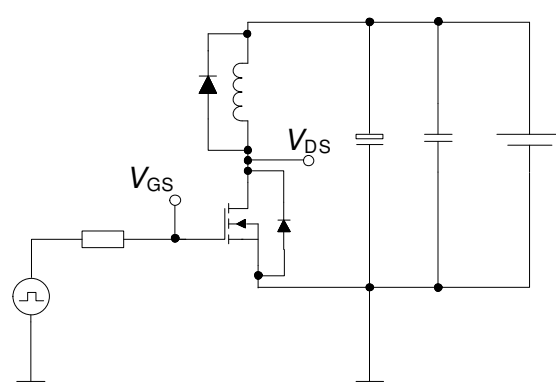
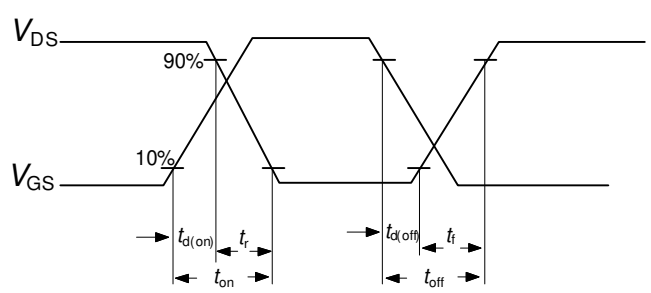
Switching times test circuit for inductive load	Switching time waveform
	

Table 21 Unclamped inductive load test circuit and waveform

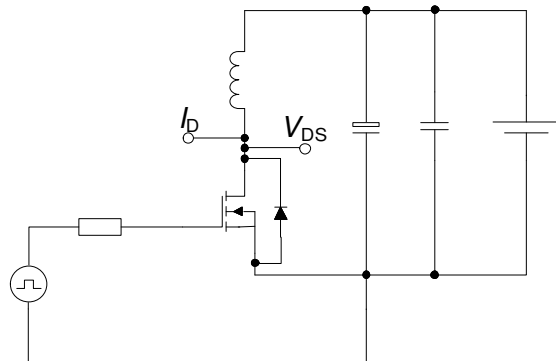
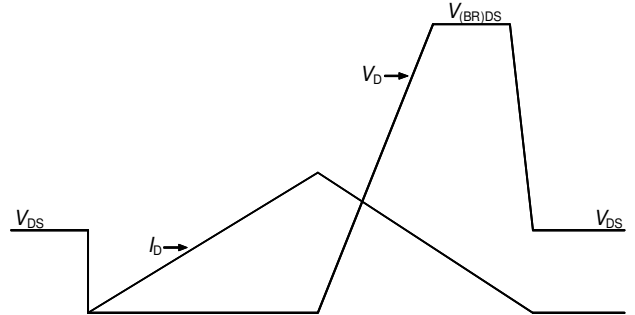
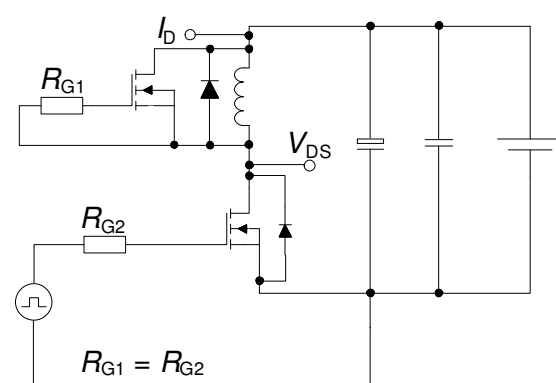
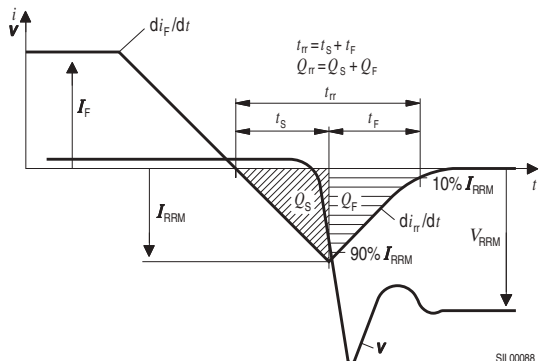
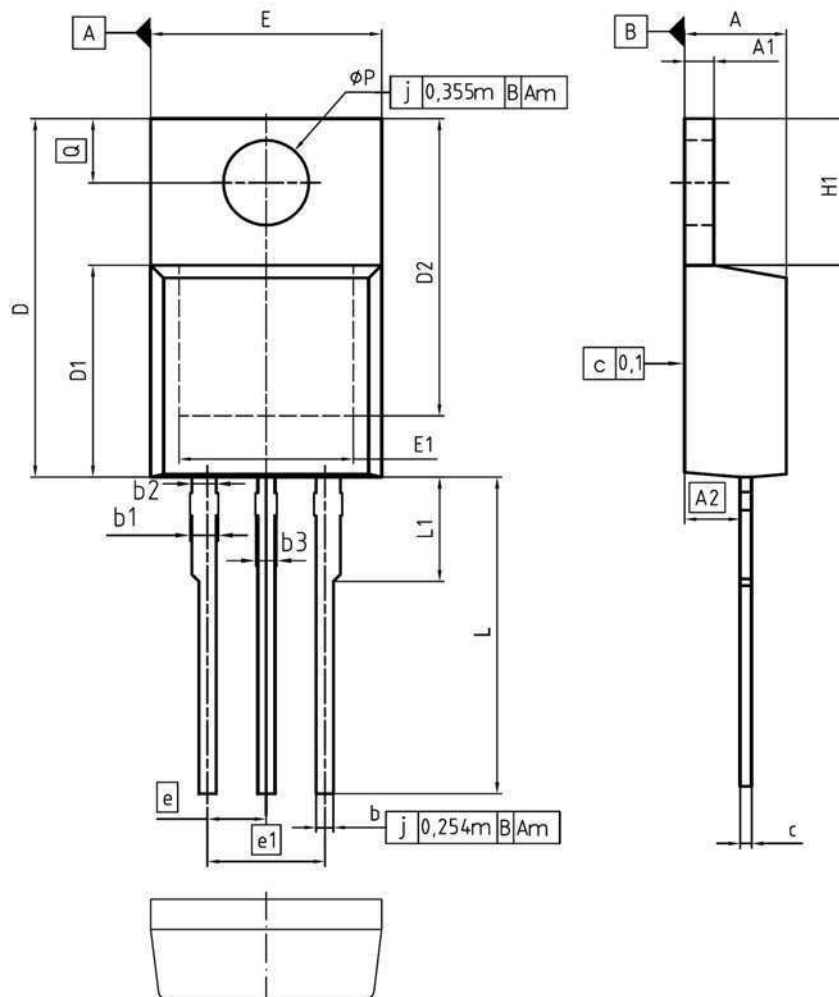
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 22 Test circuit and waveform for diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
	

7 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
phi P	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

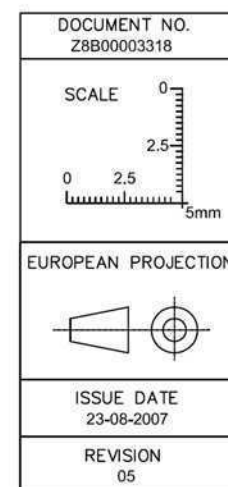


Figure 1 Outlines TO-220, dimensions in mm/inches

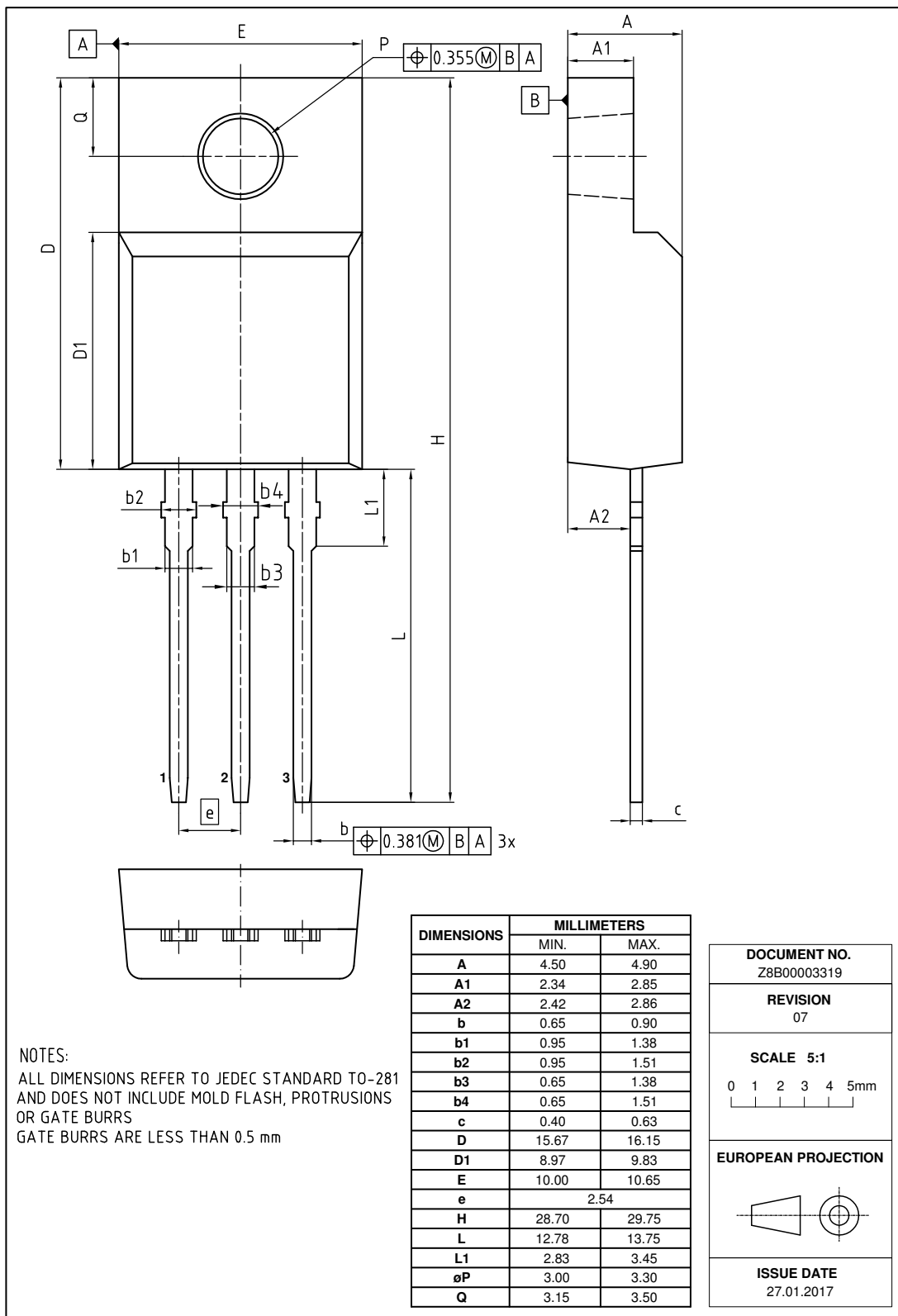
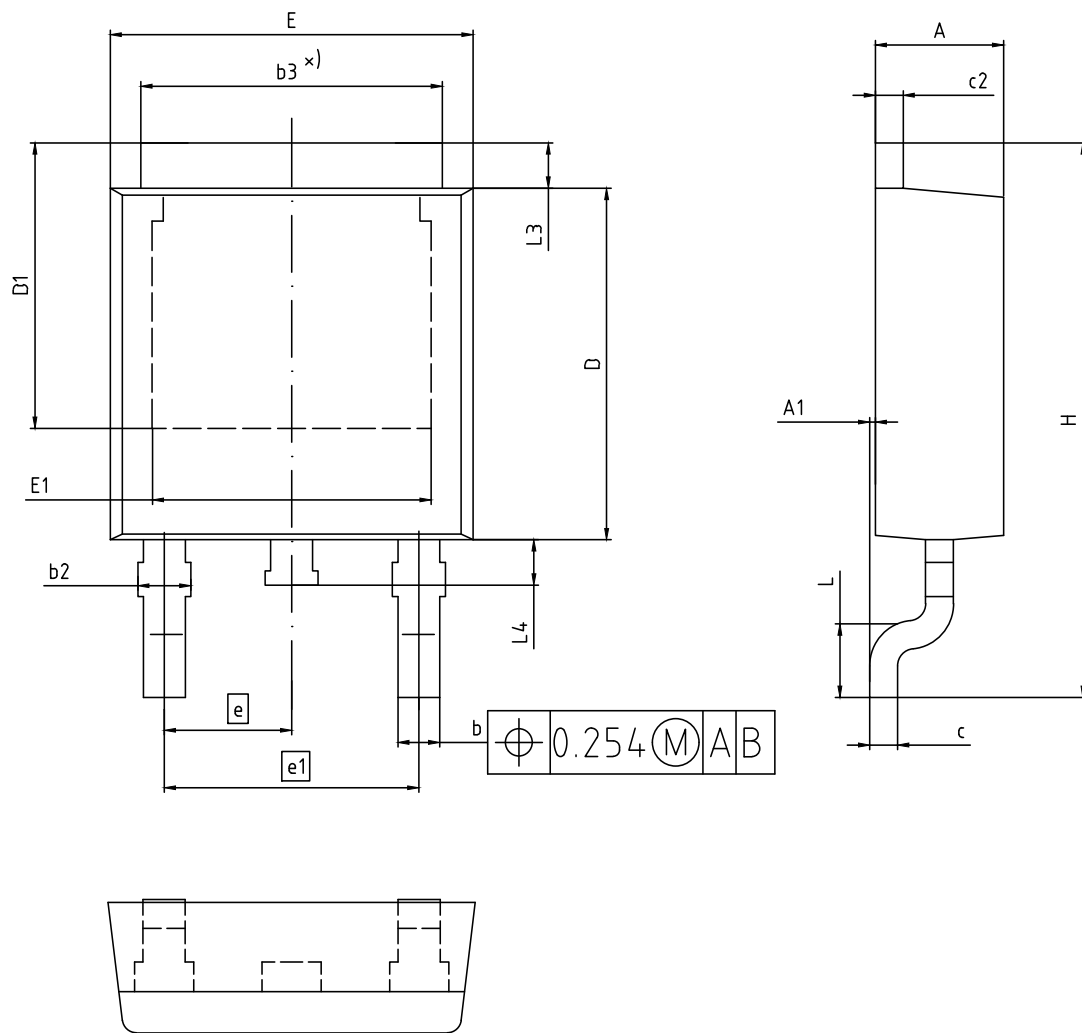


Figure 2 Outline PG-TO 220 FullPAK, dimensions in mm



ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

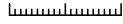
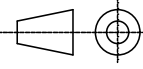
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EUROPEAN PROJECTION 
ISSUE DATE 01.04.2020

Figure 3 Outlines TO-252, dimensions in mm

Revision History

IPx60R600E6

Revision: 2020-05-20, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2011-06-08	Release final data sheet
2.1	2011-09-14	-
2.2	2015-02-11	PG-TO220 FullPAK package outline update (creation:2014-12-10)
2.3	2018-03-04	Outline PG-TO-220 FullPAK update
2.4	2020-05-20	Update of the package outlines TO-252

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