

## SiC MOSFET

### CoolSiC™ MOSFET 650 V G2

Built on Infineon's robust 2<sup>nd</sup> generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

## Features

- Ultra-low switching losses
- Benchmark gate threshold voltage,  $V_{GS(th)} = 4.5 \text{ V}$
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance

## Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

## Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

## Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

**Table 1 Key Performance Parameters**

| Parameter                         | Value | Unit |
|-----------------------------------|-------|------|
| $V_{DSS}$ over full $T_{j,range}$ | 650   | V    |
| $R_{DS(on),typ}$                  | 60    | mΩ   |
| $R_{DS(on),max}$                  | 73    | mΩ   |
| $Q_{G,typ}$                       | 18    | nC   |
| $I_{D,pulse}$                     | 96    | A    |
| $Q_{oss} @ 400 \text{ V}$         | 36    | nC   |
| $E_{oss} @ 400 \text{ V}$         | 4.8   | μJ   |

| Type/Ordering Code | Package    | Marking  | Related Links  |
|--------------------|------------|----------|----------------|
| IMTA65R060M2H      | PG-LHSOF-4 | 65R060M2 | see Appendix A |

PG-LHSOF-4

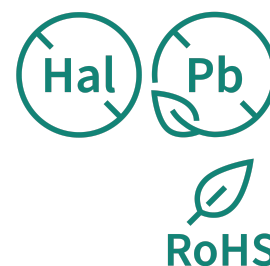
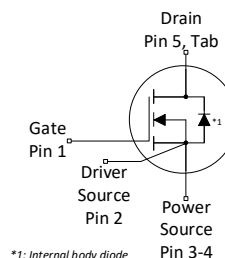
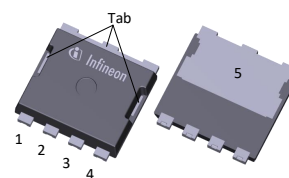




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## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

**Table 2 Maximum ratings**

| Parameter                                      | Symbol           | Values |      |          | Unit | Note/ Test Condition                                                                                        |
|------------------------------------------------|------------------|--------|------|----------|------|-------------------------------------------------------------------------------------------------------------|
|                                                |                  | Min.   | Typ. | Max.     |      |                                                                                                             |
| Continuous DC drain current <sup>1)</sup>      | $I_{\text{DDC}}$ | -      | -    | 37<br>26 | A    | $T_c = 25\text{ °C}$<br>$T_c = 100\text{ °C}$                                                               |
| Peak drain current <sup>2)</sup>               | $I_{\text{DM}}$  | -      | -    | 96       | A    | $T_c = 25\text{ °C}$ , $V_{\text{GS}} = 18\text{ V}$                                                        |
| Avalanche energy, single pulse                 | $E_{\text{AS}}$  | -      | -    | 89       | mJ   | $I_D = 3.4\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11                                         |
| Avalanche energy, repetitive                   | $E_{\text{AR}}$  | -      | -    | 0.44     | mJ   | $I_D = 3.4\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11                                         |
| Avalanche current, single pulse                | $I_{\text{AS}}$  | -      | -    | 3.4      | A    | -                                                                                                           |
| MOSFET $dv/dt$ ruggedness                      | $dv/dt$          | -      | -    | 200      | V/ns | $V_{\text{DS}} = 0 \dots 400\text{ V}$                                                                      |
| Gate source voltage (static) <sup>3)</sup>     | $V_{\text{GS}}$  | -7     | -    | 23       | V    | -                                                                                                           |
| Gate source voltage (transient)                | $V_{\text{GS}}$  | -10    | -    | 25       | V    | $t_p \leq 500\text{ ns}$ , duty cycle $\leq 1\%$                                                            |
| Power dissipation                              | $P_{\text{tot}}$ | -      | -    | 165      | W    | $T_c = 25\text{ °C}$                                                                                        |
| Storage temperature                            | $T_{\text{stg}}$ | -55    | -    | 150      | °C   | -                                                                                                           |
| Operating junction temperature                 | $T_j$            | -55    | -    | 175      | °C   | -                                                                                                           |
| Mounting torque                                | -                | -      | -    | -        | Ncm  | -                                                                                                           |
| Continuous reverse drain current <sup>1)</sup> | $I_{\text{SDC}}$ | -      | -    | 37<br>26 | A    | $V_{\text{GS}} = 18\text{ V}$ , $T_c = 25\text{ °C}$<br>$V_{\text{GS}} = 0\text{ V}$ , $T_c = 25\text{ °C}$ |
| Peak reverse drain current <sup>2)</sup>       | $I_{\text{SM}}$  | -      | -    | 96<br>29 | A    | $T_c = 25\text{ °C}$ , $t_p \leq 250\text{ ns}$<br>$T_c = 25\text{ °C}$                                     |
| Insulation withstand voltage                   | $V_{\text{ISO}}$ | -      | -    | n.a.     | V    | $V_{\text{rms}}$ , $T_c = 25\text{ °C}$ , $t = 1\text{ min}$                                                |

<sup>1)</sup> Limited by  $T_{j,\text{max}}$ .

<sup>2)</sup> Pulse width  $t_{\text{pulse}}$  limited by  $T_{j,\text{max}}$ .

<sup>3)</sup> The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter                                       | Symbol        | Values |      |      | Unit | Note/ Test Condition                                                                                     |
|-------------------------------------------------|---------------|--------|------|------|------|----------------------------------------------------------------------------------------------------------|
|                                                 |               | Min.   | Typ. | Max. |      |                                                                                                          |
| Thermal resistance, junction - case             | $R_{th(j-c)}$ | -      | -    | 0.91 | °C/W | Not subject to production test.<br>Parameter verified by design/characterization according to JESD51-14. |
| Soldering temperature, reflow soldering allowed | $T_{sold}$    | -      | -    | 260  | °C   | reflow MSL1                                                                                              |

### 3 Operating range

**Table 4**    **Operating range**

| Parameter                    | Symbol        | Values |      |      | Unit | Note/ Test Condition |
|------------------------------|---------------|--------|------|------|------|----------------------|
|                              |               | Min.   | Typ. | Max. |      |                      |
| Recommended turn-on voltage  | $V_{GS(on)}$  | -      | 18   | -    | V    | -                    |
| Recommended turn-off voltage | $V_{GS(off)}$ | -      | 0    | -    | V    | -                    |

## 4 Electrical characteristics

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 5 Static characteristics**

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| Parameter                            | Symbol       | Values |                      |                   | Unit          | Note/ Test Condition                                                                                                                                                                                                                                                                              |
|--------------------------------------|--------------|--------|----------------------|-------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                      |              | Min.   | Typ.                 | Max.              |               |                                                                                                                                                                                                                                                                                                   |
| Drain-source voltage                 | $V_{DS}$     | 650    | -                    | -                 | V             | $V_{GS} = 0\text{ V}$ , $I_D = 0.31\text{ mA}$                                                                                                                                                                                                                                                    |
| Gate threshold voltage <sup>4)</sup> | $V_{GS(th)}$ | 3.5    | 4.5                  | 5.6               | V             | $V_{DS} = V_{GS}$ , $I_D = 3.1\text{ mA}$                                                                                                                                                                                                                                                         |
| Zero gate voltage drain current      | $I_{DSS}$    | -      | 1<br>3               | 75<br>-           | $\mu\text{A}$ | $V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$<br>$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 175\text{ °C}$                                                                                                                                                 |
| Gate-source leakage current          | $I_{GSS}$    | -      | -                    | 100               | nA            | $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$                                                                                                                                                                                                                                                    |
| Drain-source on-state resistance     | $R_{DS(on)}$ | -      | 78<br>60<br>55<br>98 | -<br>73<br>-<br>- | m $\Omega$    | $V_{GS} = 15\text{ V}$ , $I_D = 15.4\text{ A}$ , $T_j = 25\text{ °C}$<br>$V_{GS} = 18\text{ V}$ , $I_D = 15.4\text{ A}$ , $T_j = 25\text{ °C}$<br>$V_{GS} = 20\text{ V}$ , $I_D = 15.4\text{ A}$ , $T_j = 25\text{ °C}$<br>$V_{GS} = 18\text{ V}$ , $I_D = 15.4\text{ A}$ , $T_j = 175\text{ °C}$ |
| Internal gate resistance             | $R_{G,int}$  | -      | 5.1                  | -                 | $\Omega$      | $f = 1\text{ MHz}$                                                                                                                                                                                                                                                                                |

<sup>4)</sup> Tested after 1 ms pulse at  $V_{GS} = +20\text{ V}$ . "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.  
Stray inductances and coupling capacitances must be minimized.  
For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter                                                  | Symbol      | Values |      |      | Unit | Note/ Test Condition                                                                                                              |
|------------------------------------------------------------|-------------|--------|------|------|------|-----------------------------------------------------------------------------------------------------------------------------------|
|                                                            |             | Min.   | Typ. | Max. |      |                                                                                                                                   |
| Input capacitance                                          | $C_{iss}$   | -      | 669  | -    | pF   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$                                                            |
| Reverse transfer capacitance                               | $C_{rss}$   | -      | 4.1  | -    | pF   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$                                                            |
| Output capacitance <sup>5)</sup>                           | $C_{oss}$   | -      | 50   | 65   | pF   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$                                                            |
| Output charge <sup>5)</sup>                                | $Q_{oss}$   | -      | 36   | 46   | nC   | calculation based on $C_{oss}$                                                                                                    |
| Effective output capacitance, energy related <sup>6)</sup> | $C_{o(er)}$ | -      | 60   | -    | pF   | $V_{GS} = 0\text{ V}$ ,<br>$V_{DS} = 0...400\text{ V}$                                                                            |
| Effective output capacitance, time related <sup>7)</sup>   | $C_{o(tr)}$ | -      | 89   | -    | pF   | $I_D = \text{constant}$ , $V_{GS} = 0\text{ V}$ , $V_{DS} = 0...400\text{ V}$                                                     |
| Turn-on delay time                                         | $t_{d(on)}$ | -      | 6.3  | -    | ns   | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ;<br>see table 10 |
| Rise time                                                  | $t_r$       | -      | 5.6  | -    | ns   | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ;<br>see table 10 |

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter                               | Symbol       | Values |      |      | Unit          | Note/ Test Condition                                                                                                              |
|-----------------------------------------|--------------|--------|------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------------|
|                                         |              | Min.   | Typ. | Max. |               |                                                                                                                                   |
| Turn-off delay time                     | $t_{d(off)}$ | -      | 13.7 | -    | ns            | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ;<br>see table 10 |
| Fall time                               | $t_f$        | -      | 4.8  | -    | ns            | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ;<br>see table 10 |
| Turn-ON switching losses <sup>8)</sup>  | $E_{on}$     | -      | 26   | -    | $\mu\text{J}$ | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$                   |
| Turn-OFF switching losses <sup>8)</sup> | $E_{off}$    | -      | 13   | -    | $\mu\text{J}$ | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$                   |
| Total switching losses <sup>8)</sup>    | $E_{tot}$    | -      | 39   | -    | $\mu\text{J}$ | $V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ ,<br>$I_D = 15.4\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$                   |

<sup>5)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

<sup>6)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

<sup>7)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

<sup>8)</sup> Values for 4-pin configuration based on PG-HDSOP-16 measurements; MOSFET used in half-bridge configuration without external diode

**Table 7 Gate charge characteristics**

| Parameter                     | Symbol       | Values |      |      | Unit | Note/ Test Condition                                                                    |
|-------------------------------|--------------|--------|------|------|------|-----------------------------------------------------------------------------------------|
|                               |              | Min.   | Typ. | Max. |      |                                                                                         |
| Plateau gate to source charge | $Q_{GS(pl)}$ | -      | 4.9  | -    | nC   | $V_{DD} = 400\text{ V}$ , $I_D = 15.4\text{ A}$ ,<br>$V_{GS} = 0\text{ to }18\text{ V}$ |
| Gate to drain charge          | $Q_{GD}$     | -      | 3.4  | -    | nC   | $V_{DD} = 400\text{ V}$ , $I_D = 15.4\text{ A}$ ,<br>$V_{GS} = 0\text{ to }18\text{ V}$ |
| Total gate charge             | $Q_G$        | -      | 18   | -    | nC   | $V_{DD} = 400\text{ V}$ , $I_D = 15.4\text{ A}$ ,<br>$V_{GS} = 0\text{ to }18\text{ V}$ |

**Table 8 Reverse diode characteristics**

| Parameter                    | Symbol   | Values |              |      | Unit | Note/ Test Condition                                                                                                                                                                                                 |
|------------------------------|----------|--------|--------------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                              |          | Min.   | Typ.         | Max. |      |                                                                                                                                                                                                                      |
| Drain-source reverse voltage | $V_{SD}$ | -      | 4.3          | -    | V    | $V_{GS} = 0\text{ V}$ , $I_S = 15.4\text{ A}$ , $T_j = 25\text{ }^\circ\text{C}$                                                                                                                                     |
| MOSFET forward recovery time | $t_{fr}$ | -      | 19.5<br>11.1 | -    | ns   | $V_{DD} = 400\text{ V}$ , $I_S = 15.4\text{ A}$ ,<br>$di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9<br>$V_{DD} = 400\text{ V}$ , $I_S = 15.4\text{ A}$ ,<br>$di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9 |

**Table 8 Reverse diode characteristics**

| Parameter                                    | Symbol    | Values |             |      | Unit | Note/ Test Condition                                                                                                                                                                                                 |
|----------------------------------------------|-----------|--------|-------------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                              |           | Min.   | Typ.        | Max. |      |                                                                                                                                                                                                                      |
| MOSFET forward recovery charge <sup>9)</sup> | $Q_{fr}$  | -      | 65<br>75    | -    | nC   | $V_{DD} = 400\text{ V}$ , $I_S = 15.4\text{ A}$ ,<br>$di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9<br>$V_{DD} = 400\text{ V}$ , $I_S = 15.4\text{ A}$ ,<br>$di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9 |
| MOSFET peak forward recovery current         | $I_{frm}$ | -      | 6.7<br>13.5 | -    | A    | $V_{DD} = 400\text{ V}$ , $I_S = 15.4\text{ A}$ ,<br>$di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9<br>$V_{DD} = 400\text{ V}$ , $I_S = 15.4\text{ A}$ ,<br>$di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9 |

<sup>9)</sup>  $Q_{fr}$  includes  $Q_{oss}$



## 5 Electrical characteristics diagrams

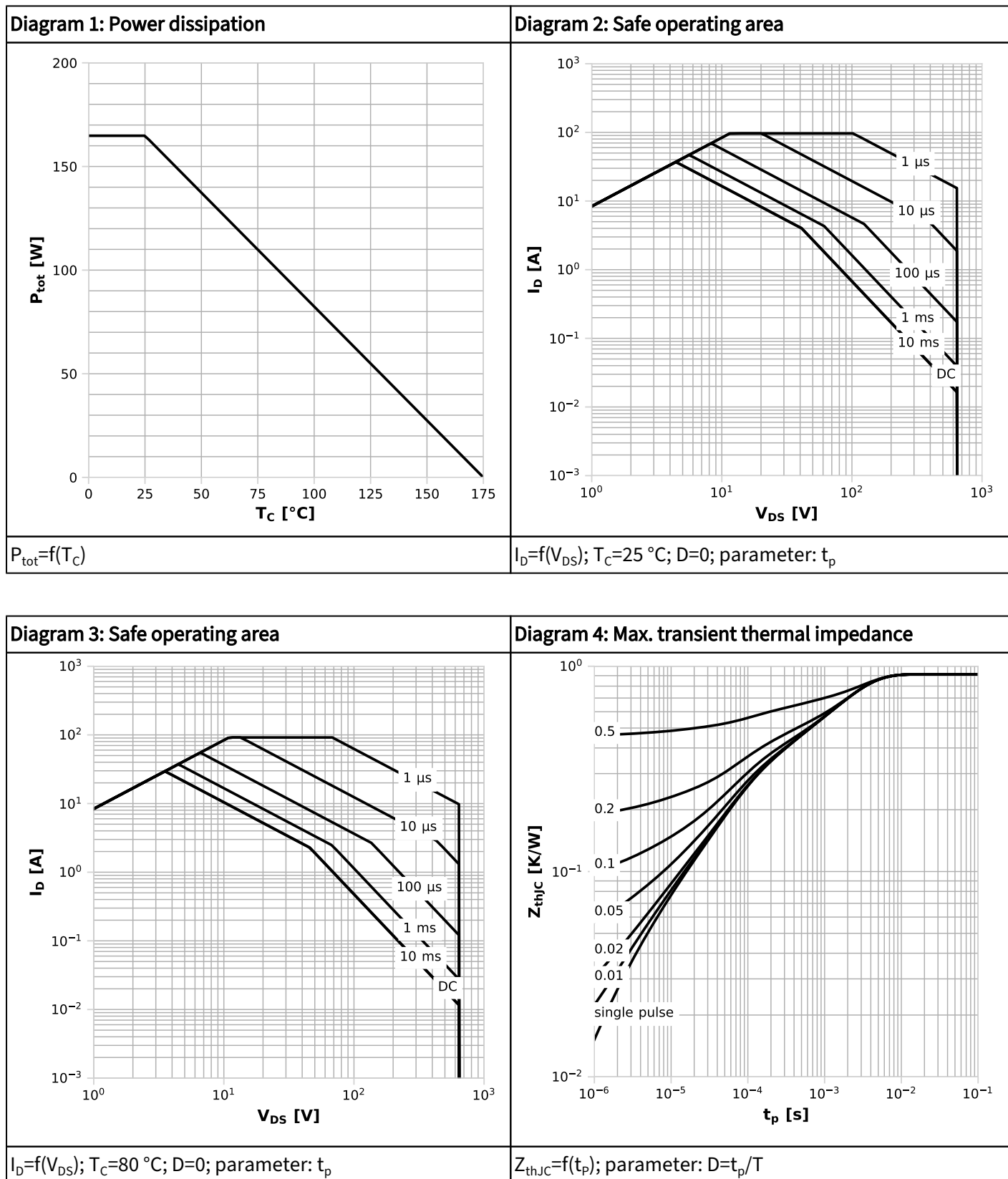
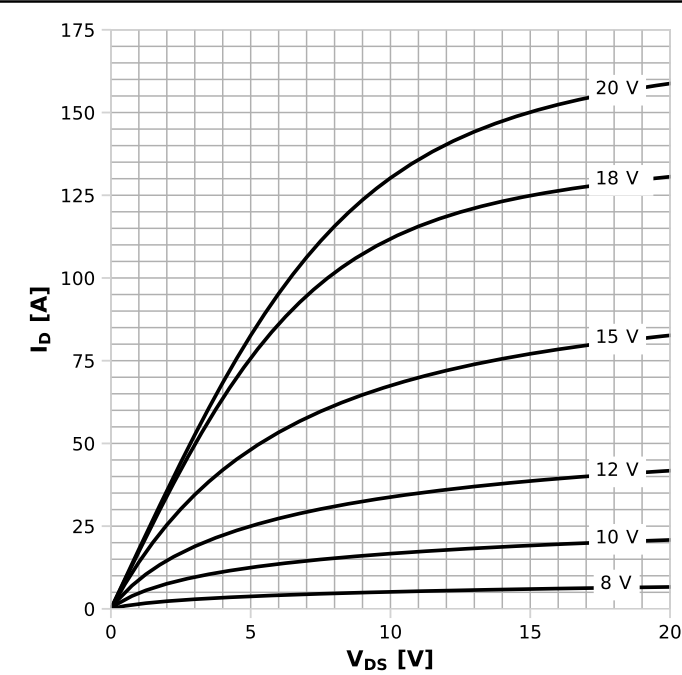
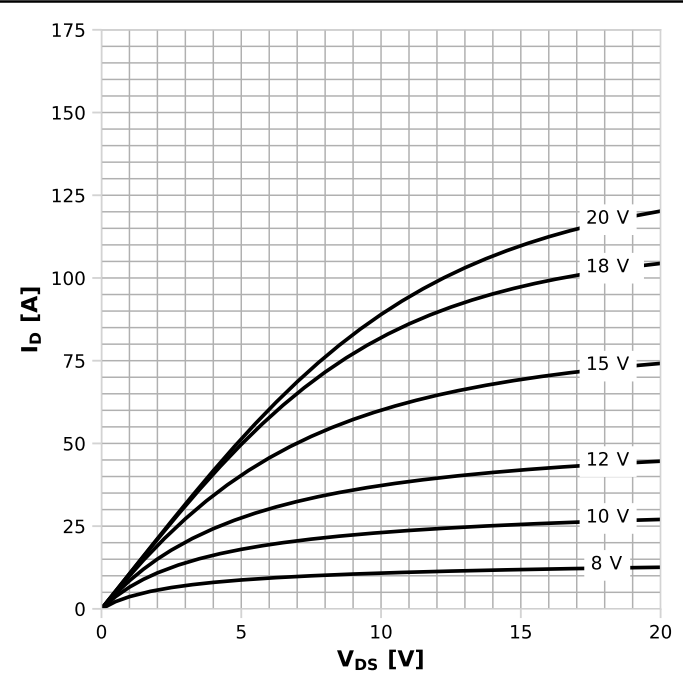


Diagram 5: Typ. output characteristics



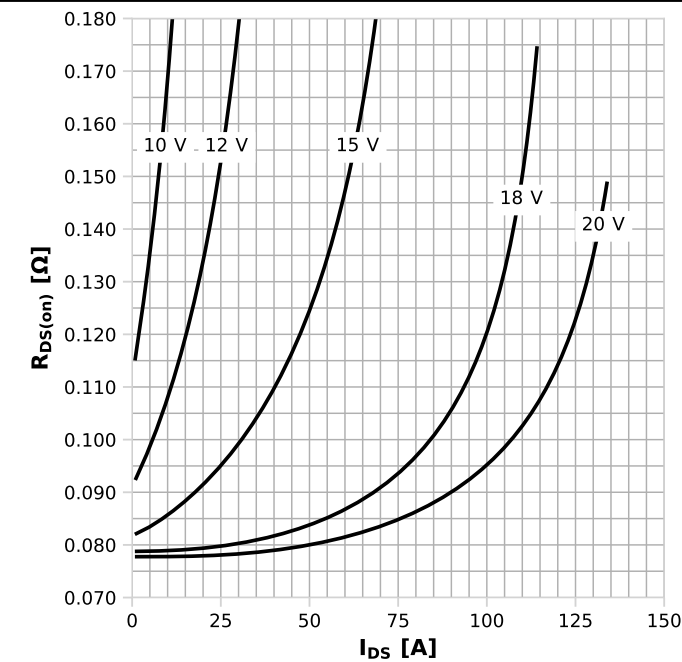
$I_D = f(V_{DS})$ ;  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



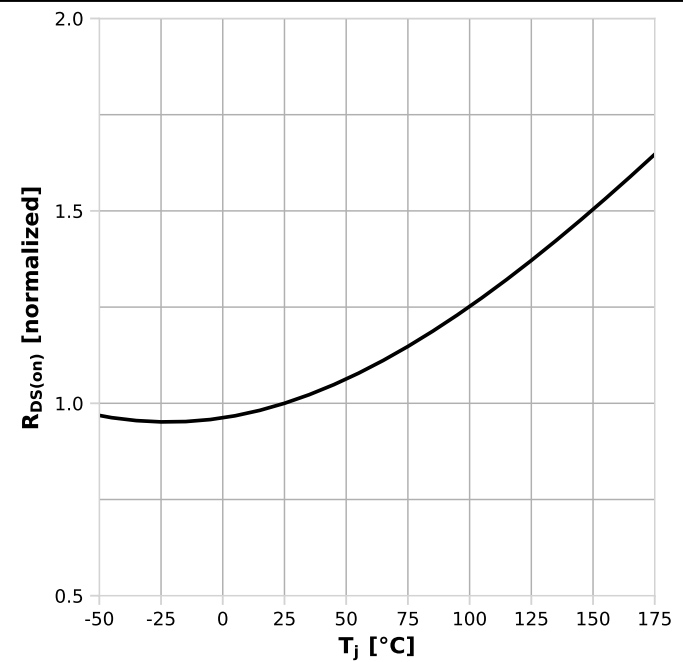
$I_D = f(V_{DS})$ ;  $T_j = 175\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_{DS})$ ;  $T_j = 125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



$R_{DS(on)} = f(T_j)$ ;  $I_D = 15.4\text{ A}$ ;  $V_{GS} = 18\text{ V}$

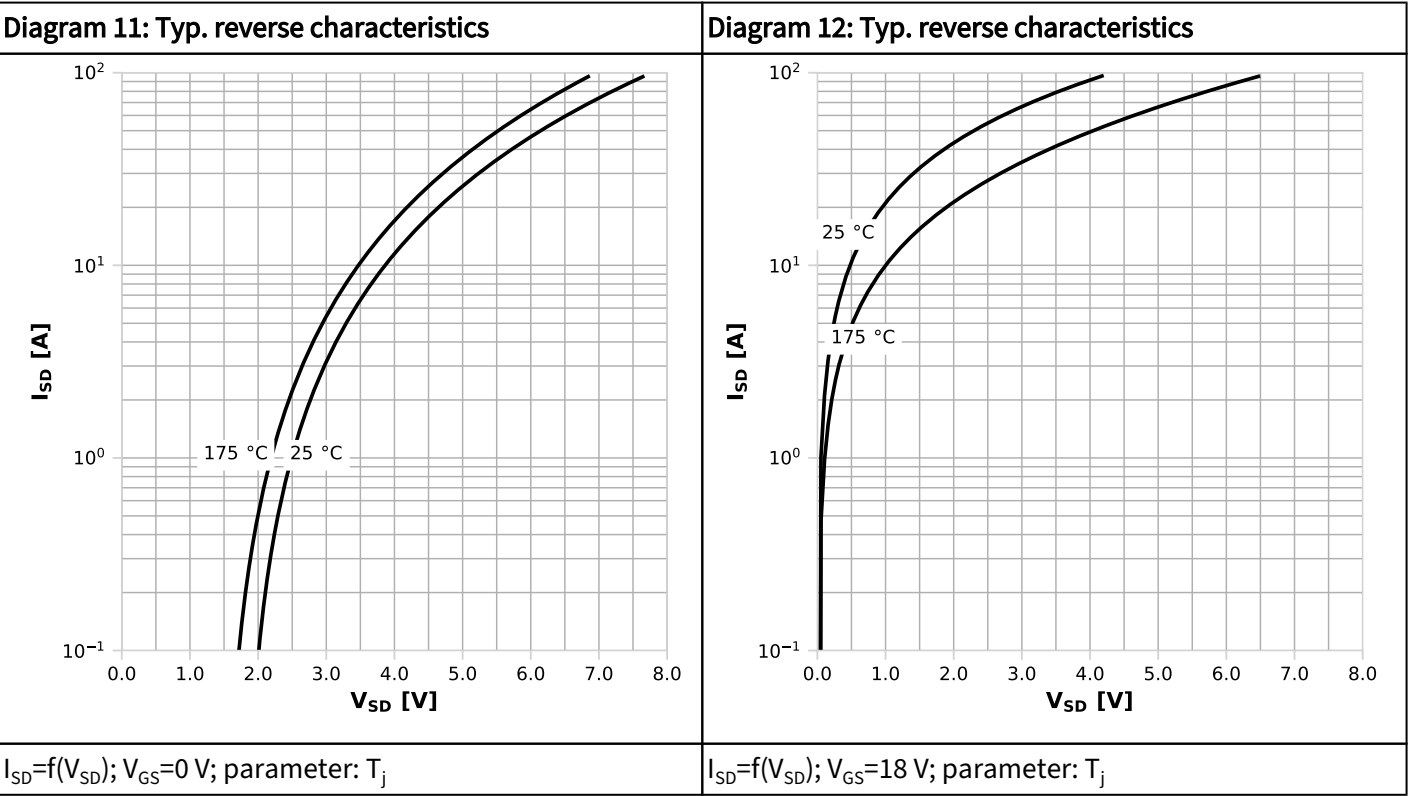
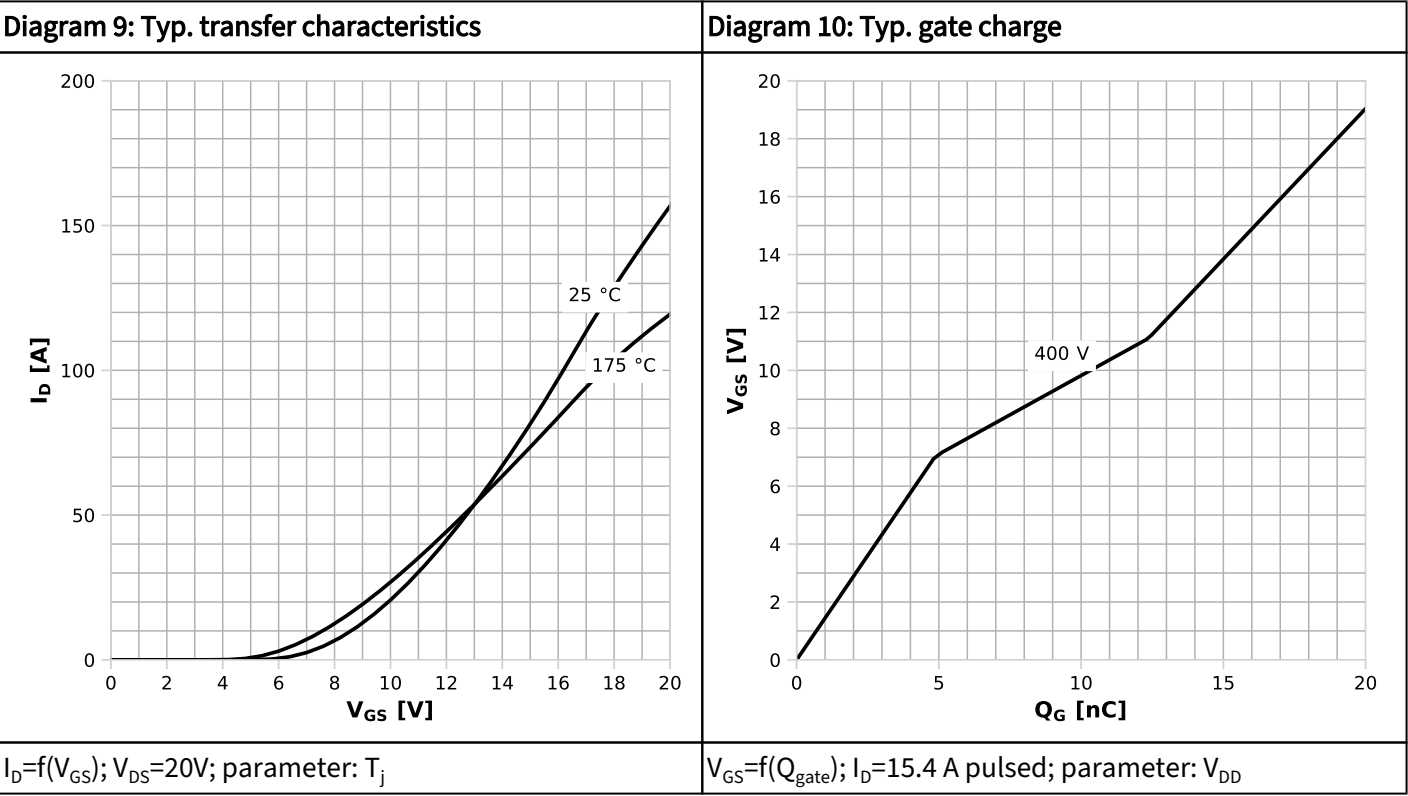
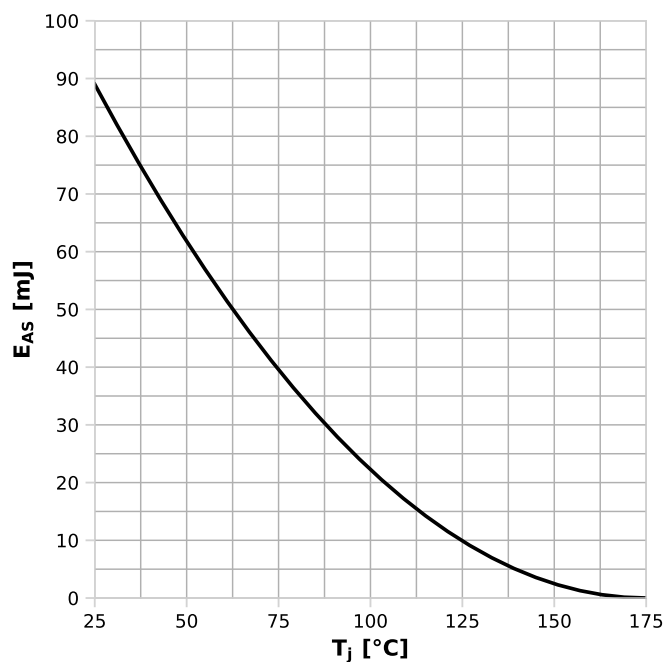
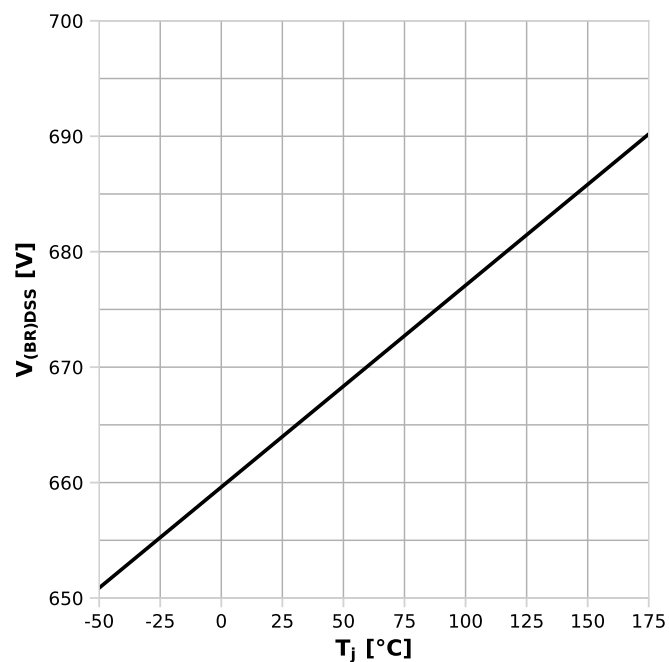


Diagram 13: Avalanche energy



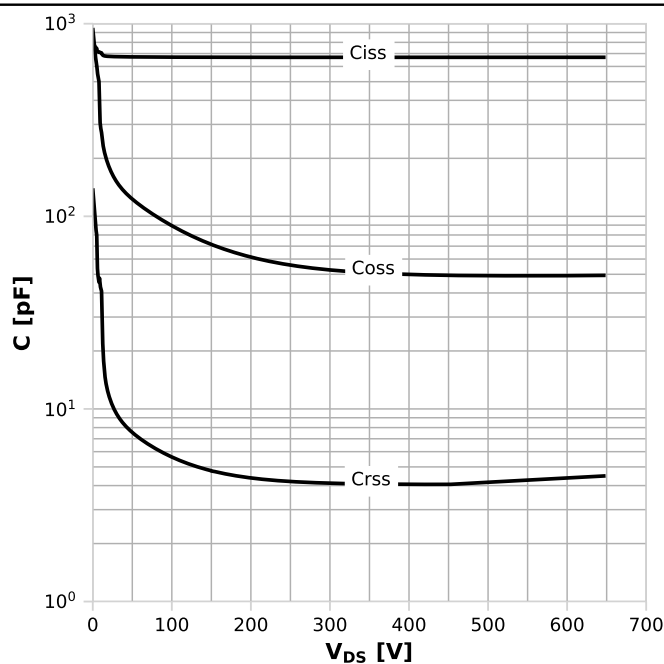
$E_{AS}=f(T_J)$ ;  $I_D=3.4$  A;  $V_{DD}=50$  V

Diagram 14: Drain-source breakdown voltage



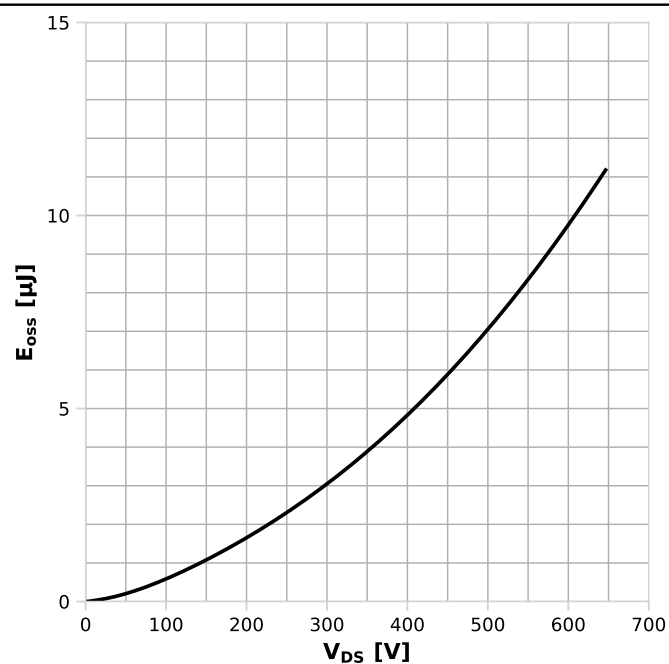
$V_{(BR)DSS}=f(T_J)$ ;  $I_D=0.31$  mA

Diagram 15: Typ. capacitances



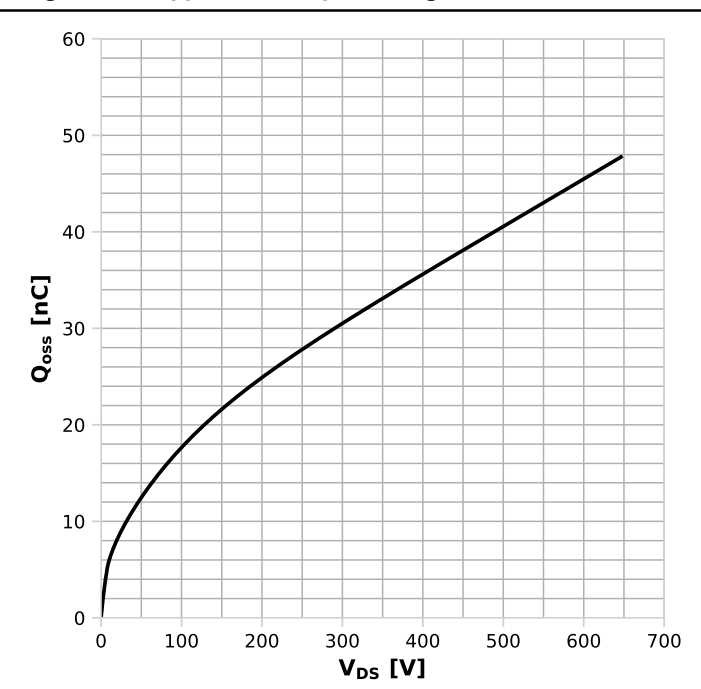
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=250$  kHz

Diagram 16: Typ. Coss stored energy



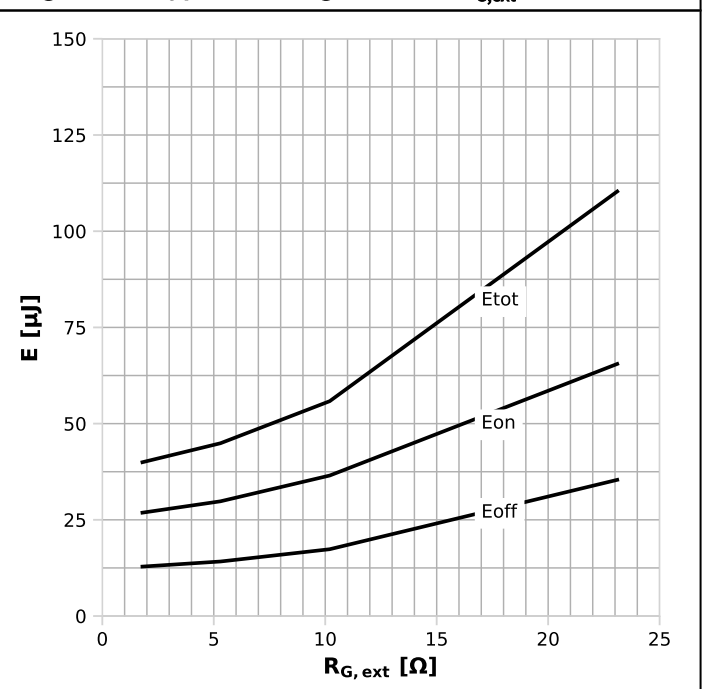
$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



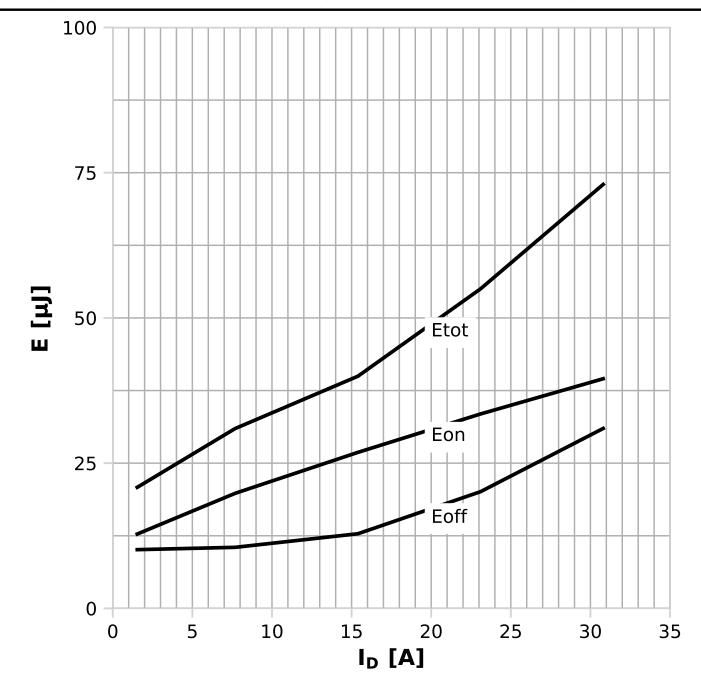
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. Switching Losses vs  $R_{G,ext}$



$E=f(R_{G,ext}); V_{DD}=400\text{ V}; V_{GS}=0-18\text{ V}; I_D=15.4\text{ A}$

Diagram 19: Typ. Switching Losses vs switching current



$E=f(I_D); V_{DD}=400\text{ V}; V_{GS}=0-18\text{ V}; R_{G,ext}=1.8\text{ }\Omega$

6 Test Circuits

Table 9 Body diode characteristics (CoolSiC)

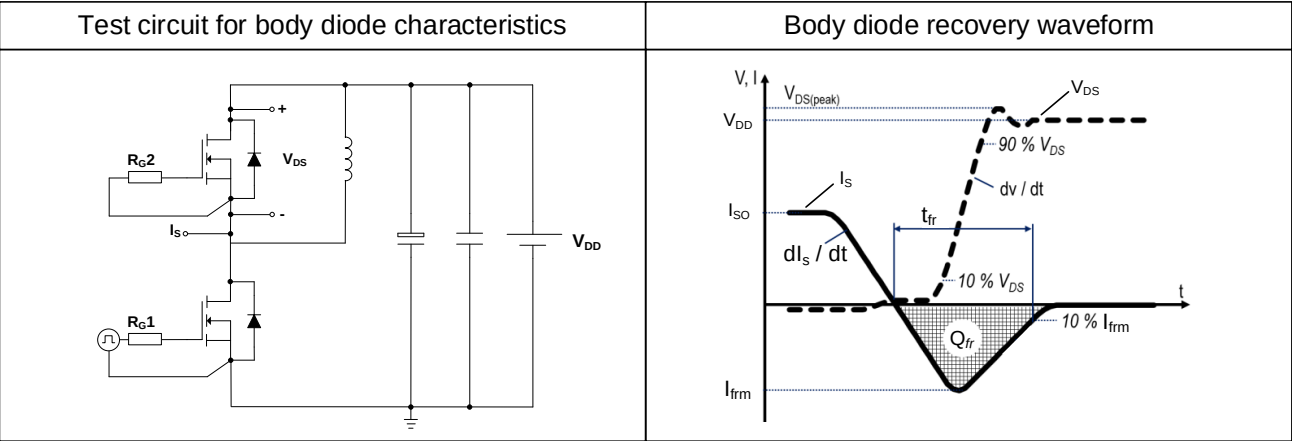


Table 10 Switching times (CoolSiC)

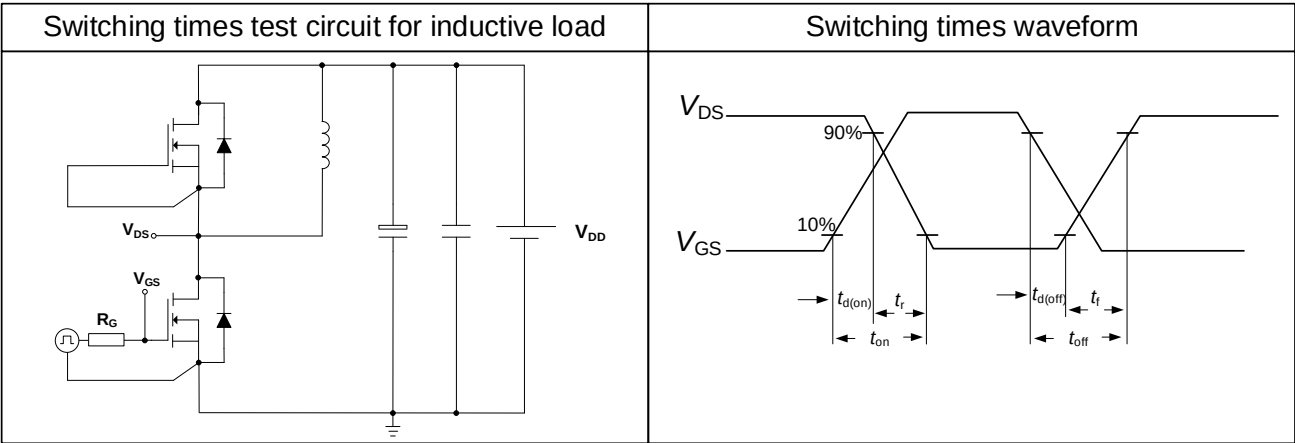
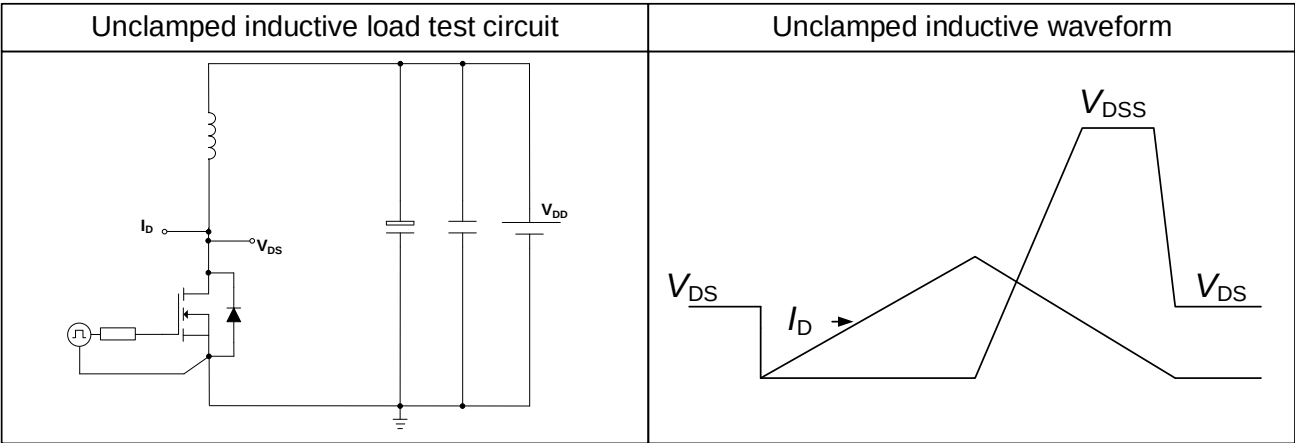
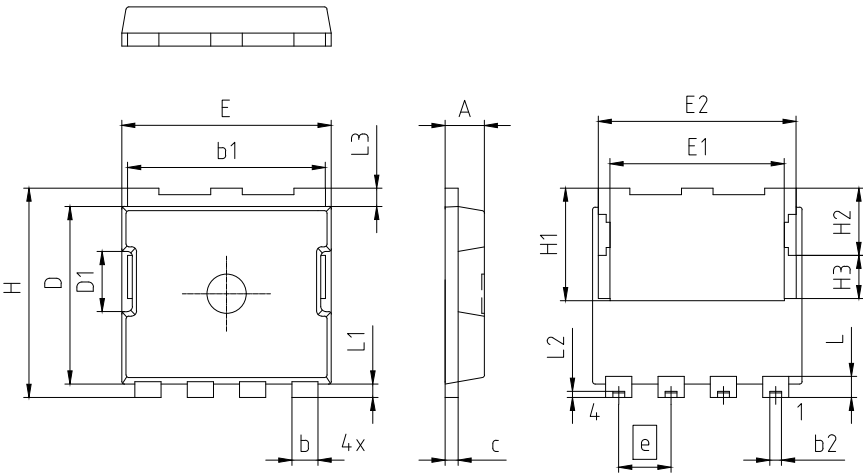


Table 11 Unclamped inductive load



## 7 Package Outlines



| PACKAGE - GROUP<br>NUMBER: PG-LHSOF-4-U01 |             |      |
|-------------------------------------------|-------------|------|
| DIMENSIONS                                | MILLIMETERS |      |
|                                           | MIN.        | MAX. |
| A                                         | 1.40        | 1.60 |
| b                                         | 0.90        | 1.10 |
| b1                                        | 7.46        | 7.66 |
| b2                                        | 0.42        | 0.50 |
| c                                         | 0.40        | 0.60 |
| D                                         | 6.59        | 6.99 |
| D1                                        | 2.30        |      |
| E                                         | 7.80        | 8.20 |
| E1                                        | 6.66        |      |
| E2                                        | 7.56        |      |
| e                                         | 2.00        |      |
| N                                         | 4           |      |
| H                                         | 7.80        | 8.20 |
| H1                                        | 4.30        |      |
| H2                                        | 2.57        |      |
| H3                                        | 1.65        |      |
| L                                         | 0.50        | 1.00 |
| L1                                        | 0.51        |      |
| L2                                        | 0.23        |      |
| L3                                        | 0.50        | 0.90 |

Figure 1 Outline PG-LHSOF-4, dimensions in mm

## 8 Appendix A

**Table 12**    **Related Links**

- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Application Note](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Simulation Model](#)
- [IFX Design tools](#)



## Revision History

IMTA65R060M2H

### Revision 2024-05-13, Rev. 2.1

Previous Revision

| Revision | Date       | Subjects (major changes since last revision) |
|----------|------------|----------------------------------------------|
| 2.0      | 2024-04-19 | Release of final                             |
| 2.1      | 2024-05-13 | Updated diagram axis max. and min. values.   |

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