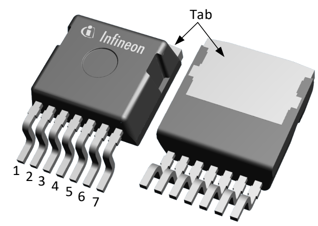
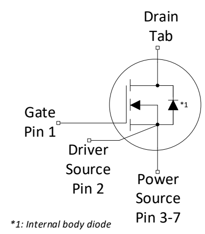
MOSFET

650 V CoolSiC™ M1 SiC Trench Power Device

The 650 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 650V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.

PG-TO263-7-12





Features

- Optimized switching behavior at higher currents
- Commutation robust fast body diode with low Q_f
- Superior gate oxide reliability
- $T_{j,max}$=175°C and excellent thermal behavior
- Lower $R_{DS(on)}$ and pulse current dependency on temperature
- Increased avalanche capability
- Compatible with standard drivers (recommended driving voltage: 0V-18V)
- Kelvin source provides up to 4 times lower switching losses

Benefits

- Unique combination of high performance, high reliability and ease of use
- Ease of use and integration
- Suitable for topologies with continuous hard commutation
- Higher robustness and system reliability
- Efficiency improvement
- Reduced system size leading to higher power density

Potential applications

- Telecom and Server SMPS
- UPS (uninterruptable power supplies)
- Solar PV inverters
- EV charging infrastructure
- Energy storage and battery formation
- Class D amplifiers

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ T_J = 25 °C	650	V
$R_{DS(on),typ}$	260	mΩ
$R_{DS(on),max}$	346	mΩ
$Q_{G,typ}$	6	nC
I_{DM}	19	A
Q_{oss} @ 400 V	22	nC
E_{oss} @ 400 V	3.4	µJ

Type / Ordering Code	Package	Marking	Related Links
IMBG65R260M1H	PG-TO263-7-12	65R260M1	see Appendix A

Table of Contents

1 Maximum ratings

at T_J = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current[1]	I_D	- -	- -	6 5	A	T_C = 25 °C T_C = 100 °C
Peak drain current[2]	I_{DM}	-	-	19	A	T_C = 25 °C
Avalanche energy, single pulse	E_{AS}	-	-	30	mJ	I_D = 1.1 A, V_{DD} = 50 V; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.15	mJ	I_D = 1.1 A, V_{DD} = 50 V; see table 11
Avalanche current, single pulse	I_{AS}	-	-	1.1	A	-
MOSFET *dv/dt* ruggedness	*dv/dt*	-	-	200	V/ns	V_{DS} = 0...400 V
Gate source voltage (static)[3]	V_{GS}	-5	-	23	V	static
Gate source voltage (transient)	V_{GS}	-7	-	25	V	$t_{pulse,positive}$ <= 1% duty cycle/f_{sw}
Power dissipation	P_{tot}	-	-	65	W	T_C = 25 °C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_J	-55	-	175	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous reverse drain current[1]	I_{SDC}	- -	- -	6 6	A	V_{GS}=18V, T_C = 25 °C V_{GS}=0V, T_C = 25 °C
Repetitive peak reverse drain current[1]	I_{SRM}	-	-	19	A	T_C = 25 °C, pulse width t_p<=250ns
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C = 25 °C, t = 1 min

[1] Limited by $T_{J,max}$
[2] Pulse width t_p limited by $T_{J,max}$
[3] The maximum gate-source voltage in the application design should be in accordance to IPC-9592B

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.30	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots[1)]	V_{GS}	-2	-	20	V	-

[1)] **Important note: the selection of positive and negative gate-source voltages impacts the long-term behavior of the device.**The design guidelines described in the CoolSiC™ MOSFET 650 V M1 trench power device application note AN_1907_PL52_1911_144109 must be considered to ensure sound operation of the device over the planned lifetime.

4 Electrical characteristics

at T_J = 25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS} = 0 V, I_D = 0.17 mA
Gate threshold voltage[1]	$V_{GS(th)}$	3.5	4.5	5.7	V	V_{DS} = V_{GS}, I_D = 1.1 mA
Zero gate voltage drain current	I_{DSS}	- -	1 3	150 -	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C V_{DS} = 650 V, V_{GS} = 0 V, T_J = 175 °C
Gate leakage current	I_{GSS}	-	-	100	nA	V_{GS} = 20 V, V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.260 0.364	0.346 -	Ω	V_{GS} = 18 V, I_D = 3.6 A, T_J = 25 °C V_{GS} = 18 V, I_D = 3.6 A, T_J =175 °C
Internal gate resistance	R_G	-	24.0	-	Ω	f = 1 MHz

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	201	-	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Reverse transfer capacitance	C_{rss}	-	4	-	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Output capacitance[2]	C_{oss}	-	37	48	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Output charge[2]	Q_{oss}	-	22	29	nC	calculation based on C_{oss}
Effective output capacitance, energy related[3]	$C_{o(er)}$	-	42	-	pF	V_{GS} = 0 V, V_{DS} = 0...400 V
Effective output capacitance, time related[4]	$C_{o(tr)}$	-	55	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0...400 V
Turn-on delay time	$t_{d(on)}$	-	5.3	-	ns	V_{DD} = 400 V, V_{GS} = 18 V, I_D = 3.6 A, R_G = 1.8 Ω; see table 10
Rise time	t_r	-	5.3	-	ns	V_{DD} = 400 V, V_{GS} = 18 V, I_D = 3.6 A, R_G = 1.8 Ω; see table 10
Turn-off delay time	$t_{d(off)}$	-	7.7	-	ns	V_{DD} = 400 V, V_{GS} = 18 V, I_D = 3.6 A, R_G = 1.8 Ω; see table 10
Fall time	t_f	-	13	-	ns	V_{DD} = 400 V, V_{GS} = 18 V, I_D = 3.6 A, R_G = 1.8 Ω; see table 10

1) Tested after 1 ms pulse at V_{GS} = +20 V
2) Maximum specification is defined by calculated six sigma upper confidence bound
3) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V
4) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 7 Gate charge characteristics

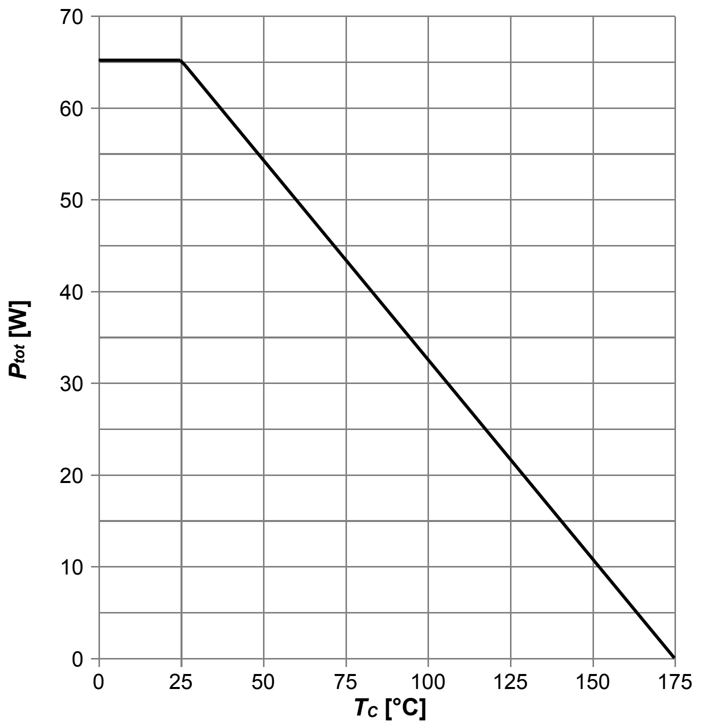
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1	-	nC	V_{DD} = 400 V, I_D = 3.6 A, V_{GS} = 0 to 18 V
Gate to drain charge	Q_{gd}	-	1	-	nC	V_{DD} = 400 V, I_D = 3.6 A, V_{GS} = 0 to 18 V
Gate charge total	Q_g	-	6	-	nC	V_{DD} = 400 V, I_D = 3.6 A, V_{GS} = 0 to 18 V

Table 8 Body diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	4.0	-	V	V_{GS} = 0 V, I_S = 3.6 A, T_J = 25 °C
MOSFET forward recovery time	t_{fr}	-	16.6	-	ns	V_{DD} = 400 V, I_{S0} = 3.6 A, di_S/dt = 1000 A/µs; see table 9
MOSFET forward recovery charge	Q_{f}	-	33	-	nC	V_{DD} = 400 V, I_{S0} = 3.6 A, di_S/dt = 1000 A/µs; see table 9
MOSFET peak forward recovery current	I_{frm}	-	4.2	-	A	V_{DD} = 400 V, I_{S0} = 3.6 A, di_S/dt = 1000 A/µs; see table 9

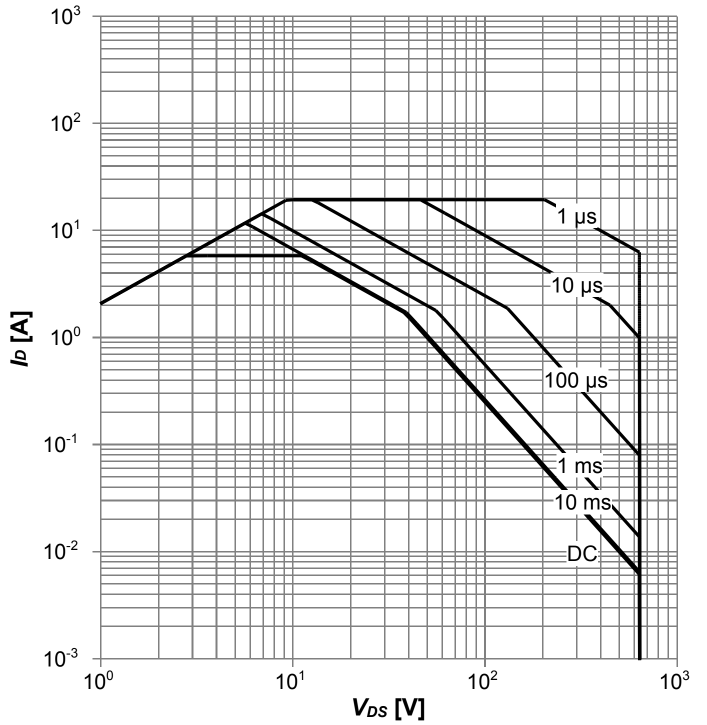
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



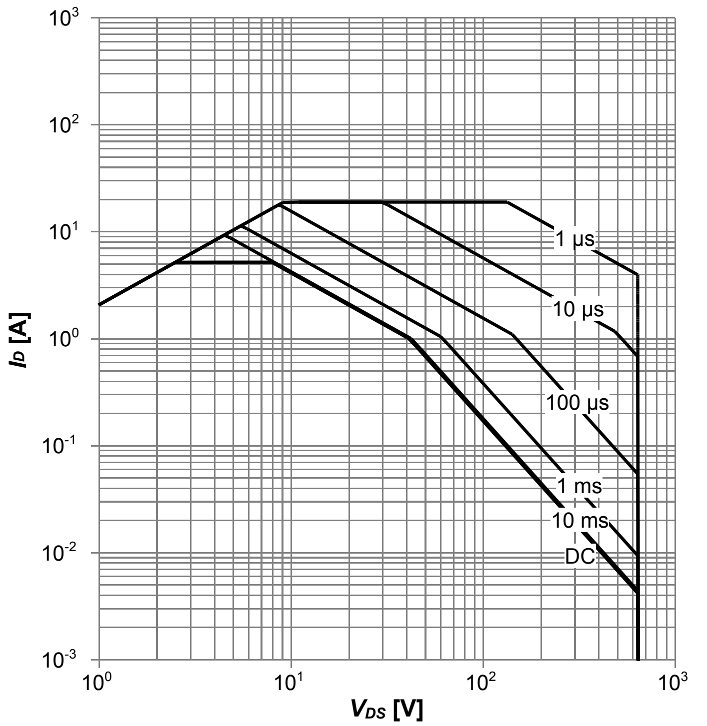
P_{tot}=f(T_C)

Diagram 2: Safe operating area



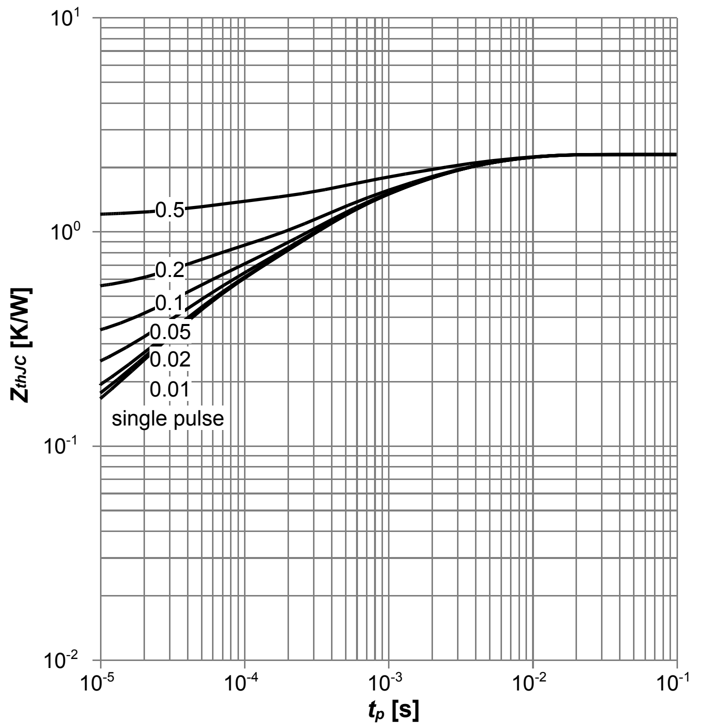
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



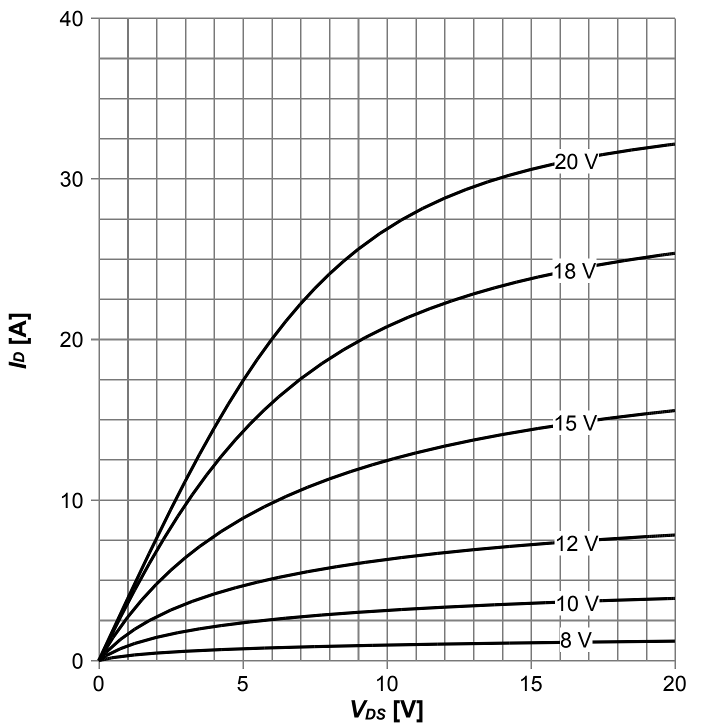
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



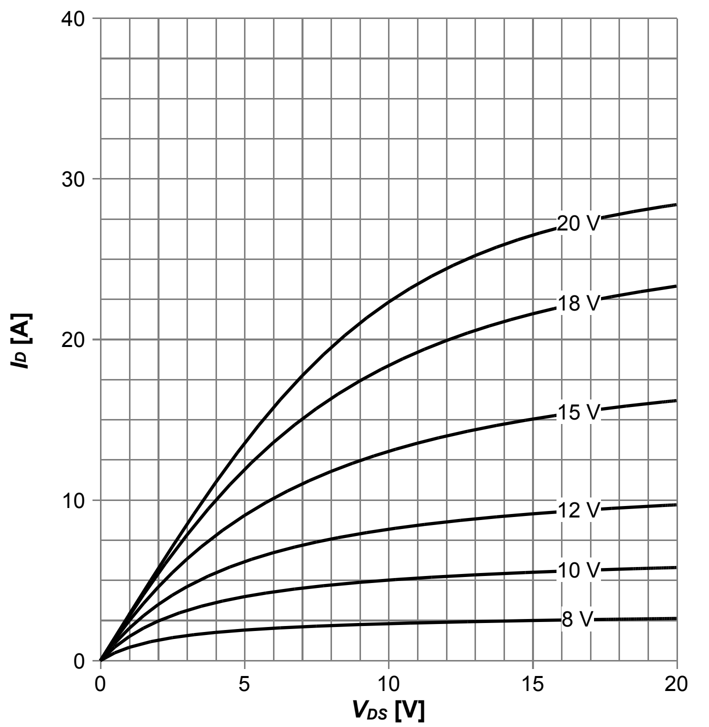
Z_{thJC}=f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



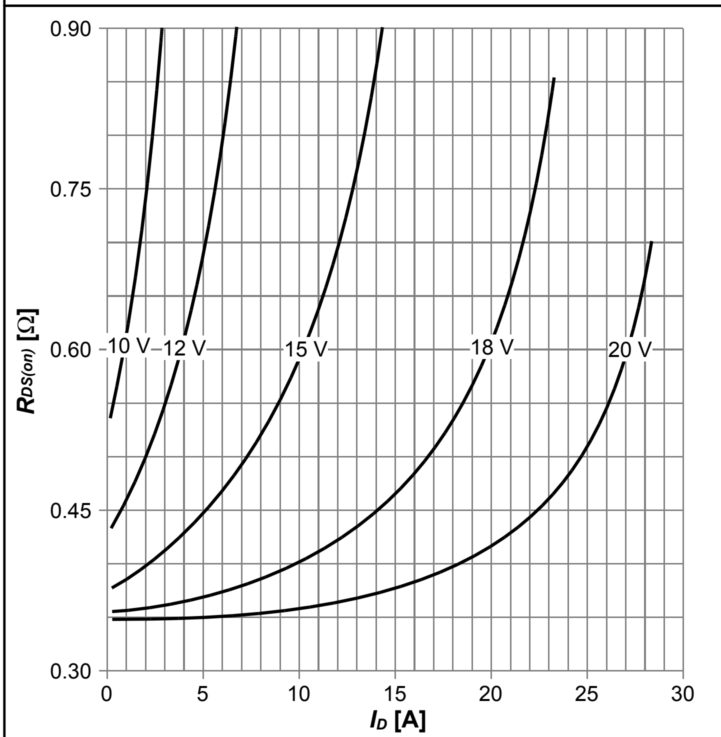
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



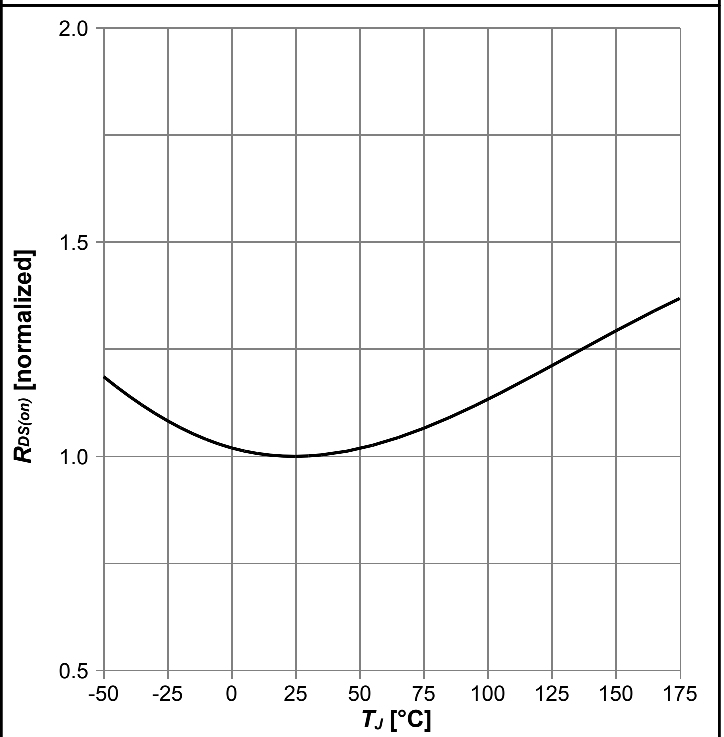
I_D=f(V_{DS}); T_j=150 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



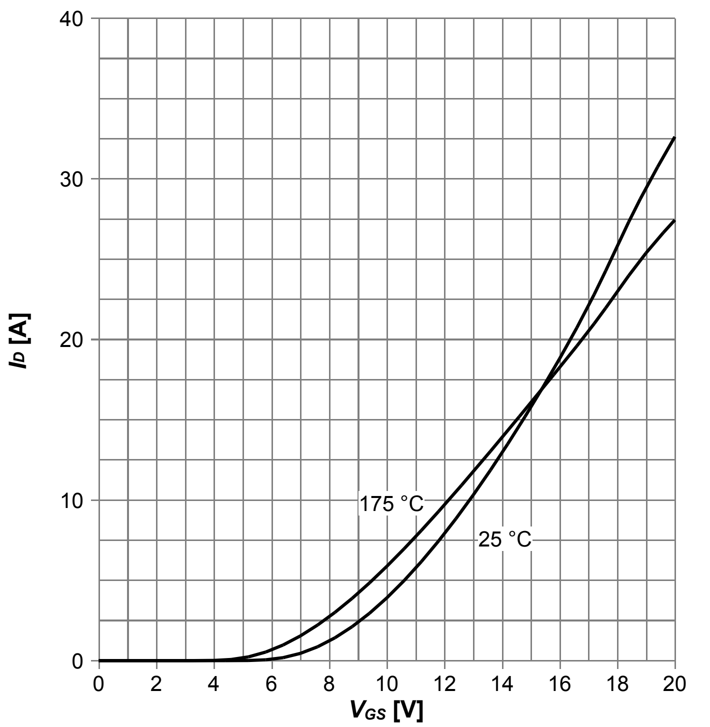
$R_{DS(on)}$=f(I_D); T_j=150 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



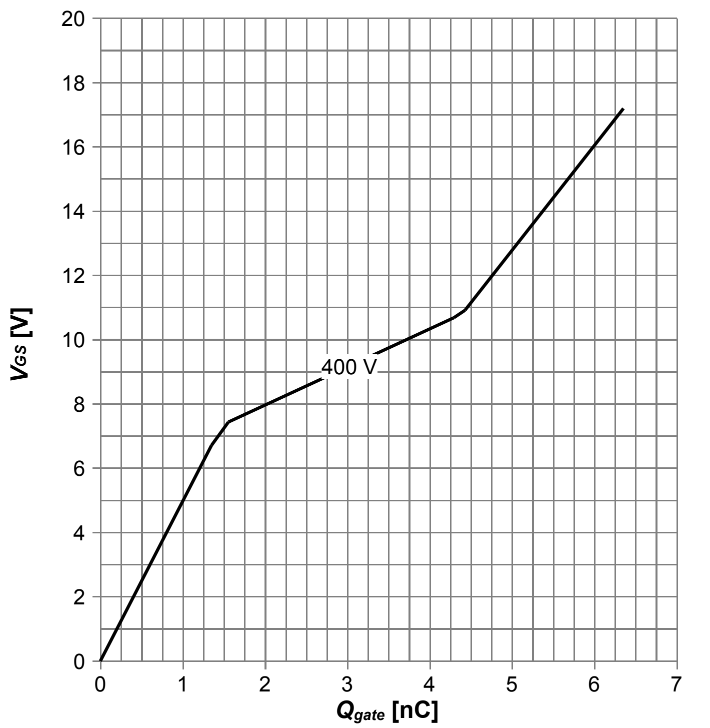
$R_{DS(on)}$=f(T_j); I_D=3.6 A; V_{GS}=18 V

Diagram 9: Typ. transfer characteristics



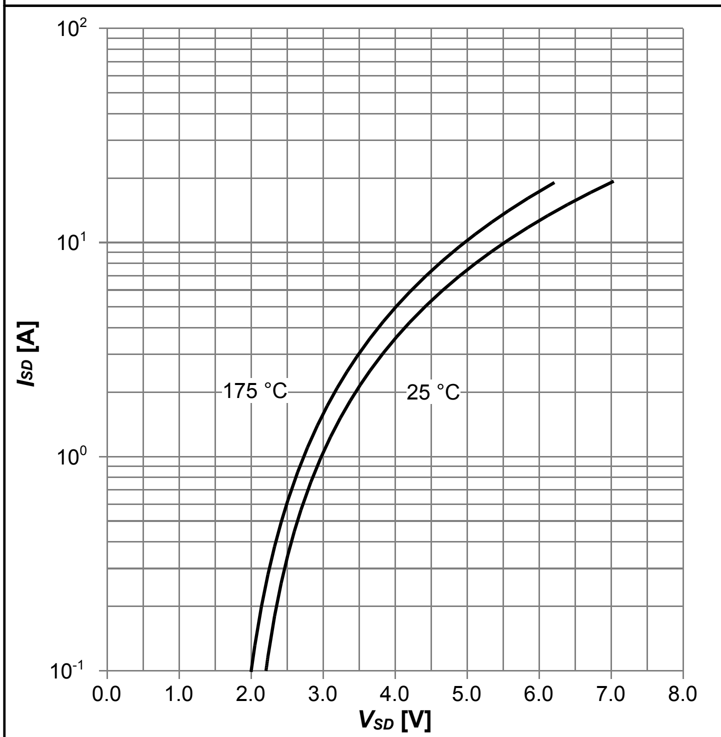
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



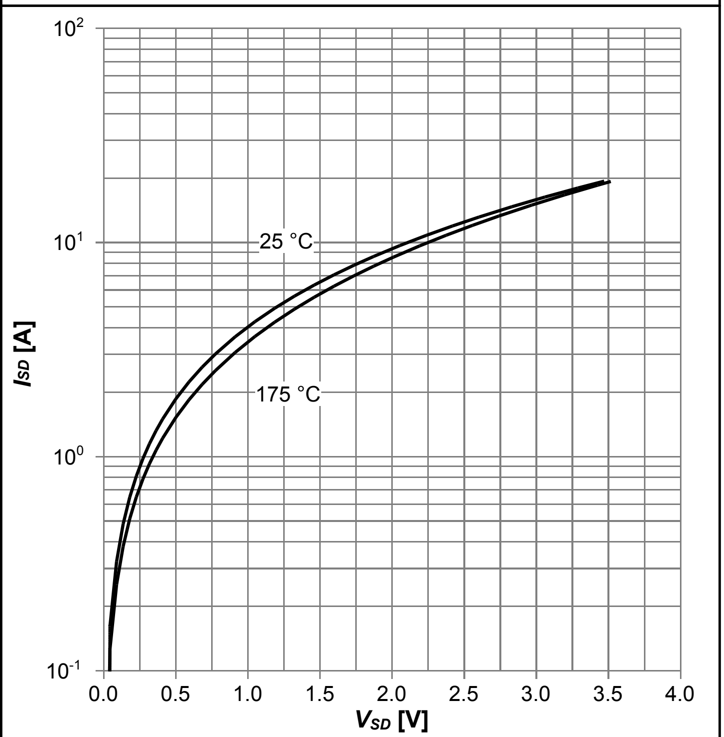
V_{GS}=f(Q_{gate}); I_D=3.6 A pulsed; parameter: V_{DD}

Diagram 11: Typ. reverse characteristics



I_{SD}=f(V_{SD}); V_{GS}=0 V; parameter: T_j

Diagram 12: Typ. reverse characteristics



I_{SD}=f(V_{SD}); V_{GS}=18 V; parameter: T_j

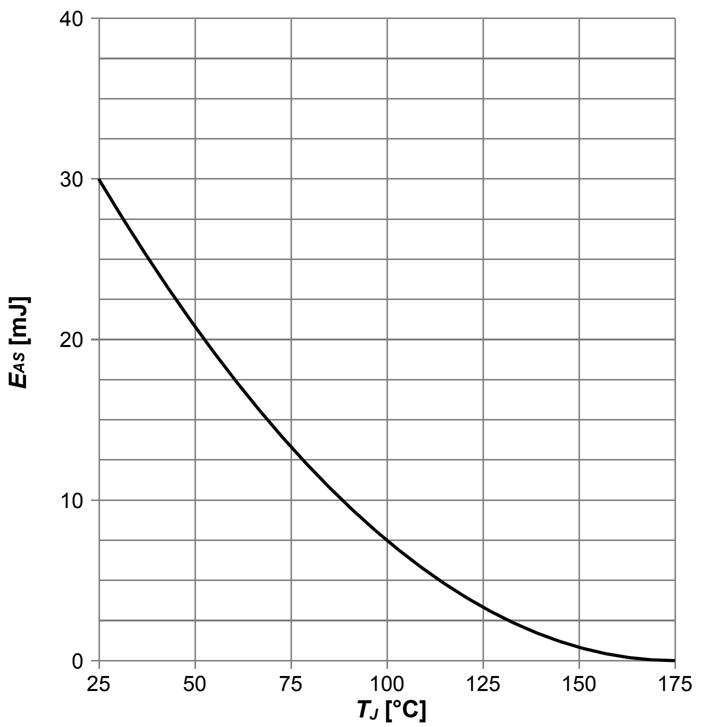
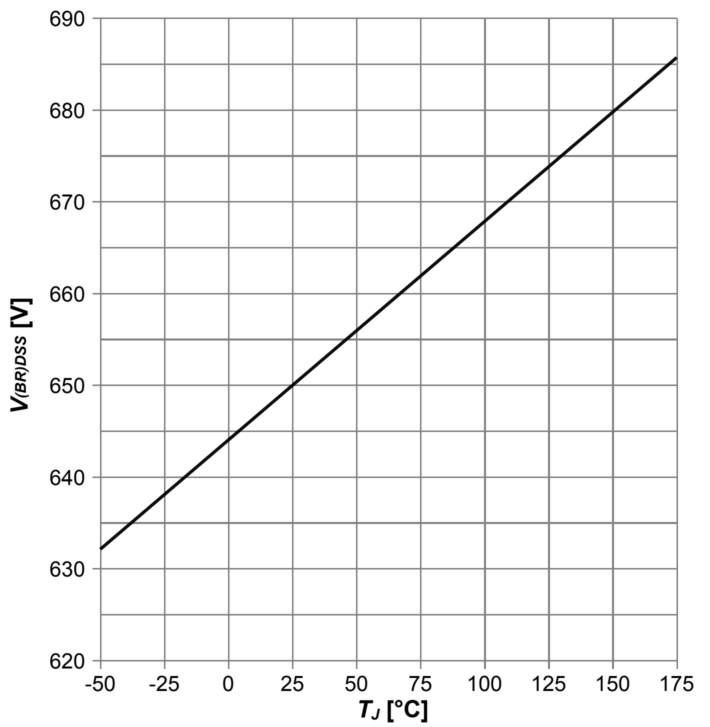
Diagram 13: Avalanche energy	Diagram 14: Drain-source breakdown voltage
	
E_{AS}=f(T_j); I_D=1.1 A; V_{DD}=50 V	$V_{(BR)DSS}$=f(T_j); I_D=0.17 mA

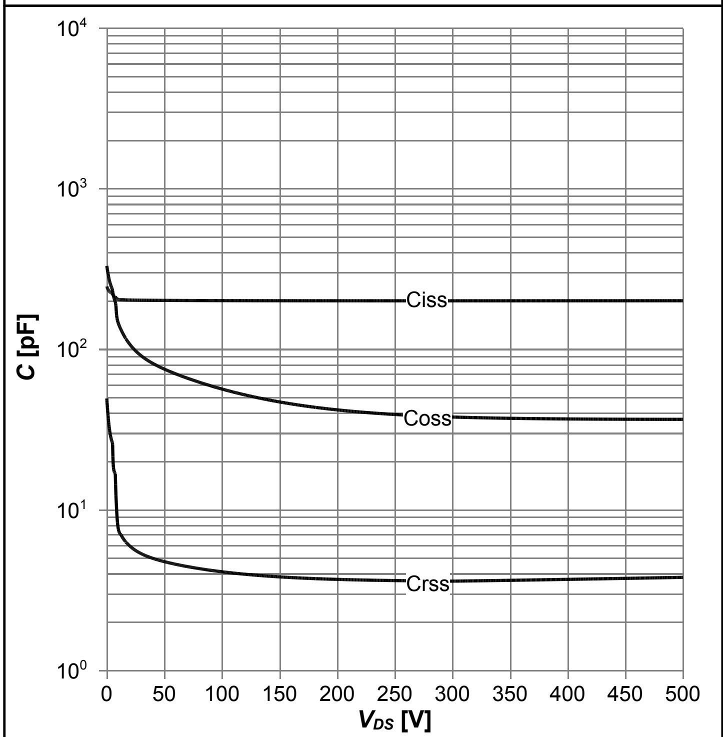
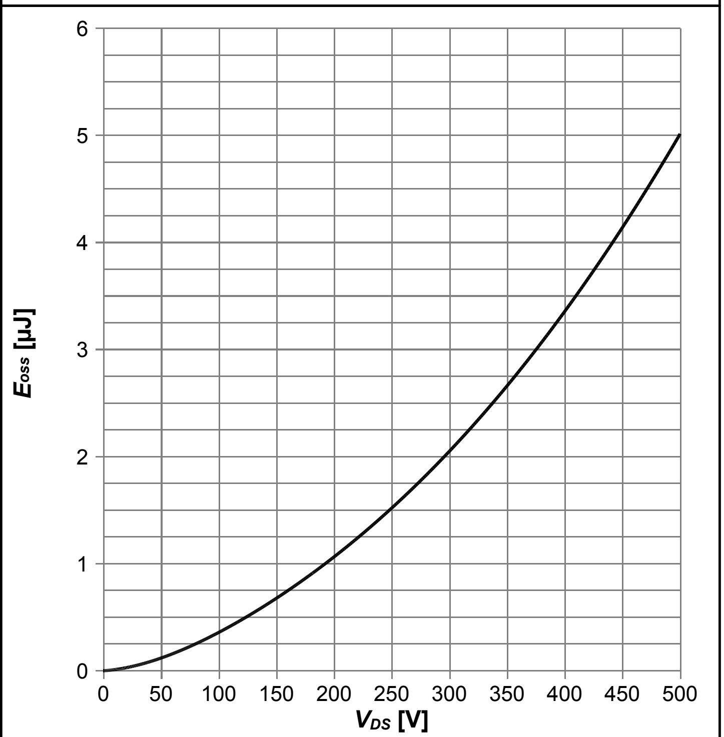
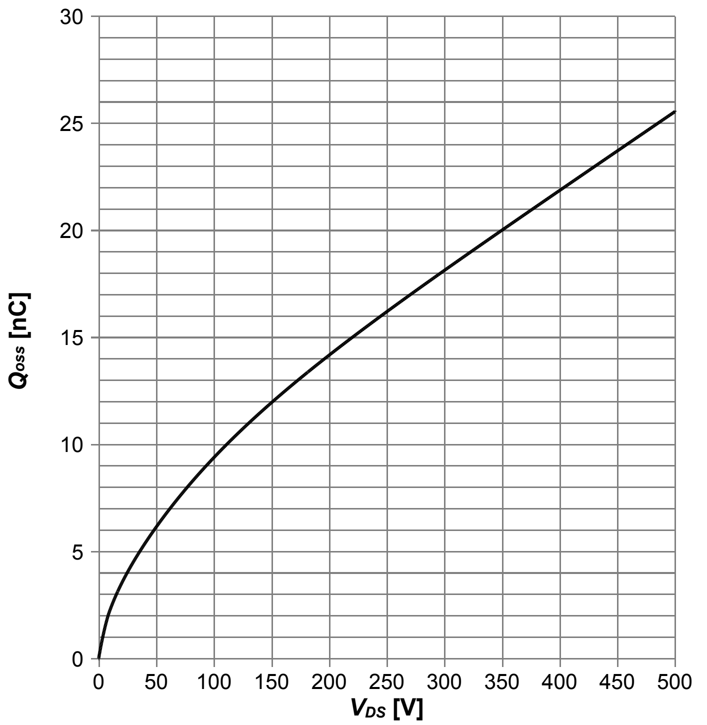
Diagram 15: Typ. capacitances	Diagram 16: Typ. Coss stored energy
	
C=f(V_{DS}); V_{GS}=0 V; f=250 kHz	E_{oss}=f(V_{DS})

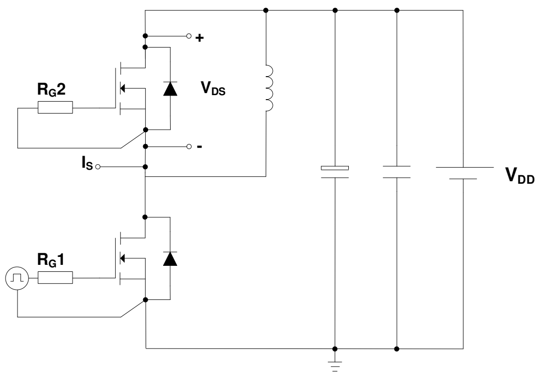
Diagram 17: Typ. Qoss output charge



Q_{oss}=f(V_{DS})

6 Test Circuits

Table 9 Body diode characteristics (650V CoolSiC)

<table>
<tr><th>Test circuit for body diode characteristics</th><th>Body diode recovery waveform</th></tr>
<tr><td>


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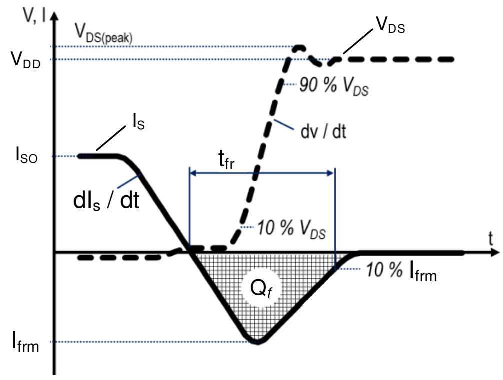

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Table 10 Switching times (650V CoolSiC)

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<tr><th>Switching times test circuit for inductive load</th><th>Switching times waveform</th></tr>
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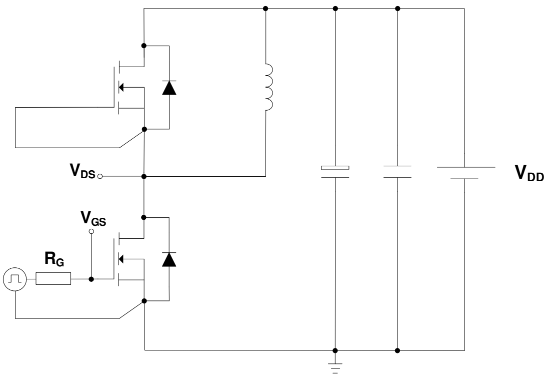

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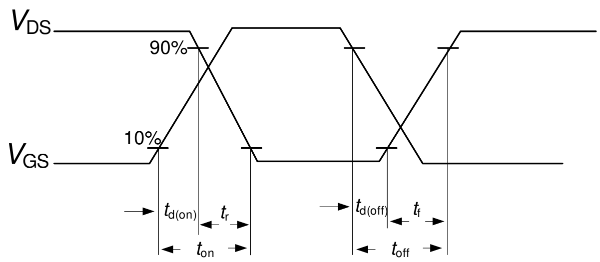

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Table 11 Unclamped inductive load (650V CoolSiC)

<table>
<tr><th>Unclamped inductive load test circuit</th><th>Unclamped inductive waveform</th></tr>
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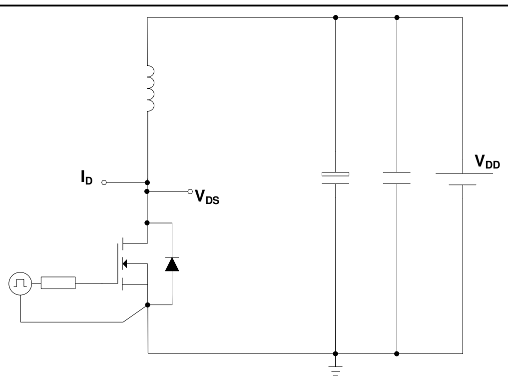

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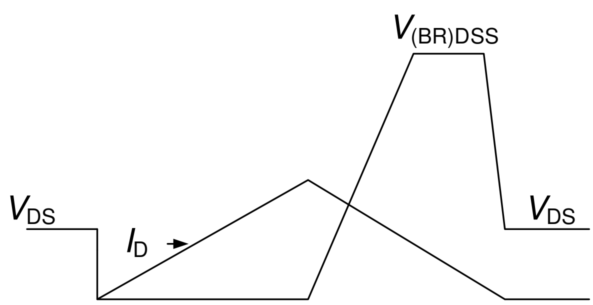

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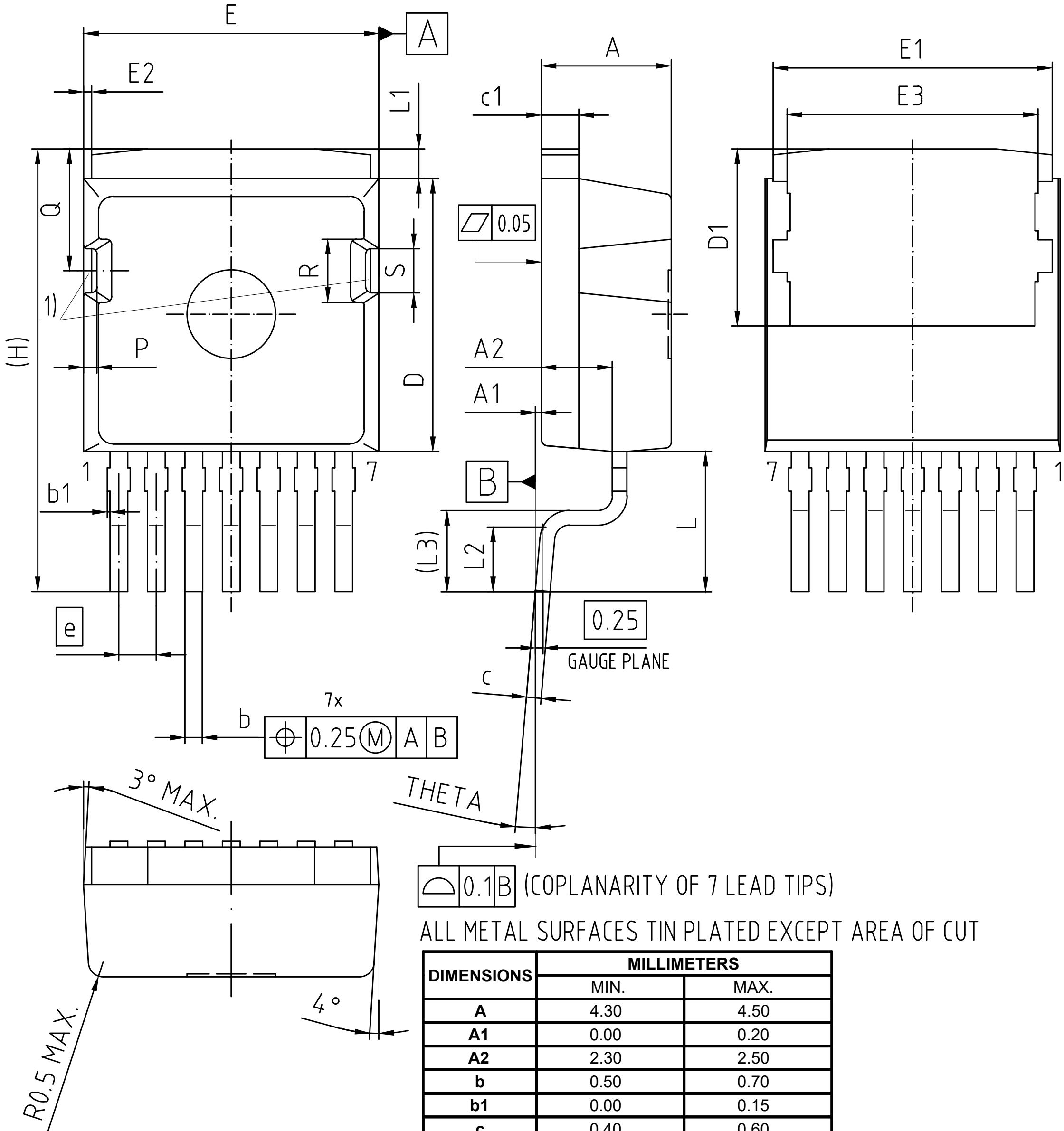
7 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.20
A2	2.30	2.50
b	0.50	0.70
b1	0.00	0.15
c	0.40	0.60
c1	1.17	1.37
D	9.05	9.45
D1	5.90	6.10
E	9.80	10.20
E1	9.36	9.56
E2	0.00	0.30
E3	8.40	8.60
e	1.27	
H	15.00	
L	4.20	5.20
L1	0.70	1.30
L2	1.70	2.30
L3	2.70	
P	0.35	0.55
Q	4.02	4.22
R	2.03	2.23
S	1.40	1.60
THETA	0.00°	8.00°

1) MOLD FILLING ACCEPTABLE
AT THIS AREA

DOCUMENT NO. Z8B00189674
REVISION 01
SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION
ISSUE DATE 14.02.2020

Figure 1 Outline PG-TO263-7-12, dimensions in mm

8 Appendix A

Table 12 Related Links

- **IFX CoolSiC M1 Webpage:** www.infineon.com
- **IFX CoolSiC M1 application note:** www.infineon.com
- **IFX CoolSiC M1 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IMBG65R260M1H

Revision: 2021-12-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-12-10	Release of final version

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