

# MOSFET

## CoolSiC™ MOSFET 650 V G2

Built on Infineon's robust 2<sup>nd</sup> generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

### Features

- Ultra-low switching losses
- Benchmark gate threshold voltage,  $V_{GS(th)} = 4.5\text{ V}$
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance

### Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

### Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

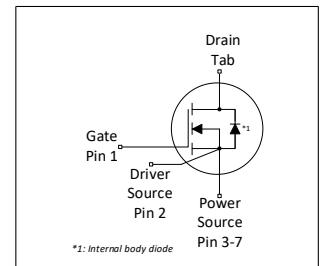
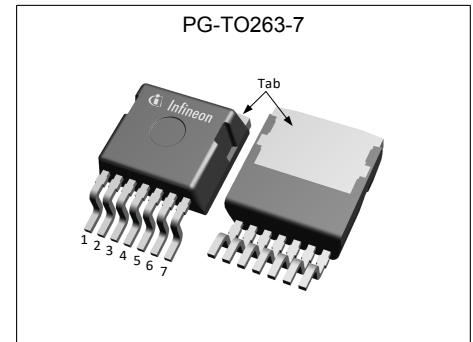
### Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.*

**Table 1 Key Performance Parameters**

| Parameter                         | Value | Unit |
|-----------------------------------|-------|------|
| $V_{DSS}$ over full $T_{j,range}$ | 650   | V    |
| $R_{DS(on),typ}$                  | 6.7   | mΩ   |
| $R_{DS(on),max}$                  | 8.5   | mΩ   |
| $Q_{G,typ}$                       | 179   | nC   |
| $I_{D,pulse}$                     | 897   | A    |
| $Q_{oss} @ 400\text{ V}$          | 337   | nC   |
| $E_{oss} @ 400\text{ V}$          | 45.7  | μJ   |



RoHS

| Type / Ordering Code | Package    | Marking  | Related Links  |
|----------------------|------------|----------|----------------|
| IMBG65R007M2H        | PG-TO263-7 | 65R007M2 | see Appendix A |

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## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

**Table 2 Maximum ratings**

| Parameter                                      | Symbol    | Values |      |            | Unit | Note / Test Condition                                                                         |
|------------------------------------------------|-----------|--------|------|------------|------|-----------------------------------------------------------------------------------------------|
|                                                |           | Min.   | Typ. | Max.       |      |                                                                                               |
| Continuous DC drain current <sup>1)</sup>      | $I_{DDC}$ | -      | -    | 238<br>167 | A    | $T_C = 25\text{ °C}$<br>$T_C = 100\text{ °C}$                                                 |
| Peak drain current <sup>2)</sup>               | $I_{DM}$  | -      | -    | 897        | A    | $T_C = 25\text{ °C}$ , $V_{GS} = 18\text{ V}$                                                 |
| Avalanche energy, single pulse                 | $E_{AS}$  | -      | -    | 848        | mJ   | $I_D = 31.8\text{ A}$ , $V_{DD} = 50\text{ V}$ ; see table 11                                 |
| Avalanche energy, repetitive                   | $E_{AR}$  | -      | -    | 4.24       | mJ   | $I_D = 31.8\text{ A}$ , $V_{DD} = 50\text{ V}$ ; see table 11                                 |
| Avalanche current, single pulse                | $I_{AS}$  | -      | -    | 31.8       | A    | -                                                                                             |
| MOSFET $dv/dt$ ruggedness                      | $dv/dt$   | -      | -    | 200        | V/ns | $V_{DS} = 0\ldots 400\text{ V}$                                                               |
| Gate source voltage (static) <sup>3)</sup>     | $V_{GS}$  | -7     | -    | 23         | V    | -                                                                                             |
| Gate source voltage (transient)                | $V_{GS}$  | -10    | -    | 25         | V    | $t_p \leq 500\text{ ns}$ , duty cycle $\leq 1\%$                                              |
| Power dissipation                              | $P_{tot}$ | -      | -    | 789        | W    | $T_C = 25\text{ °C}$                                                                          |
| Storage temperature                            | $T_{stg}$ | -55    | -    | 150        | °C   | -                                                                                             |
| Operating junction temperature                 | $T_j$     | -55    | -    | 175        | °C   | -                                                                                             |
| Mounting torque                                | -         | -      | -    | -          | Ncm  | -                                                                                             |
| Continuous reverse drain current <sup>1)</sup> | $I_{SDC}$ | -      | -    | 238<br>155 | A    | $V_{GS} = 18\text{ V}$ , $T_C = 25\text{ °C}$<br>$V_{GS} = 0\text{ V}$ , $T_C = 25\text{ °C}$ |
| Peak reverse drain current <sup>2)</sup>       | $I_{SM}$  | -      | -    | 897<br>276 | A    | $T_C = 25\text{ °C}$ , $t_p \leq 250\text{ ns}$<br>$T_C = 25\text{ °C}$                       |
| Insulation withstand voltage                   | $V_{ISO}$ | -      | -    | n.a.       | V    | $V_{rms}$ , $T_C = 25\text{ °C}$ , $t = 1\text{ min}$                                         |

<sup>1)</sup> Limited by  $T_{j,max}$

<sup>2)</sup> Pulse width  $t_{pulse}$  limited by  $T_{j,max}$ .

<sup>3)</sup> The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter                                       | Symbol        | Values |      |      | Unit | Note / Test Condition                                                                                 |
|-------------------------------------------------|---------------|--------|------|------|------|-------------------------------------------------------------------------------------------------------|
|                                                 |               | Min.   | Typ. | Max. |      |                                                                                                       |
| Thermal resistance, junction - case             | $R_{th(j-c)}$ | -      | -    | 0.19 | °C/W | Not subject to production test. Parameter verified by design/characterization according to JESD51-14. |
| Soldering temperature, reflow soldering allowed | $T_{solder}$  | -      | -    | 260  | °C   | reflow MSL1                                                                                           |

## 3 Operating range

**Table 4 Operating range**

| Parameter                    | Symbol        | Values |      |      | Unit | Note / Test Condition |
|------------------------------|---------------|--------|------|------|------|-----------------------|
|                              |               | Min.   | Typ. | Max. |      |                       |
| Recommended turn-on voltage  | $V_{GS(on)}$  | -      | 18   | -    | V    | -                     |
| Recommended turn-off voltage | $V_{GS(off)}$ | -      | 0    | -    | V    | -                     |

## 4 Electrical characteristics

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 5 Static characteristics**

| Parameter                            | Symbol       | Values |         |         | Unit          | Note / Test Condition                                                                                                                             |
|--------------------------------------|--------------|--------|---------|---------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|                                      |              | Min.   | Typ.    | Max.    |               |                                                                                                                                                   |
| Drain-source voltage                 | $V_{DSS}$    | 650    | -       | -       | V             | $V_{GS} = 0\text{ V}$ , $I_D = 2.97\text{ mA}$                                                                                                    |
| Gate threshold voltage <sup>1)</sup> | $V_{GS(th)}$ | 3.5    | 4.5     | 5.6     | V             | $V_{DS} = V_{GS}$ , $I_D = 29.7\text{ mA}$                                                                                                        |
| Zero gate voltage drain current      | $I_{DSS}$    | -      | 1<br>10 | 75<br>- | $\mu\text{A}$ | $V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$<br>$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 175\text{ °C}$ |
| Gate-source leakage current          | $I_{GSS}$    | -      | -       | 100     | nA            | $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$                                                                                                    |
| Drain-source on-state resistance     | $R_{DS(on)}$ | -      | 8.7     | -       | m $\Omega$    | $V_{GS} = 15\text{ V}$ , $I_D = 146.3\text{ A}$ , $T_j = 25\text{ °C}$                                                                            |
|                                      |              | -      | 6.7     | 8.5     |               | $V_{GS} = 18\text{ V}$ , $I_D = 146.3\text{ A}$ , $T_j = 25\text{ °C}$                                                                            |
|                                      |              | -      | 6.1     | -       |               | $V_{GS} = 20\text{ V}$ , $I_D = 146.3\text{ A}$ , $T_j = 25\text{ °C}$                                                                            |
|                                      |              | -      | 11      | -       |               | $V_{GS} = 18\text{ V}$ , $I_D = 146.3\text{ A}$ , $T_j = 175\text{ °C}$                                                                           |
| Internal gate resistance             | $R_{G,int}$  | -      | 1.0     | -       | $\Omega$      | $f = 1\text{ MHz}$                                                                                                                                |

<sup>1)</sup> Tested after 1 ms pulse at  $V_{GS} = +20\text{ V}$ . "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter                                                  | Symbol       | Values |      |      | Unit | Note / Test Condition                                                                                                          |
|------------------------------------------------------------|--------------|--------|------|------|------|--------------------------------------------------------------------------------------------------------------------------------|
|                                                            |              | Min.   | Typ. | Max. |      |                                                                                                                                |
| Input capacitance                                          | $C_{iss}$    | -      | 6359 | -    | pF   | $V_{GS} = 0 \text{ V}$ , $V_{DS} = 400 \text{ V}$ , $f = 250 \text{ kHz}$                                                      |
| Reverse transfer capacitance                               | $C_{rss}$    | -      | 35   | -    | pF   | $V_{GS} = 0 \text{ V}$ , $V_{DS} = 400 \text{ V}$ , $f = 250 \text{ kHz}$                                                      |
| Output capacitance <sup>1)</sup>                           | $C_{oss}$    | -      | 471  | 613  | pF   | $V_{GS} = 0 \text{ V}$ , $V_{DS} = 400 \text{ V}$ , $f = 250 \text{ kHz}$                                                      |
| Output charge <sup>1)</sup>                                | $Q_{oss}$    | -      | 337  | 439  | nC   | calculation based on $C_{oss}$                                                                                                 |
| Effective output capacitance, energy related <sup>2)</sup> | $C_{o(er)}$  | -      | 571  | -    | pF   | $V_{GS} = 0 \text{ V}$ ,<br>$V_{DS} = 0 \dots 400 \text{ V}$                                                                   |
| Effective output capacitance, time related <sup>3)</sup>   | $C_{o(tr)}$  | -      | 844  | -    | pF   | $I_D = \text{constant}$ , $V_{GS} = 0 \text{ V}$ ,<br>$V_{DS} = 0 \dots 400 \text{ V}$                                         |
| Turn-on delay time                                         | $t_{d(on)}$  | -      | 22   | -    | ns   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$ ;<br>see table 10 |
| Rise time                                                  | $t_r$        | -      | 41   | -    | ns   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$ ;<br>see table 10 |
| Turn-off delay time                                        | $t_{d(off)}$ | -      | 53   | -    | ns   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$ ;<br>see table 10 |
| Fall time                                                  | $t_f$        | -      | 20   | -    | ns   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$ ;<br>see table 10 |
| Turn-ON switching losses <sup>4)</sup>                     | $E_{on}$     | -      | 753  | -    | μJ   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$                   |
| Turn-OFF switching losses <sup>4)</sup>                    | $E_{off}$    | -      | 1638 | -    | μJ   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$                   |
| Total switching losses <sup>4)</sup>                       | $E_{tot}$    | -      | 2391 | -    | μJ   | $V_{DD} = 400 \text{ V}$ , $V_{GS} = 0/18 \text{ V}$ ,<br>$I_D = 146.3 \text{ A}$ , $R_{G,ext} = 5.2 \Omega$                   |

**Table 7 Gate charge characteristics**

| Parameter                     | Symbol       | Values |      |      | Unit | Note / Test Condition                                                                         |
|-------------------------------|--------------|--------|------|------|------|-----------------------------------------------------------------------------------------------|
|                               |              | Min.   | Typ. | Max. |      |                                                                                               |
| Plateau gate to source charge | $Q_{GS(pl)}$ | -      | 47   | -    | nC   | $V_{DD} = 400 \text{ V}$ , $I_D = 146.3 \text{ A}$ ,<br>$V_{GS} = 0 \text{ to } 18 \text{ V}$ |
| Gate to drain charge          | $Q_{GD}$     | -      | 33   | -    | nC   | $V_{DD} = 400 \text{ V}$ , $I_D = 146.3 \text{ A}$ ,<br>$V_{GS} = 0 \text{ to } 18 \text{ V}$ |
| Total gate charge             | $Q_G$        | -      | 179  | -    | nC   | $V_{DD} = 400 \text{ V}$ , $I_D = 146.3 \text{ A}$ ,<br>$V_{GS} = 0 \text{ to } 18 \text{ V}$ |

<sup>1)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

<sup>2)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

<sup>3)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

<sup>4)</sup> MOSFET used in half-bridge configuration without external diode

**Table 8 Reverse diode characteristics**

| Parameter                                    | Symbol    | Values |              |        | Unit | Note / Test Condition                                                                                                                                                                                                        |
|----------------------------------------------|-----------|--------|--------------|--------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                              |           | Min.   | Typ.         | Max.   |      |                                                                                                                                                                                                                              |
| Drain-source reverse voltage                 | $V_{SD}$  | -      | 4.3          | -      | V    | $V_{GS} = 0 \text{ V}$ , $I_S = 146.3 \text{ A}$ , $T_j = 25 \text{ °C}$                                                                                                                                                     |
| MOSFET forward recovery time                 | $t_{fr}$  | -<br>- | 29.3<br>22.7 | -<br>- | ns   | $V_{DD} = 400 \text{ V}$ , $I_S = 146.3 \text{ A}$ ,<br>$di_S/dt = 1000 \text{ A}/\mu\text{s}$ ; see table 9<br>$V_{DD} = 400 \text{ V}$ , $I_S = 146.3 \text{ A}$ ,<br>$di_S/dt = 4000 \text{ A}/\mu\text{s}$ ; see table 9 |
| MOSFET forward recovery charge <sup>1)</sup> | $Q_{fr}$  | -<br>- | 362<br>607   | -<br>- | nC   | $V_{DD} = 400 \text{ V}$ , $I_S = 146.3 \text{ A}$ ,<br>$di_S/dt = 1000 \text{ A}/\mu\text{s}$ ; see table 9<br>$V_{DD} = 400 \text{ V}$ , $I_S = 146.3 \text{ A}$ ,<br>$di_S/dt = 4000 \text{ A}/\mu\text{s}$ ; see table 9 |
| MOSFET peak forward recovery current         | $I_{frm}$ | -<br>- | 24.7<br>53.5 | -<br>- | A    | $V_{DD} = 400 \text{ V}$ , $I_S = 146.3 \text{ A}$ ,<br>$di_S/dt = 1000 \text{ A}/\mu\text{s}$ ; see table 9<br>$V_{DD} = 400 \text{ V}$ , $I_S = 146.3 \text{ A}$ ,<br>$di_S/dt = 4000 \text{ A}/\mu\text{s}$ ; see table 9 |

<sup>1)</sup>  $Q_{fr}$  includes  $Q_{oss}$

5 Electrical characteristics diagrams

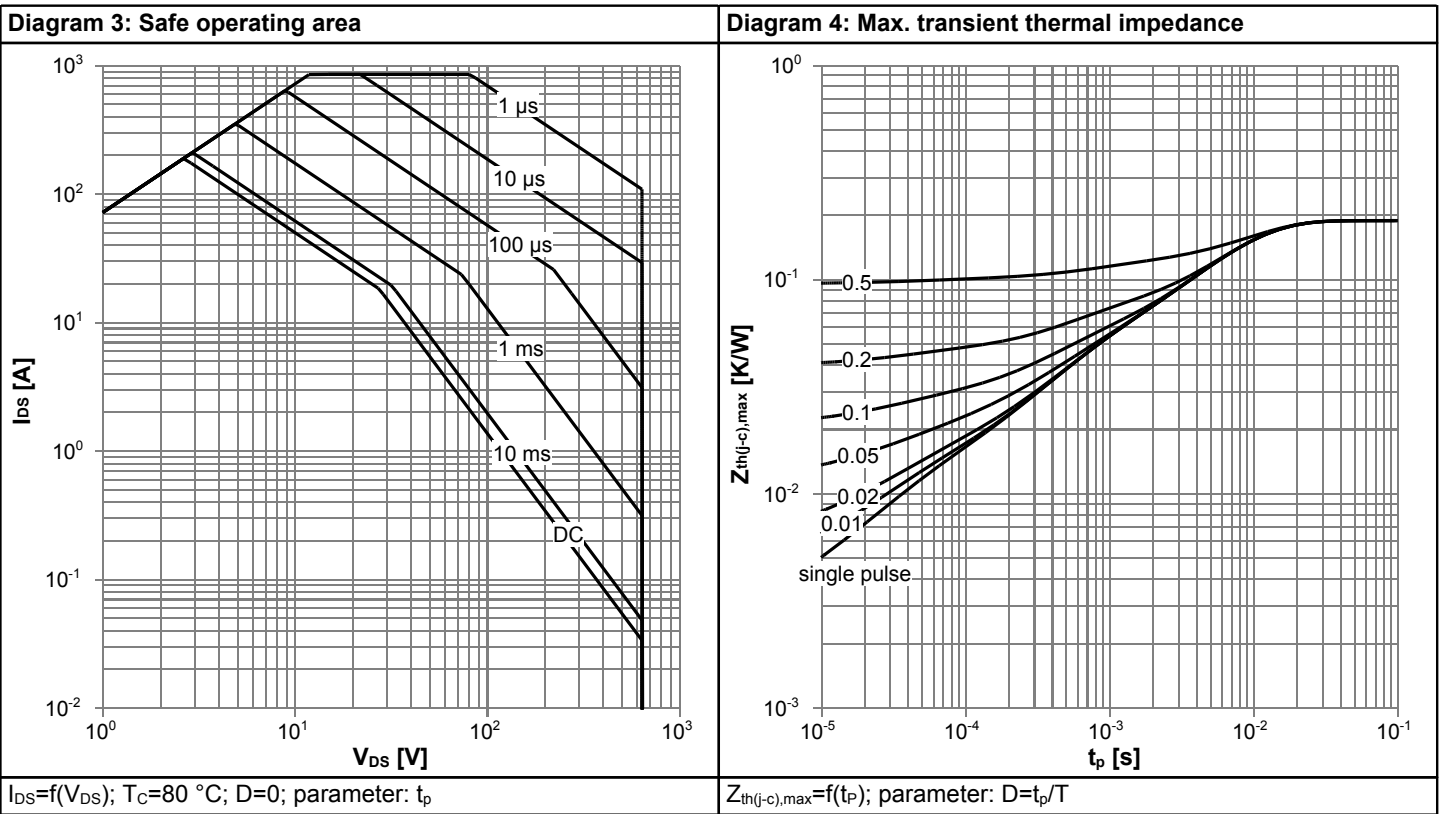
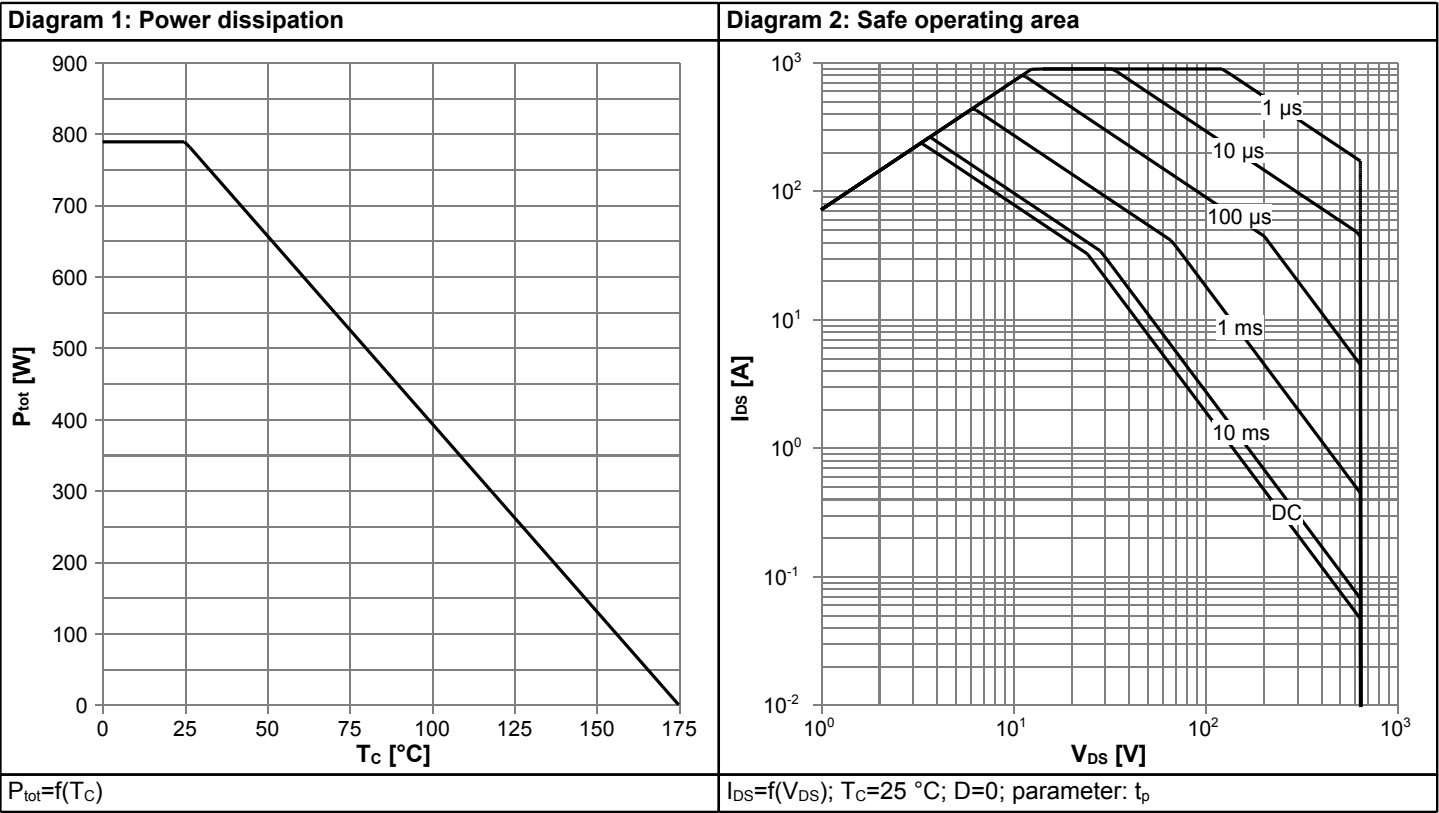
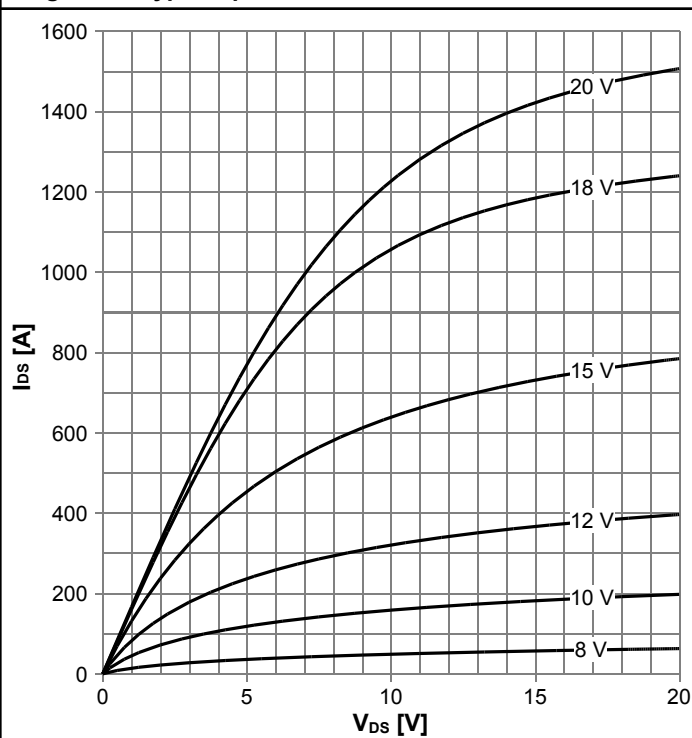
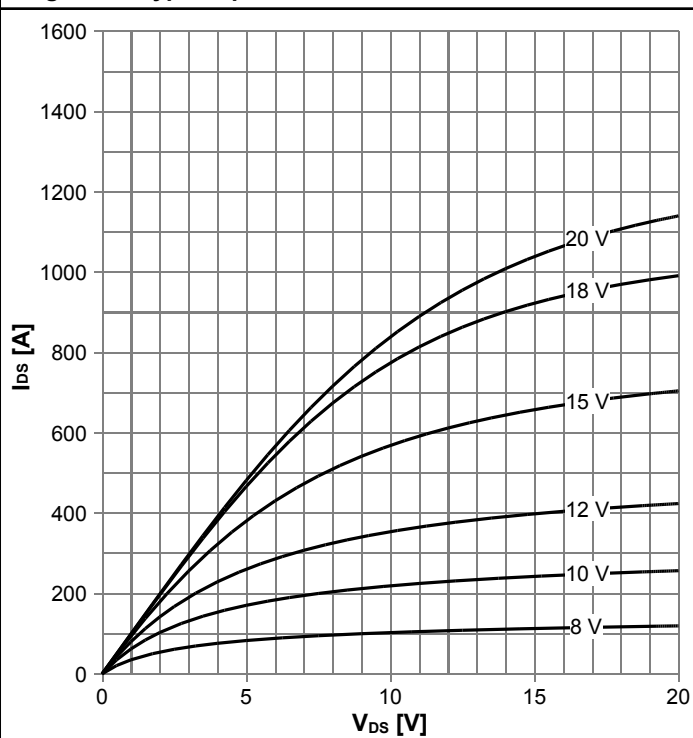


Diagram 5: Typ. output characteristics



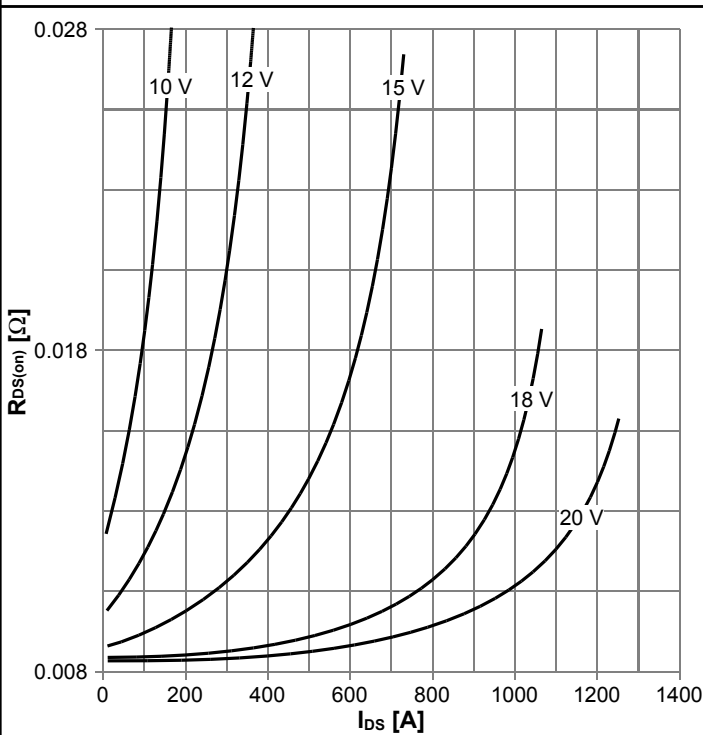
$I_{DS}=f(V_{DS})$ ;  $T_J=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



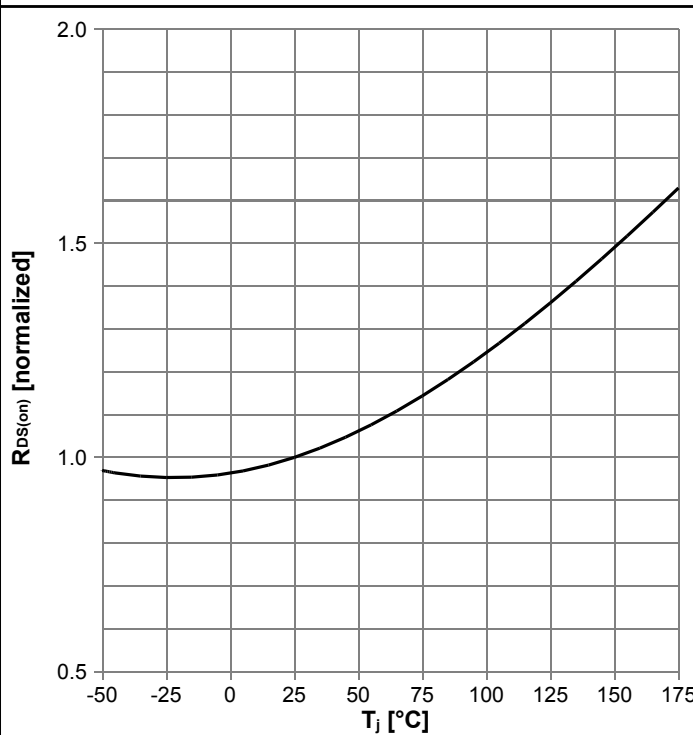
$I_{DS}=f(V_{DS})$ ;  $T_J=175\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



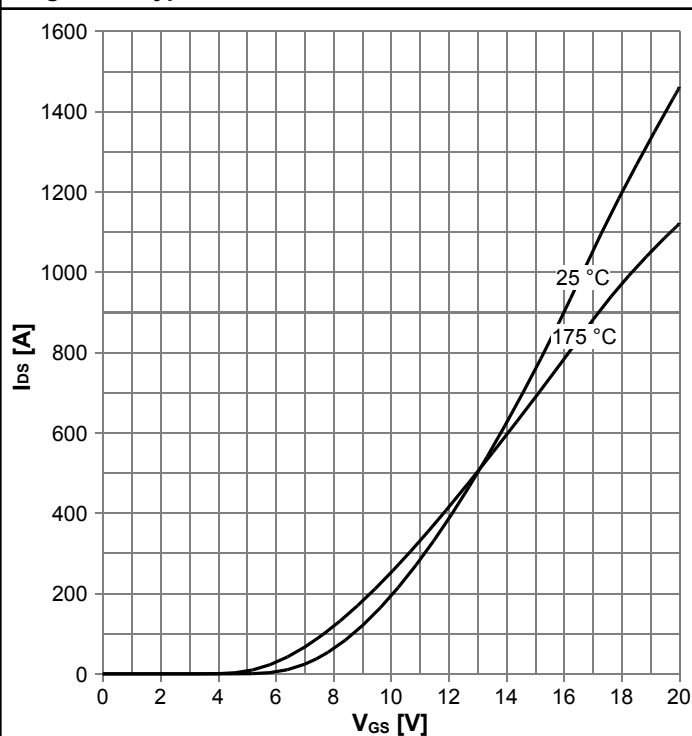
$R_{DS(on)}=f(I_{DS})$ ;  $T_J=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



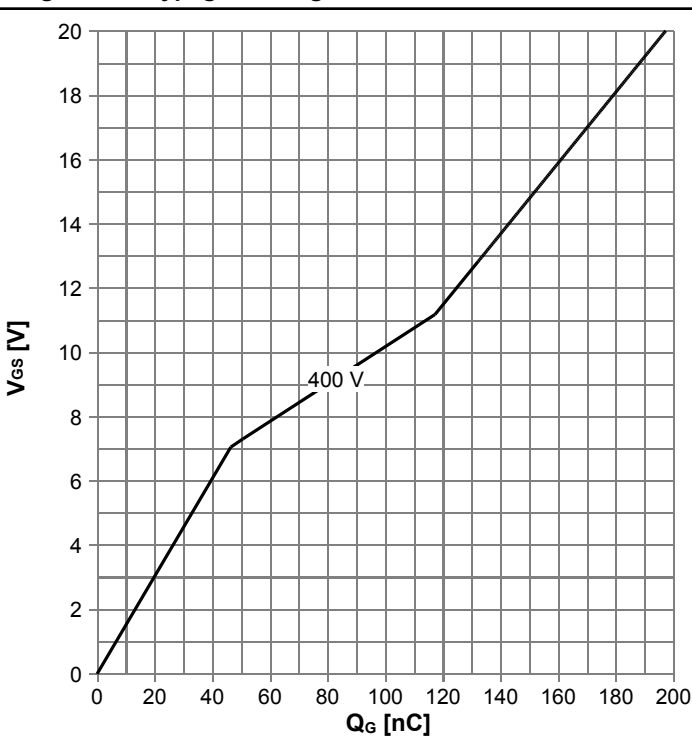
$R_{DS(on)}=f(T_J)$ ;  $I_D=146.3\text{ A}$ ;  $V_{GS}=18\text{ V}$

Diagram 9: Typ. transfer characteristics



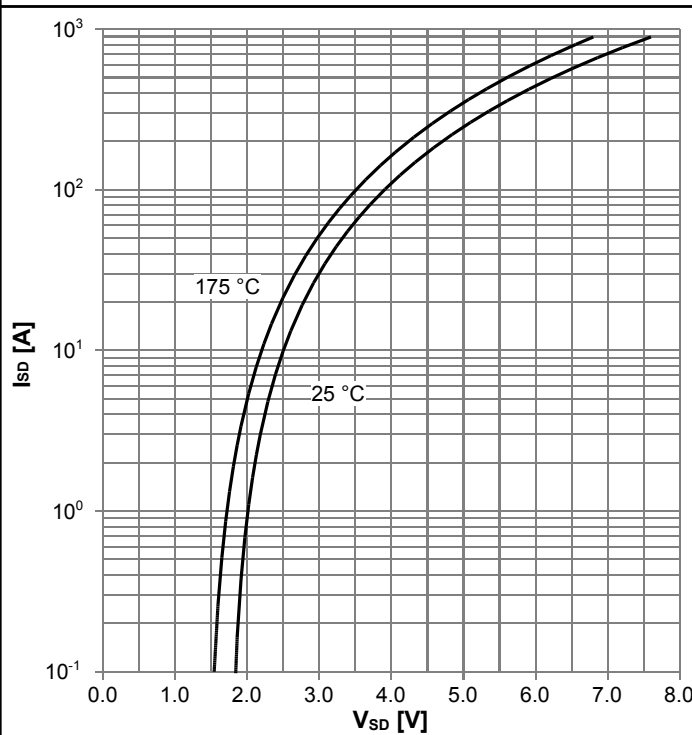
$I_{DS}=f(V_{GS})$ ;  $V_{DS}=20$  V; parameter:  $T_j$

Diagram 10: Typ. gate charge



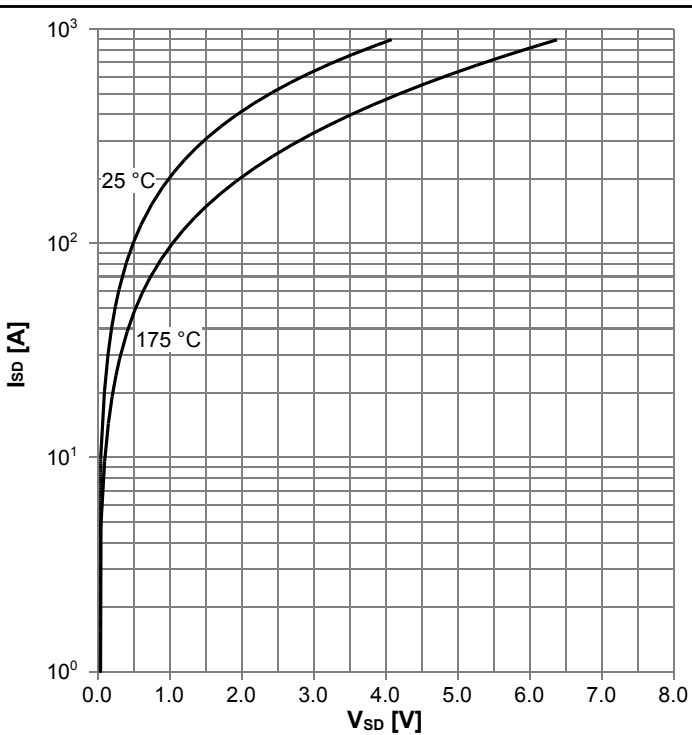
$V_{GS}=f(Q_G)$ ;  $I_D=146.3$  A pulsed; parameter:  $V_{DD}$

Diagram 11: Typ. reverse drain current characteristics



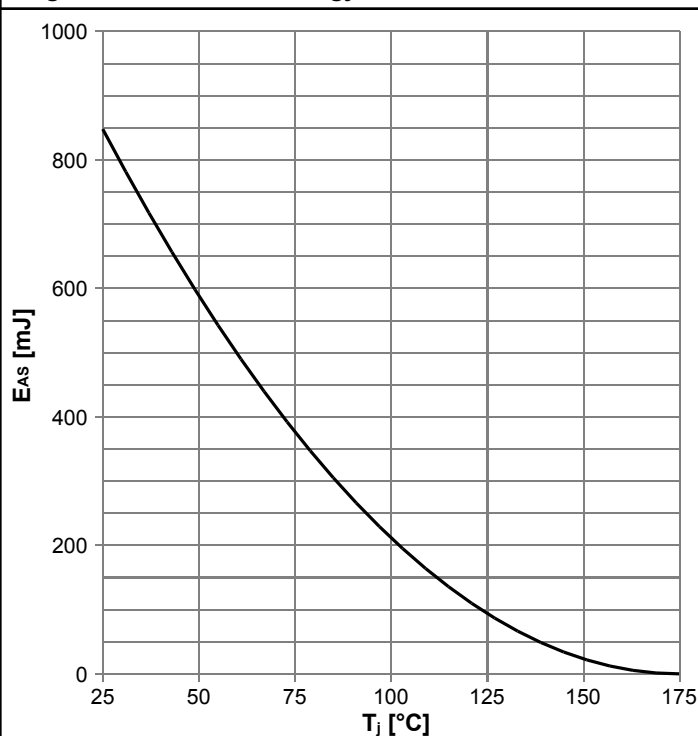
$I_{SD}=f(V_{SD})$ ;  $V_{GS}=0$  V; parameter:  $T_j$

Diagram 12: Typ. reverse drain current characteristics



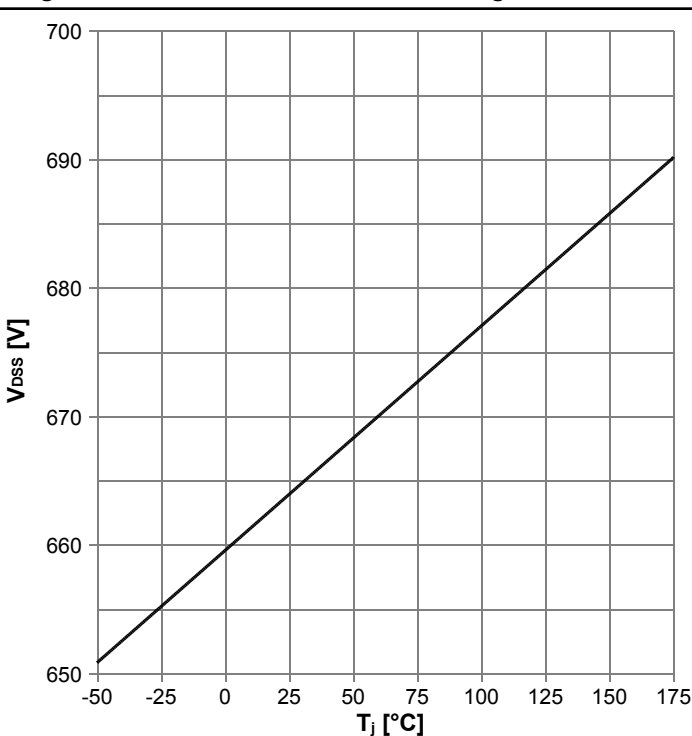
$I_{SD}=f(V_{SD})$ ;  $V_{GS}=18$  V; parameter:  $T_j$

Diagram 13: Avalanche energy



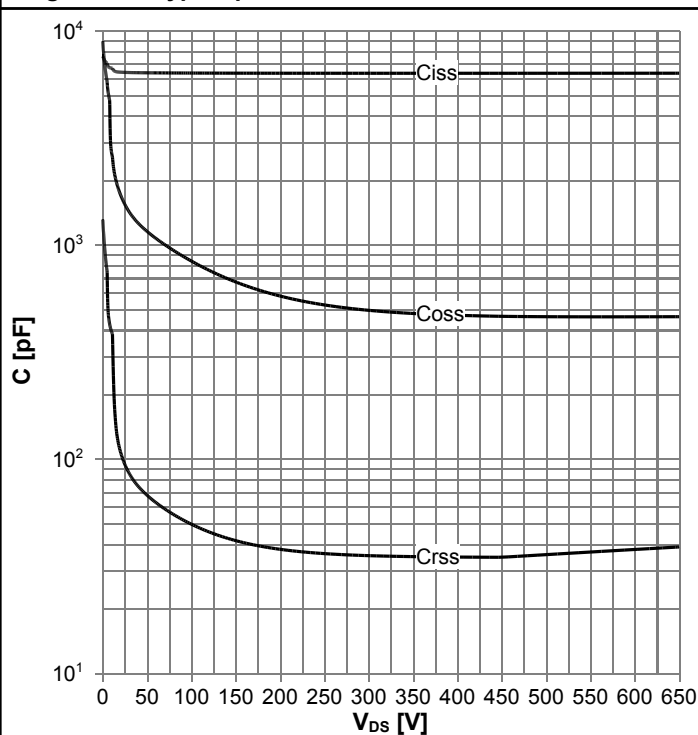
$E_{AS}=f(T_j)$ ;  $I_D=31.8\text{ A}$ ;  $V_{DD}=50\text{ V}$

Diagram 14: Drain-source breakdown voltage



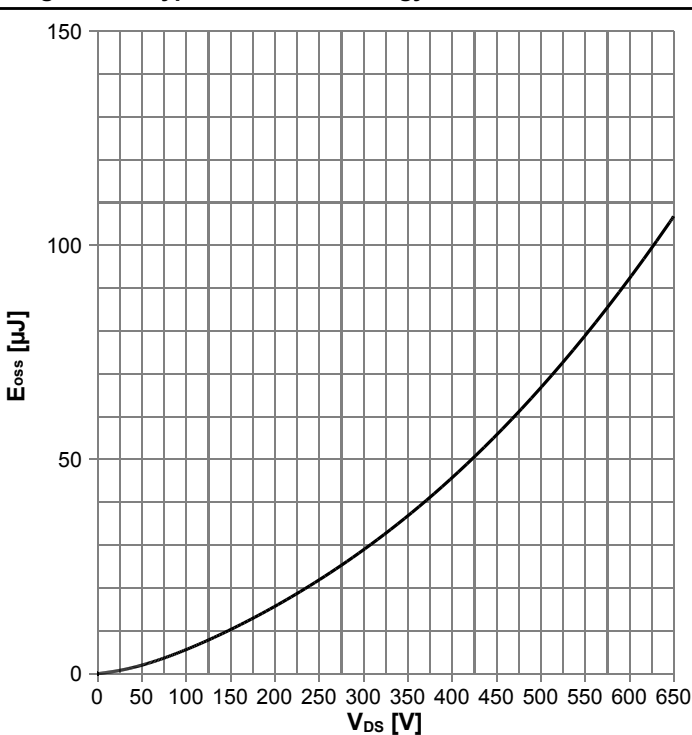
$V_{DSS}=f(T_j)$ ;  $I_D=2.97\text{ mA}$

Diagram 15: Typ. capacitances



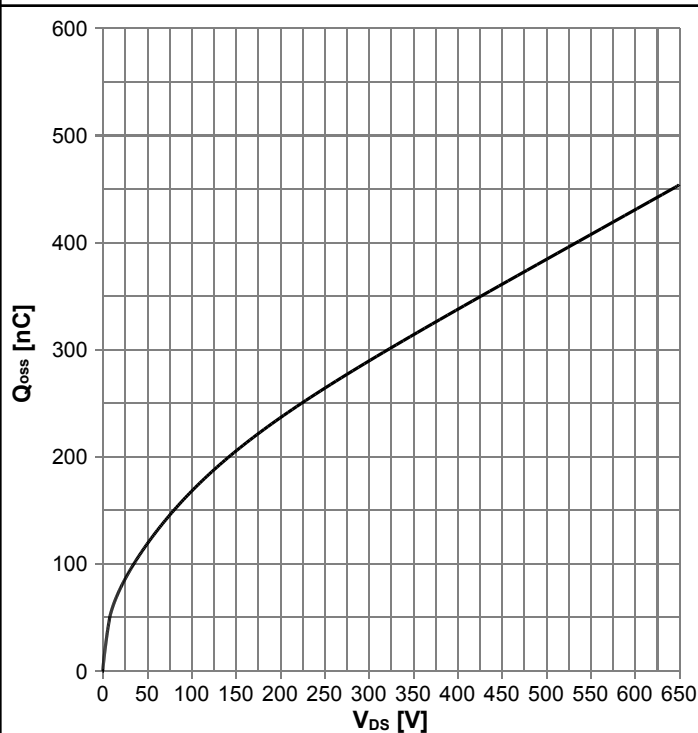
$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=250\text{ kHz}$

Diagram 16: Typ. Coss stored energy



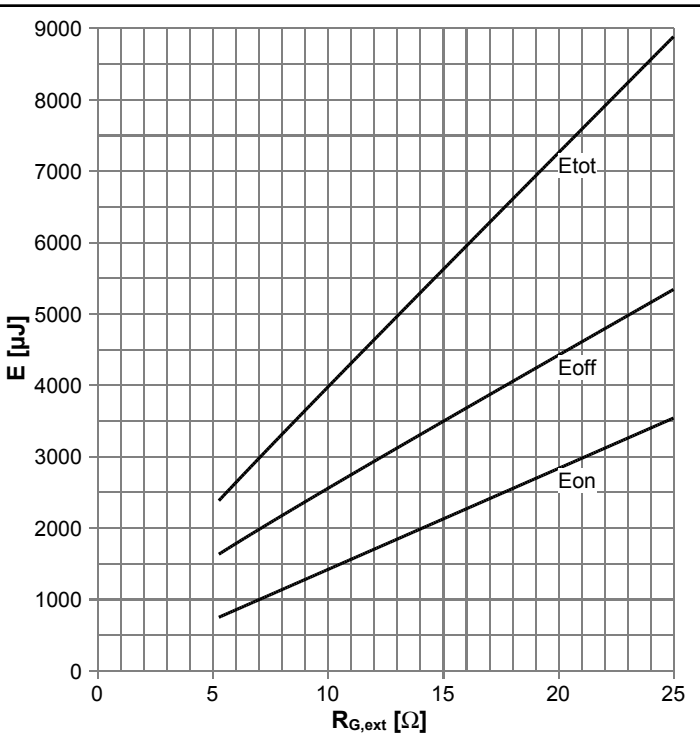
$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



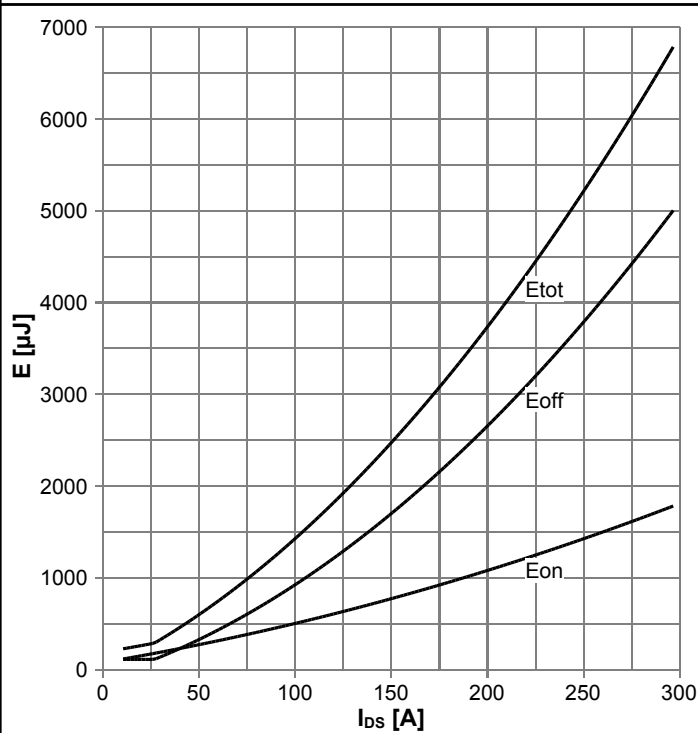
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. Switching Losses vs  $R_{G,ext}$



$E=f(R_{G,ext}); V_{DD}=400\text{ V}; V_{GS}=0/18\text{ V}; I_D=146.3\text{ A}$

Diagram 19: Typ. Switching Losses vs switching current



$E=f(I_{DS}); V_{DD}=400\text{ V}; V_{GS}=0/18\text{ V}; R_{G,ext}=5.3\text{ }\Omega$

6 Test Circuits

Table 9 Body diode characteristics

| Test circuit for body diode characteristics | Body diode recovery waveform |
|---------------------------------------------|------------------------------|
|                                             |                              |

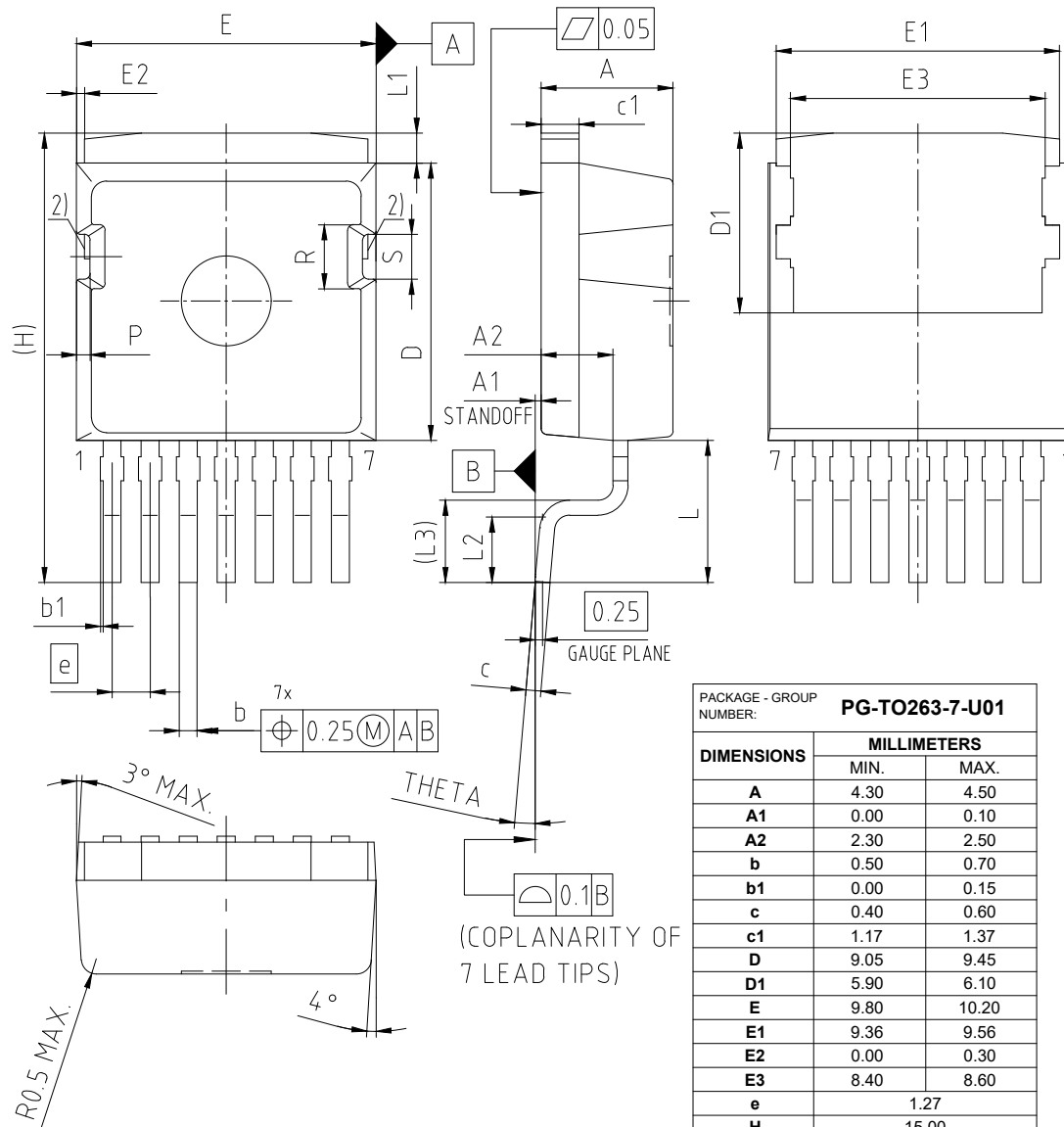
Table 10 Switching times

| Switching times test circuit for inductive load | Switching times waveform |
|-------------------------------------------------|--------------------------|
|                                                 |                          |

Table 11 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---------------------------------------|------------------------------|
|                                       |                              |

## 7 Package Outlines



NOTES:

- 1) ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT  
2) MOLD FILLING IS ACCEPTABLE AT THIS AREA

|                            |             |                |  |
|----------------------------|-------------|----------------|--|
| PACKAGE - GROUP<br>NUMBER: |             | PG-TO263-7-U01 |  |
| DIMENSIONS                 | MILLIMETERS |                |  |
|                            | MIN.        | MAX.           |  |
| A                          | 4.30        | 4.50           |  |
| A1                         | 0.00        | 0.10           |  |
| A2                         | 2.30        | 2.50           |  |
| b                          | 0.50        | 0.70           |  |
| b1                         | 0.00        | 0.15           |  |
| c                          | 0.40        | 0.60           |  |
| c1                         | 1.17        | 1.37           |  |
| D                          | 9.05        | 9.45           |  |
| D1                         | 5.90        | 6.10           |  |
| E                          | 9.80        | 10.20          |  |
| E1                         | 9.36        | 9.56           |  |
| E2                         | 0.00        | 0.30           |  |
| E3                         | 8.40        | 8.60           |  |
| e                          | 1.27        |                |  |
| H                          | 15.00       |                |  |
| L                          | 4.20        | 5.20           |  |
| L1                         | 0.70        | 1.30           |  |
| L2                         | 1.70        | 2.30           |  |
| L3                         | 2.70        |                |  |
| P                          | 0.35        | 0.55           |  |
| R                          | 2.03        | 2.23           |  |
| S                          | 1.40        | 1.60           |  |
| THETA                      | 0.00°       | 8.00°          |  |

**Figure 1** Outline PG-TO263-7, dimensions in mm

## **8 Appendix A**

### **Table 12 Related Links**

- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IMBG65R007M2H

**Revision: 2024-03-05, Rev. 2.2**

Previous Revision

| Revision | Date       | Subjects (major changes since last revision)                      |
|----------|------------|-------------------------------------------------------------------|
| 2.0      | 2023-09-26 | Release of final version                                          |
| 2.1      | 2024-02-29 | updated simulation model; included Eon and Eoff data and diagrams |
| 2.2      | 2024-03-05 | minor layout changes                                              |

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