CoolGaN™ Integrated Power Stage IGI60F140A1L

140 mΩ / 600 V GaN power switch with robust, fast and accurate isolated gate driver

Features

- 140 mΩ GaN switch with dedicated functional isolated gate driver
  - Source / sink peak driving current 1 A / 2 A
  - Application-configurable turn-on and turn-off speed
- Fast input-to-output propagation (47 ns typ.) with low variation
- PWM input signal (switching frequency up to 3 MHz)
- Standard logic input levels compatible with digital controllers
- Wide supply operating range
- Single gate driver supply voltage possible (typ. 8 V) with fast UVLO recovery.
- Low-side open source for current sensing with external shunt resistor
- Galvanic input-to-output isolation based on robust coreless transformer technology
- Gate driver with very high common mode transient immunity (CMTI) > 150 V/ns
- Thermally enhanced 8 x 8 mm QFN-21 package with large exposed pad
- Product is fully qualified acc. JEDEC for Industrial Applications

Description

IGI60F140A1L combines a single 140 mΩ (typ.) / 600 V enhancement-mode CoolGaN™ switch with a dedicated gate driver in a thermally enhanced 8 x 8 mm QFN-21 package. Due to the galvanic functional isolation between input and output the power stage is able to cover a broad spectrum of applications and topologies.
Infineon's CoolGaN™ and related power switches provide a very robust gate structure. When driven by a continuous gate current of a few mA in the "on" state, a minimum on-resistance R_{dson} is always guaranteed, independent of temperature and parameter variations.

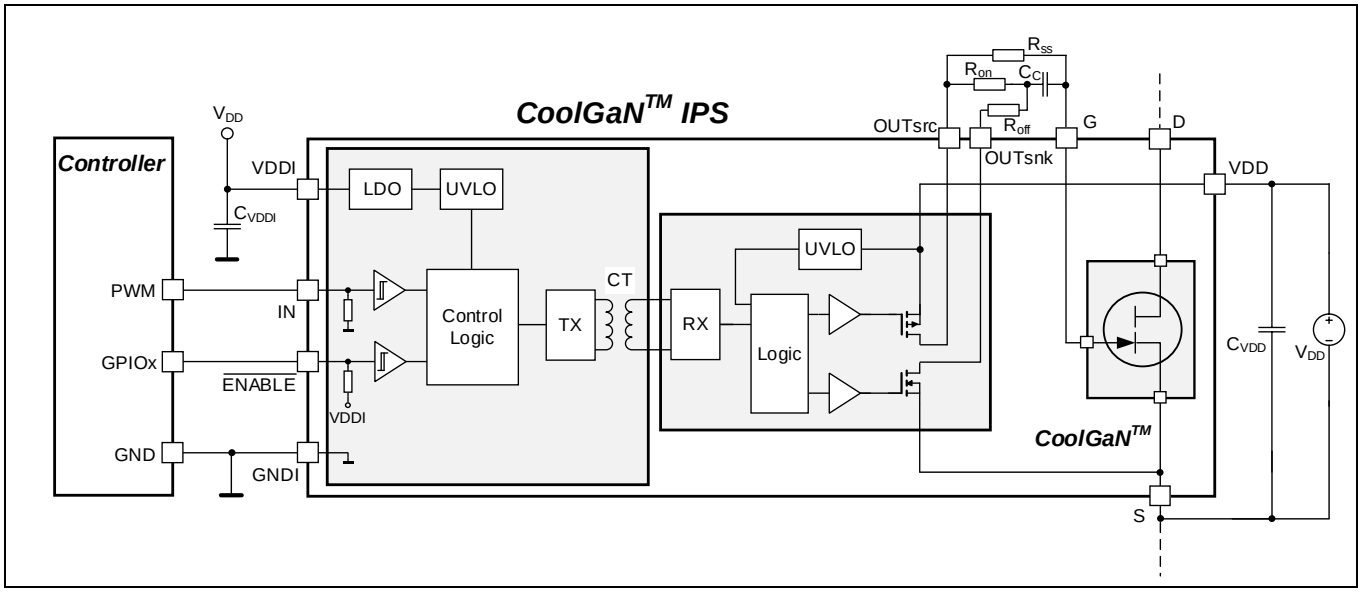

Figure 1 Typical Application

Due to the GaN-specific low threshold voltage and the fast switching transients, a negative gate drive voltage is required in certain applications to both enable fast turn-off and avoid cross-conduction effects. This can be achieved by the well-known RC interface between driver and switch. A few external SMD resistors and caps enable easy adaptation to different power topologies.
The driver utilizes on-chip coreless transformer technology (CT) to achieve signal level-shifting to the high-side. Further, CT guarantees robustness even for extremely fast switching transients above 300 V/ns.

Applications

- Charger and Adaptors
- Server, Telecom & Networking SMPS
- Motor Drive
- Energy Storage Systems
- LED Lighting

Power Topologies

- Active clamp flyback or hybrid flyback converters
- LLC or LCC resonant converters
- Single or interleaved synchronous buck or boost converter
- Single phase or multiphase two-level inverters

Product Versions

Table 1 CoolGaN™ integrated power stage single channel products overview

Part Number	OPN	Package	Typ. R_{dson} 25°C	Marking
IGI60F100A1L	IGI60F100A1LAUMA1	PG-TIQFN-21-1 8 x 8 mm	100 mΩ	60F100A
IGI60F140A1L	IGI60F140A1LAUMA1	PG-TIQFN-21-1 8 x 8 mm	140 mΩ	60F140A
IGI60F200A1L	IGI60F200A1LAUMA1	PG-TIQFN-21-1 8 x 8 mm	200 mΩ	60F200A
IGI60F270A1L	IGI60F270A1LAUMA1	PG-TIQFN-21-1 8 x 8 mm	270 mΩ	60F270A

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1 Pin configuration and description

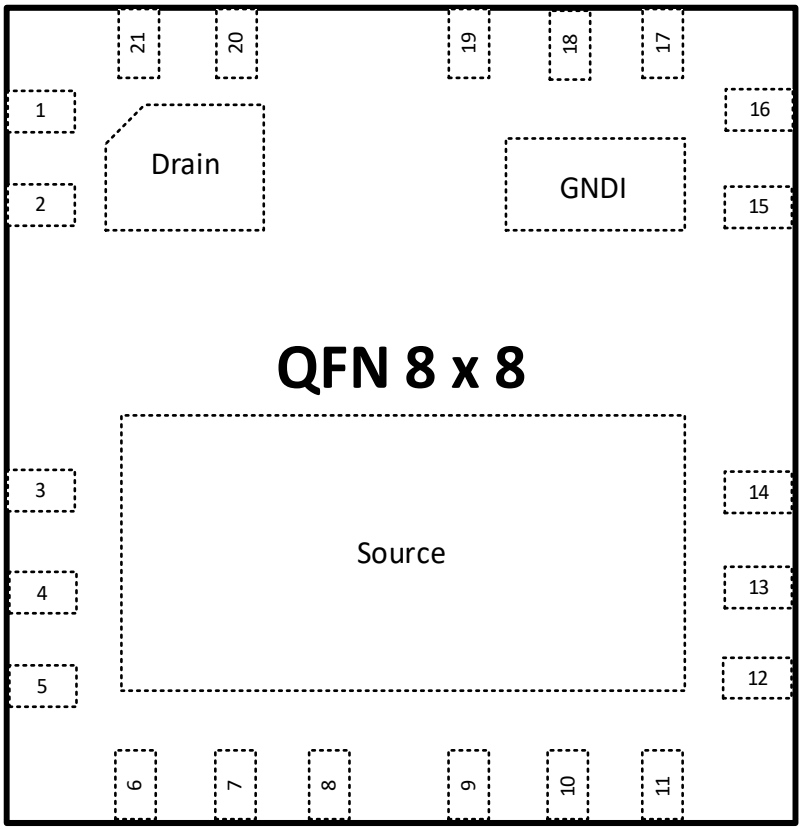


Figure 2 Pin configuration and exposed for QFN-21 8 x 8 mm package, top view (not to scale)

Table 2 Pin description

Pin No.	Symbol	Description
1, 2, 20, 21	D	Drain connection GaN switch
3 – 9, 14	S	Source connection GaN switch
10	G	Gate connection GaN switch
11	OUTSNK	Driver output sink (connects to S)
12	OUTSRC	Driver output source (connects to VDD)
13	VDD	Driver supply voltage (typ. 8 V)
15, 19	GNDI	Ground connection of driver input stage
16	VDDI	Supply voltage driver input stage
17	IN	Input signal (default state “Low”); controls GaN switch
18	$\overline{\text{ENABLE}}$	Input signal (default state “High” – driver output set to “Low” state); logic “Low” required to activate driver output

2 Functional description

2.1 Block Diagram

A simplified functional block diagram of the GaN Power Stage is given in **Figure 3**. For level-shifting of the input signal to a high-side switch an on-chip coreless transformer (CT) is utilized, resulting in a galvanic input-to-output isolation.

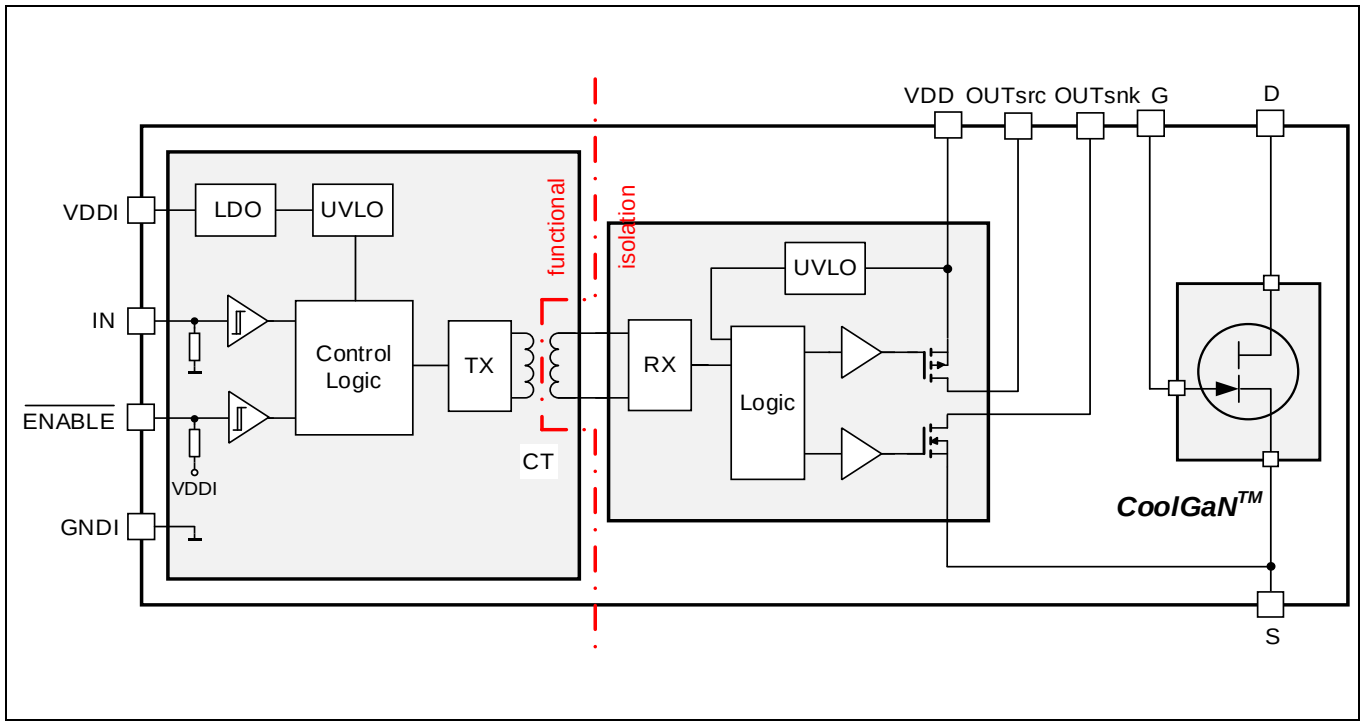


Figure 3 Block Diagram IGI60F140A1L

2.2 Power supply

Basically the Power Stage requires two supply voltages: a µController ground-related V_{DDI} (3 to 15 V) for the driver input circuitry and a source-related V_{DD} (8 to 12 V) as the gate drive supply. In low-side applications usually a single 8 V supply voltage can be used for both V_{DDI} and V_{DD}. Operation as a high-side switch, however, requires a floating gate driver supply. In applications with moderate duty cycle variations (e. g. LLC), this high-side supply voltage can be generated from the ground-related one via bootstrapping. Independent Undervoltage Lockout (UVLO) functions for both supply voltages ensure a defined start-up and robust functionality under all operating conditions.

2.2.1 Driver input supply voltage

The driver input die is supplied via V_{DDI}. Any applied voltage up to 15 V is regulated by an internal LDO to 3.3V. A ceramic bypass capacitance C_{VDDI} of typ. 100 nF has to be placed close to pin VDDI. The Undervoltage Lockout threshold, defining the minimum V_{DDI}, is set to typically 2.85 V.

Power consumption to some extent depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the CT. Due to the chosen robust encoding scheme the average pulse repetition rate and thus the average supply current depends on the switching frequency f_{sw}. However, for f_{sw} < 500 kHz this effect is very small.

2.2.2 Driver output supply voltage

The output stage has to be supplied by a voltage V_{DD} of typically 8 V related to the source of the GaN switch. In low-side applications V_{DD} can be ground-related. A ceramic bypass capacitance C_{VDD} of typ. 100 nF has to be placed close to pin VDD. The minimum operating supply voltage is defined by the implemented undervoltage lockout function.

2.3 Input configurations

The input IN is an independent logic (PWM) channel. The input signal is transferred non-inverted to the corresponding gate driver outputs OUTsrc and OUTsnk. All inputs are compatible with LV-TTL threshold levels with a hysteresis of typ. 0.8 V. The hysteresis is independent of the supply voltage VDDI.

The PWM inputs are internally pulled down to a logic low voltage level (GNDI). In case the PWM-controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off"-state (low). If the Enable input is high, OUTsrc will have high impedance and OUTsnk will be low, regardless of the state of IN. **Table 3** shows the logic table in normal operation.

Table 3 Logic table (UVLO input inactive, both output side UVLO inactive; normal operation)

Inputs		Gate Drive Ouput	
Enable	**IN**	**OUTsrc**	**OUTsnk**
H	x	Z	L
L	H	H	Z
L	L	Z	L

2.4 Driver output

The rail-to-rail driver output stage realized with complementary MOS transistors is able to provide a typical 1 A sourcing and 2 A sinking current. This is by far sufficient when driving a GaN HEMT due to the low gate charge. In addition, the relatively low driver output resistance is beneficial, too. With an R_{on} of 3.1 Ω for the sourcig pMOS and 1.2 Ω for the sinking nMOS transistor the driver can be considered as nearly ideal. The gate drive parameters can thus be determined easily and accurately by the external components as described in chapter 4. The p-channel sourcing transistor allows real rail-to-rail behavior without suffering from a source follower's voltage drop.

2.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the gate drive outputs can be switched to their high level only, if both input and output supply voltages exceed the corresponding UVLO threshold voltages. Thus it can be guaranteed that the GaN switches are in “off” state, if the driving voltage is too low for complete and fast switching-on, thereby avoiding excessive power dissipation and keeping the switch transistors within their safe operating area (SOA).

The UVLO level for the output supply voltage V_{DD} is set to a typical “on”-value of 4.2 V (with 0.3 V hysteresis), whereas $UVLO_{in}$ for V_{DDI} is set to 2.85 V with 0.15 V hysteresis.

Table 4 Logic table (dependence on UVLO status)

Inputs					Gate Drive Ouput
Enable	**IN**	**UVLO input**	**UVLO output**	**OUTsrc**	**OUTsnk**
x	x	Active	x	Z	L
x	x	x	Active	Z	L
H	L	Inactive	Inactive	Z	L
H	H	Inactive	Inactive	H	Z

2.6 Start-up and active clamping

Special attention has been paid to cover all possible operating conditions, like start-up or arbitrary supply voltage situations:

- if V_{DDI} drops below $UVLO_{in}$, a “switch-to-low” command is sent to the gate driver output
- for V_{DD} lower than the respective output UVLO level, a new fast active clamping circuit provides a low-impedance path from the gate driver output to the source of the GaN switch. As soon as the output voltage exceeds a low threshold level (typ. below 1 V), the clamp is activated within approximately 20 ns.

As the result, safe operation of the GaN Power Stage can be guaranteed under any circumstances.

2.7 CT Communication and Data Transmission

A Coreless Transformer (CT) based communication module is used for PWM signal transfer between input and output. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog time-out at the receiver side enables recovery from communication fails and ensures safe system shut-down in failure cases.

2.8 CoolGaN output stage

he output stage consists of a CoolGaN™ 600V switch. The switch is characterized by a typical R_{dson} of 140 mΩ @ 25 °C. And thanks to the current driving concept, this value increases by a comparably moderate 85 % @ 150 °C. As typical for GaN, gate and output charges are very small and there is no reverse recovery charge due to the lack of a physical body diode (for more information please refer to [1]).

3 Characteristics

3.1 Absolute maximum ratings

The absolute maximum ratings are listed in **Table 3**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or Test Conditions
		Min.	Max.		
Drain-to-source voltage continuous	V_{DS}	-	600	V	V_{GS} = 0 V
Drain-to-source voltage pulsed	$V_{DS,pulse}$	-	750[1]	V	T_J = 25°C, V_{GS} ≤ 0 V, cumulated stress time < 1h
		-	650	V	T_J = 125°C, V_{GS} ≤ 0 V, cumulated stress time < 1h
Continuous drain current[2]	I_D	-	10.6	A	T_{Case} = 25°C
		-	7.8	A	T_{Case} = 125°C (see Fig. 8)
Pulsed drain current[3]	$I_{D,pulse}$	-	23	A	T_{Case} = 25°C
		-	11[4]	A	T_{Case} = 125°C (see Fig. 8)
Supply voltage input chip	V_{DDI}	-0.3	17	V	
Supply voltage output chips	V_{DD}	-0.3	22	V	
Voltage at pins IN and ENABLE	V_{IN}	-0.3	17	V	
Voltage at pin OUT	V_{OUT}	-0.3	V_{DD} + 0.3	V	
Junction temperature	T_J	- 40	150	°C	
Storage temperature	T_S	- 55	150	°C	
Soldering temperature	T_{sold}	-	260	°C	Reflow/wave soldering[5]
ESD capability	V_{ESD_HBM}	-	2	kV	Human Body Model[6]
	V_{ESD_CDM}	-	1	kV	Charged Device Model[7]

[1] Acc to JEDEC-JEP180

[2] Limited by T_{jmax}. Maximum Duty Cycle D=0.5

[3] Limits derived from product characterization, parameter not measured during production

[4] Parameter is influenced by reliability requirements. Please contact the local Infineon Sales Office to get an assessment of your application

[5] Acc. to JESD22A111

[6] Acc. to ANSI/ESDA/JEDEC JS-001

[7] Acc. to ANSI/ESDA/JEDEC JS-002

3.2 Thermal characteristics

Table 6 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Thermal resistance junction-to-case	R_{thJC}	-	-	2.1	°C/W	
Thermal resistance junction-to-ambient	R_{thJA}	-	31	-	°C/W	Device mounted on four-layer PCB with 600 mm² total cooling area

3.3 Recommended Operating range

Table 7 Recommended Operating range

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	3	-	15	V	
Driver output supply voltage	V_{DD}	5.5	8	12	V	min. defined by $UVLO_{out}$
Logic input voltage at pins IN and /ENABLE	V_{IN}	-0.3	-	15	V	
Gate current, continuous[1] [2]	$I_{G, avg}$	-	-	9.6	mA	
Junction temperature	T_J	-40	-	125[3]	°C	

[1] Parameter is influenced by rel-requirements. Contact the local Infineon Sales Office to get an assessment of your application.

[2] We recommend to use RC interface gate drive to optimize the device performance. Please see gate drive application note for details.

[3] continuous operation above 125 °C may reduce lifetime

3.4 Electrical characteristics

Unless otherwise noted, min/max values of characteristics are the lower and upper limits, respectively. They are valid within the full operating range. Typical values are given at T_J = 25 °C with V_{DDI} = V_{DD} = 8 V.

Table 8 Power supply

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
V_{DDI} quiescent current	I_{VDDIqu}	-	0.9	-	mA	no switching
V_{DD} quiescent current	I_{VDDqu}	-	0.7	-	mA	no switching
Undervoltage Lockout input ($UVLO_{in}$) turn-on threshold	$UVLO_{in}$	2.7	2.85	3.0	V	
$UVLO_{in}$ turn-off threshold	$UVLO_{in-}$	-	2.65	-	V	
$UVLO_{in}$ threshold hysteresis	$\Delta UVLO_{in}$	0.15	0.2	0.25	V	
Undervoltage Lockout outputs ($UVLO_{out}$) turn-on threshold	$UVLO_{out}$	4.0	4.2	4.4	V	
$UVLO_{out}$ turn-off threshold	$UVLO_{out-}$	-	3.9	-	V	
$UVLO_{out}$ threshold hysteresis	$\Delta UVLO_{out}$	0.2	0.3	0.4	V	

Table 9 Logic inputs IN and ENABLE

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.2	2.5	V	independent of V_{DDI}
Input voltage threshold for transition HL	V_{INL}	1.0	1.3	1.6	V	independent of V_{DDI}
Input voltage threshold hysteresis	V_{IN_hys}	-	0.9	-	V	
Input pull down resistor	R_{IN}	-	75	-	kΩ	
Input pull up resistor (/ENABLE)	R_{ENA}	-	75	-	kΩ	

Table 10 Static gate driver output characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
High-level (sourcing) output resistance	R_{on}	1.4	3.4	6.2	Ω	
Peak sourcing output current[1]	$I_{src,pk}$	-	1	-	A	actively limited to 1.3 A
Low-level (sinking) output resistance	R_{off}	0.6	1.6	2.9	Ω	
Peak sinking output current[2]	$I_{snk,pk}$	-	-2	-	A	actively limited to -2.6 A
Active clamp threshold voltage	V_{clmp}	-	1	-	V	

Table 11 Output characteristics GaN switch

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
R_{dson}	R_{dson}	-	140	190	mΩ	I_G = 9.6 mA, I_D = 5 A, T_J = 25°C
		-	260	-	mΩ	I_G = 9.6 mA, I_D = 5 A, T_J = 150°C
Drain-source leakage current	I_{DSS}	-	0.4	-	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 25°C
		-	8	-	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 150°C
Total gate charge[3]	Q_G	-	2.2	-	nC	I_G = 0 to 3 mA, V_{DS} = 400 V; I_D = 2 A

[1]Verified by design / characterization, not tested in production

[2]Verified by design / characterization, not tested in production

[3] Verified by design / characterization, not tested in production

Table 12 Static characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V	I_{DS} = 0.96 mA, V_{DS} = 10 V, T_j =25 °C I_{DS} = 0.96 mA, V_{DS} = 10 V, T_j =125 °C
Gate-source reverse clamping voltage	$V_{GS,\ clamp}$	-	-	-8	V	I_{GSS}[1] = -1 mA, T_j =25 °C
Gate resistance	$R_{G,int}$	-	0.74	-	Ω	LCR impedance measurement

Table 13 Dynamic characteristics SWITCH

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	157	-	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	-	28	-	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1 MHz
Reverse transfer capacitance	C_{rss}	-	0.15	-	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	-	32.5	-	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective output capacitance, time related[3]	$C_{o(tr)}$	-	40	-	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Output charge	Q_{oss}	-	16	-	nC	V_{DS} = 0 to 400 V

[1] Gate-Source leakage current

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 14 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	VSD	-	2.5	3	V	V_{GS} = 0V, I_{SD} = 5 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	23	A	I_G = 9.6 mA
Reverse recovery charge	Q_{rr}[1]	-	0	-	nC	I_{SD} = 5 A, V_{DS} = 400V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

Table 15 Dynamic Characteristics[2] DRIVER (see Figure 4, Figure 5)

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
INL to SW propagation delay “on”	t_{PDonL}	-	47	-	ns	R_{tr} = 50 Ω
INL to SW propagation delay “off”	t_{PDoffL}	-	47	-	ns	I_{load} = 2 A
ENABLE to SW propagation delay	$t_{PD\_DIS\_ON}$, $t_{PD\_DIS\_OFF}$	-	70 70	-	ns ns	
Rise time SW	t_{rise}	-	6	-	ns	10 % to 90 %
Fall time SW	t_{fall}	-	5	-	ns	90 % to 10 %
Minimum input pulse width that changes output state	t_{PW}	-	18	-	ns	
Input-side start-up time[2]	$t_{START,VDDI}$	-	7	-	µs	see **Figure 6**
Input-side deactivation time[2]	$t_{STOP,VDDI}$	-	255	-	ns	see **Figure 6**
Output-side start-up time[2]	$t_{START,VDDL/H}$	-	5	-	ns	see **Figure 6**
Output-side deactivation time[2]	$t_{STOP,VDDL/H}$	-	110	-	ns	see **Figure 6**

[1] Excluding Q_{oss}

[2] Verified by design / characterization, not tested in production

Table 16 Functional isolation input-to-output

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input-to-output isolation voltage	V_{ISO}	1200	-	-	V_{DC}	production test > 10 ms
Package clearance	CLR	-	1.9	-	mm	shortest distance over air, from any input pin to any output pin
Package creepage	CPG	-	1.9	-	mm	shortest distance over surface, from any input pin to any output pin
Common Mode Transient Immunity	CMTI	150	-	-	V/ns	acc. to DIN V VDE V0884-10, static and dynamic test

Table 17 Package characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Comparative Tracking Index of package mold	CTI	400	-	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	-	-	2	-	-	according to IEC 60112

3.5 Timing diagram and test circuit

Figure 4 depicts rise, fall and delay times measured at the drain node of the GaN switch.

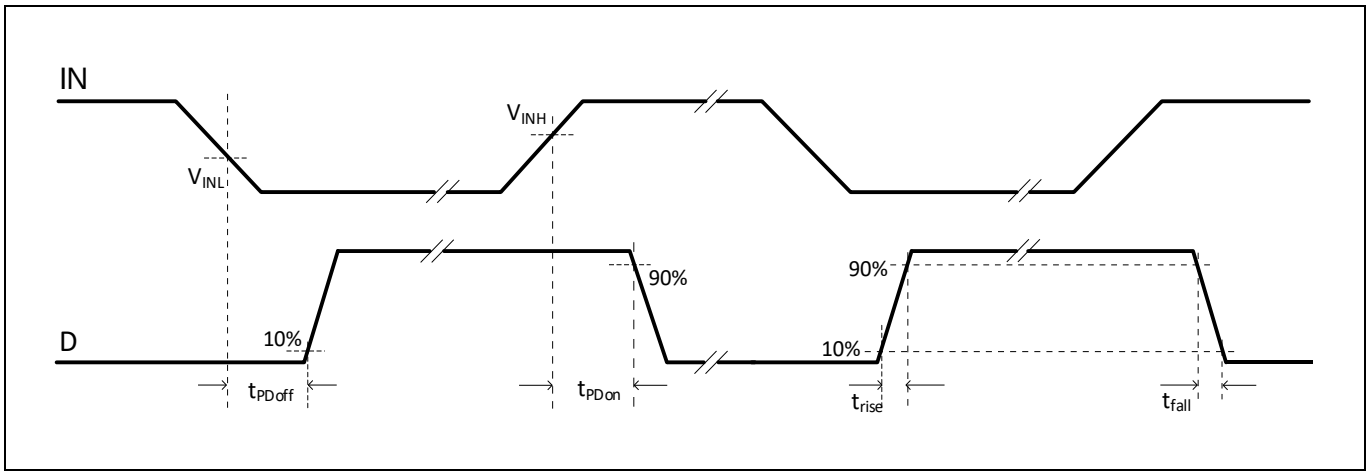


Figure 4 Propagation delay, rise and fall time

Figure 5 shows the associated test circuit. The power stage is operated in a boost configuration at a constant current I_{load}. In this so-called double-pulse arrangement I_{load} is determined by the high-voltage supply (400 V), the output inductance and the length of the first “on”-phase of the IN-signal. The specified delay and transient times are related to an I_{load} value of 2 A (particularly the “off” transient strongly depends on this current).

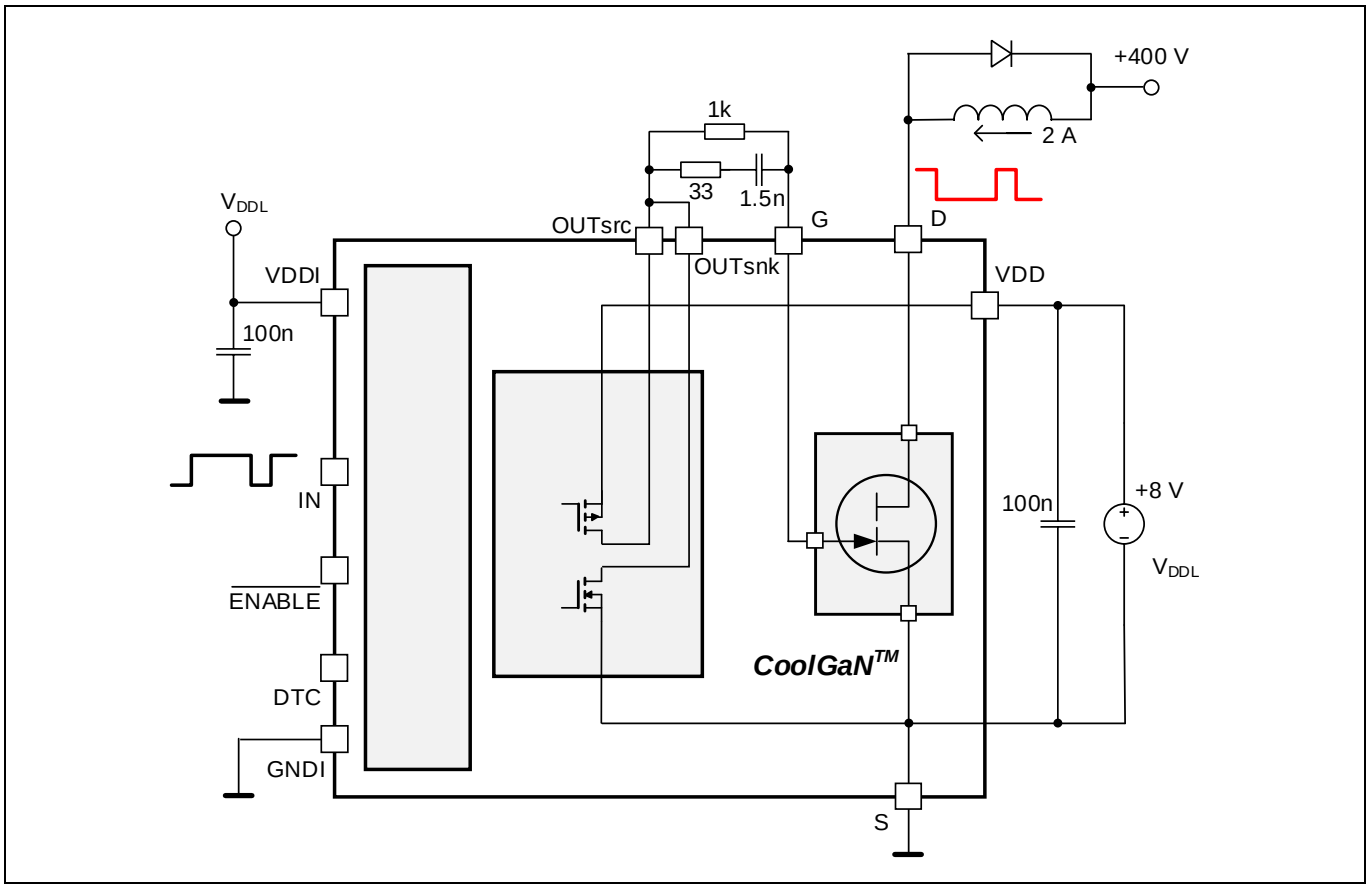


Figure 5 Test circuit

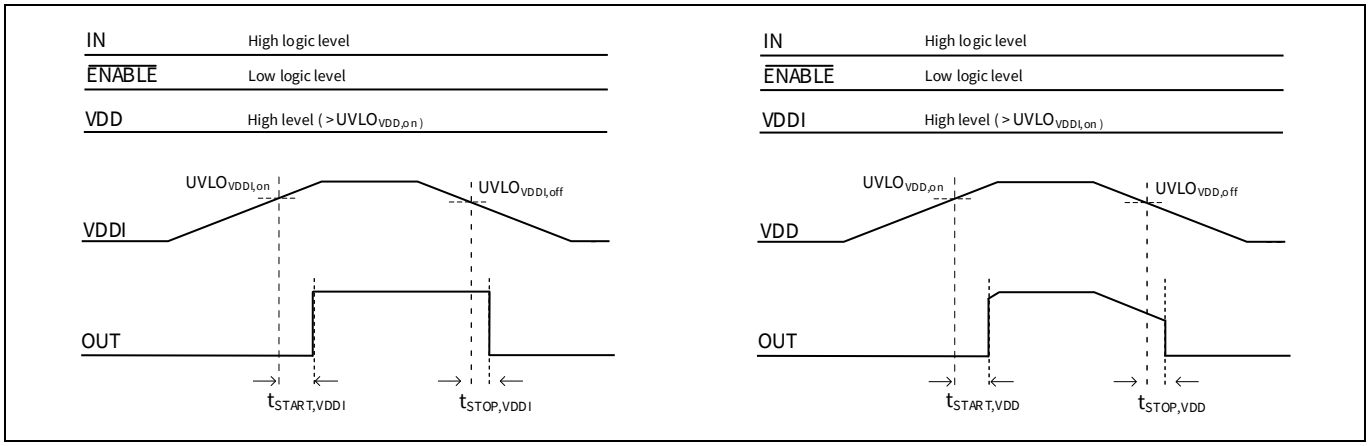


Figure 6 UVLO behavior, start-up and deactivation time (unloaded output)

4 Driving CoolGaN™ HEMTs

Although Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) with ohmic connection to a pGaN gate are robust enhancement-mode (“normally-off”) devices, they differ significantly from MOSFETs. The gate module is not isolated from the channel, but behaves like a diode with a forward voltage V_F of 3 to 4 V. Equivalent circuit and typical gate input characteristic are given in **Figure 7**. In the steady “on” state a continuous gate current is required to achieve stable operating conditions. The switch is “normally-off”, but the threshold voltage V_{th} is rather low (~ +1 V). This is why in many applications a negative gate voltage -V_N, typically in the range of several Volts, is required to safely keep the switch “off” (**Figure 7b**).

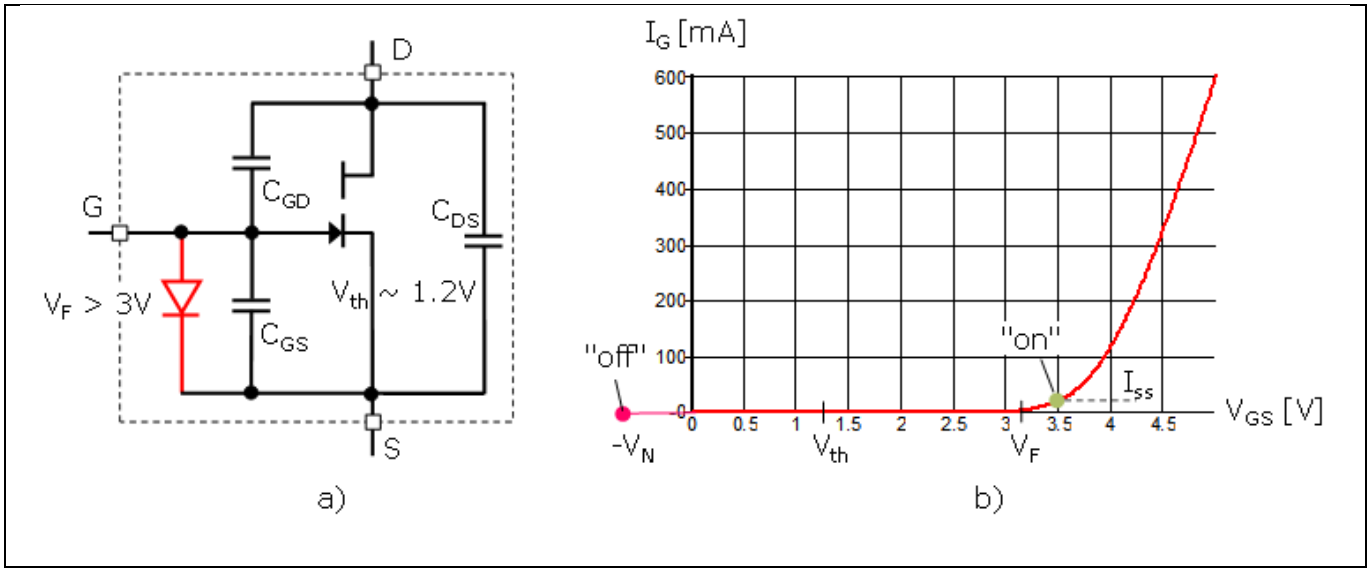


Figure 7 Equivalent circuit (a) and gate input characteristics (b) of typical normally-off GaN HEMT

Obviously the transistor in **Figure 7** cannot be driven like a conventional MOSFET due to the need for a steady-state “on” current I_{ss} and a negative “off” voltage –V_N. While an I_{ss} of a few mA is sufficient, fast switching transients require gate charging currents I_{on} and I_{off} in the 1 A range. To avoid a dedicated driver with 2 separate “on” paths and bipolar supply voltage, the solution depicted in **Figure 8** is usually chosen, combining a standard gate driver with a passive RC circuit to achieve the intended behavior. The high-current paths containing the small gate resistors R_{tr} and R_{off}, respectively, are connected to the gate via a coupling capacitance C_C. C_C is chosen to have no significant effect on the dynamic gate currents I_{on} and I_{off}. In parallel to the high-current charging path the much larger resistor R_{ss} forms a direct gate connection to continuously deliver the small steady-state gate current I_{ss}. In addition, C_C can be used to generate a negative gate voltage. Obviously, in the “on”-state C_C is charged to the difference of driver supply V_{DD} and diode voltage V_F. When switching off, this charge is redistributed between C_C and C_{GS} and causes an initial negative V_{GS} of value:

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}} \quad (2)$$

with Q_G denoting the total gate charge Q_{GS} + Q_{GD} 3 nC. V_N can thus be controlled by proper choice of V_{DD} and C_C. During the „off“ state the negative V_{GS} decreases, as C_C is discharged via R_{SS}. The associated time constant cannot be chosen independently, but is related to the steady-state current and is typically in the 1 µs range. The negative gate voltage at the end of the “off” phase (V_{Nf} in **Figure 8b**) thus depends on the “off” duration. It lowers the effective driver voltage for the following switching-on event, resulting in a slight dependence of switching dynamics on frequency and duty cycle. However, in most applications the impact of this effect is negligible.

Another situation requires attention, too. If there is by any reason a longer period with both switches of a half-bridge in “off”-state (e.g. during system start-up, burst mode operation etc.), both capacitors C_C will be discharged. That means, for the first switching pulse after such an extended non-switching period no negative voltage is available.

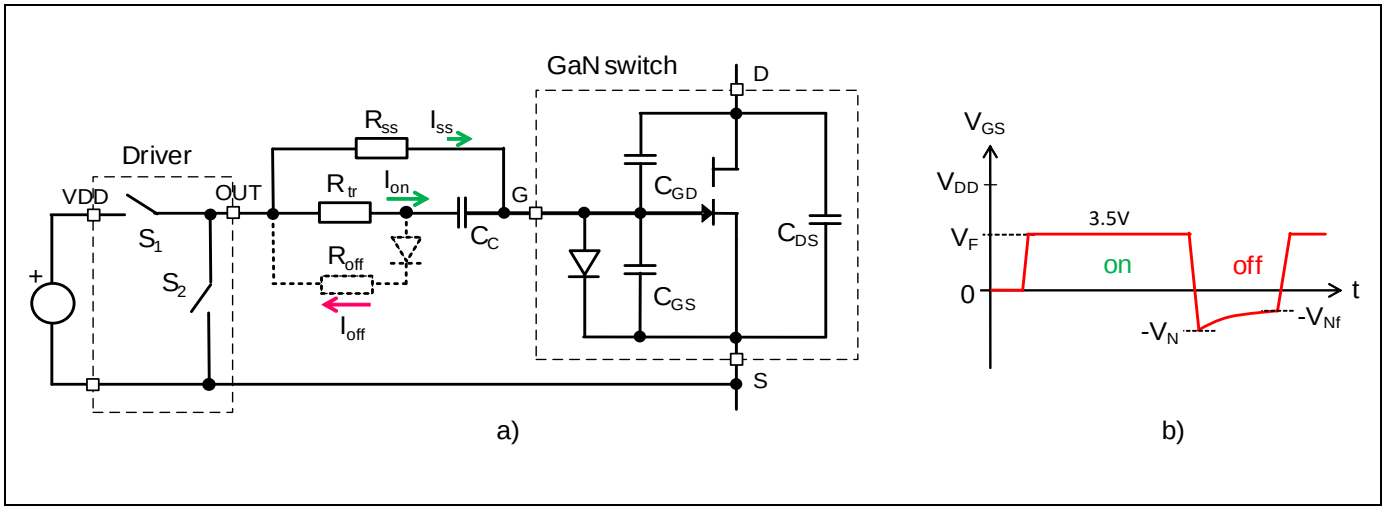


Figure 8 Equivalent circuit of GaN switch with RC gate drive (a) and gate-to-source voltage V_{GS} (b)

In the topology of **Figure 8** often a single resistor R_{tr} can be used for setting the maximum transient charging and discharging current. If this is not acceptable by any reason, an additional resistor R_{off} with series diode in parallel with R_{tr} can be used to realize independent gate impedances for the “on” and “off” transient, respectively.
All relevant driving parameters are easily programmable by choosing V_{DD}, R_{ss}, R_{tr}, R_{off} and C_C according to the relations

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}}$$

$$I_{ss} = \frac{V_{DD} - V_F}{R_{ss}}, \qquad I_{on,max} \sim \frac{V_{DD} - V_{Nf}}{R_{tr}}, \qquad I_{off,max} \sim \frac{(V_{th} + V_N) \cdot (R_{off} + R_{tr})}{R_{off} \cdot R_{tr}} \tag{3}$$

The main guidelines for dimensioning gate drive parameters are as follows:

- V_N must always be positive; a target value of 2 V in soft-switching and 4 V to 5 V in hard-switching systems is recommended
- The target value of I_{ss} is around 4 mA, R_{ss} has to be chosen accordingly
- R_{tr} sets the transient speed for a hard switching “on” event. For soft switching systems R_{tr} is anyway uncritical.
- If a separate R_{off} is used, it should not be above 5 Ω to guarantee sufficient damping of oscillations in the gate loop.

For a given driving voltage the values for the gate drive components can now be derived from equations (3).
V_{DD} = 8 V, for example, yields

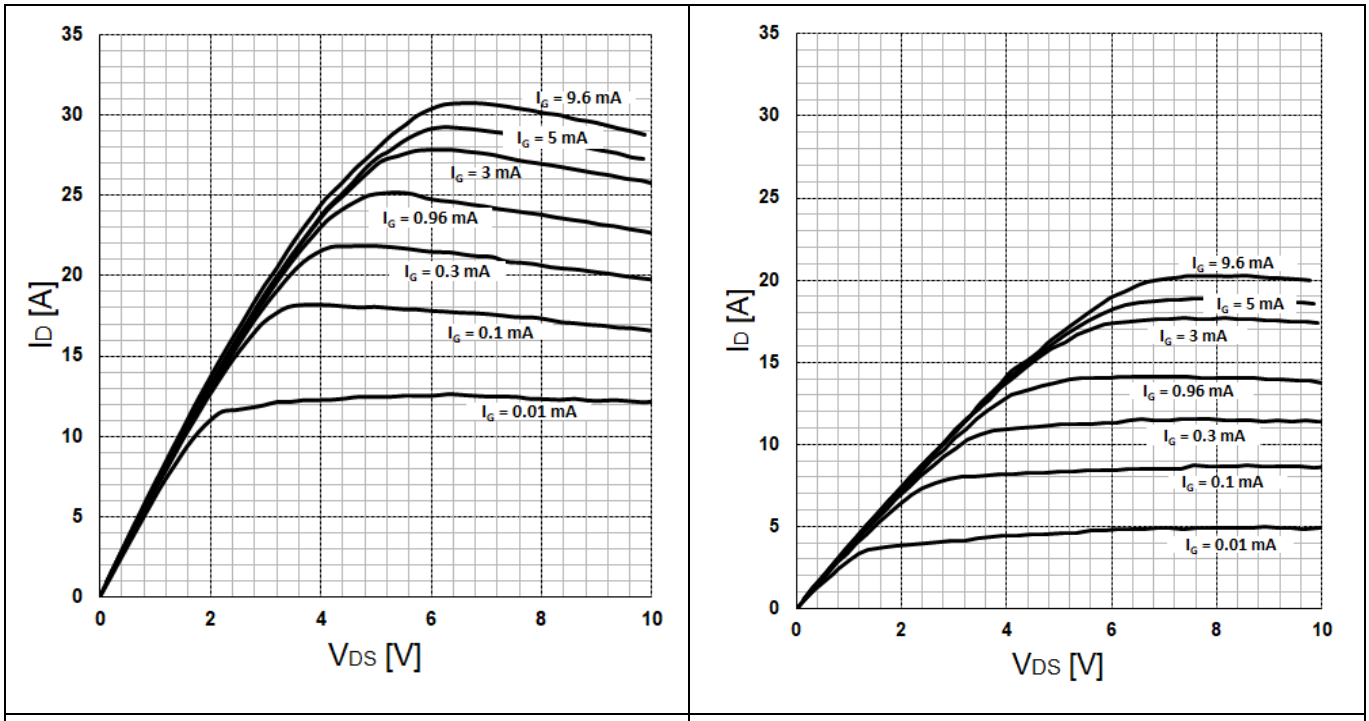
- C_C = 1.5 nF
- R_{ss} = 1.8 kΩ
- R_{tr} = 20 … 50 Ω
- R_{off} = 4.7 Ω (if used)

For more information regarding how to drive GaN HEMT refer to [2].

5 Typical characteristics

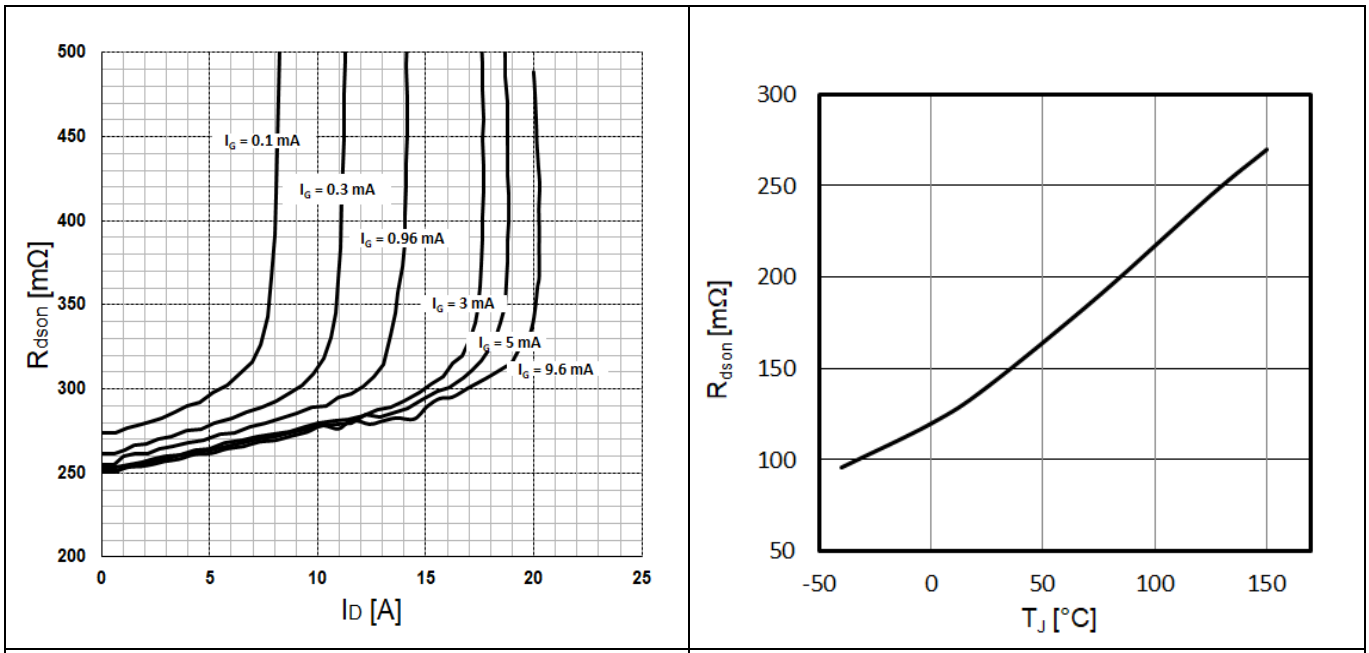
5.1 GaN switch characteristics

The following graphs refer to a single GaN switch.



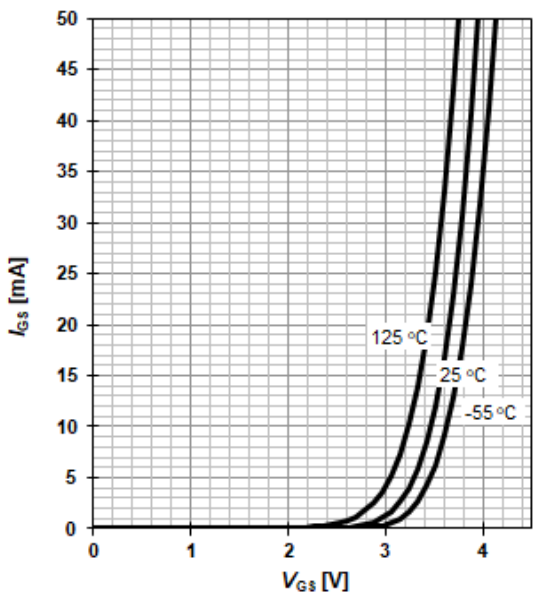
$I_D=f(V_{DS},I_{GS})$; T_j=25°C	$I_D=f(V_{DS},I_{GS})$; T_j=125°C

Figure 9 Typical output characteristics

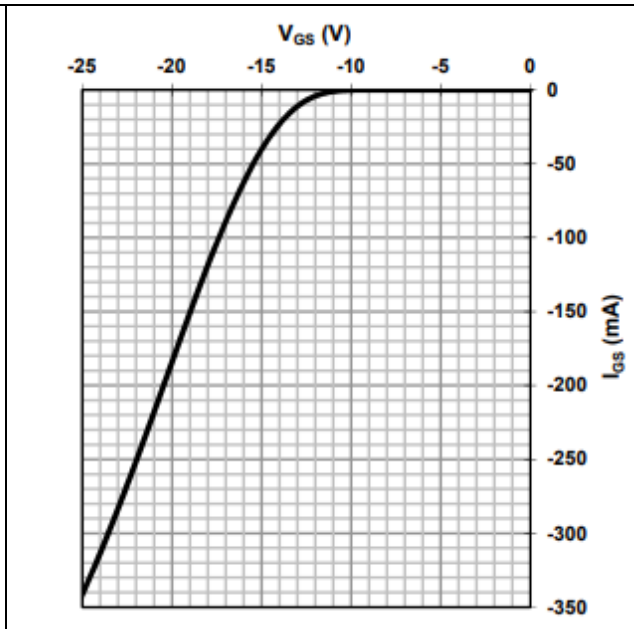


$R_{DS(on)}=f(I_D,I_G)$; T_j=125°C	$R_{DS(on)}=f(T_j)$; I_D=5 A

Figure 10 Typical drain-source on-resistance

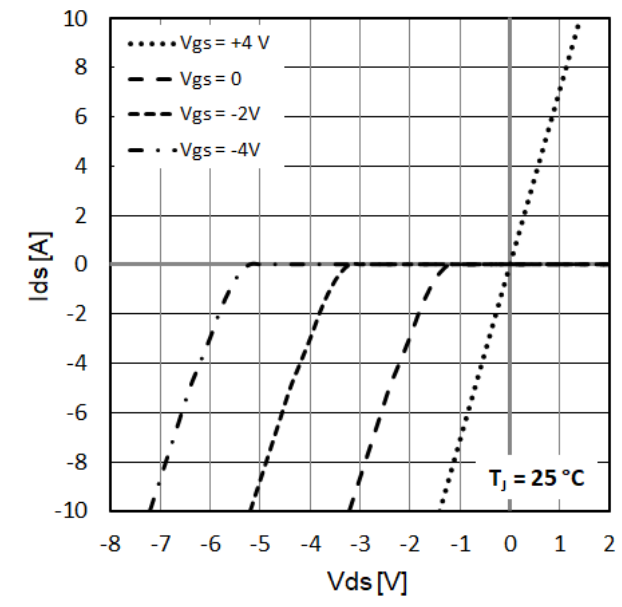


$I_{GS}=f(V_{GS},T_j)$; Open Darin



$I_{GS}=f(V_{GS},T_j)$; T_j=25°C

Figure 11 Typical gate characteristics forward and reverse



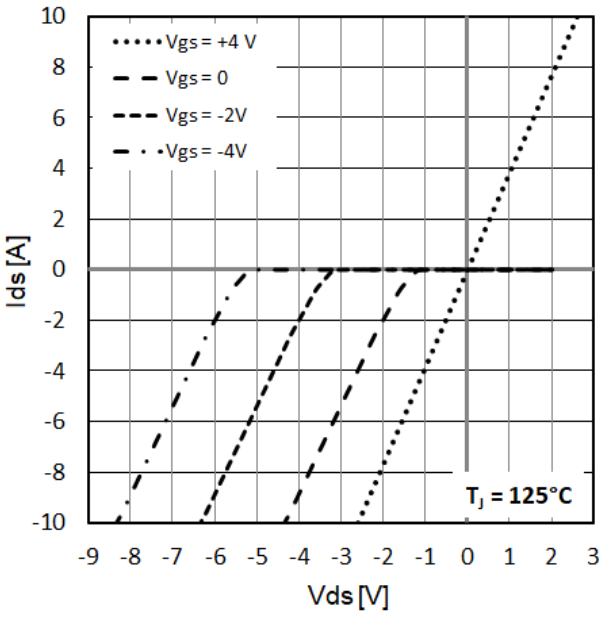
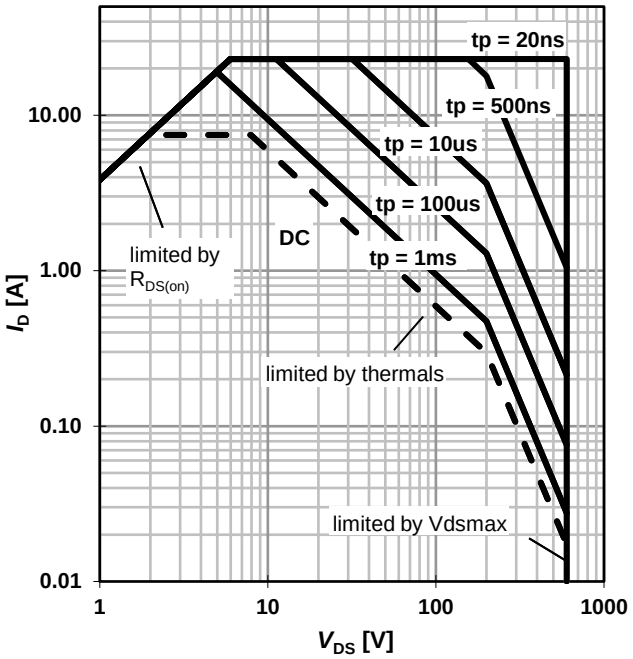
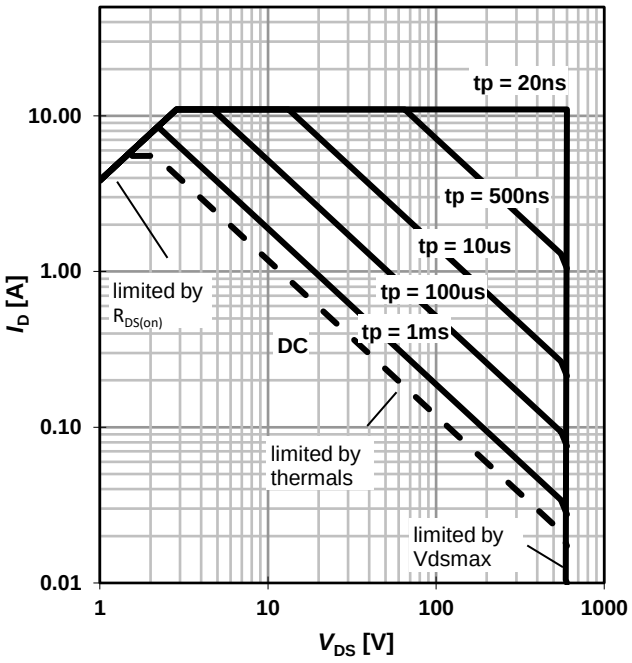


Figure 12 Output characteristic I_{ds} (V_{ds}) in normal and reverse operation (parameter V_{gs})

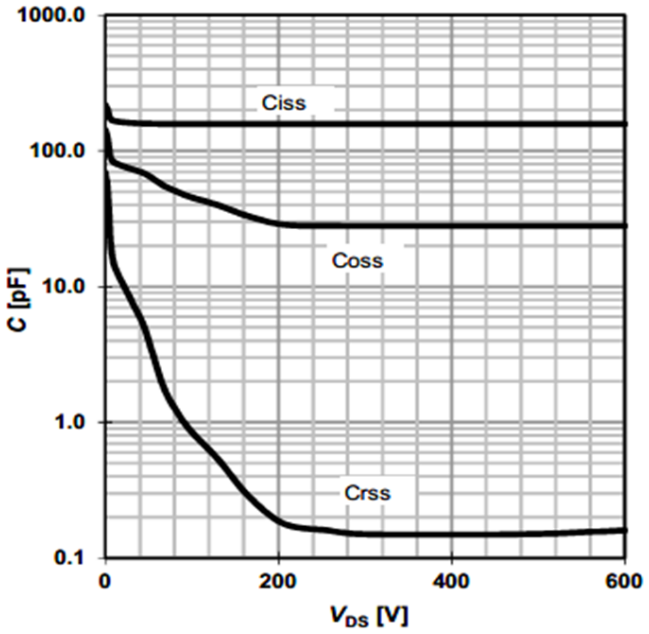


$I_D=f(V_{DS})$; $T_C=25°C$

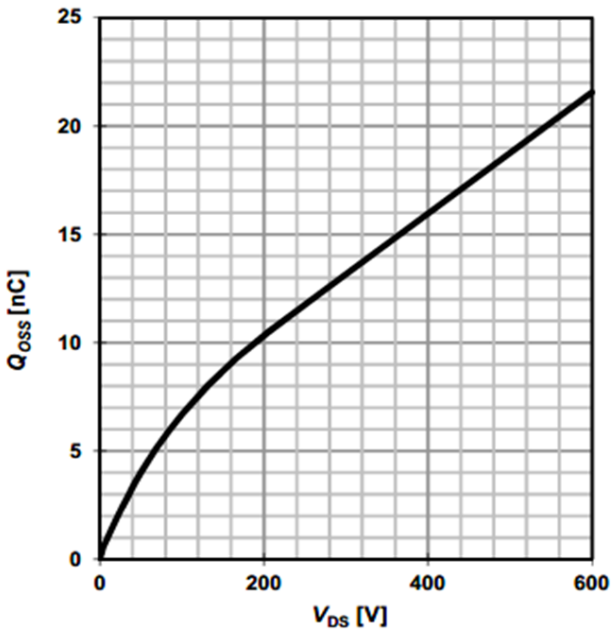


$I_D=f(V_{DS})$; $T_C=125°C$

Figure 13 Safe Operating Area (SOA)



Typical V_{DS}-dependence of terminal capacitances



Typical V_{DS}-dependence of output charge

Figure 14 Terminal capacitances and output charge

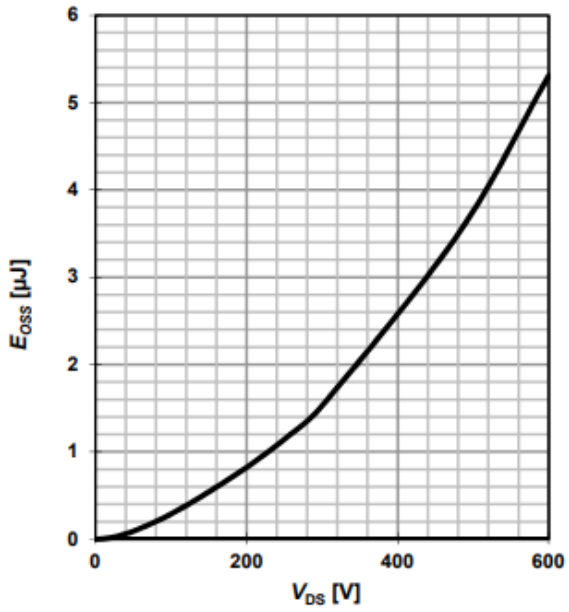
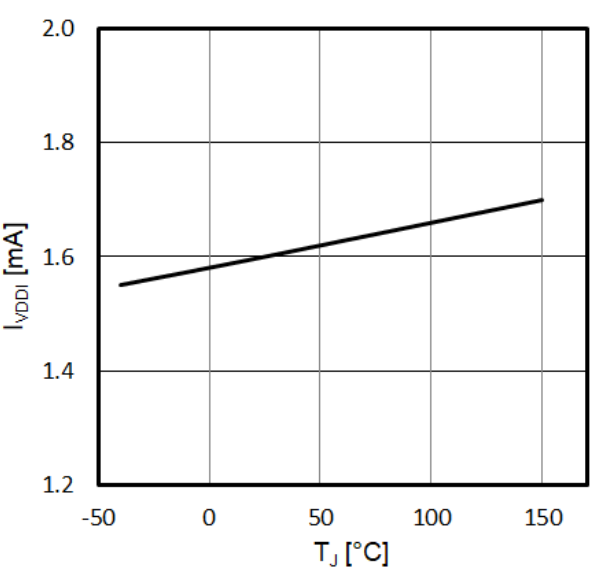
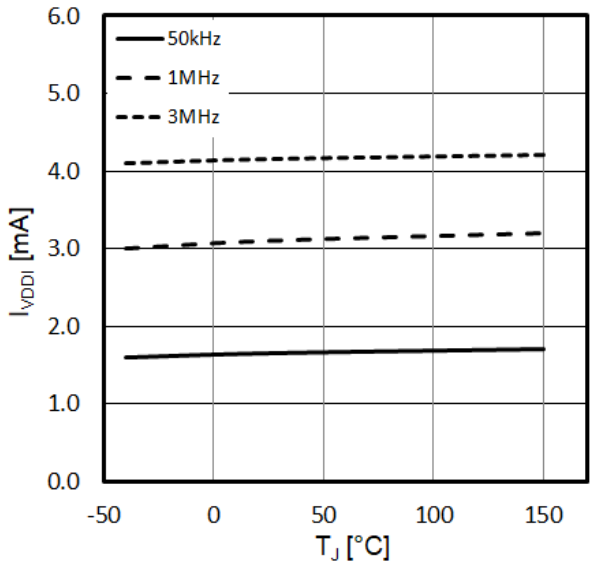


Figure 15 Typical output energy

5.2 Gate driver characteristics

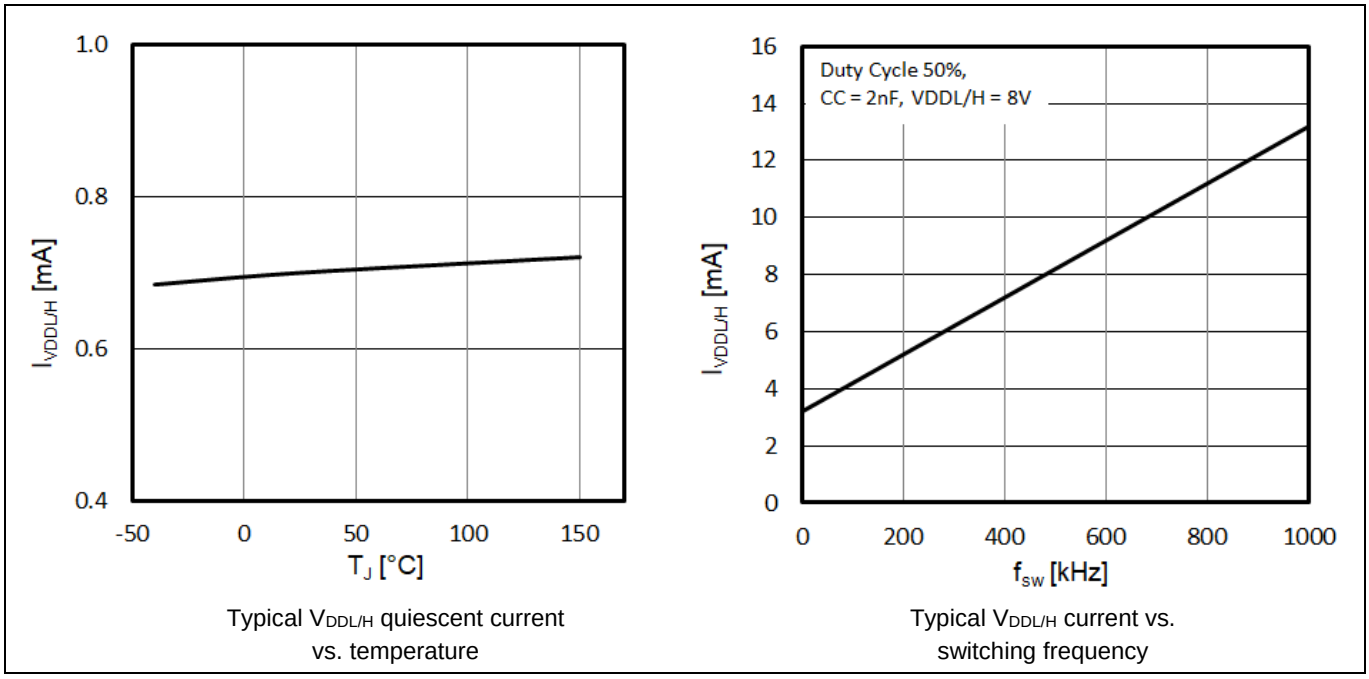


Typical V_{DDI} quiescent current vs. temperature



Typical V_{DDI} current vs. temperature and frequency

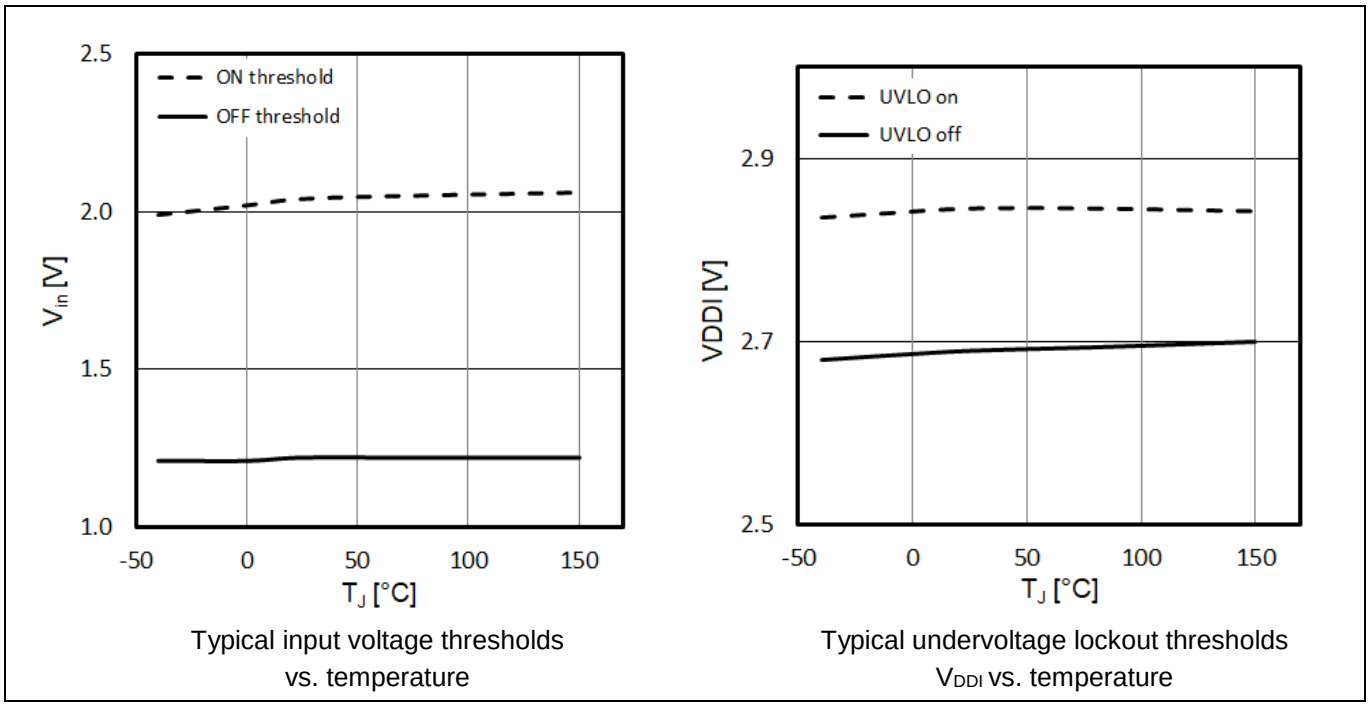
Figure 16 Supply current V_{DDI}



Typical $V_{DDL/H}$ quiescent current vs. temperature

Typical $V_{DDL/H}$ current vs. switching frequency

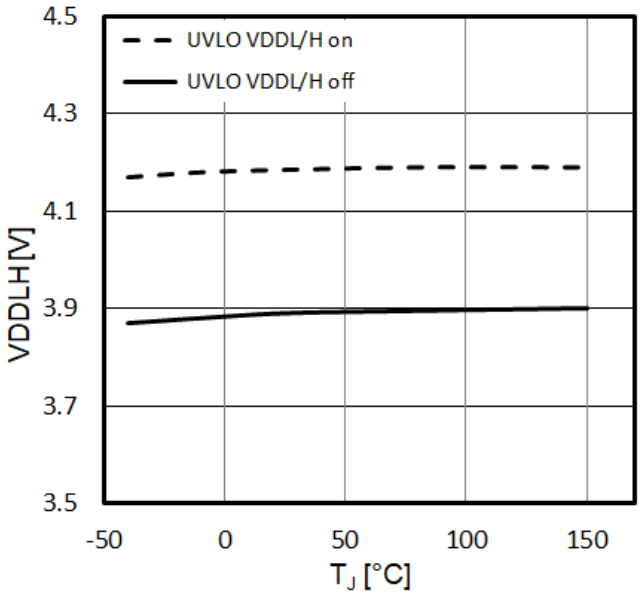
Figure 17 Supply current $V_{DDL/H}$



Typical input voltage thresholds vs. temperature

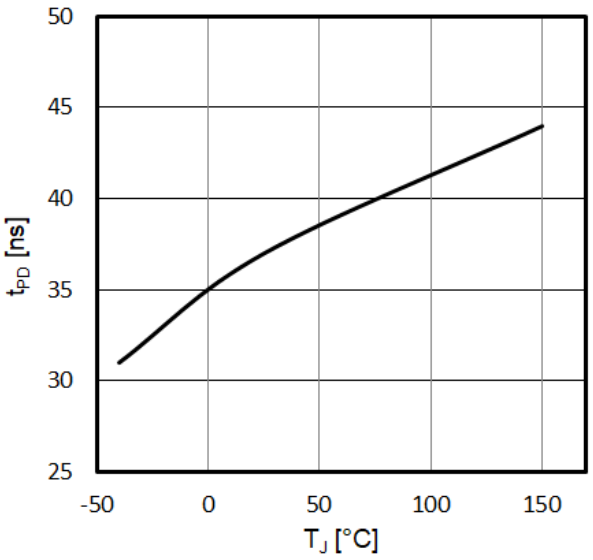
Typical undervoltage lockout thresholds V_{DDI} vs. temperature

Figure 18 Logic input thresholds and V_{DDI} UVLO

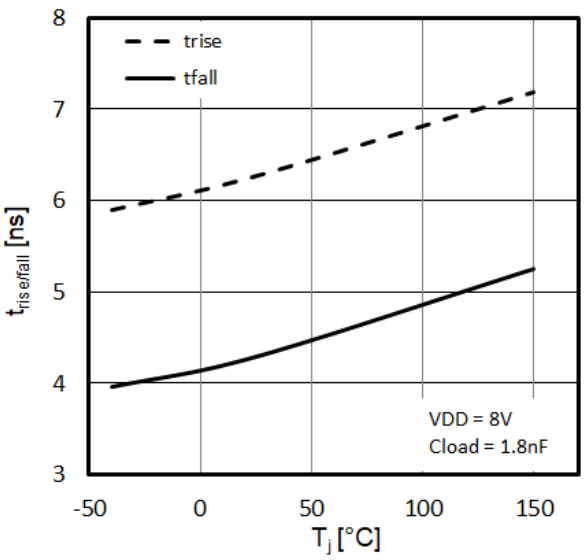


Typical undervoltage lockout thresholds $V_{DDL/H}$ vs. temperature

Figure 19 $V_{DDL/H}$ UVLO



Typical propagation delays vs. temperature



Typical rise and fall time vs. temperature

Figure 20 Propagation delay and rise / fall times

6 Application circuit

Figure 14 shows a typical application of IGI60F140A1L as the primary side switches in an LLC converter. Two integrated power stages are operated from a single 8 V supply, with the high-side supply generated by bootstrapping (diode D_{boot}, capacitance C_{boot} and resistor R_{boot}).

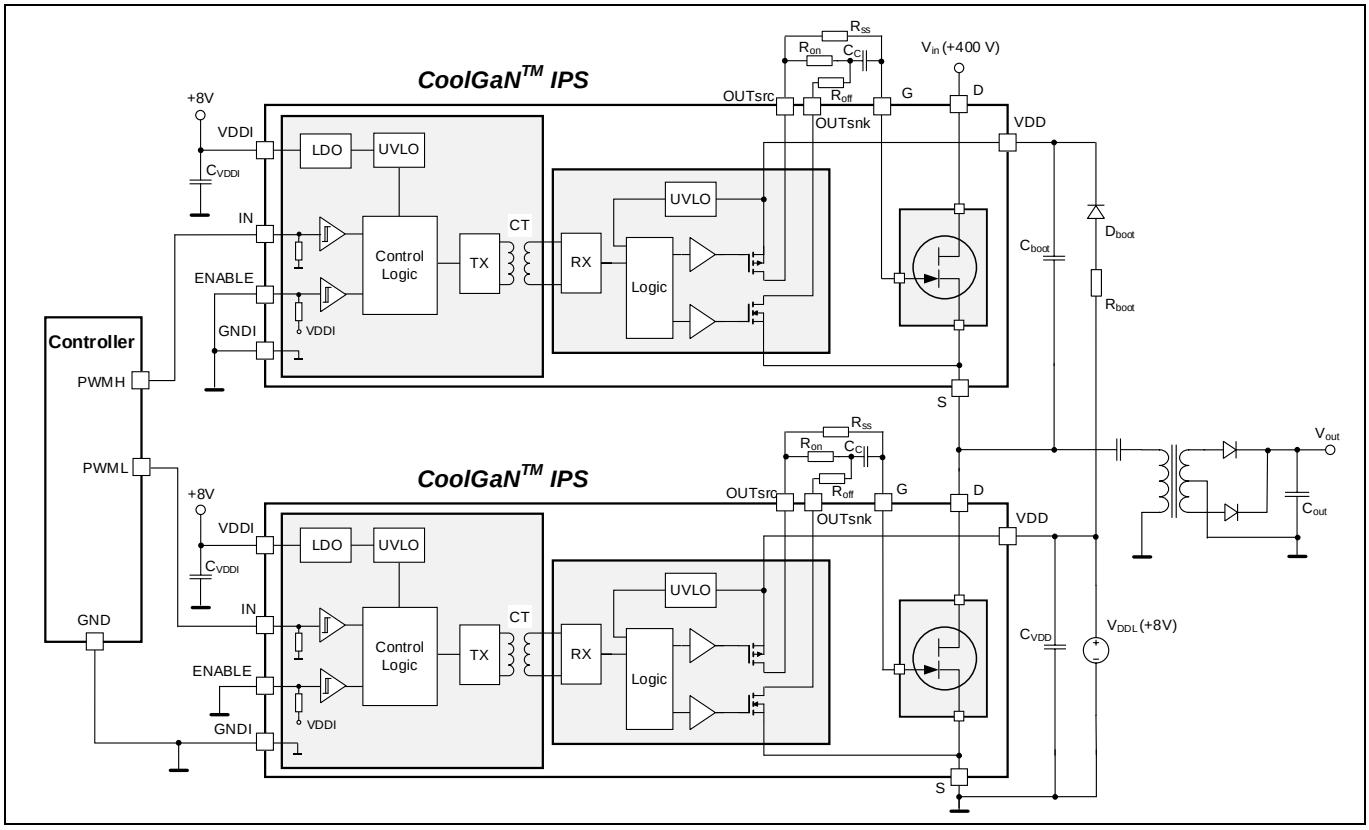
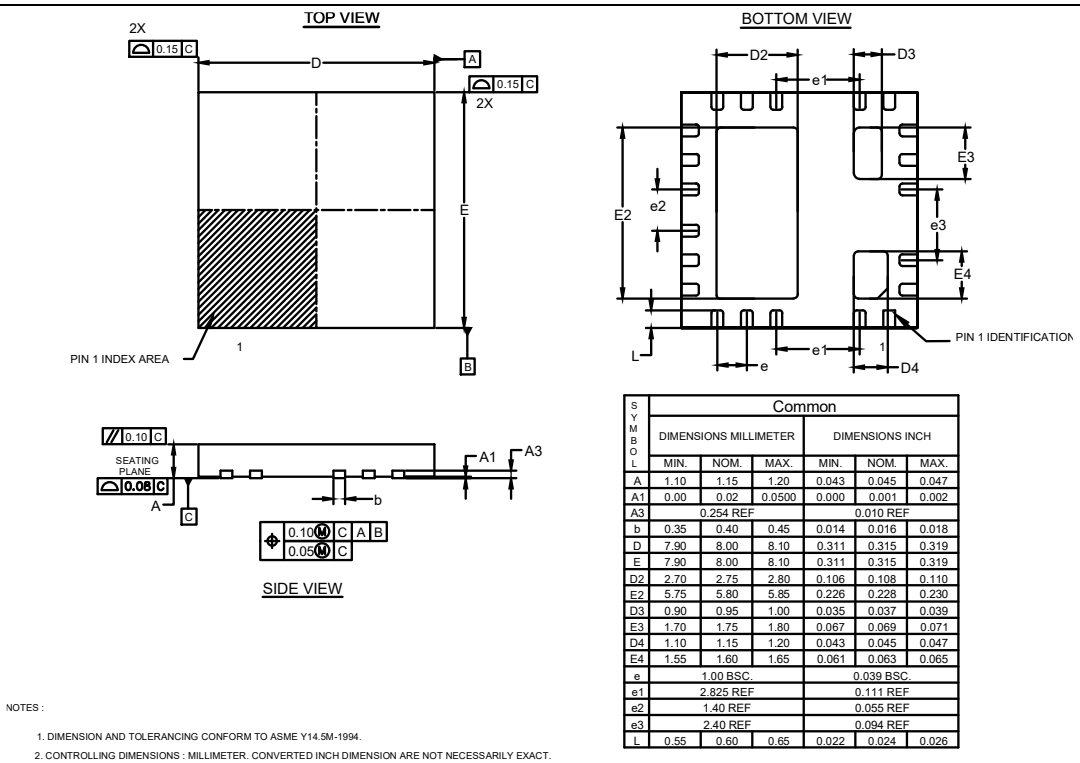


Figure 21 Application of IGI65F140A1L in LLC primary stage

7 Package information



SYMBOL	Common					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.10	1.15	1.20	0.043	0.045	0.047
A1	0.00	0.02	0.0500	0.000	0.001	0.002
A3	0.254 REF			0.010 REF		
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D2	2.70	2.75	2.80	0.106	0.108	0.110
E2	5.75	5.80	5.85	0.226	0.228	0.230
D3	0.90	0.95	1.00	0.035	0.037	0.039
E3	1.70	1.75	1.80	0.067	0.069	0.071
D4	1.10	1.15	1.20	0.043	0.045	0.047
E4	1.55	1.60	1.65	0.061	0.063	0.065
e	1.00 BSC.			0.039 BSC.		
e1	2.825 REF			0.111 REF		
e2	1.40 REF			0.055 REF		
e3	2.40 REF			0.094 REF		
L	0.55	0.60	0.65	0.022	0.024	0.026

Figure 22 TIQFN-21-1 8 x 8mm package outline

Revision history

Document version	Date of release	Description of changes
V1.0	2023-06-07	1st version Final Datasheet

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Edition 2023-06-07

Published by

Infineon Technologies AG

81726 Munich, Germany

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