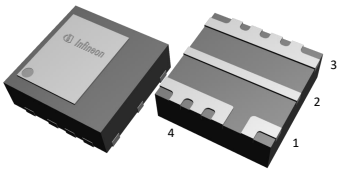
CoolGaN™

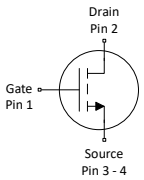
PG-TSON-4

CoolGaN™ Transistor 100 V G3



Features

- Ultra fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade 3x3 package



Top side is exposed silicon substrate, internally connected to source terminal. Not recommended to use as an electrical connection.

Potential applications

- Telecom & Datacenter 48V IBC
- Sync Rectification for AC-DC and DC-DC converters
- Robotics and drones
- Battery powered tools
- 48V servo drive
- e-Mobility, UAVs
- Class D Audio
- Solar & Energy storage systems
- Point of Load Converters

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	9.4	mΩ
I_D	23	A
Q_{oss}	14	nC
Q_G	3.4	nC
Q_{rr}	0	nC

Type / Ordering code	Package	Marking	Related links
IGB110S10S1	PG-TSON-4	BA1	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	V_{GS}=0 V
Pulsed drain-source voltage [1]	$V_{DS,\ pulse}$	-	-	120	V	V_{GS}=0 V, 1 h total time
Continuous drain current	I_D	-	-	23 9.0	A	V_{GS}=5 V, T_C=25 °C V_{GS}=5 V, T_A=25 °C, R_{thJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	210 97	A	T_j=25 °C T_j=150 °C
Pulsed gate-source voltage [1]	V_{GS}	-6.5	-	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	15 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 °C/W [2]
Storage temperature	T_{stg}	-55	-	150	°C	-
Junction temperature	T_j	-40	-	150	°C	

1) Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

2) Device on 4-layer FR4 PCB, vertical in still air.

3) Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	1.4	1.7	°C/W	-
Thermal resistance, junction - case, bottom	R_{thJC}	-	5.6	8.1	°C/W	
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	70	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	50	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical Characteristics

at T_j=25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	2.0	2.9	V	V_{DS}=V_{GS}, I_D=3.0 mA
Drain-source leakage current	I_{DSS}	-	0.1 2.0	0.5 20	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	5.0 0.003 40 0.003	50 0.009 370 0.012	µA	V_{GS}=5 V, T_j=25 °C V_{GS}=-4 V, T_j=25 °C V_{GS}=5 V, T_j=125 °C V_{GS}=-4 V, T_j=125 °C
Drain-source on-state resistance	$R_{DS(on)}$	-	9.4	11	mΩ	V_{GS}=5 V, I_D=10 A
Gate resistance [4]	R_G	-	0.5	-	Ω	-

[4] Defined by design. Not subject to production test.

Table 6 Capacitance characteristics [5]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	300	340	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance	C_{oss}	-	140	150	pF	
Reverse transfer capacitance	C_{rss}	-	2.3	3.0	pF	

[5] Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.0	-	nC	V_{DS}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Gate charge at threshold	$Q_{g(th)}$	-	0.7	-	nC	
Gate to drain charge [6]	Q_{gd}	-	0.9	-	nC	
Switching charge	Q_{sw}	-	1.2	-	nC	
Gate charge total [6]	Q_g	-	3.4	4.4	nC	
Gate plateau voltage	$V_{plateau}$	-	2.8	-	V	
Output charge [6]	Q_{oss}	-	14	15	nC	V_{DS}=50 V, V_{GS}=0 V

[6] Defined by design. Not subject to production test.

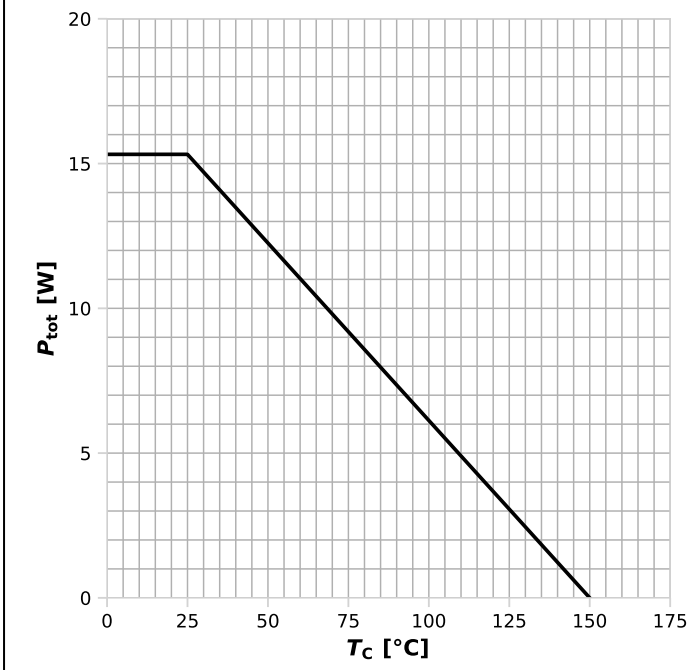
Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	5.0	A	T_C=25 °C
Pulsed current, reverse	$I_{S,pulse}$	-	-	92	A	
Source-Drain reverse voltage	V_{SD}	-	2.6 2.2	3.4 -	V	V_{GS}=0 V, $I_{S,pulse}$=10 A, T_j=25 °C V_{GS}=0 V, $I_{S,pulse}$=0.5 A, T_j=25 °C
Reverse recovery charge [7)]	Q_{rr}	-	0	-	nC	V_R=50 V, $I_{S,pulse}$=10 A, d$i_{S,pulse}$/dt =100 A/µs

7) Defined by design. Not subject to production test.

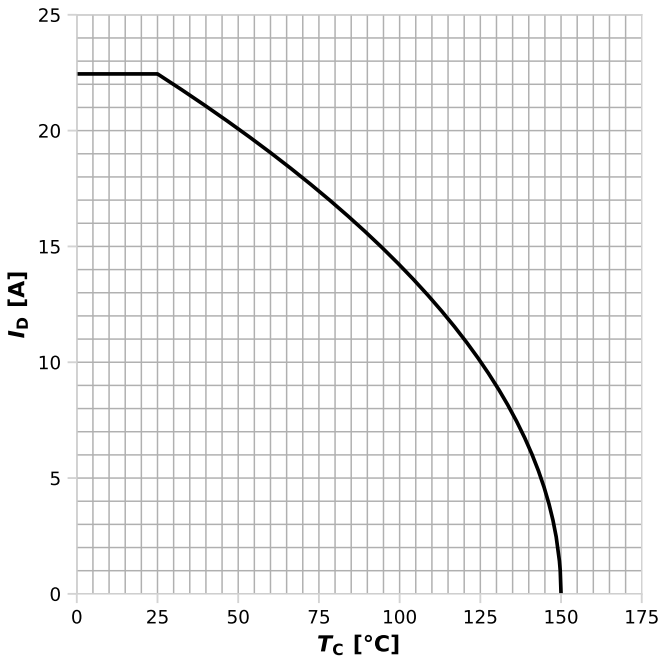
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



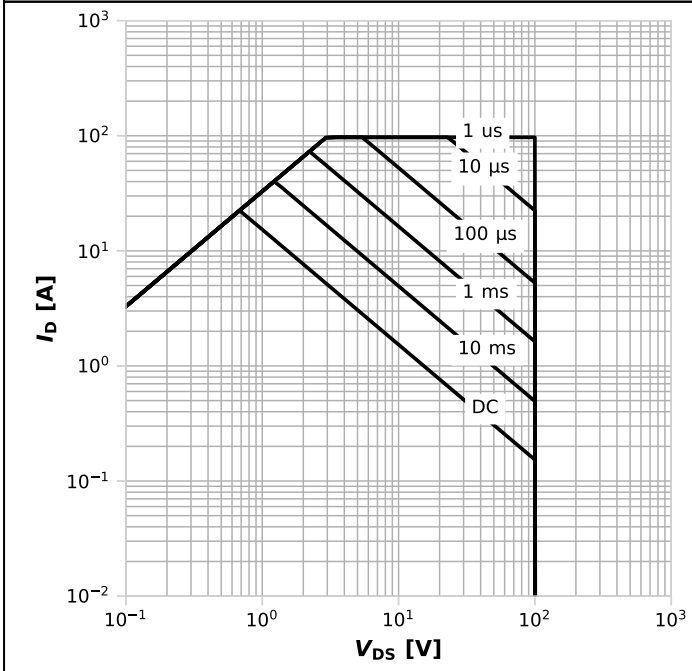
P_{tot}=f(T_C)

Diagram 2: Drain Current



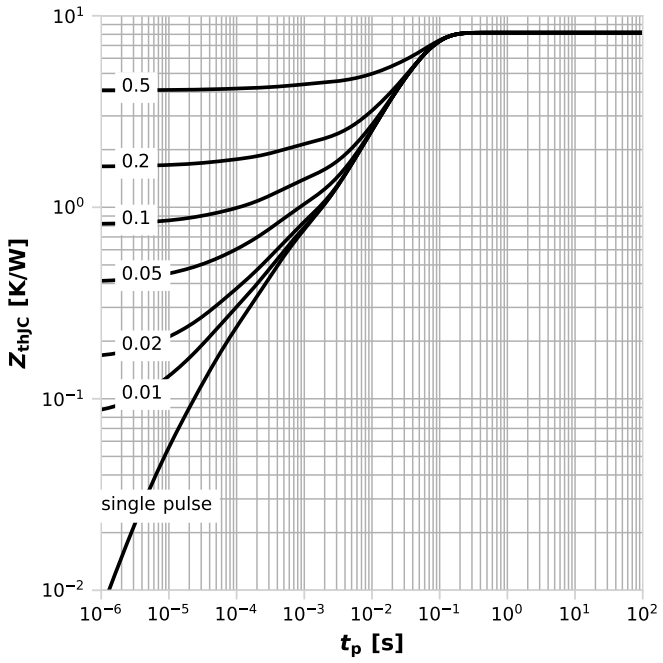
I_D=f(T_C)

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

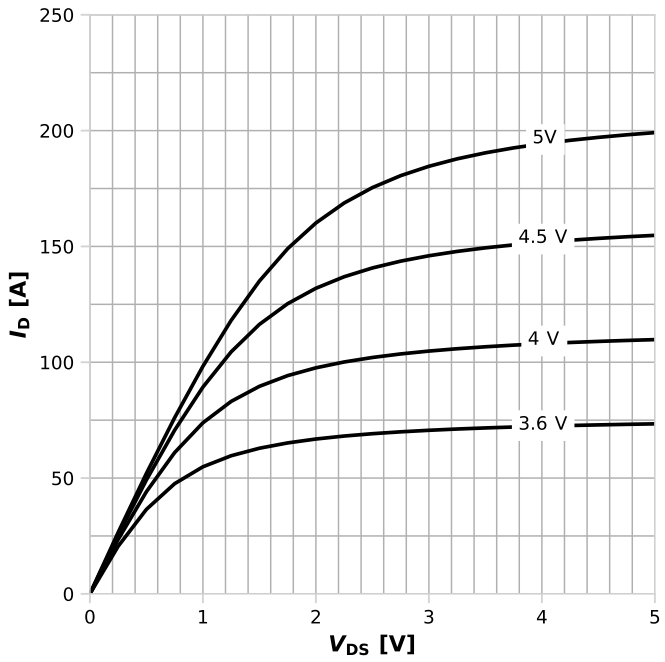
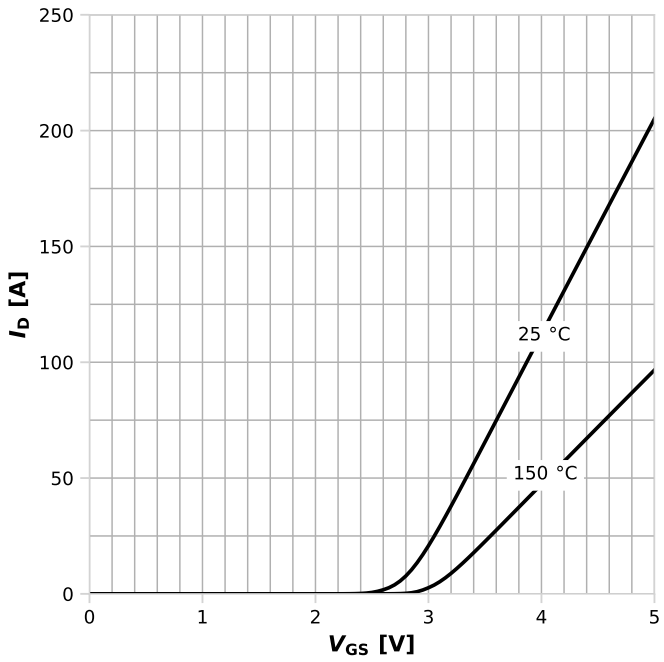
Diagram 5: Typ. output characteristics	Diagram 6: Typ. transfer characteristics
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

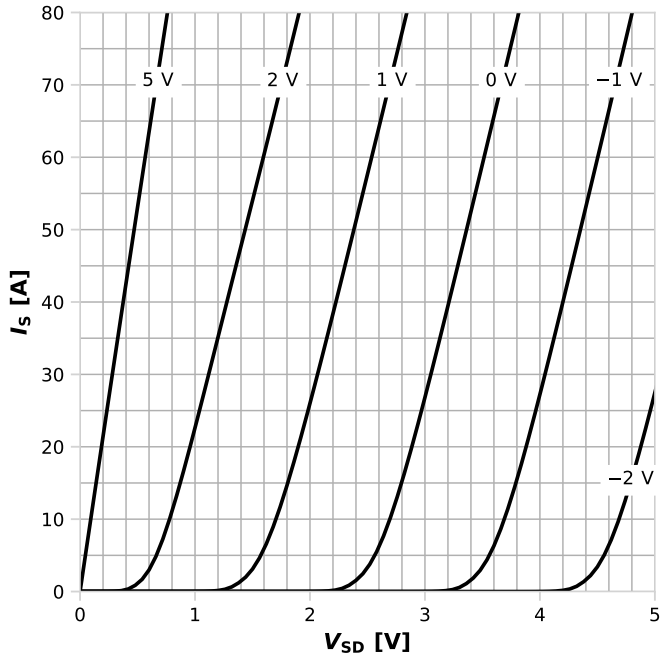
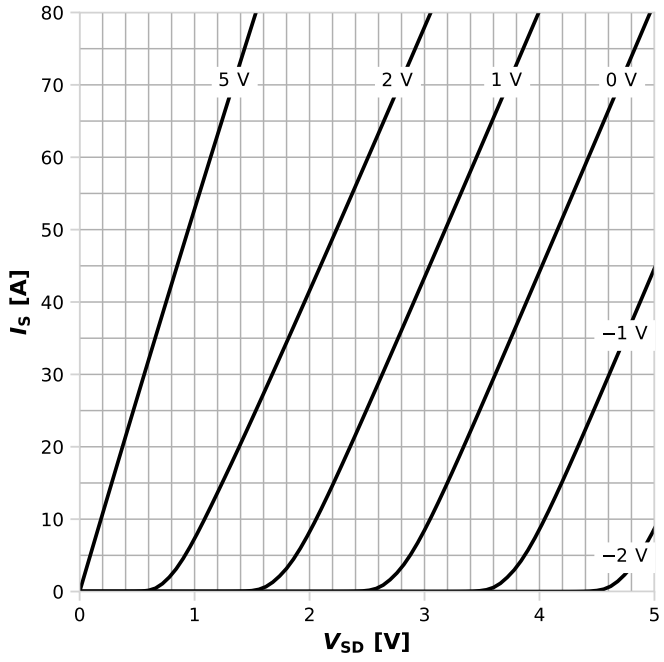
Diagram 7: Typ. channel reverse characteristics	Diagram 8: Typ. channel reverse characteristics
	
I_S=f(V_{SD}); T_j=25 °C; parameter: V_{GS}	I_S=f(V_{SD}); T_j=125 °C; parameter: V_{GS}

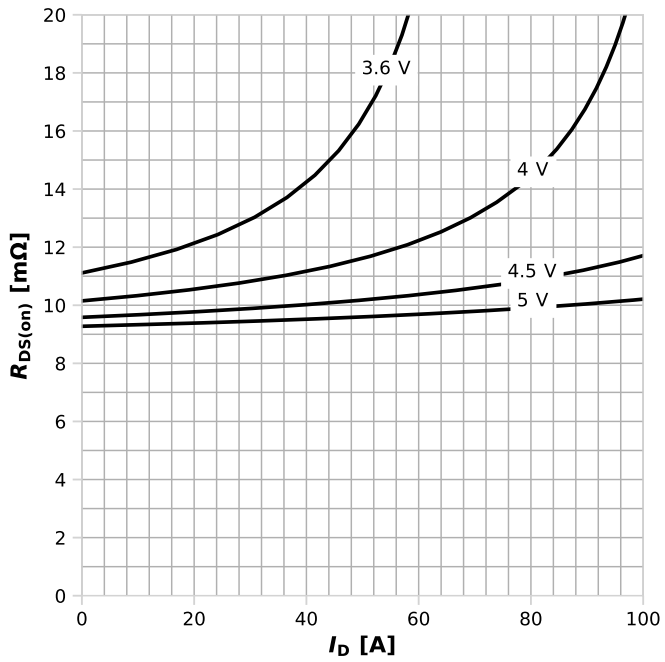
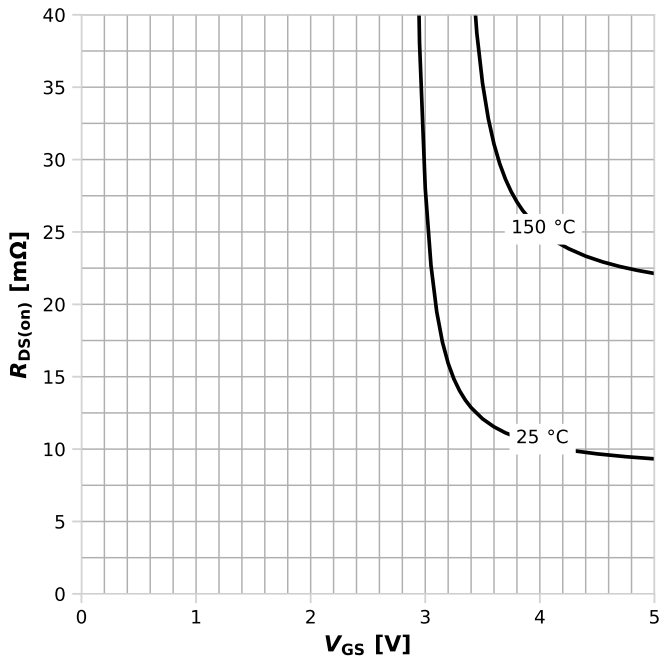
Diagram 9: Typ. drain-source on-state resistance	Diagram 10: Typ. Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(V_{GS}); I_D=10 A; parameter: T_j

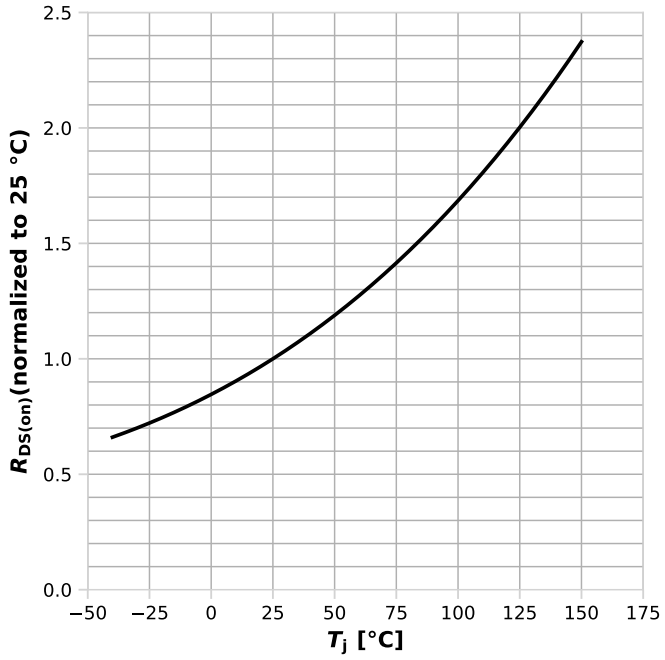
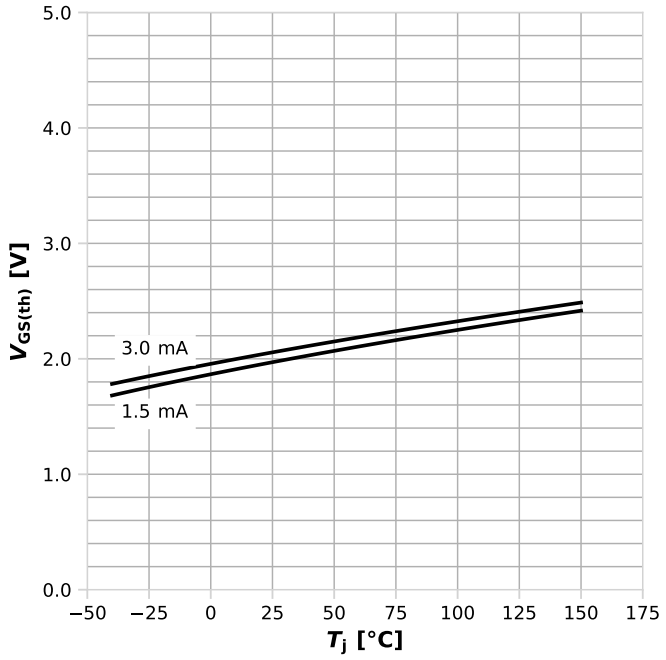
Diagram 11: Drain-source on-state resistance	Diagram 12: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=10 A, V_{GS}=5V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

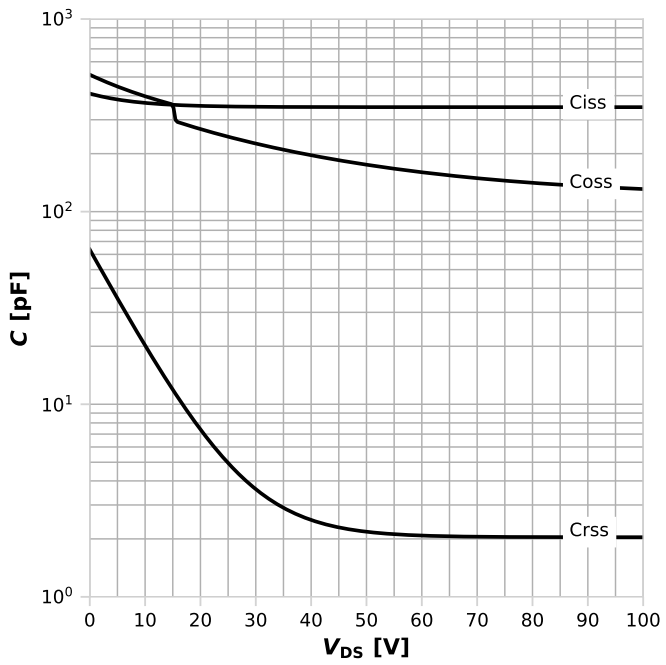
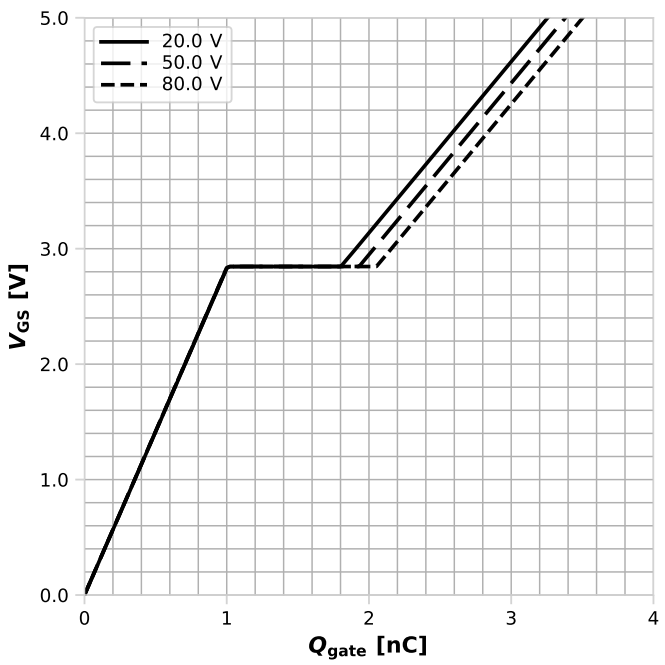
Diagram 13: Typ. capacitances	Diagram 14 Typ. gate charge
	
C=f(V_{DS}); V_{GS}=0 V	V_{GS}=f(Q_{gate}); I_D=10 A pulsed; parameter: V_{DS}

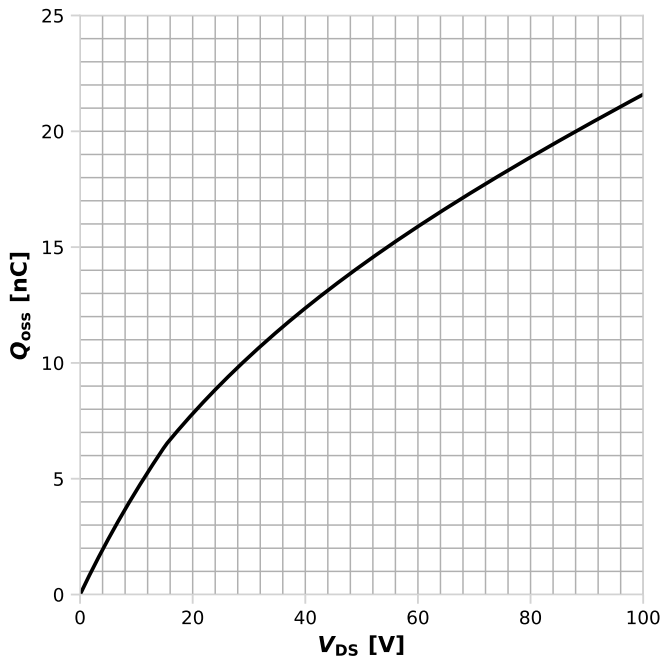
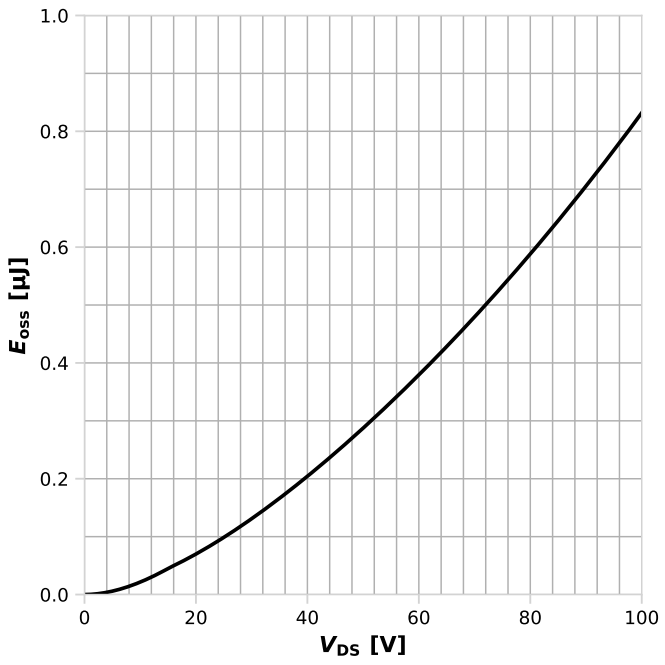
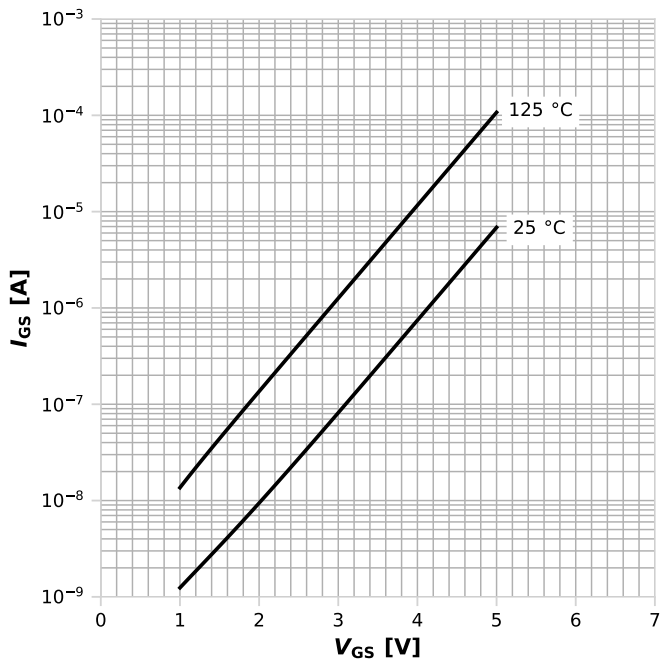
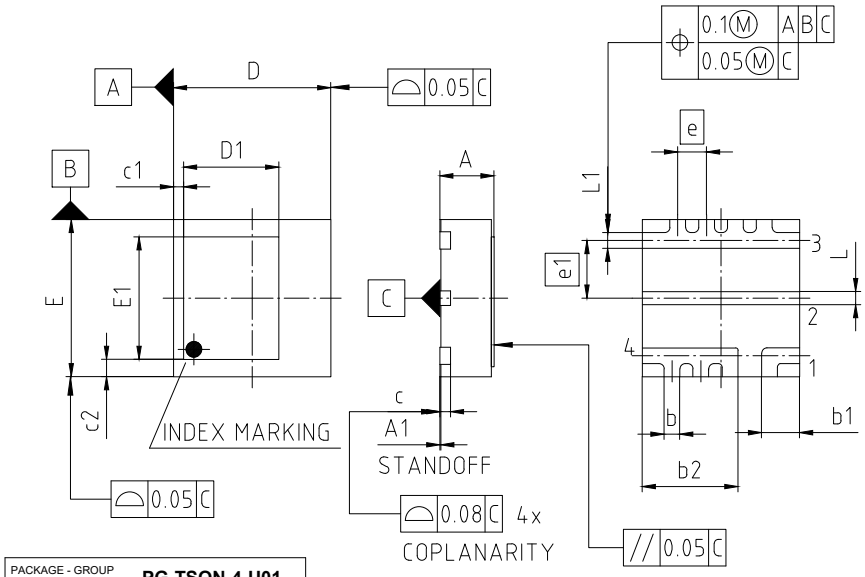
Diagram 15: Typ. output charge	Diagram 16: Typ. Coss stored Energy
	
Q_{oss}=f(V_{DS}), V_{GS}=0 V	E_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 17: Typ. gate characteristics forward



I_{GS}=f(V_{GS}); V_{DS}=0 V; parameter: T_j

6 Package outlines



PACKAGE - GROUP NUMBER:	PG-TSON-4-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A		1.032
A1	0	0.05
b	0.20	0.40
b1	0.715	0.735
b2	1.815	1.835
c		0.20
c1	0.192	
c2	0.332	
D	2.90	3.10
D1	1.716	1.916
E	2.90	3.10
E1	2.236	2.436
L	0.20	0.30
L1	0.25	0.35
e	0.55	
e1	1.10	
N	4	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSON-4, dimensions in mm

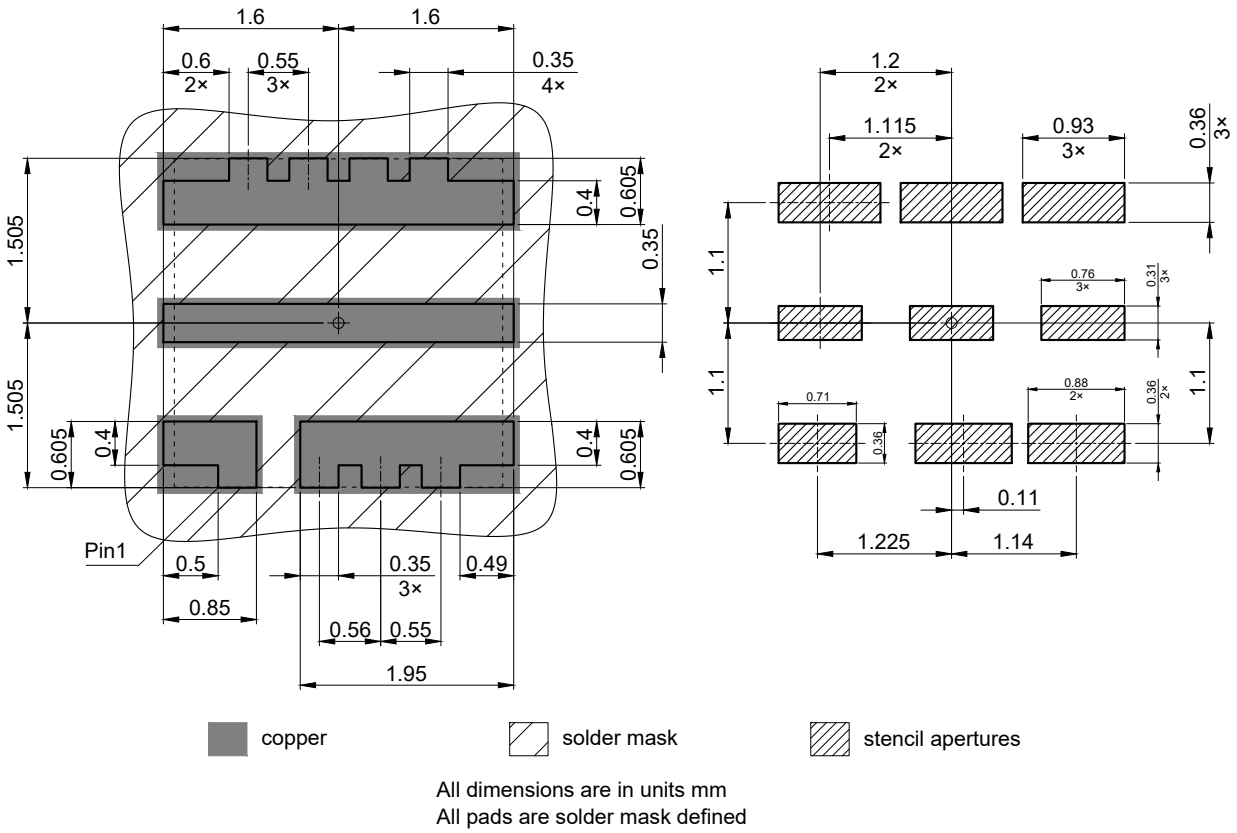


Figure 2 Footprint drawing PG-TSON-4, dimensions in mm

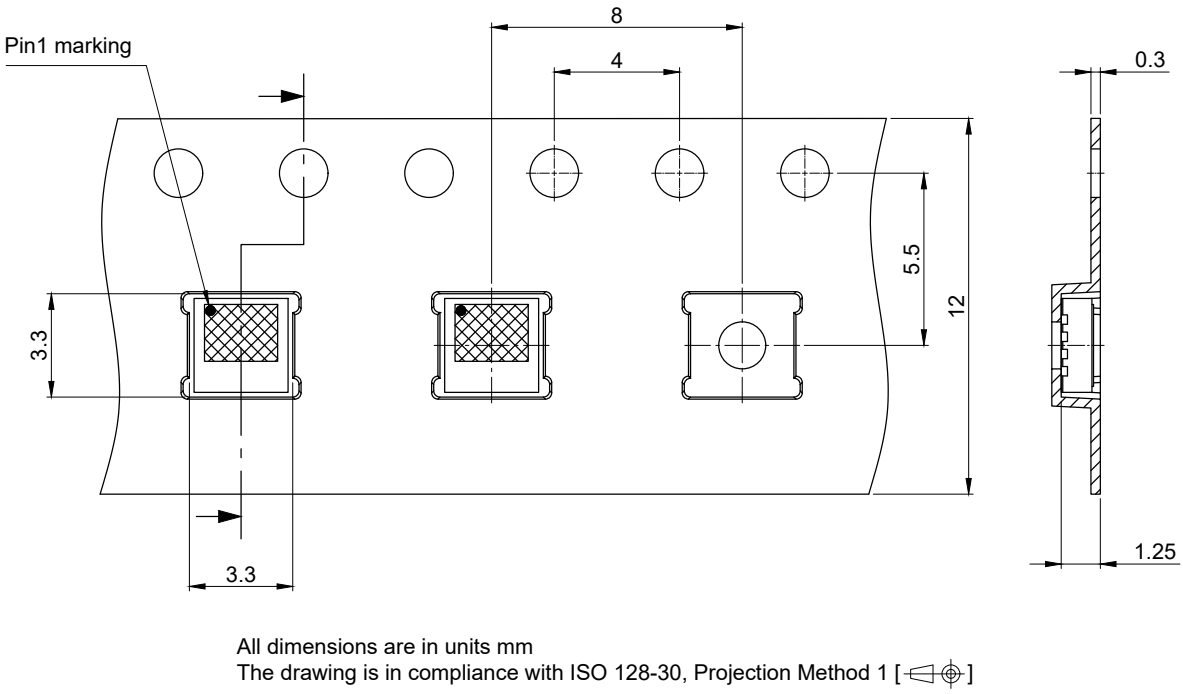


Figure 3 Packaging variant PG-TSON-4, dimensions in mm

7 Appendix A

Table 9 Related links

- IFX CoolGaN™ GaN webpage
- IFX CoolGaN™ reliability white paper
- IFX CoolGaN™ gate driver application note
- IFX CoolGaN™ Evaluation Boards
- IFX Packages Description-PG-TSON-4-2

Revision history

IGB110S10S1

Revision 2024-12-13, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-12-13	Release of final version

Published by
Infineon Technologies AG
81726 München, Germany

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:

IGB110S10S1XTMA1