

OptiMOS™ -5 Power Transistor



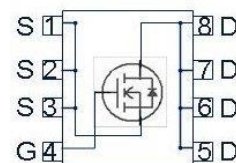
Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	14	mΩ
I_D	30	A

PG-TSDSON-8-32



Type	Package	Marking
IAUZ30N06S5L140	PG-TSDSON-8-32	5N6L140

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	30	A
		$V_{GS}=10\text{ V}$, DC current	30	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,3)}	8	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	85	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=15\text{ A}$	27	mJ
Avalanche current, single pulse	I_{AS}	-	30	A
Gate source voltage	V_{GS}	-	± 16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	33	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	4.6	K/W
Thermal resistance, junction - ambient ³⁾	R_{thJA}	-	-	37.2	-	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=10\mu A$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=15A$	-	16.3	19.6	m Ω
		$V_{GS}=10V, I_D=15A$	-	11.2	14	
Gate resistance ²⁾	R_G	-	-	1.4	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=30V,$ $f=1MHz$	-	683	888	pF
Output capacitance	C_{oss}		-	136	177	
Reverse transfer capacitance	C_{rss}		-	10	15	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $I_D=15A, R_{G,ext}=3.5\Omega$	-	1.6	-	ns
Turn-off delay time	$t_{d(off)}$		-	4.1	-	
Rise time	t_r		-	1.0	-	
Fall time	t_f		-	1.8	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=30V, I_D=15A,$ $V_{GS}=0 \text{ to } 10V$	-	2.3	2.9	nC
Gate to drain charge	Q_{gd}		-	1.6	2.4	
Gate charge total	Q_g		-	9.4	12.2	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	30	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25^\circ C, t_p=100\mu s$	-	-	85	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=15A,$ $T_J=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30V, I_F=30A,$ $di_F/dt=100A/\mu s$	-	26	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	18	-	nC

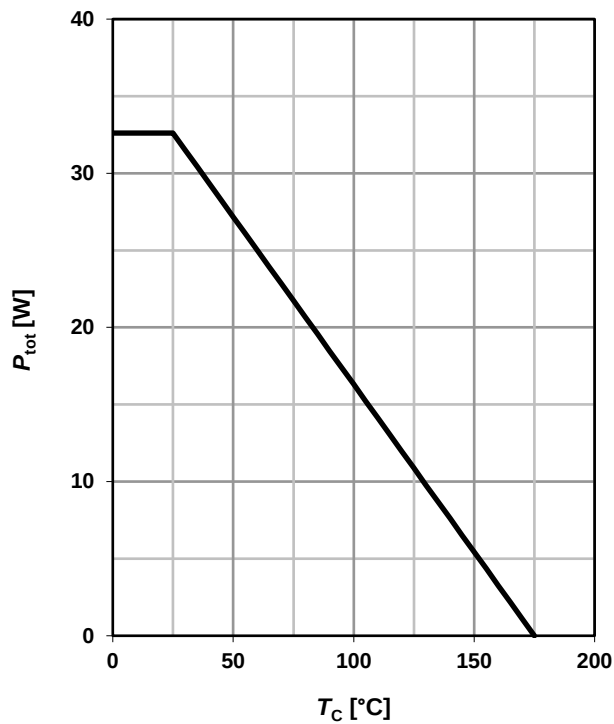
¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production test - verified by design/characterization.

³⁾ Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

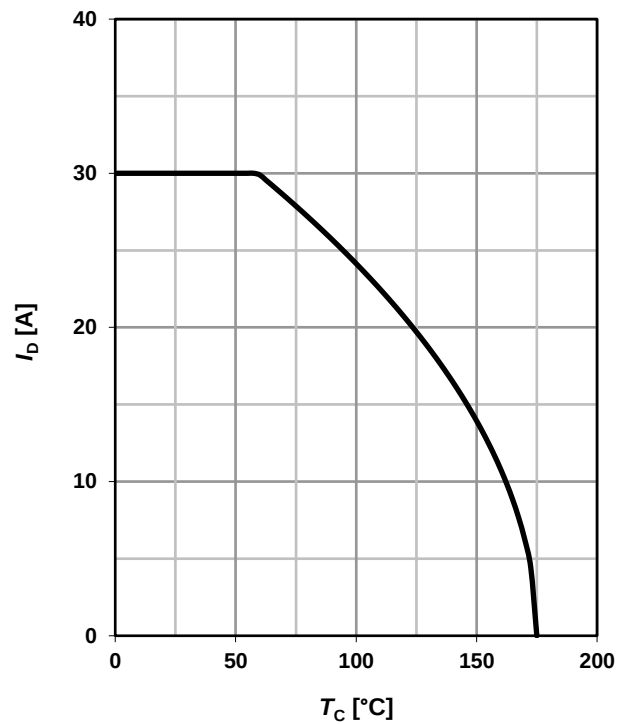
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

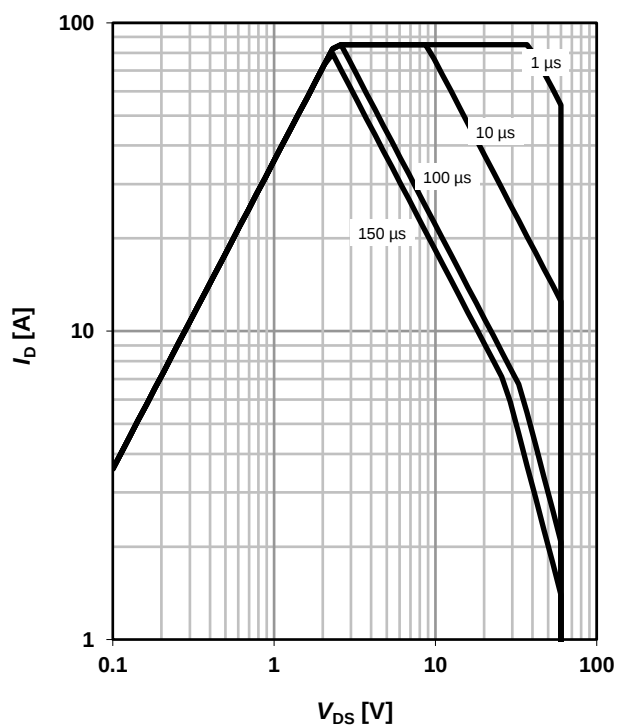
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

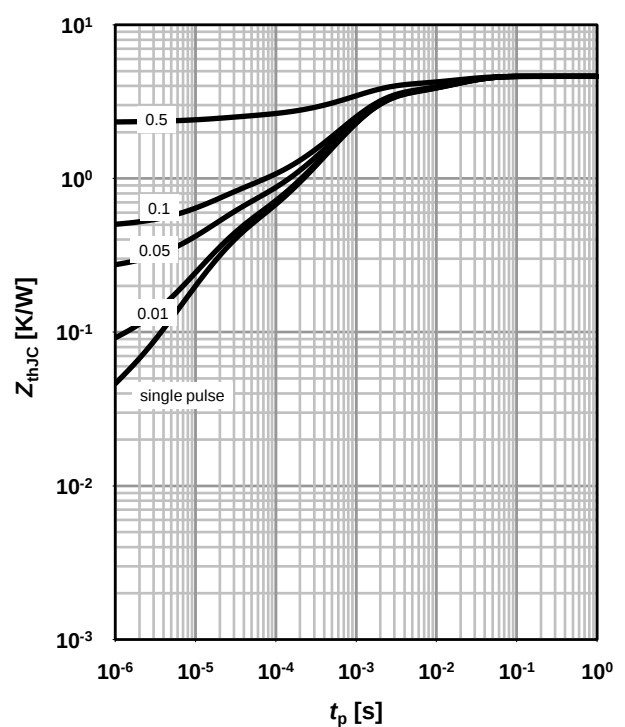
parameter: t_p



4 Max. transient thermal impedance

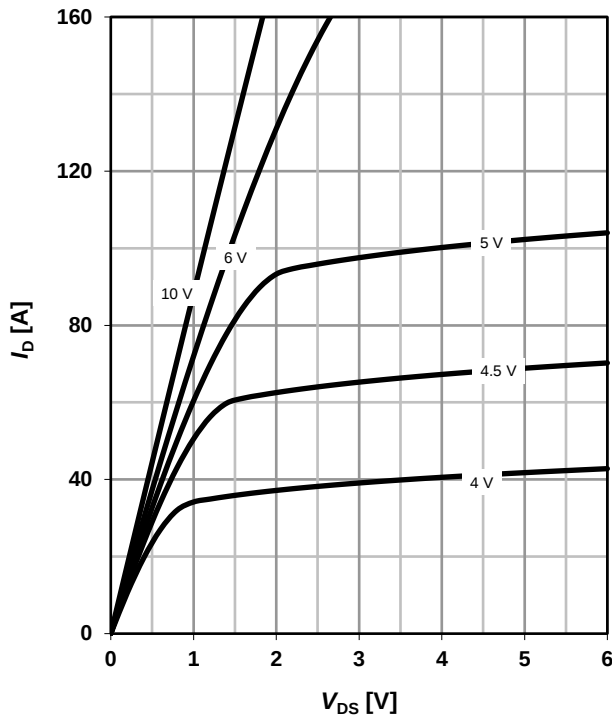
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



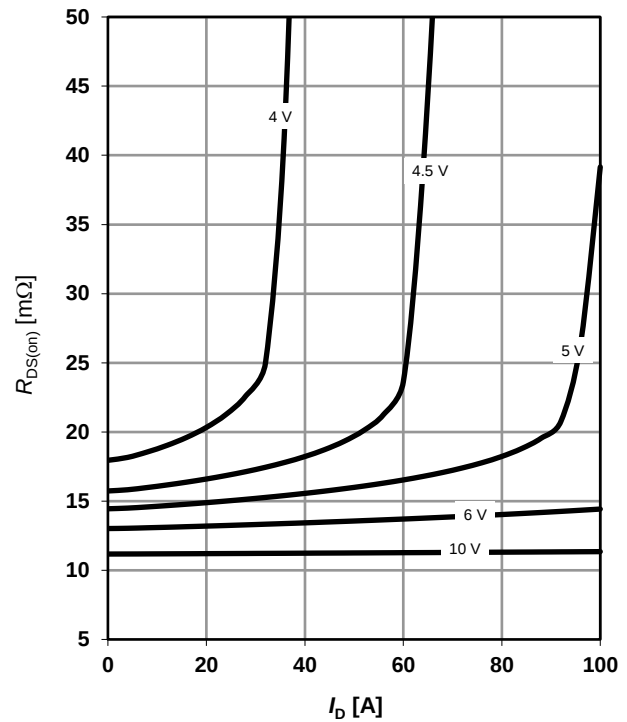
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


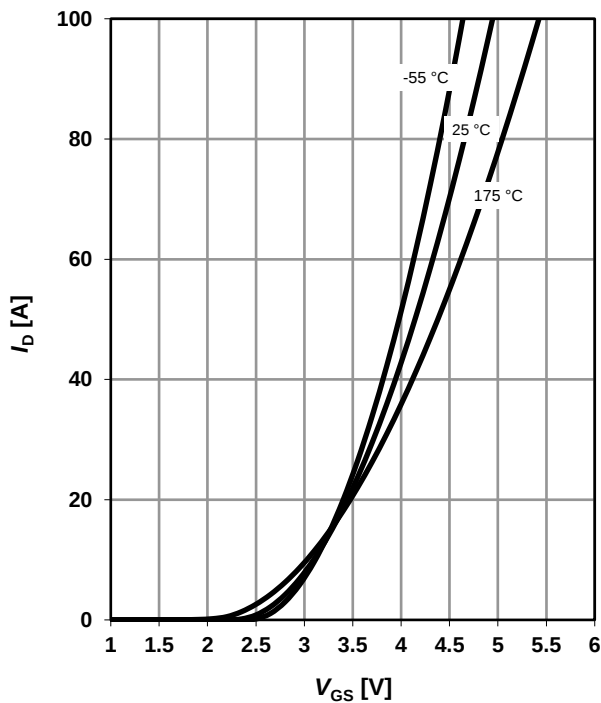
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


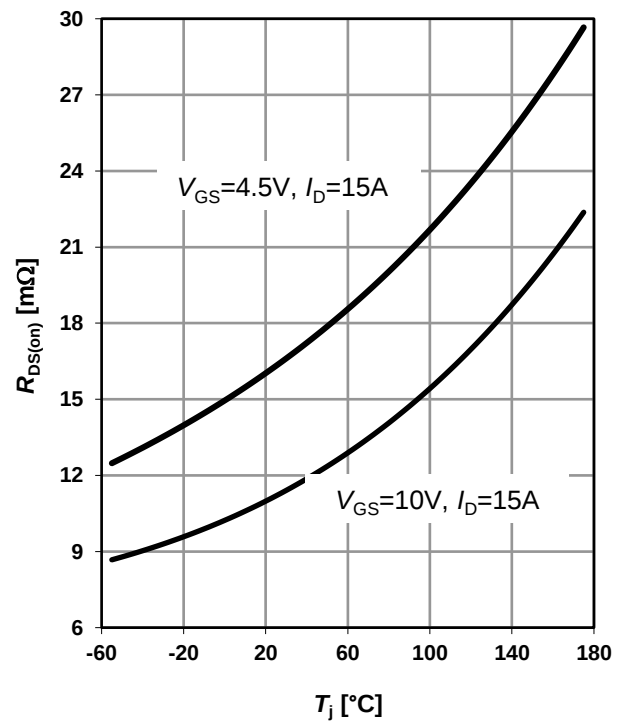
7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


8 Typ. drain-source on-state resistance

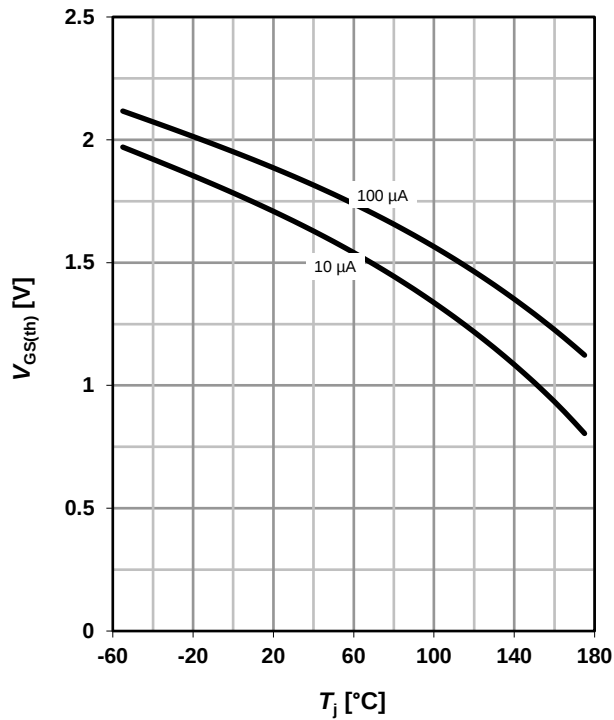
 $R_{DS(on)} = f(T_j);$

parameter: I_D, V_{GS}


9 Typ. gate threshold voltage

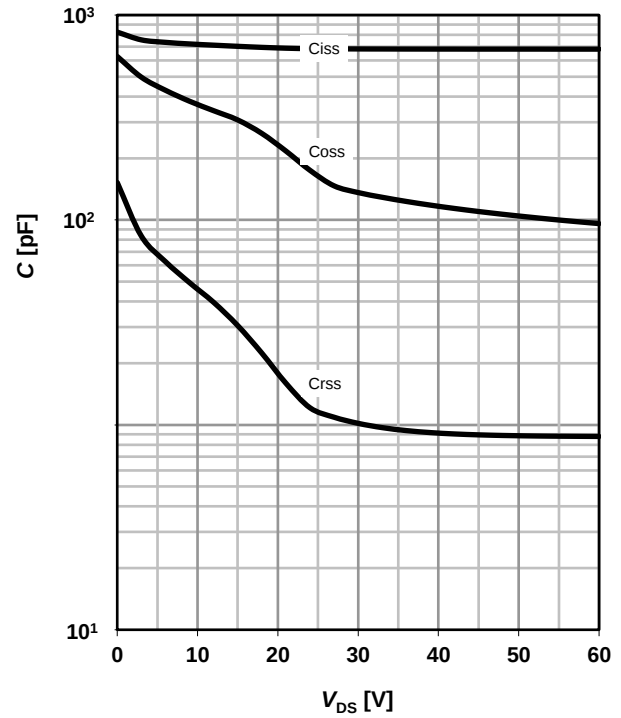
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

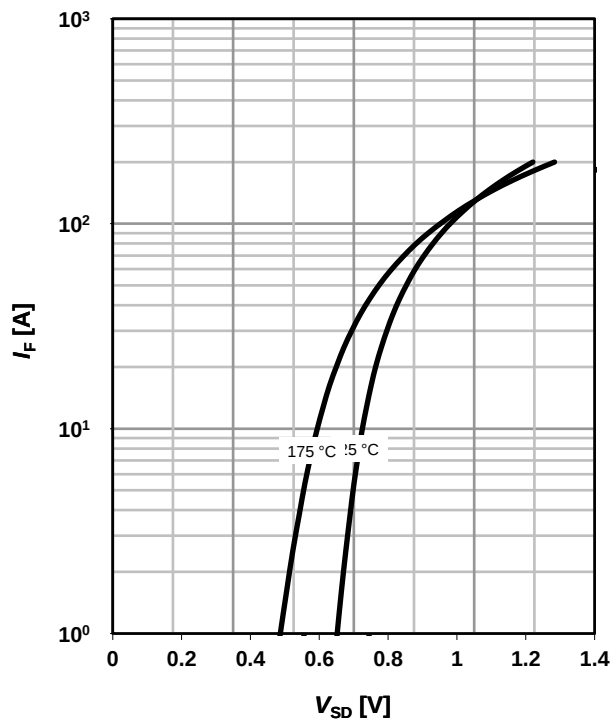
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

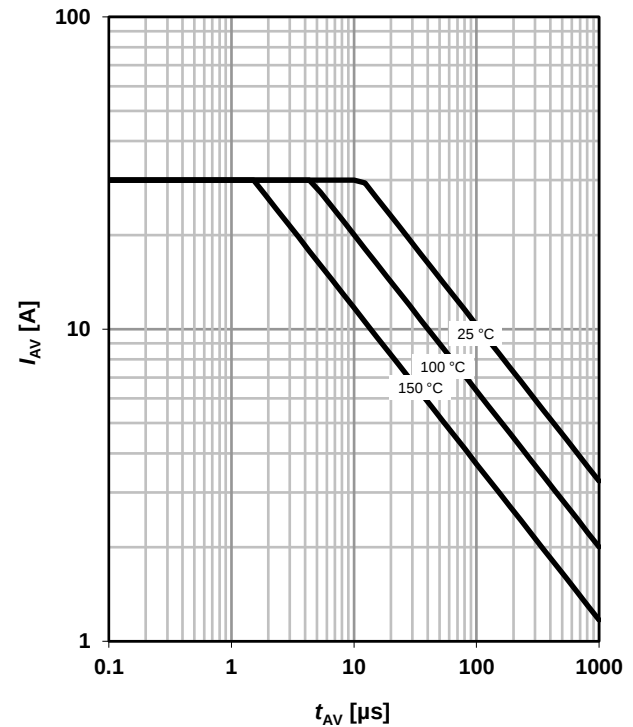
parameter: T_j



12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

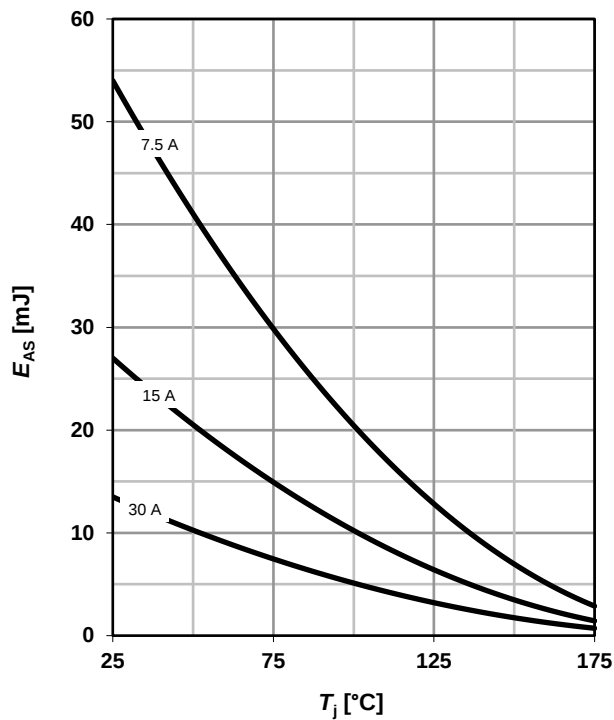
parameter: $T_{j(start)}$



13 Avalanche energy

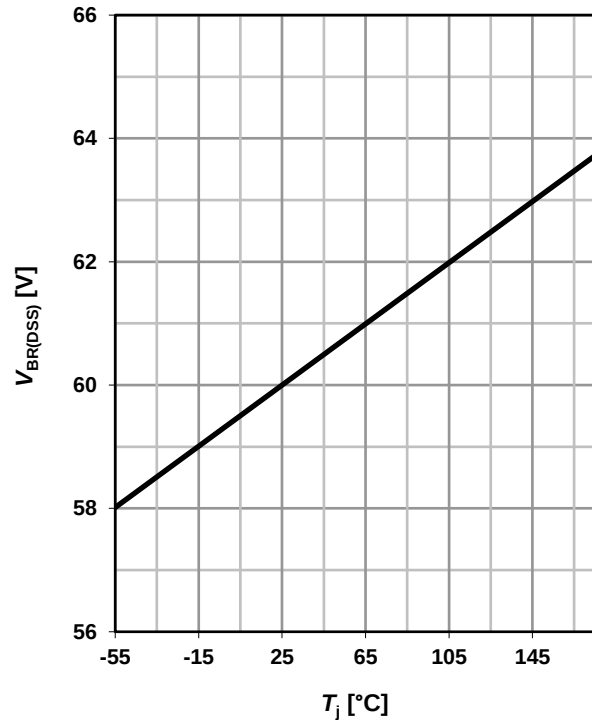
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

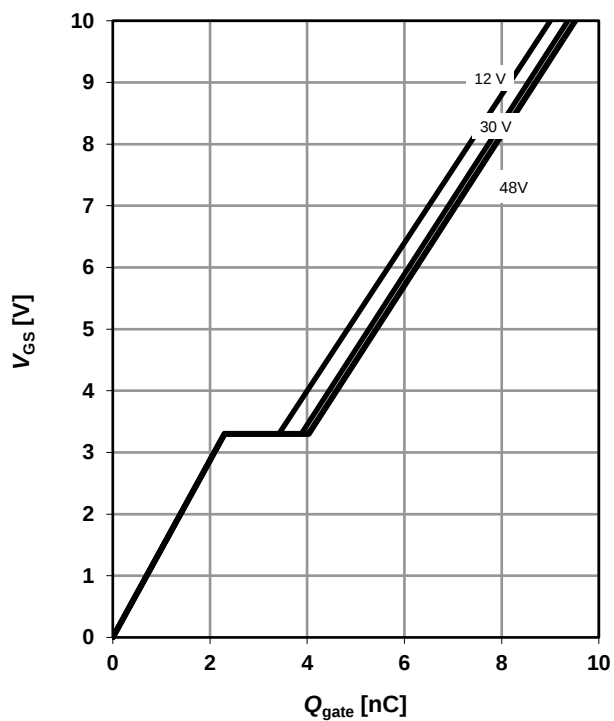
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



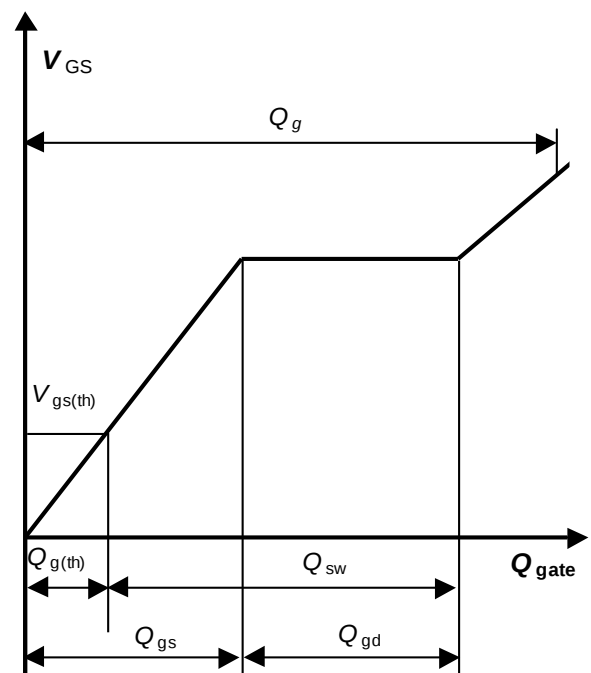
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 15 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of a PCB showing top, bottom, and side views with dimensions and a coordinate system.

Top View: A square board with overall dimensions of 3.3 by 3.3. A central square area is defined by a 1.85 by 1.45 footprint. A 0.25 gap is shown between the central area and the board edge. A 0.07 Min dimension is indicated at the bottom edge.

Bottom View: Shows the underside of the board. The central square area is 2.29 by 2.11. The board thickness is 0.4. A 0.05 Min dimension is indicated at the bottom edge. A 0.65 dimension is shown for the central area, and a 0.34 dimension is shown for the bottom edge. A coordinate system is shown with Pin 1 at the bottom right corner.

Side View: Shows the profile of the board. The total thickness is 1.0. The central area has a thickness of 0.05. The board has a 0.2 thickness at the top and bottom edges. A 0.1 dimension is shown for the central area.

Dimensions:

- Top View: 3.3 (width), 3.3 (height), 1.85 (central width), 1.45 (central height), 0.25 (gap), 0.07 Min (bottom edge).
- Bottom View: 2.29 (width), 2.11 (height), 0.4 (thickness), 0.05 Min (bottom edge), 0.65 (central width), 0.34 (bottom edge).
- Side View: 1.0 (total thickness), 0.2 (top/bottom thickness), 0.1 (central area thickness), 0.05 (central area thickness).

Technical drawing of a rectangular plate with dimensions and labels. The drawing includes a top view and a side view. The top view shows a rectangular plate with a width of 12 and a length of 8. There are six circular holes along the top edge, with a center-to-center distance of 3.6 between the first and second holes. The first hole has a diameter of 0.3. The plate has a thickness of 3.6. The side view shows the plate's profile with a thickness of 3.6 and a top edge that is slightly curved. The label 'PIN 1' points to the first hole, and 'INDEX MARKING' points to the first hole's center. The drawing is labeled '12' at the bottom right.

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History

Version	Date	Changes
Revision 1.0	07.05.2020	Final Data Sheet
Revision 1.1	18.03.2021	Modified package outline and footprint

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