

OptiMOS™-5 Power-Transistor



Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Quality Features

- Infineon Automotive Quality
- Extended qualification beyond AEC Q101
- Enhanced testing
- Advanced adhesion against delamination
- Complementary testing for board level reliability



Advanced
adhesion



Robust

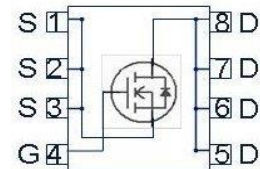
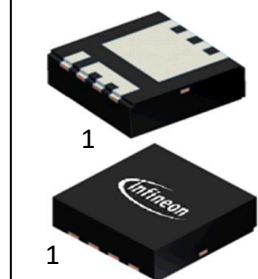


Enhanced
tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	30	mΩ
I_D	20	A

PG-TSDSON-8



Type	Package	Marking
IAUZ20N08S5L300	PG-TSDSON-8	5N8L300

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{ V}$	20	A
		$T_C=100\text{ °C}, V_{GS}=10\text{ V}^{1)}$	14	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	80	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=10\text{ A}$	20	mJ
Avalanche current, single pulse	I_{AS}	-	10	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	30	W
Operating and storage temperature	T_J, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	5	K/W
Thermal resistance, junction - ambient ²⁾	R_{thJA}	-	-	40	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=8\text{ }\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=85\text{ °C}^{1)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=10\text{ A}$	-	29.8	41.0	m Ω
		$V_{GS}=10\text{ V}, I_D=10\text{ A}$	-	22.4	30	
Gate resistance ¹⁾	R_G		-	0.9	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	461	599	pF
Output capacitance	C_{oss}		-	83	108	
Reverse transfer capacitance	C_{rss}		-	7.7	11.6	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=3.5\ \Omega$	-	2	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	5	-	
Fall time	t_f		-	3	-	

Gate Charge characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=10\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	1.5	1.9	nC
Gate to drain charge	Q_{gd}		-	1.8	2.7	
Gate charge total	Q_g		-	8.1	10.5	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V

Reverse Diode

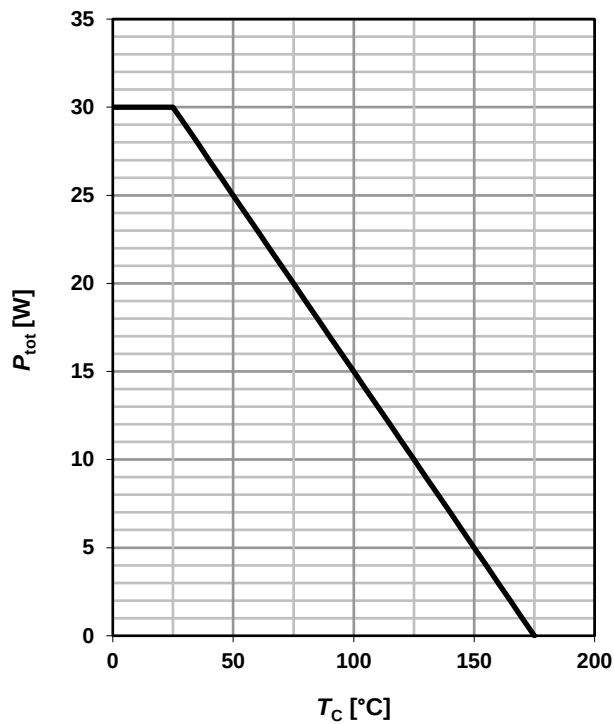
Diode continuous forward current ¹⁾	I_S	$T_C=25\text{ °C}$	-	-	20	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	43	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=10\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=40\text{ V}, I_F=20\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	29	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	20	-	nC

¹⁾ The parameter is not subject to production test - verified by design/characterization.

²⁾ Device on four layer 2s2p PCB defined in accordance with JEDEC standards (JESD51-5-7).
PCB is vertical in still air.

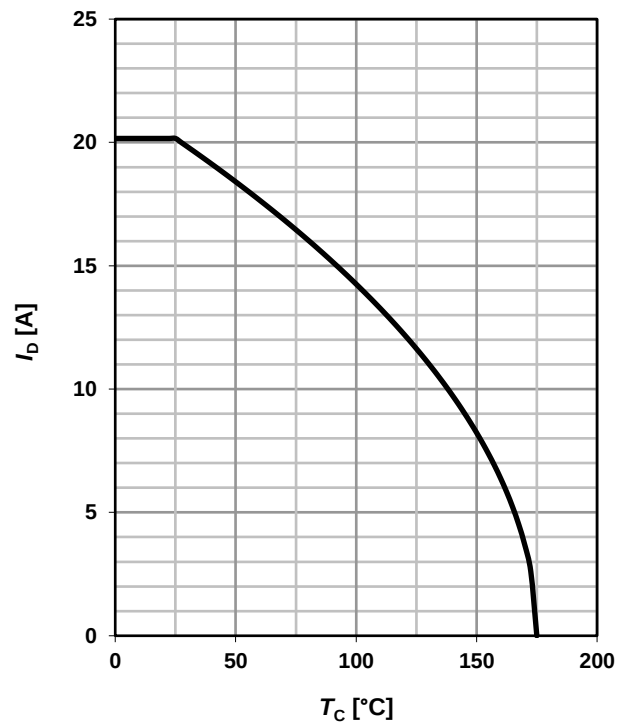
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

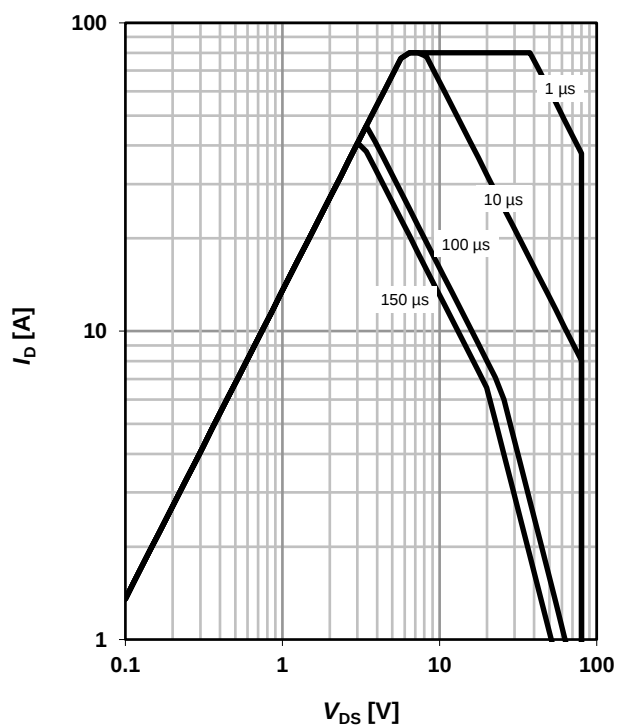
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

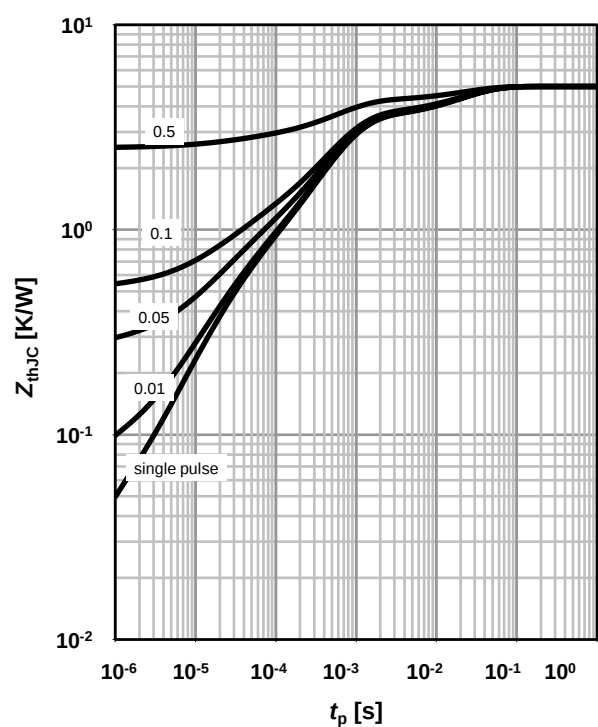
parameter: t_p



4 Max. transient thermal impedance

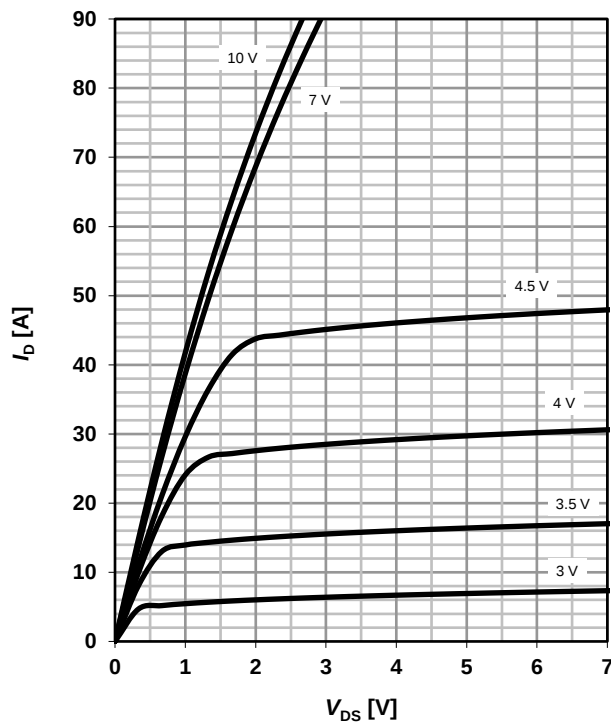
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



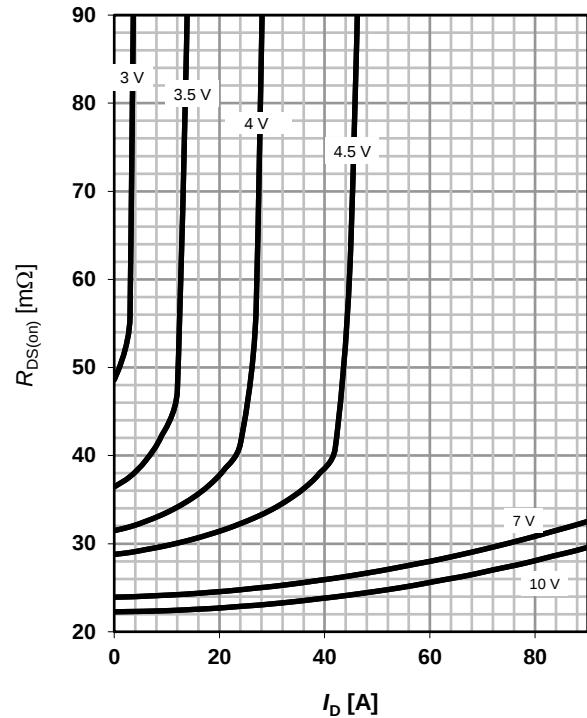
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


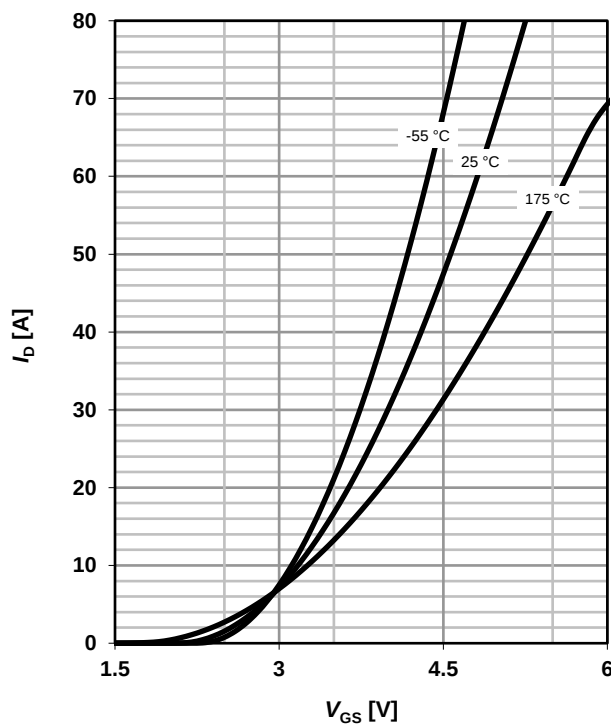
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

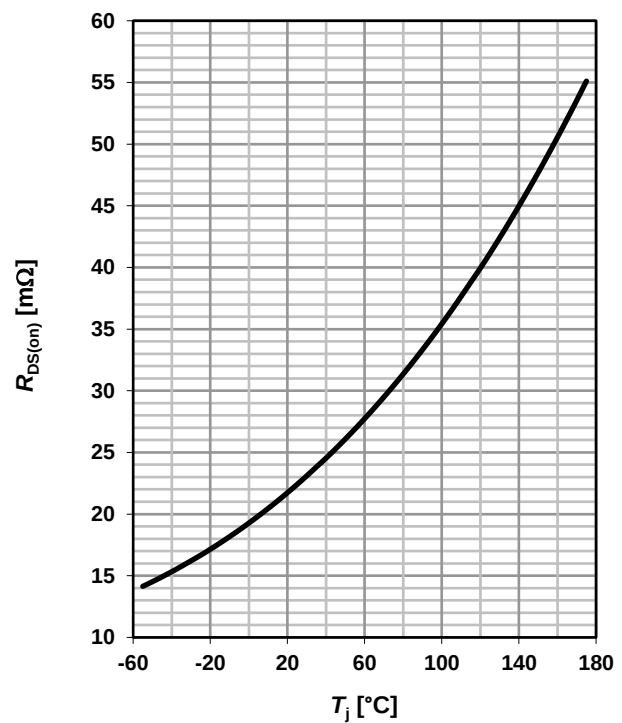
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


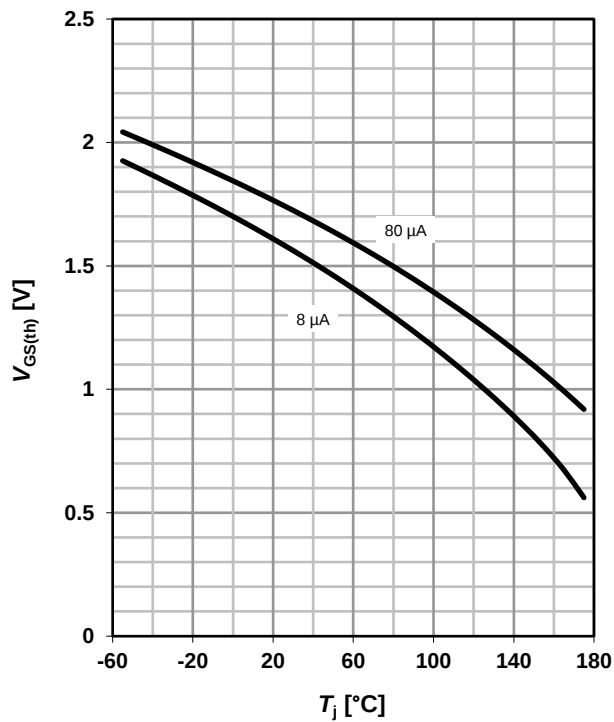
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 10\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

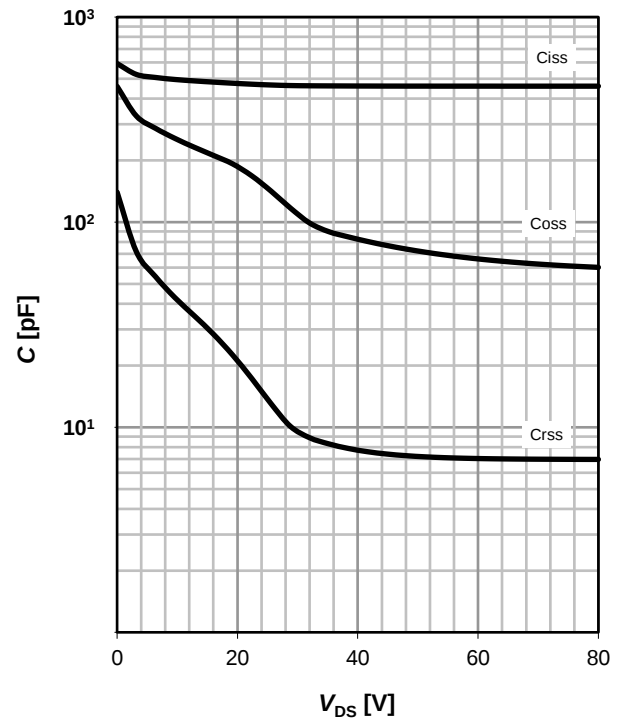
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

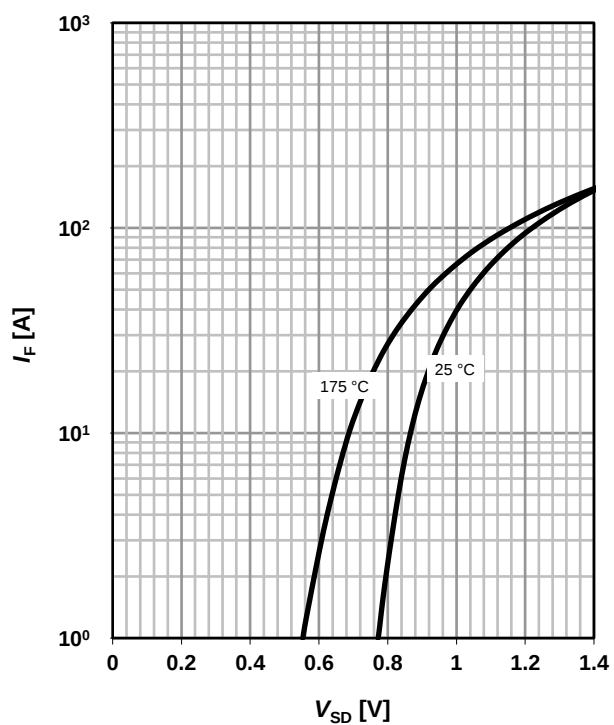
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

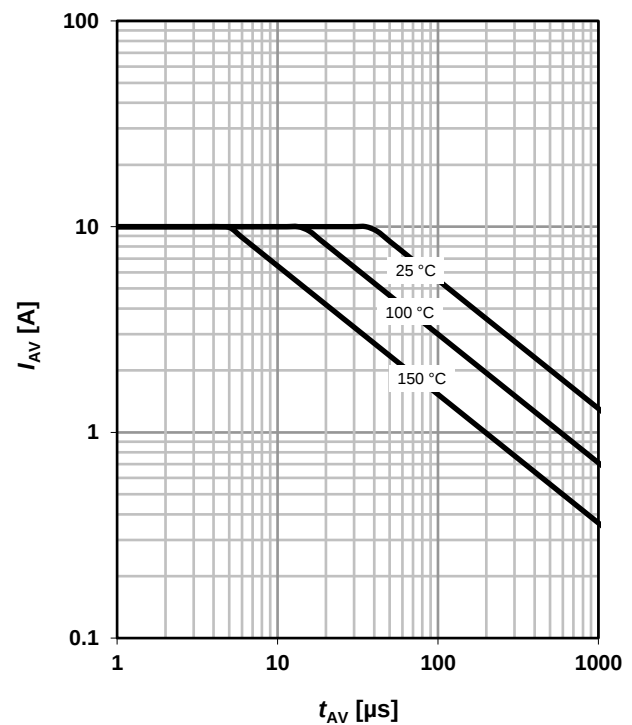
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

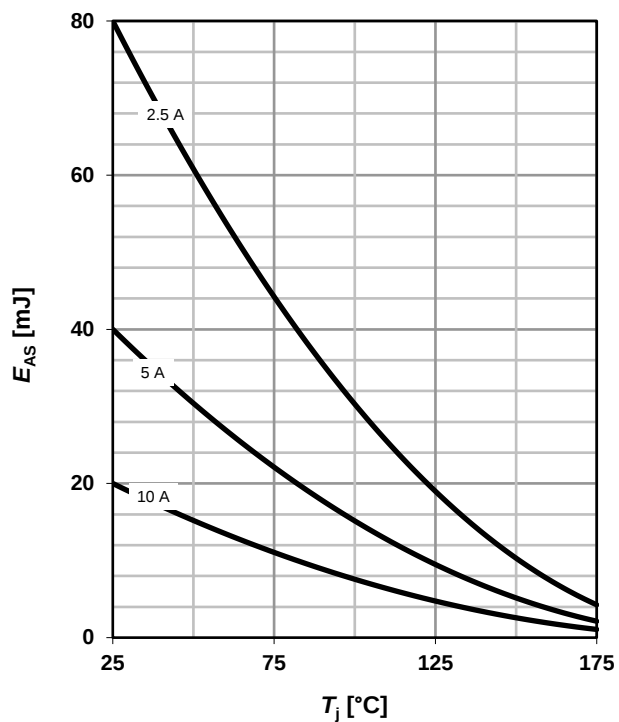
parameter: $T_{j(start)}$



13 Typical avalanche energy

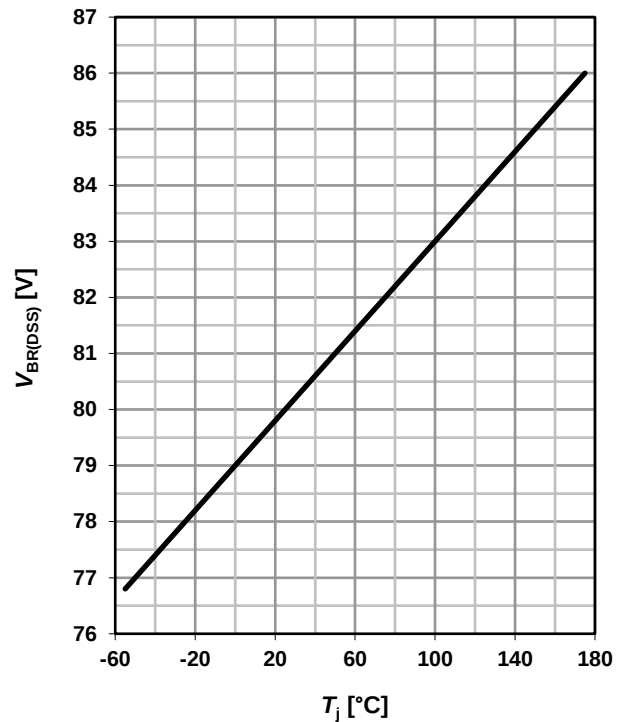
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

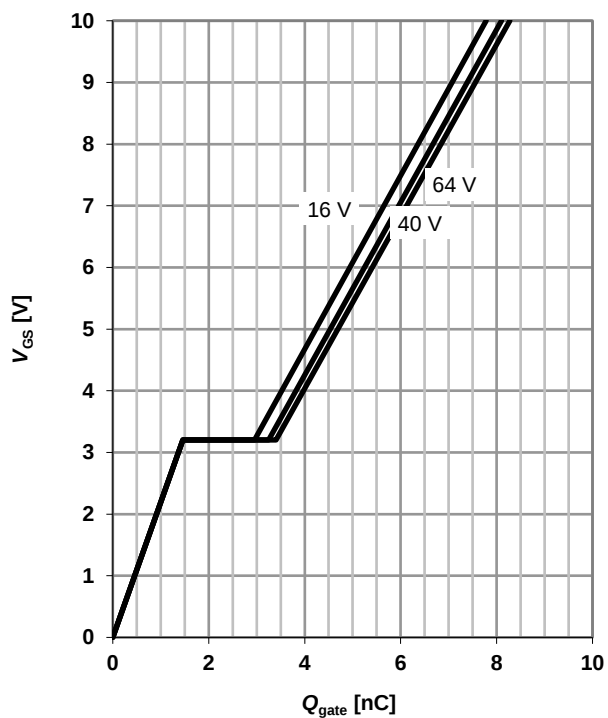
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



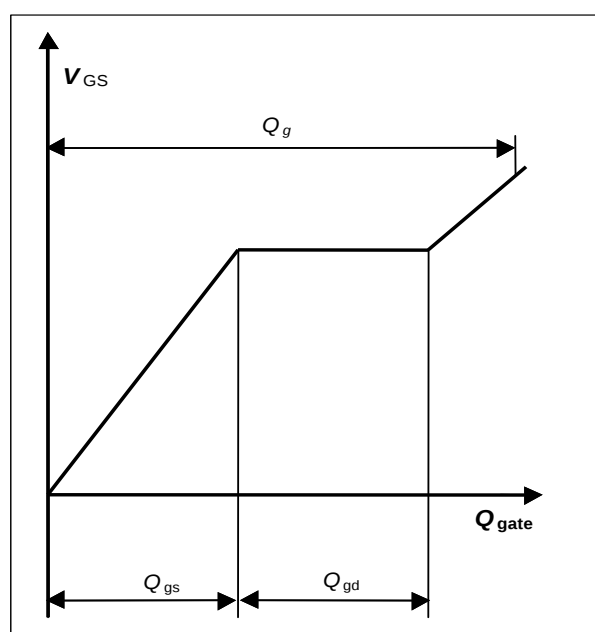
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 10 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



[illegible]

Technical drawings of a mechanical part, showing front and side views with dimensions in millimeters.

Front View (Left):

- Overall width: 2.29
- Overall height: 2.36
- Top edge features: 0.65 (width of first feature), 0.34 (width of second feature).
- Right side features: 0.48 (width of top feature), 1.58 (height of top feature), 1.45 (height of bottom feature).
- Bottom edge features: 0.9 (height of left feature), 0.45 (height of middle feature), 0.34 (width of left feature), 1.64 (width of middle feature), 0.65 (width of right feature), 0.34 (width of right feature).

Side View (Right):

- Overall width: 0.31
- Overall height: 0.41
- Top edge features: 0.325 (width of first feature), 0.24 (width of second feature), 0.6 (width of third feature), 1.4 (width of fourth feature).
- Right side features: 0.6 (height of top feature), 1.4 (height of middle feature), 1.5 (height of bottom feature), 0.7 (height of right feature).
- Bottom edge features: 0.41 (width of first feature), 0.24 (width of second feature), 0.41 (width of third feature), 0.24 (width of fourth feature).
- Internal features: 1.55 (height of top feature), 0.35 (width of top feature), 1.09 (width of middle feature), 0.67 (width of bottom feature), 0.2 (width of bottom feature).

Technical drawing of a rectangular plate with the following dimensions and features:

- Overall width: 12
- Overall height: 12
- Distance between center lines of the three square holes: 8
- Distance from the left edge to the center line of the first square hole: 3.6
- Distance from the center line of the last square hole to the right edge: 3.6
- Height of the square holes: 3.6
- Thickness of the plate: 0.2
- Features: Three square holes with rounded corners and a small circular hole in the center of each. A label "PIN 1 INDEX MARKING" points to the top-left corner.

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