

OptiMOS™-5 Power-Transistor



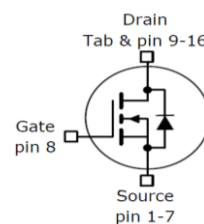
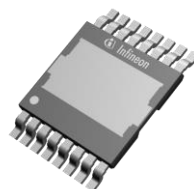
Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	1.4	mΩ
I_D	300	A

PG-HDSOP-16-2



Type	Package	Marking
IAUS300N08S5N014T	PG-HDSOP-16-2	5N08014

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	327	A
		$V_{GS}=10\text{ V}$, DC current ³⁾	300	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	108	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ μs}$	1186	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=150\text{ A}$	600	mJ
Avalanche current, single pulse	I_{AS}	-	300	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	300	W
Operating and storage temperature	T_J, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	Top	-	-	0.5	K/W
		Bottom (Pin 1-7)	-	9	-	
		Bottom (Pin 9-16)	-	3	-	
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	Top	-	2.8	-	
		Bottom (through PCB)	-	40	-	

Electrical characteristics, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=230\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^{\circ}\text{C}$	-	0.1	1	μA
		$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=85\text{ }^{\circ}\text{C}^{2)}$	-	1	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}$, $I_D=75\text{ A}$	-	1.6	2.1	m Ω
		$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$	-	1.2	1.4	
Gate resistance ²⁾	R_G	-	-	1.3	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	10137	13178	pF
Output capacitance	C_{oss}		-	1626	2114	
Reverse transfer capacitance	C_{rss}		-	71	106	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\text{ }\Omega$	-	25	-	ns
Rise time	t_r		-	15	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	t_f		-	46	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	46	60	nC
Gate to drain charge	Q_{gd}		-	30	47	
Gate charge total	Q_g		-	144	187	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	300	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ }^\circ\text{C}, t_p=100\text{ }\mu\text{s}$	-	-	2000	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	83	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	156	-	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

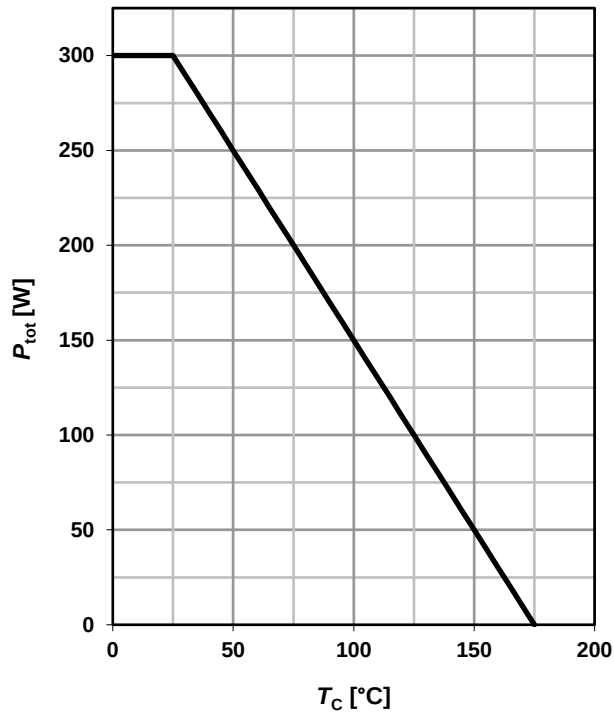
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Current is limited by the bondwires.

⁴⁾ Device on a four-layer 2s2p FR4 PCB with topside cooling. Thermal insulation material is 100 μm thick and has a conductivity of 0.7 W/mK. Top surface of heat sink is fixed at ambient temperature. Bottom surface of PCB is left at free convection. Values may vary depending on the customer-specific design.

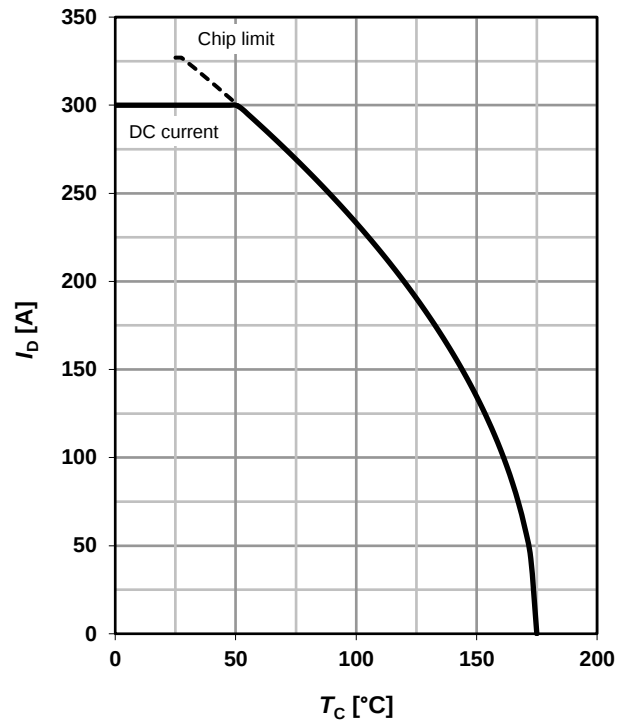
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

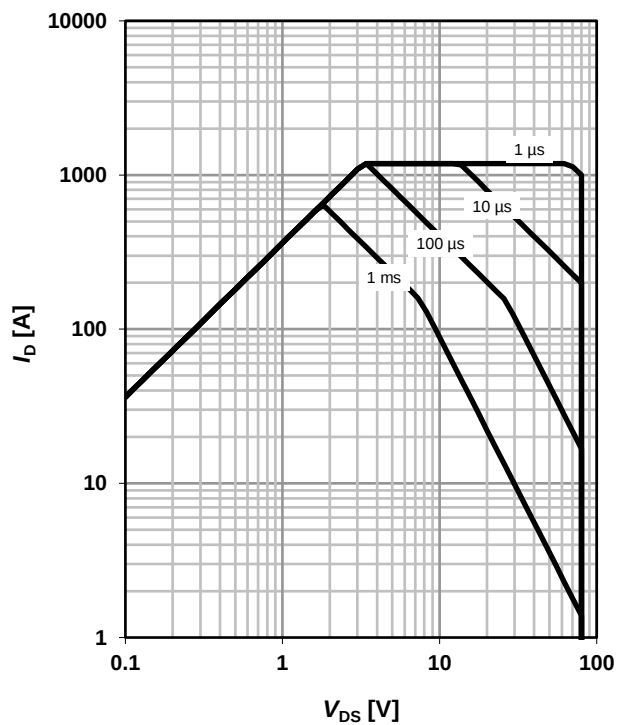
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

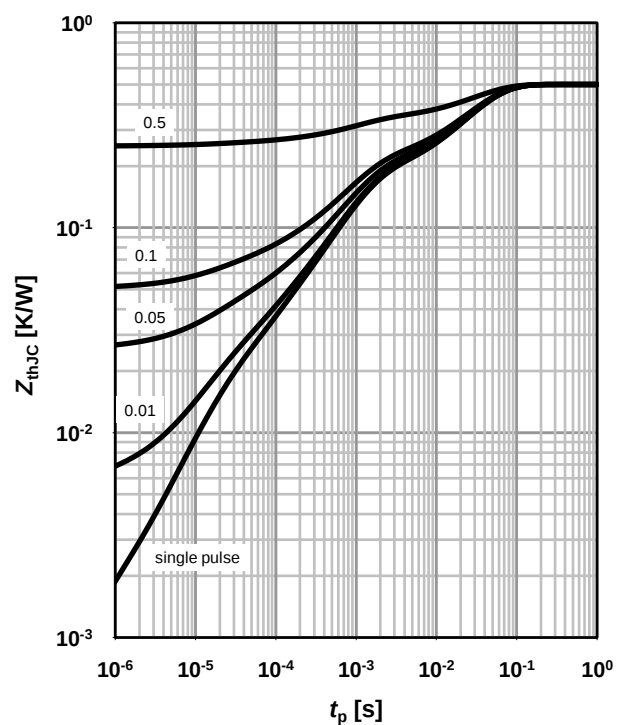
parameter: t_p



4 Max. transient thermal impedance

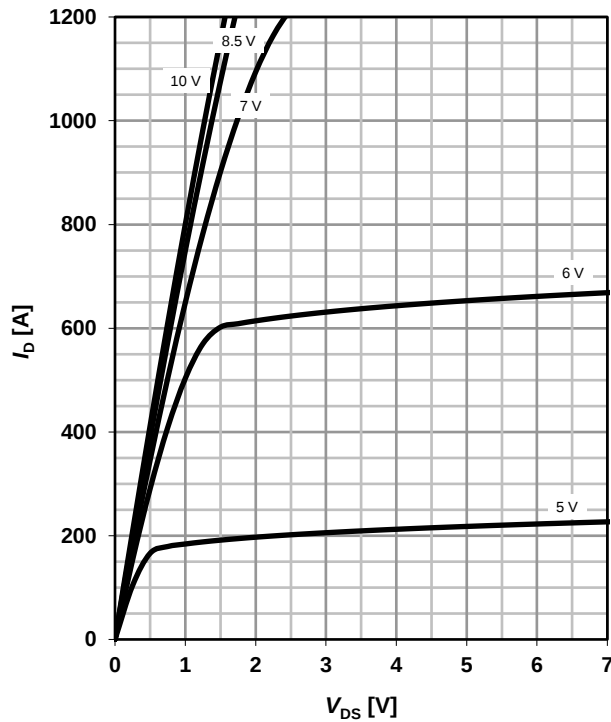
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



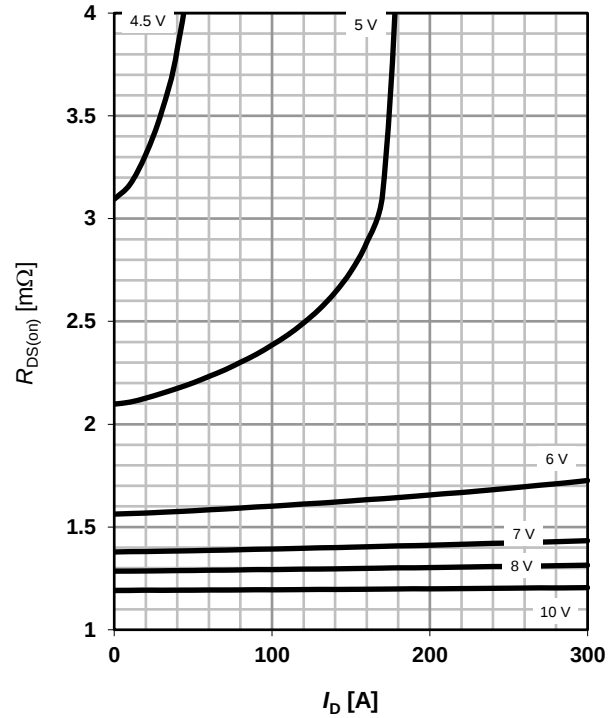
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


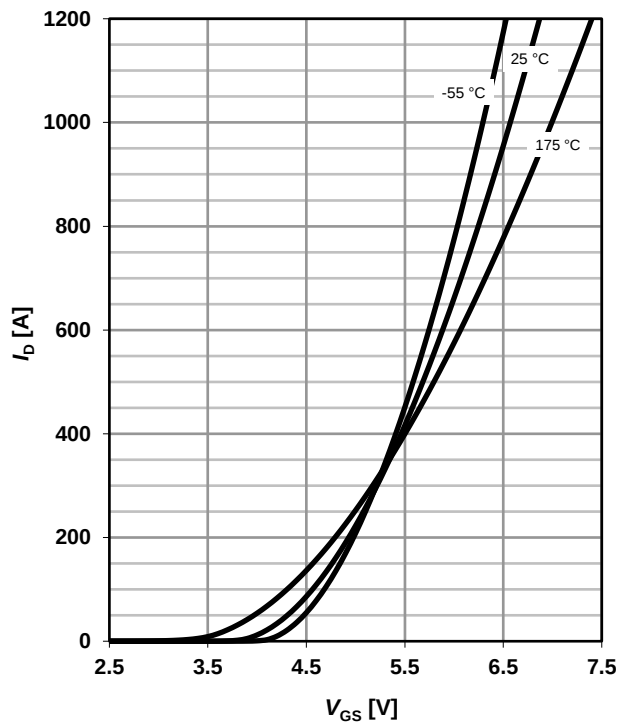
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


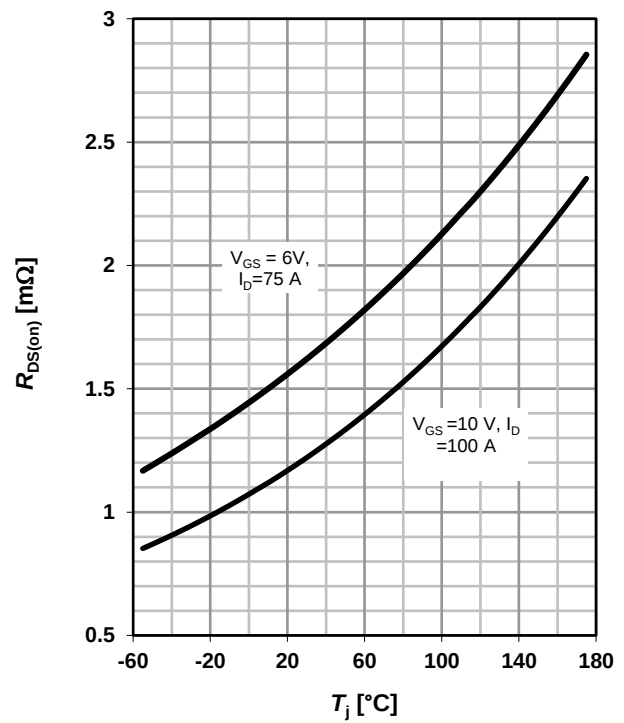
7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


8 Typ. drain-source on-state resistance

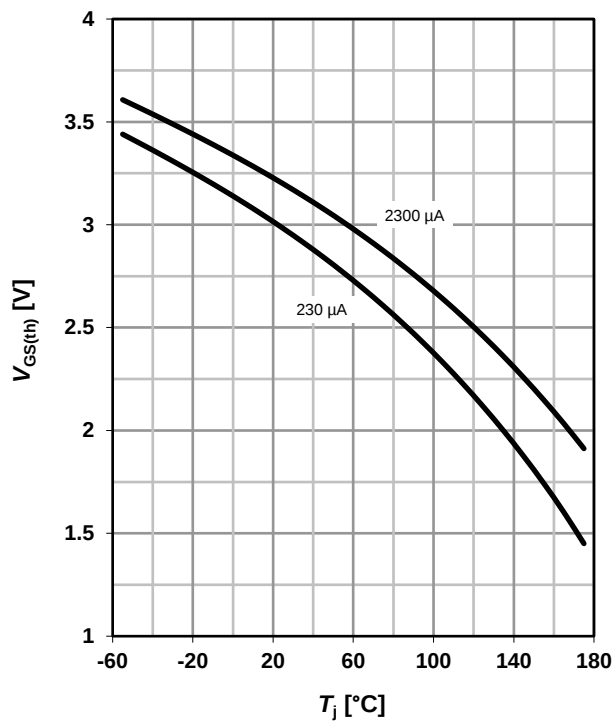
 $R_{DS(on)} = f(T_j)$

parameter: I_D, V_{GS}


9 Typ. gate threshold voltage

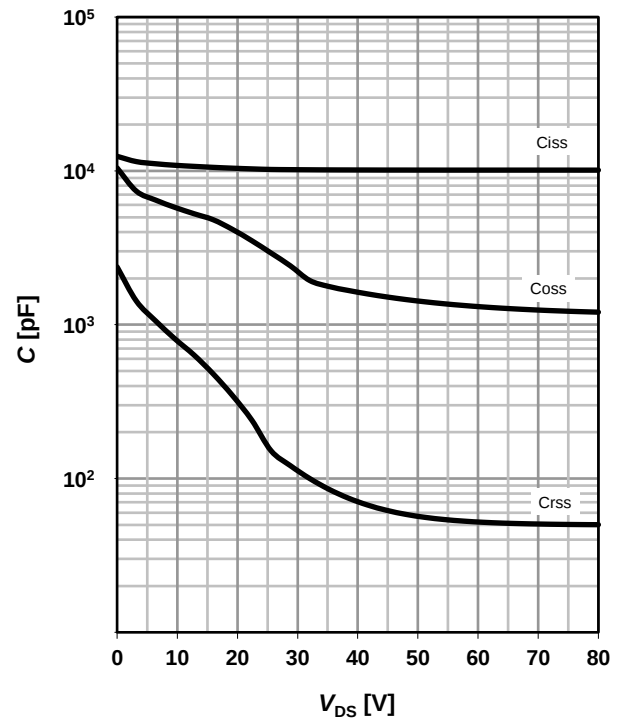
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

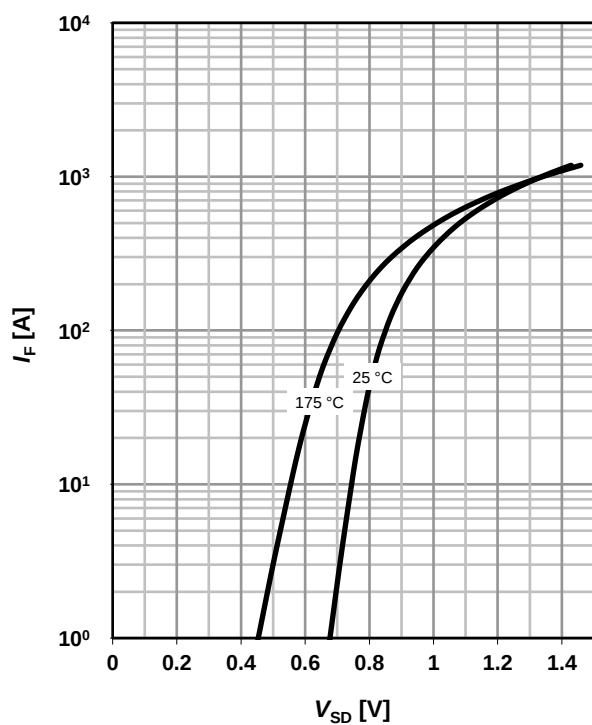
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

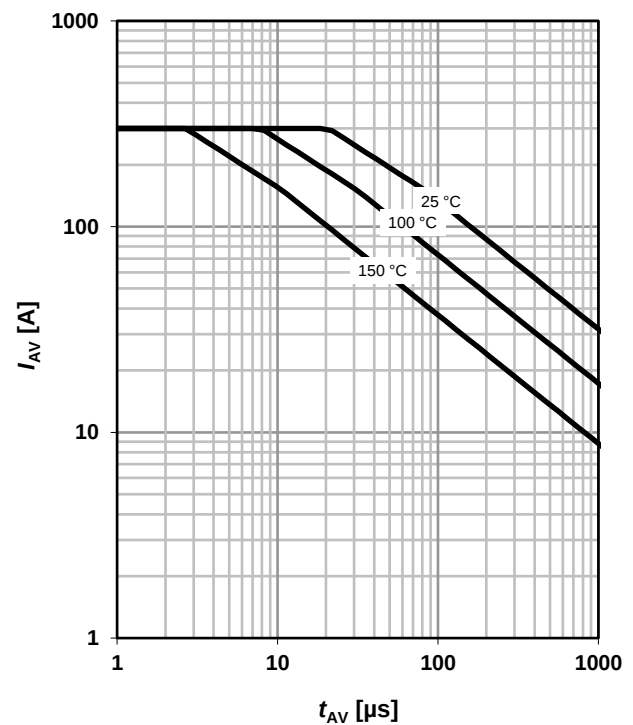
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

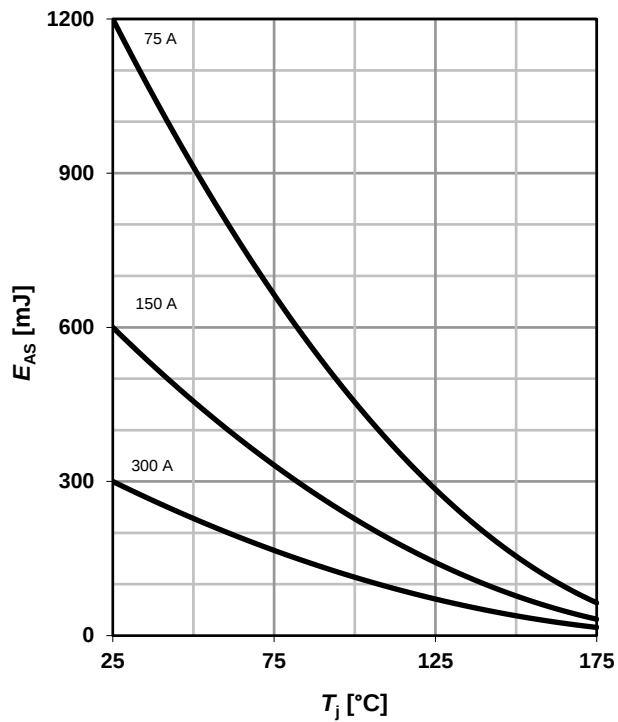
parameter: $T_{j(start)}$



13 Typical avalanche energy

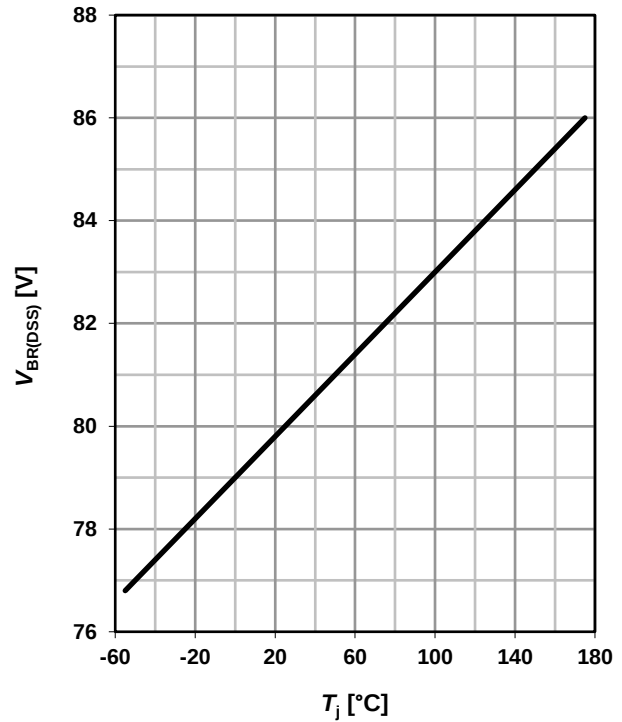
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

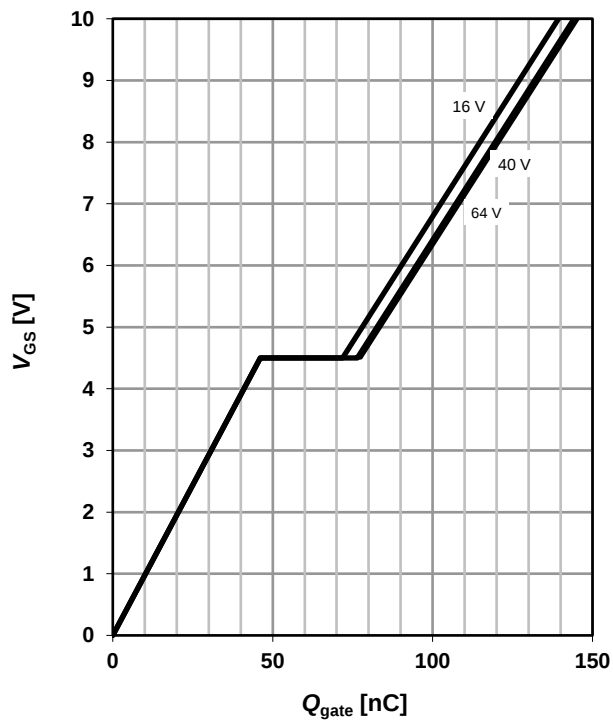
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



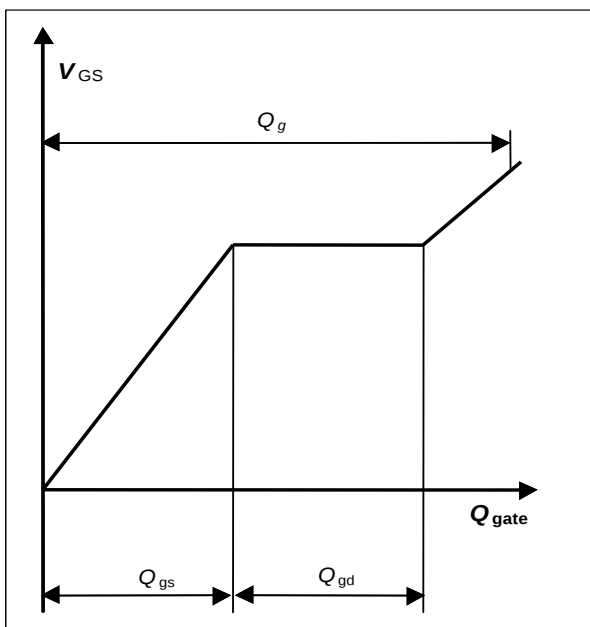
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of the 16-pin connector showing three views: Front View, Side View, and Bottom View.

Front View: Shows the connector with 16 pins. Key dimensions include:

- Overall width: 9.9 ± 0.2
- Pin pitch: 0.5 (14x) and 1.2
- Pin 1 Marking: Indicated by a circle and the number 1.
- Heatsink: Indicated by a label and a line pointing to the central rectangular area.
- Overall height: $10.1^{+0.2}_{-0.1}$
- Pin height: 2.45
- Pin 16: Indicated by the number 16 at the top right.
- Pin 9: Indicated by the number 9 at the top center.
- Pin 8: Indicated by the number 8 at the bottom right.
- Pin 1: Indicated by the number 1 at the bottom left.

Side View: Shows the profile of the connector. Key dimensions include:

- Overall height: 15 ± 0.20
- Pin height: 1.5
- Pin pitch: $0.01 \dots 0.16$ Max Stand Off
- Pin 16: Indicated by the number 16 at the top right.
- Pin 9: Indicated by the number 9 at the top center.
- Pin 8: Indicated by the number 8 at the bottom right.
- Pin 1: Indicated by the number 1 at the bottom left.

Bottom View: Shows the underside of the connector. Key dimensions include:

- Overall width: 9.27
- Pin pitch: 0.7
- Pin 16: Indicated by the number 16 at the top right.
- Pin 9: Indicated by the number 9 at the top center.
- Pin 8: Indicated by the number 8 at the bottom right.
- Pin 1: Indicated by the number 1 at the bottom left.

Figure 1: Dimensions of the PCB layout. The figure includes a top-down view of the PCB layout and two detailed views of the solder mask and stencil apertures. The top-down view shows a central copper pad (7.187 x 7.187) surrounded by a solder mask clearance (0.6). The layout is defined by dimensions 14x, 16x, 1.2, 0.8, 3.375, 1.75, 7, 10.2, and 0.6. The detailed views show the solder mask and stencil apertures with dimensions 0.8, 16x, 3.375, 0.6, and 7.187. A legend at the bottom identifies the materials: copper (solid black), solder mask (white), and stencil apertures (hatched).

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Revision History

Version	Date	Changes
Version 1.0	01.10.2020	Final Datasheet

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