

OptiMOS™-5 Power-Transistor



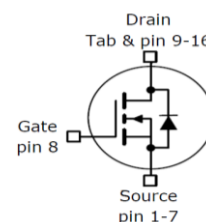
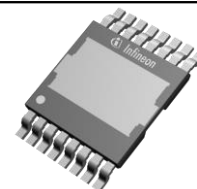
Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	1.1	mΩ
I_D	300	A

PG-HDSOP-16-2



Type	Package	Marking
IAUS300N08S5N011T	PG-HDSOP-16-2	5N08011

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	400	A
		$V_{GS}=10\text{ V}$, DC current ³⁾	300	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	123	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ μs}$	1450	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=150\text{ A}$	817	mJ
Avalanche current, single pulse	I_{AS}	-	300	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	375	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	Top	-	-	0.4	K/W
		Bottom (Pin 1-7)	-	9	-	
		Bottom (Pin 9-16)	-	3	-	
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	Top	-	2.8	-	
		Bottom (through PCB)	-	40	-	

Electrical characteristics, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=275\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^{\circ}\text{C}$	-	0.1	1	μA
		$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=85\text{ }^{\circ}\text{C}^{2)}$	-	1	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}$, $I_D=75\text{ A}$	-	1.4	1.8	m Ω
		$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$	-	1.0	1.1	
Gate resistance ²⁾	R_G	-	-	1.5	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	12500	16250	pF
Output capacitance	C_{oss}		-	2000	2600	
Reverse transfer capacitance	C_{rss}		-	86	130	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\ \Omega$	-	31	-	ns
Rise time	t_r		-	19	-	
Turn-off delay time	$t_{d(off)}$		-	69	-	
Fall time	t_f		-	55	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	56	73	nC
Gate to drain charge	Q_{gd}		-	37	56	
Gate charge total	Q_g		-	178	231	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	-	-	300	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	-	-	2300	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	86	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	177	-	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

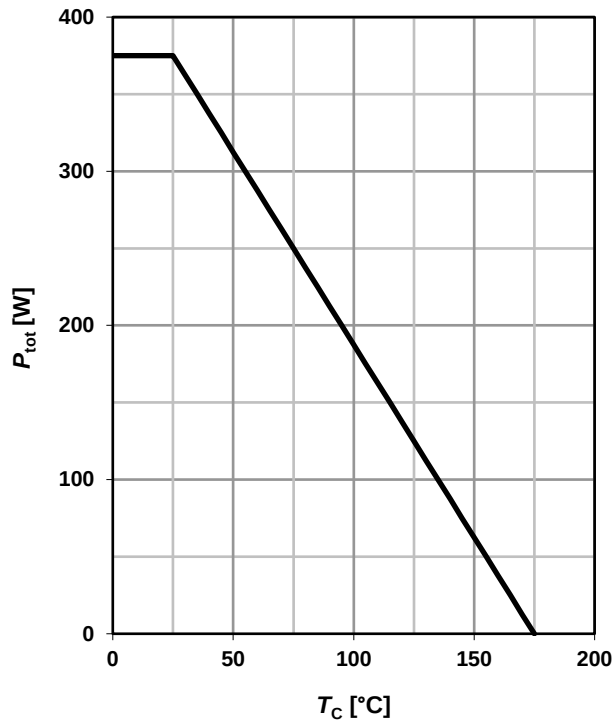
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Current is limited by the bondwires.

⁴⁾ Device on a four-layer 2s2p FR4 PCB with topside cooling. Thermal insulation material is 100 μm thick and has a conductivity of 0.7 W/mK. Top surface of heat sink is fixed at ambient temperature. Bottom surface of PCB is left at free convection. Values may vary depending on the customer-specific design.

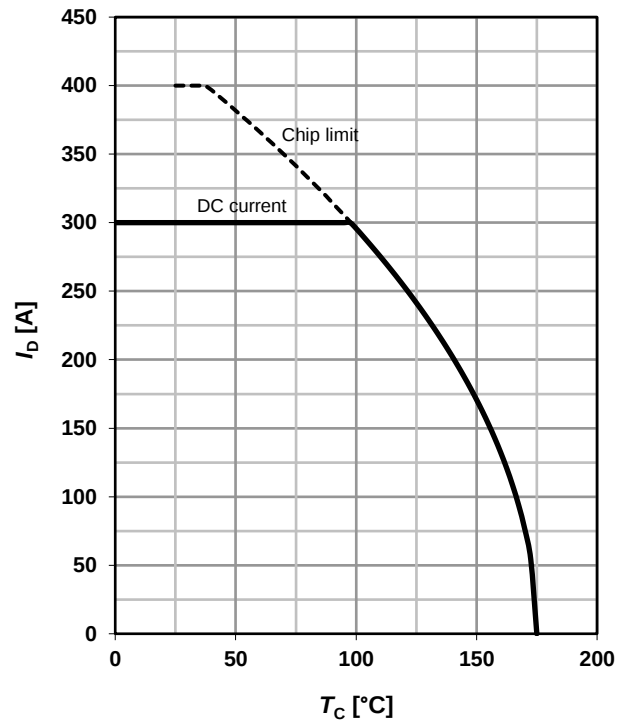
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

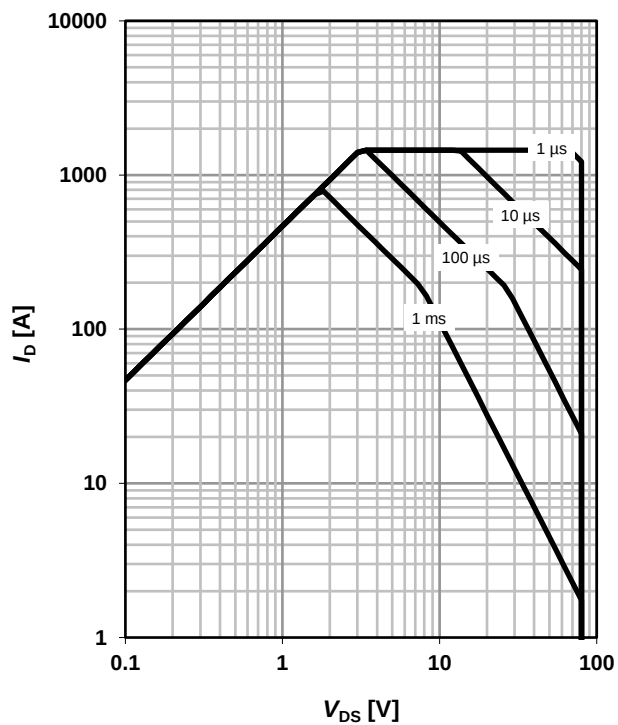
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

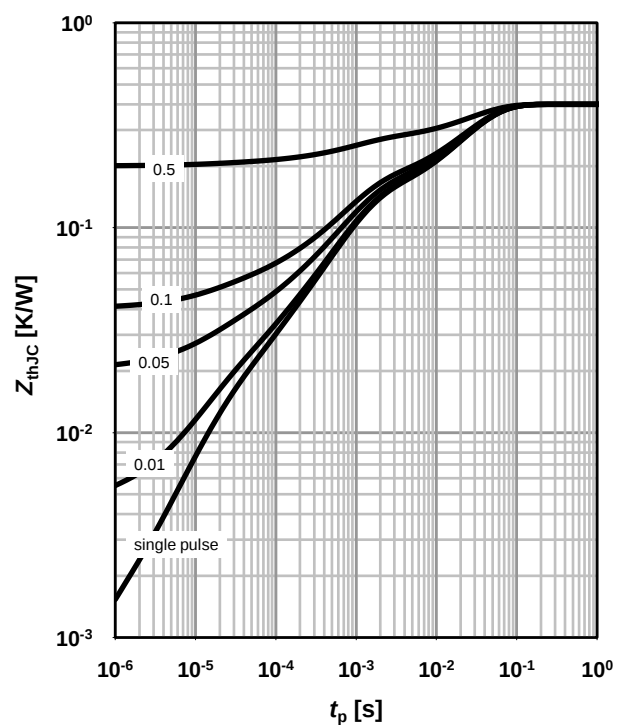
parameter: t_p



4 Max. transient thermal impedance

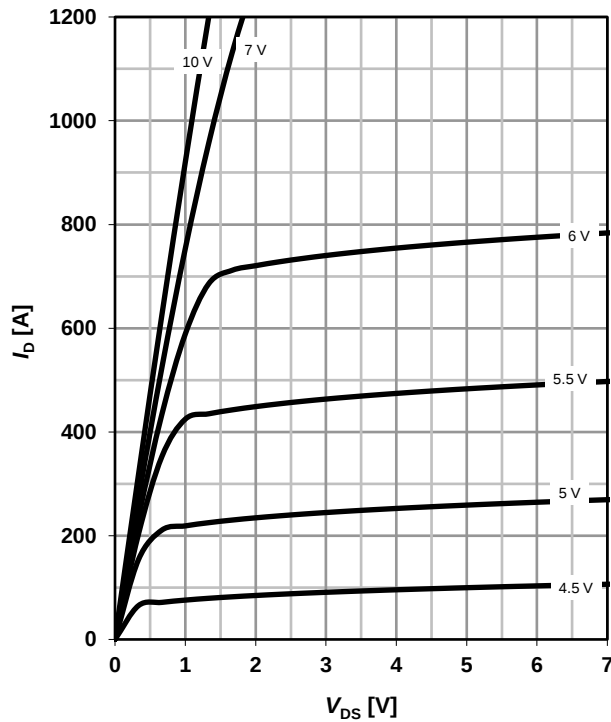
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



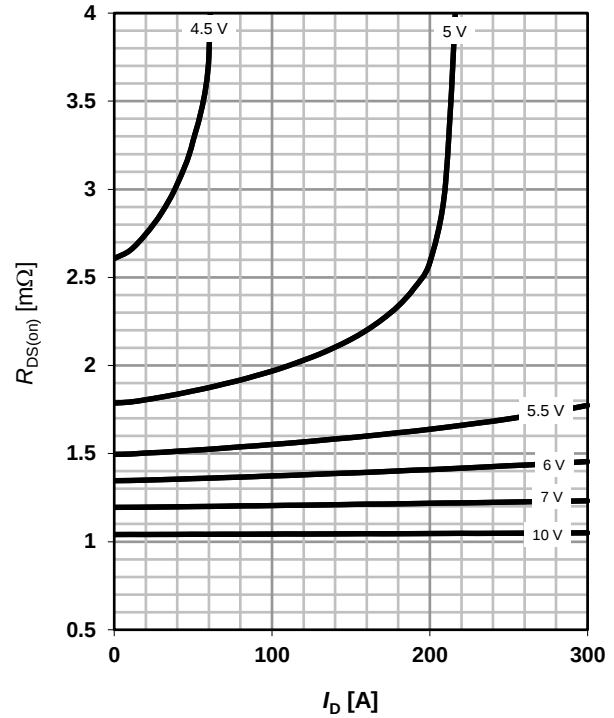
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


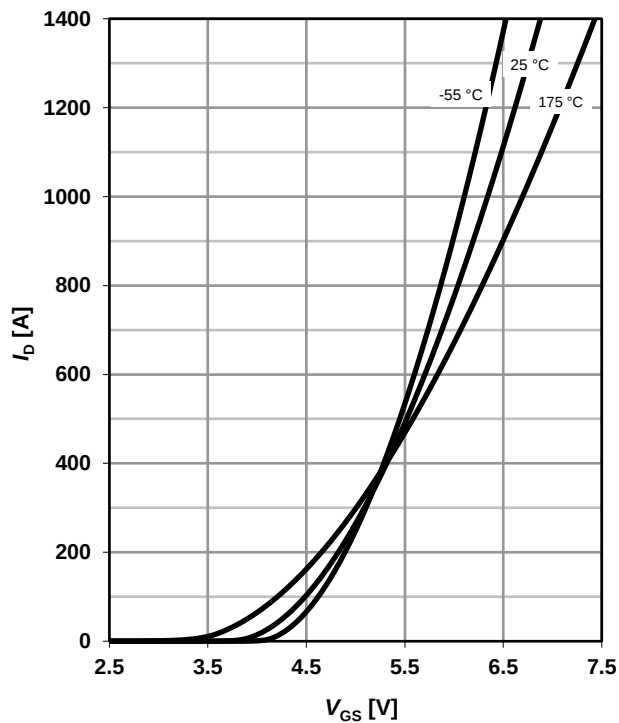
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


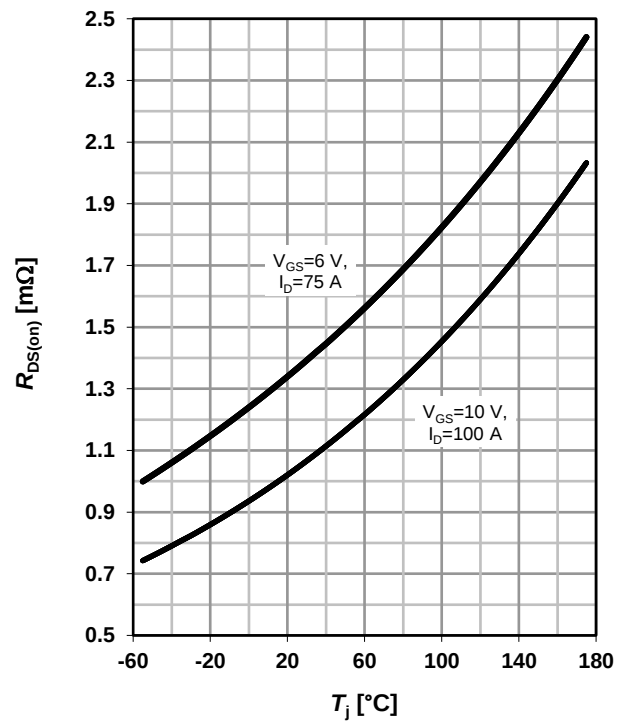
7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


8 Typ. drain-source on-state resistance

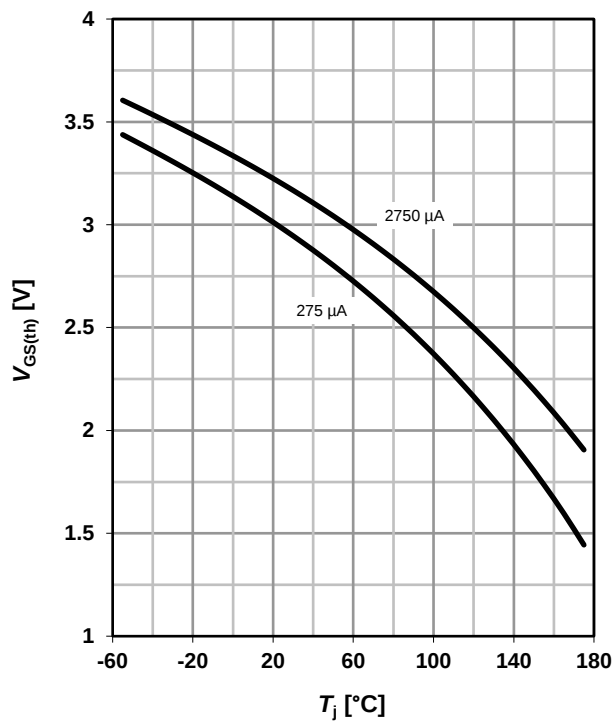
 $R_{DS(on)} = f(T_j)$

parameter: I_D, V_{GS}


9 Typ. gate threshold voltage

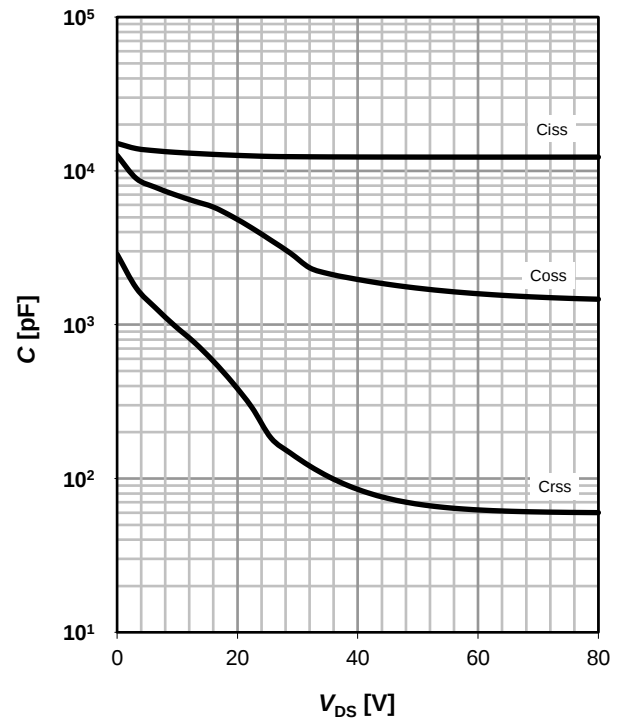
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

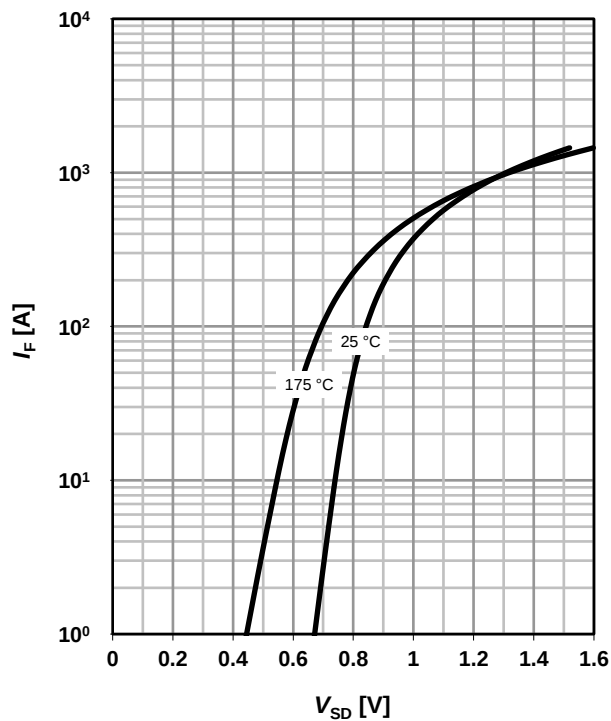
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

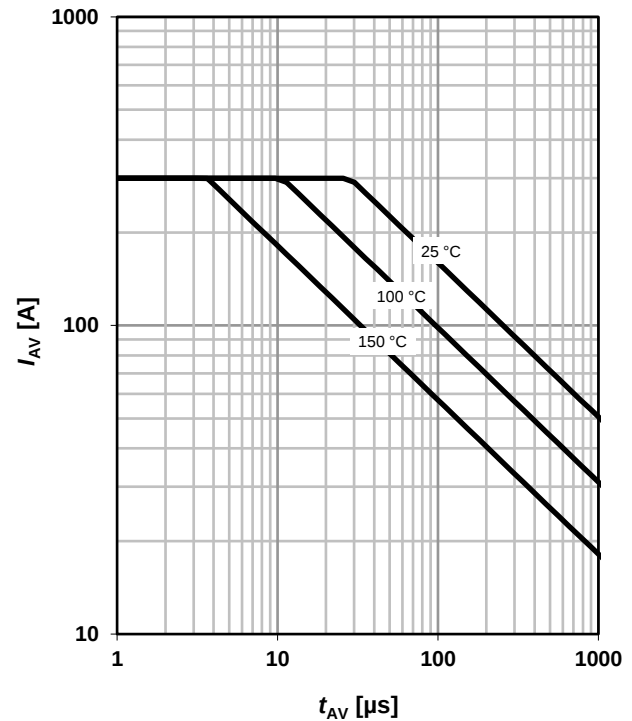
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

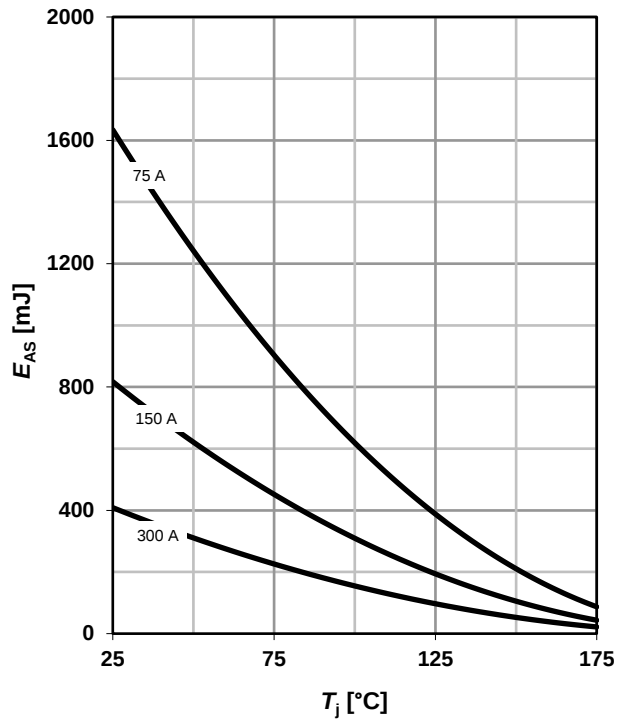
parameter: $T_{j(start)}$



13 Typical avalanche energy

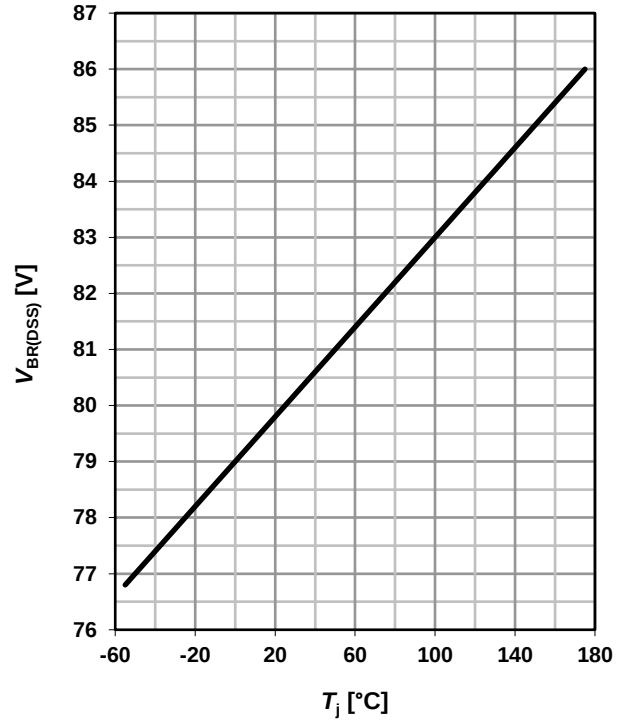
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

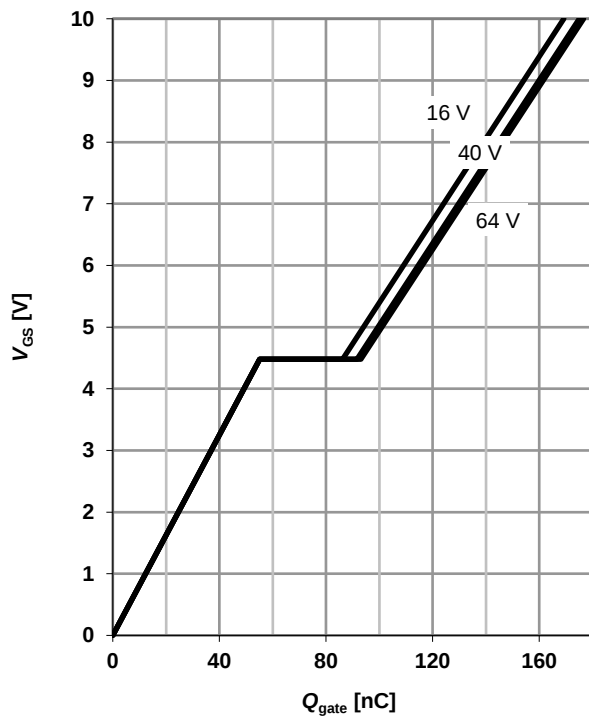
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



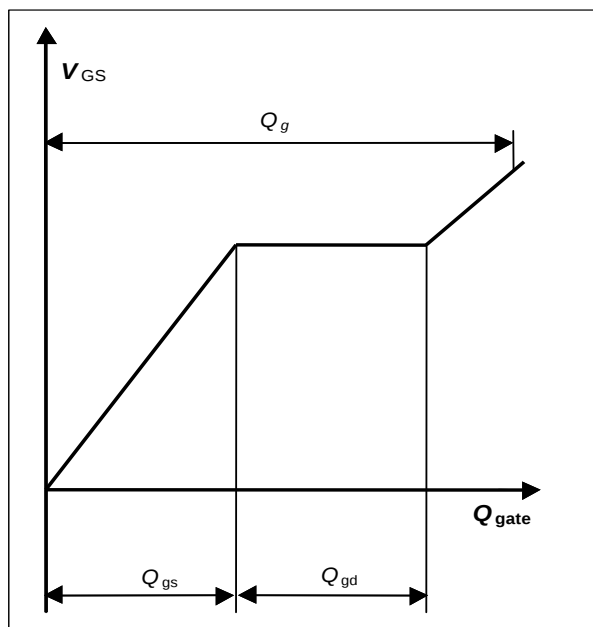
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



The drawing consists of three views: Front View, Side View, and Bottom View.

- Front View:** Shows the connector's footprint. Key dimensions include:
 - Overall width: 9.9 ± 0.2
 - Pin pitch: 0.5 (14x)
 - Pin 1 marking offset: 1.2
 - Heatsink width: 8.30
 - Heatsink height: 5.67
 - Pin 1 marking diameter: $\varnothing 0.2$
 - Pin 1 marking offset from center: 2.24
 - Pin 1 marking offset from edge: 4.05
 - Pin 1 marking offset from center (alternative): 2.24
 - Pin 1 marking offset from edge (alternative): 10.1 ± 0.1
 - Pin 1 marking offset from center (alternative): 2.24
 - Pin 1 marking offset from edge (alternative): 10.1 ± 0.1
- Side View:** Shows the connector's profile. Key dimensions include:
 - Overall height: 15 ± 0.20
 - Pin 1 marking offset from center: 2.28
 - Pin 1 marking offset from edge: $0.01 \dots 0.16$ Max Stand Off
 - Pin 1 marking offset from center (alternative): 0.02
 - Pin 1 marking offset from edge (alternative): 0.02
 - Pin 1 marking offset from center (alternative): 0.02
 - Pin 1 marking offset from edge (alternative): 0.02
- Bottom View:** Shows the connector's underside. Key dimensions include:
 - Overall width: 9.27
 - Pin 1 marking offset from center: 0.7
 - Pin 1 marking offset from edge: 0.7
 - Pin 1 marking offset from center (alternative): 0.7
 - Pin 1 marking offset from edge (alternative): 0.7

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Revision History

Version	Date	Changes
Version 1.0	01.10.2020	Final Datasheet

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