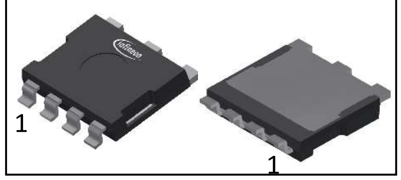
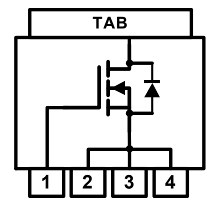
Automotive MOSFET

OptiMOS™ 5 Power-Transistor

PG-HSOG-4-1





Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL2 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	1.3	mΩ
I_D (chip limited)	350	A

Type	Package	Marking
IAUMN08S5N013G	PG-HSOG-4-1	5N08N013

Table of Contents

Maximum ratings

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, Chip limitation[1,2]	350	A
		V_{GS}=10V, DC current[3]	250	
		T_a=100 °C, V_{GS}=10 V, R_{thJA} on 2s2p[2,4]	30	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C, t_p= 100 µs	1400	
Avalanche energy, single pulse[2]	E_{AS}	I_D=125 A	535	mJ
Avalanche current, single pulse	I_{AS}	–	250	A
Gate source voltage	V_{GS}	–	±20	V
Power dissipation	P_{tot}	T_C=25 °C	307	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	0.49	K/W
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	–	23	–	

Electrical characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	V_{GS}=0 V, I_D=1 mA	80	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=214 µA	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C	–	–	1	µA
		V_{DS}=80 V, V_{GS}=0 V, T_j=100 °C[2)]	–	–	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=6 V, I_D=50 A	–	1.6	1.8	mΩ
		V_{GS}=10 V, I_D=100 A	–	1.0	1.3	
Gate resistance[2)]	R_G	–	–	1.4	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	–	9612	12496	pF
Output capacitance	C_{oss}		–	1657	2160	
Reverse transfer capacitance	C_{rss}		–	84	130	
Turn-on delay time	$t_{d(on)}$	V_{DD}=40 V, V_{GS}=10 V, I_D=100 A, R_G=3.5 Ω	–	24	–	ns
Rise time	t_r		–	15	–	
Turn-off delay time	$t_{d(off)}$		–	48	–	
Fall time	t_f		–	51	–	

Gate Charge Characteristics[2]

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V	–	44	57	nC
Gate to drain charge	Q_{gd}		–	30	45	
Gate charge total	Q_g		–	138	179	
Gate plateau voltage	$V_{plateau}$		–	4.6	–	V

Reverse Diode

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode continous forward current[2]	I_S	T_C=25 °C	–	–	250	A
Diode pulse current[2]	$I_{S,pulse}$	T_C=25 °C, t_p= 100 µs	–	–	1400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	–	0.9	1.2	V
Reverse recovery time[2]	t_{rr}	V_R=40 V, I_F=50A, di_F/dt =100 A/µs	–	49	73	ns
Reverse recovery charge[2]	Q_{rr}		–	55	109	nC

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

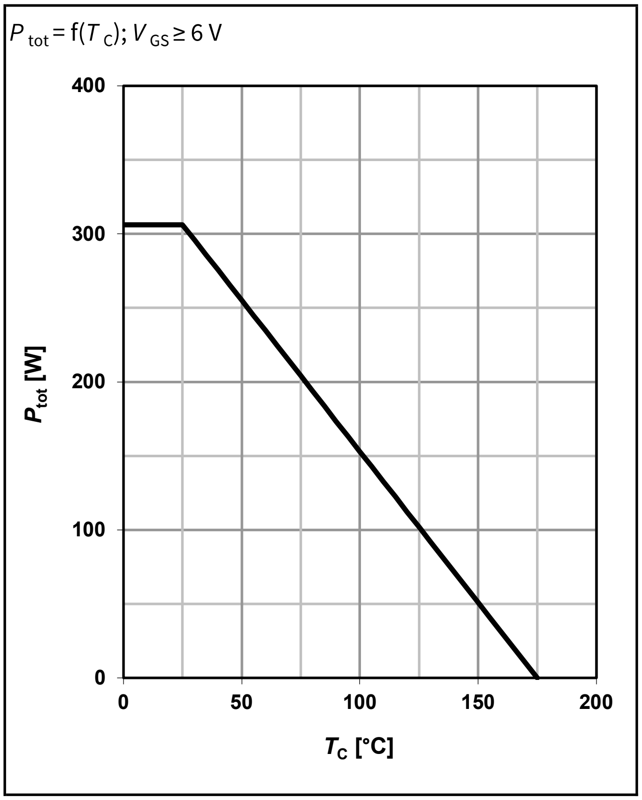
[2] The parameter is not subject to production testing – specified by design.

[3] Current is limited by package.

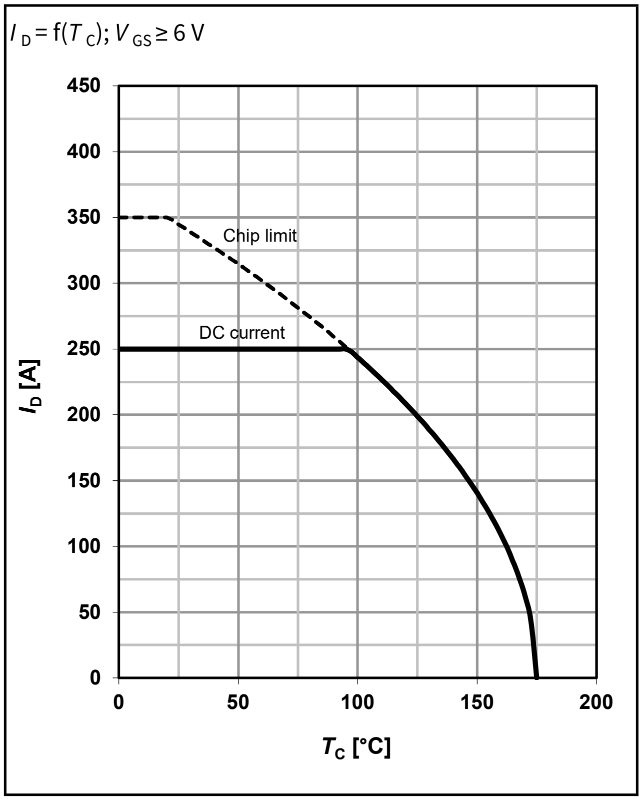
[4] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

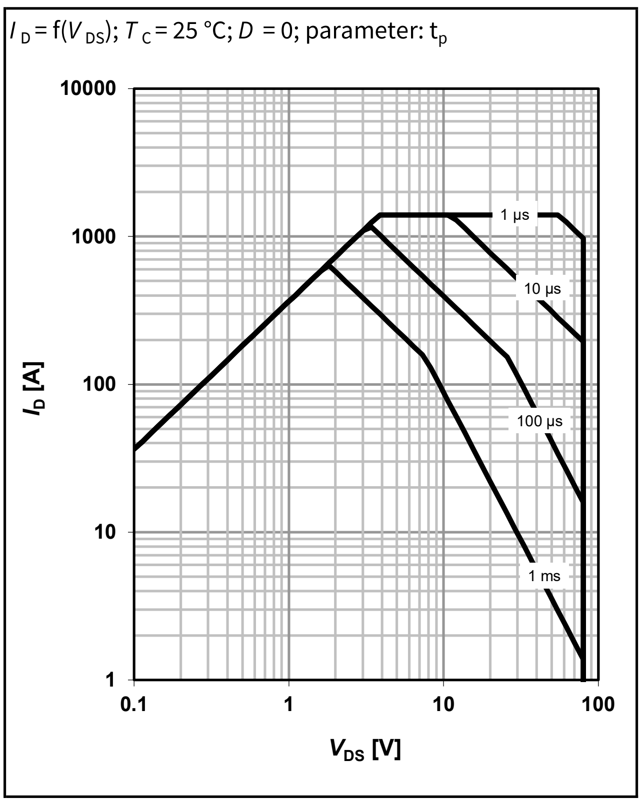
1 Power dissipation



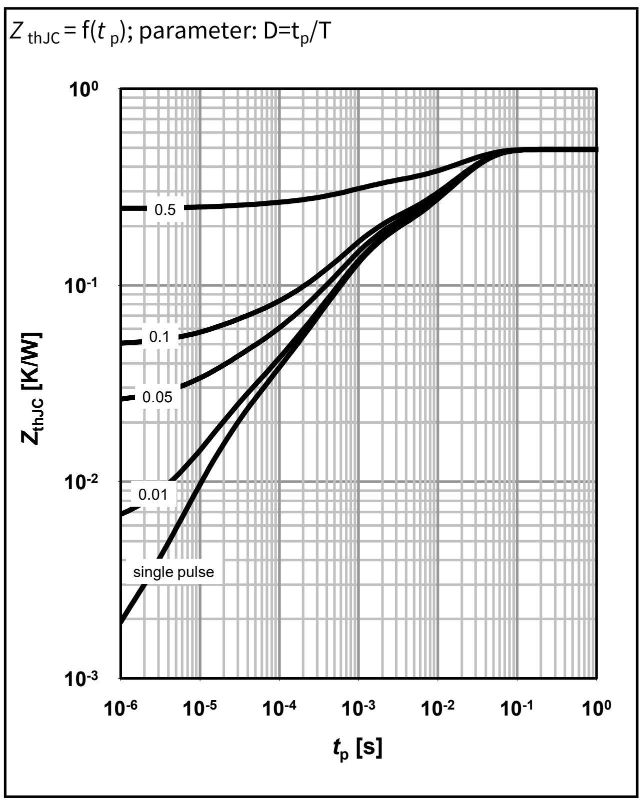
2 Drain current



3 Safe operating area

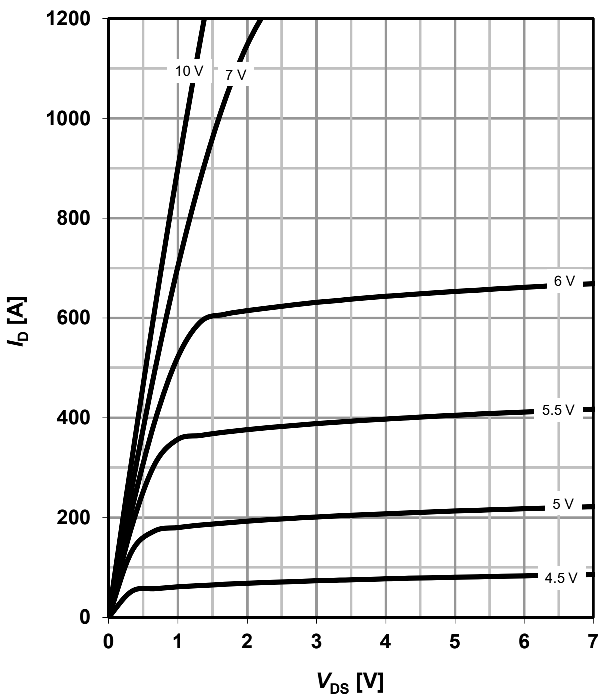


4 Max. transient thermal impedance



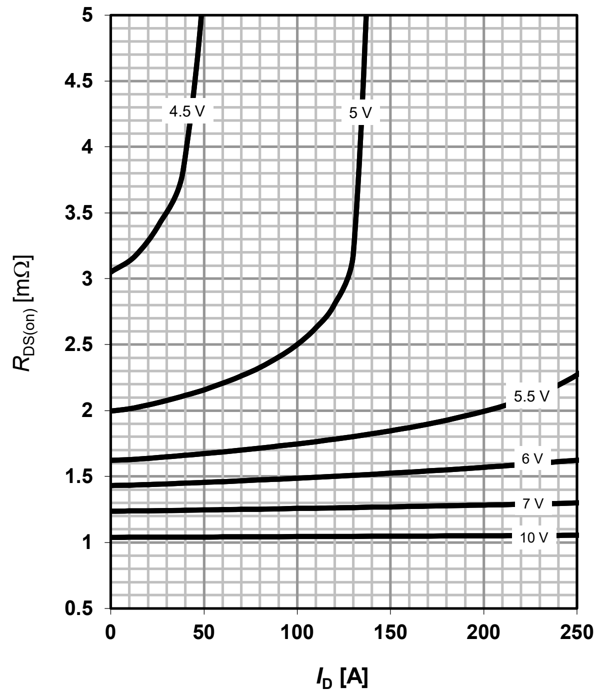
5 Typ. output characteristics

$I_D = f(V_{DS})$; T_j = 25 °C; parameter: V_{GS}



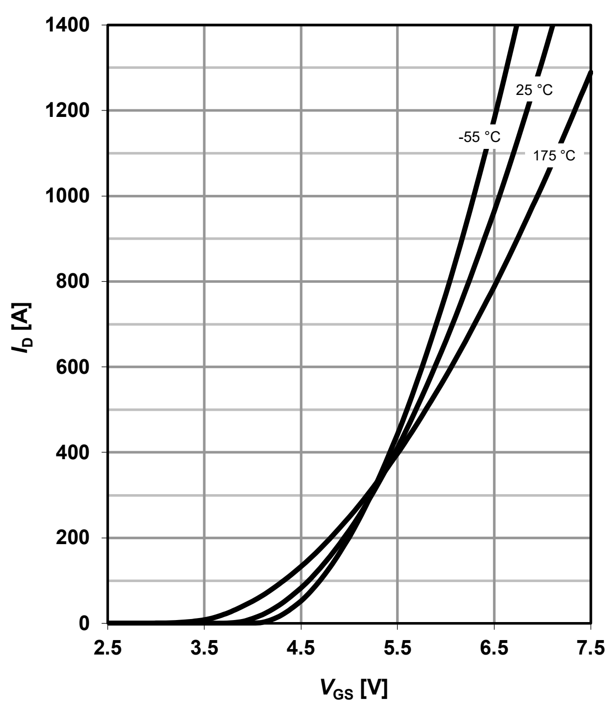
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; T_j = 25 °C; parameter: V_{GS}



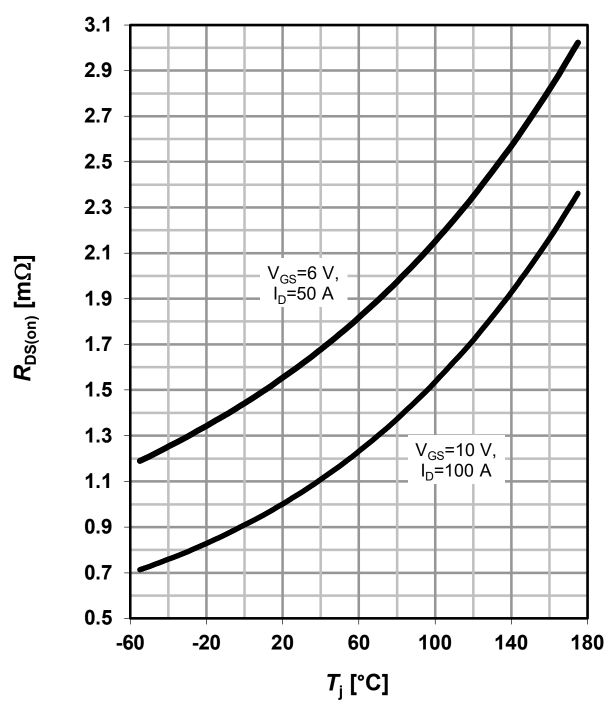
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; V_{DS} = 6V: parameter: T_j



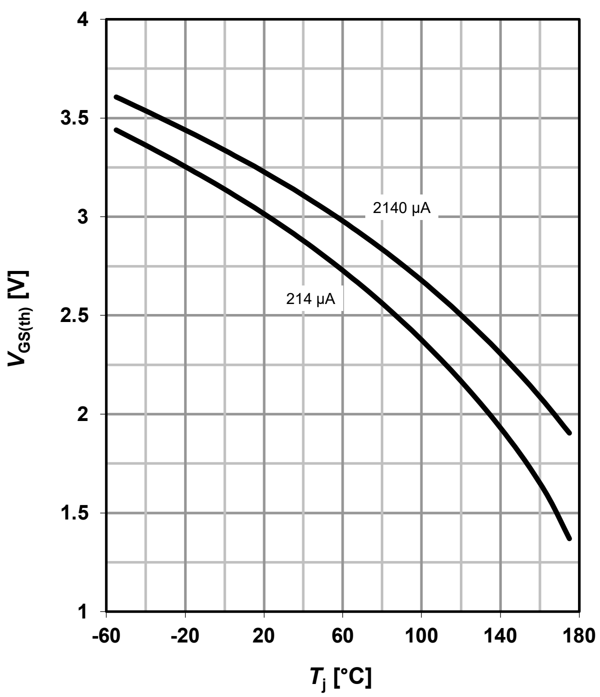
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



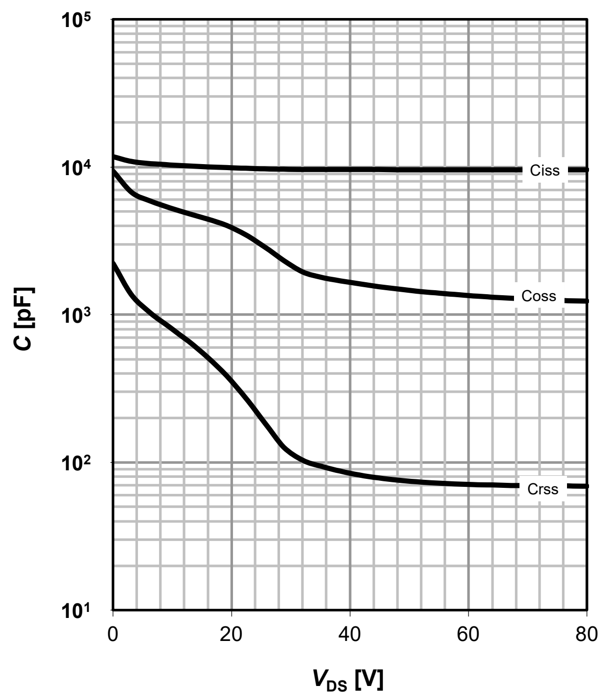
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



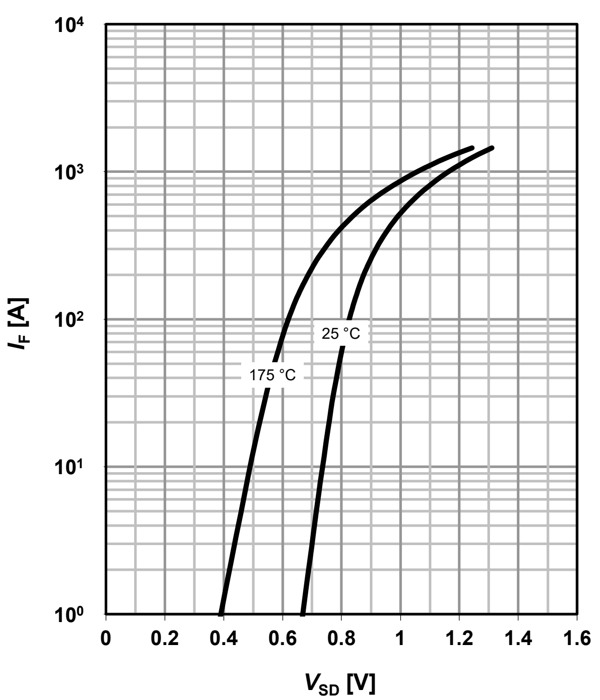
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



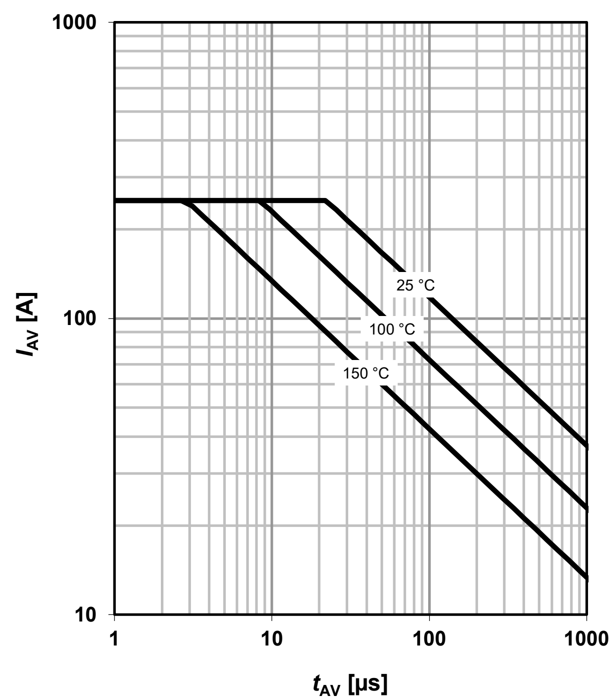
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



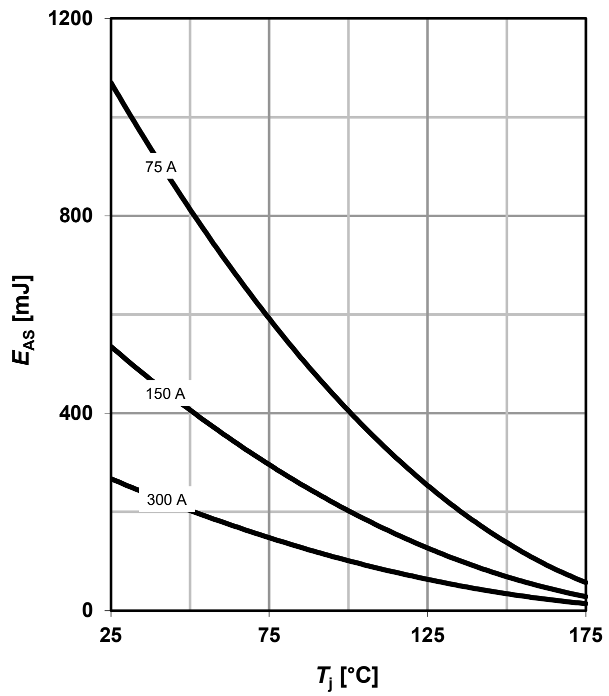
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



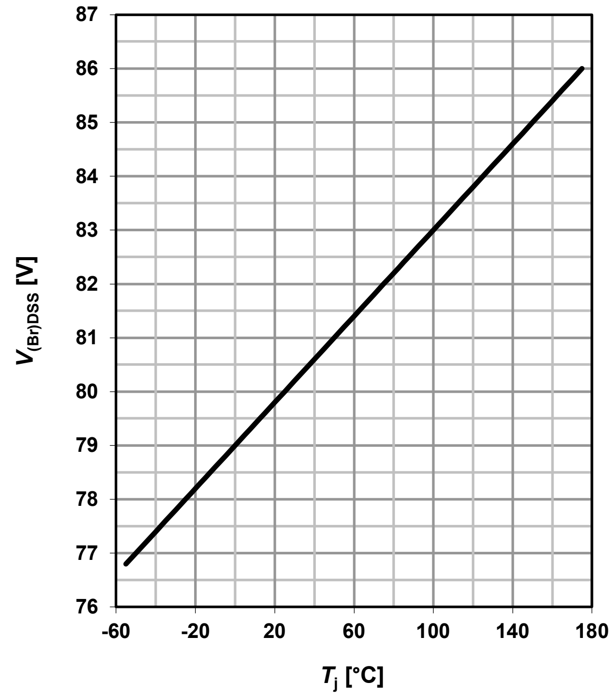
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



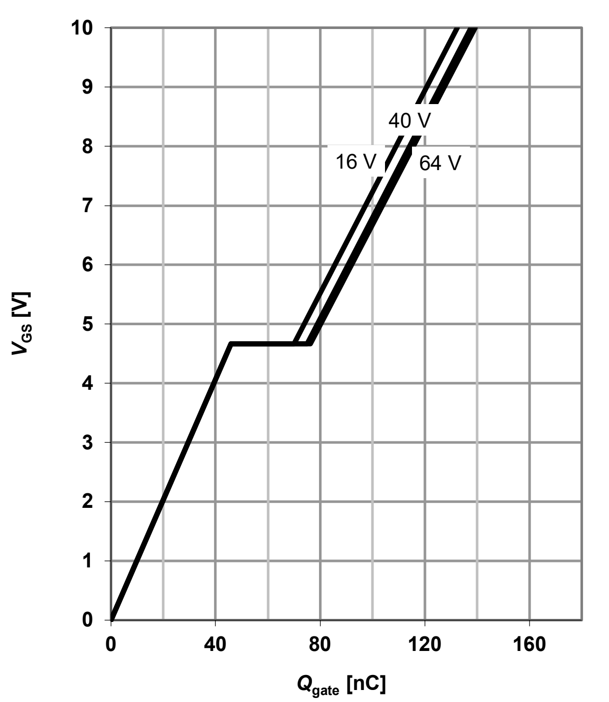
14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; $I_D = 1$ mA

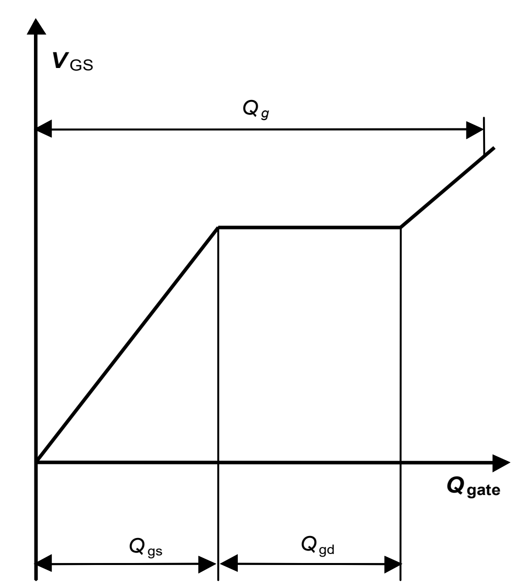


15 Typ. gate charge

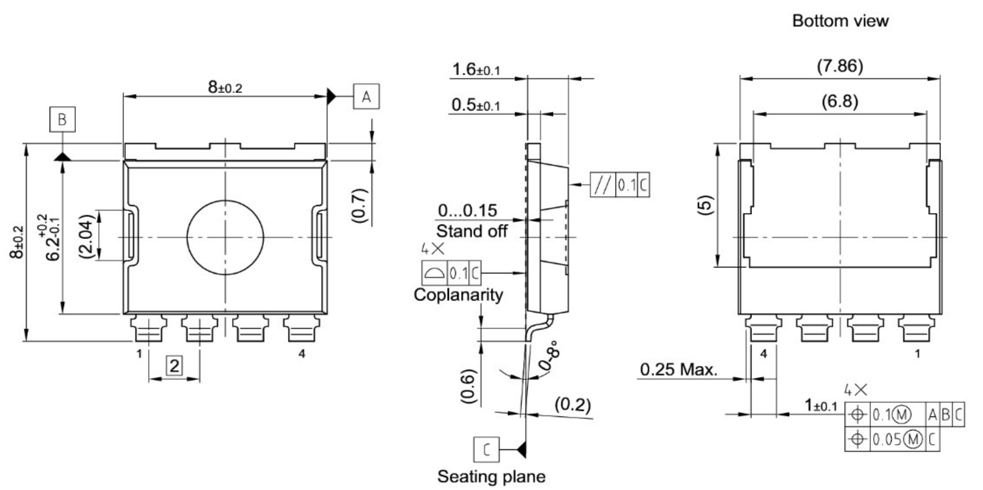
$V_{GS} = f(Q_{gate})$; $I_D = 100$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms

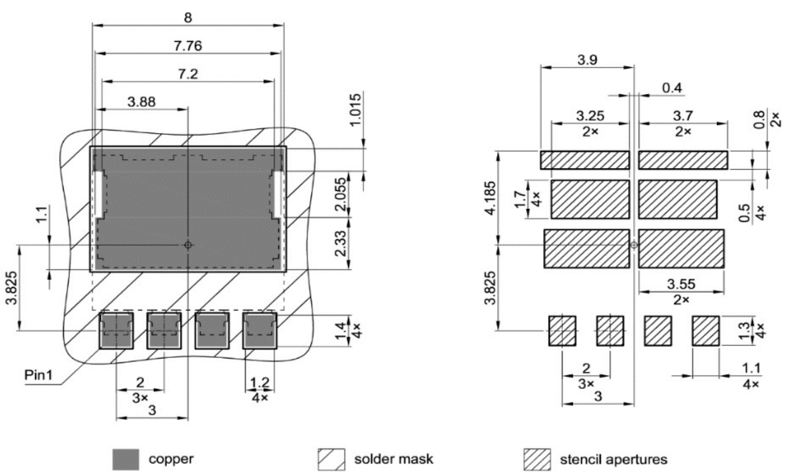


Package Outline



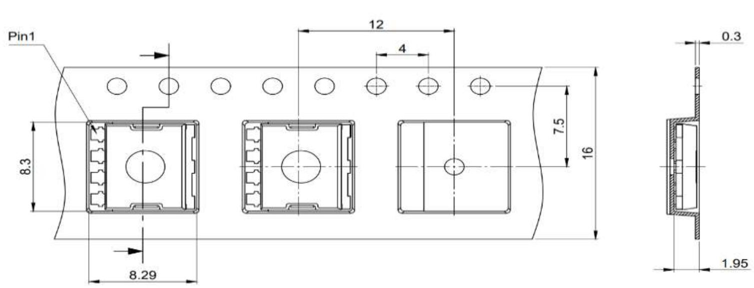
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Footprint



All dimensions are in units mm
All pads are non-solder mask defined

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1

Revision History

Revision	Date	Changes
Revision 1.0	02.05.2024	Final Data Sheet

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-05-02

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have any questions about any aspect of this document?

Email: erratum@infineon.com

Document reference: IAUMN08S5N013G-Data-Sheet-01-Infineon