

OptiMOS™ - 6 Power-Transistor



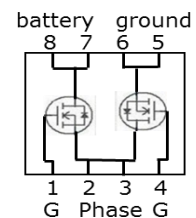
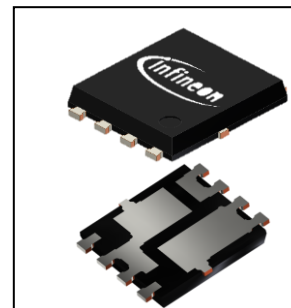
Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	7.0	m Ω
I_D	45	A

Features

- OptiMOS™ - power MOSFET for automotive applications
- Half-Bridge - N-channel - Enhancement mode - Normal Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TDSON-8-57



Type	Package	Marking
IAUC45N04S6N070H	PG-TDSON-8-57	6N04N070

Maximum ratings per channel, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS}=10\text{V}$, Chip Limitation ^{1,2)}	55	A
		$V_{GS}=10\text{V}$, DC current ³⁾	45	
		$T_a=85^\circ\text{C}$, $V_{GS}=10\text{V}$, R_{thJA} on 2s2p ^{2,4)}	14	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$, $t_p=100\mu\text{s}$	119	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=9\text{A}$, $R_{g,min}=25\Omega$	38	mJ
Avalanche current, single pulse	I_{AS}	$R_{g,min}=25\Omega$	9	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	41	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	$^\circ\text{C}$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	3.7	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	-	-	36	-	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=9\mu A$	2.2	2.6	3.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7V, I_D=22A$	-	6.8	9.0	m Ω
		$V_{GS}=10V, I_D=22A$	-	5.6	7.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	539	701	pF
Output capacitance	C_{oss}		-	173	224	
Reverse transfer capacitance	C_{rss}		-	14	21	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=45A, R_G=3.5\Omega$	-	3	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	4	-	
Fall time	t_f		-	2	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32V, I_D=45A,$ $V_{GS}=0 \text{ to } 10V$	-	2.5	3.4	nC
Gate to drain charge	Q_{gd}		-	2.1	3.1	
Gate charge total	Q_g		-	9	12	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	37	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25^\circ C, t_p=100\mu s$	-	-	150	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=22A,$ $T_J=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20V, I_F=45A,$ $di_F/dt=100A/\mu s$	-	16	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	6	-	nC

¹⁾ Practically the current is limited by overall system design including customer specific PCB.

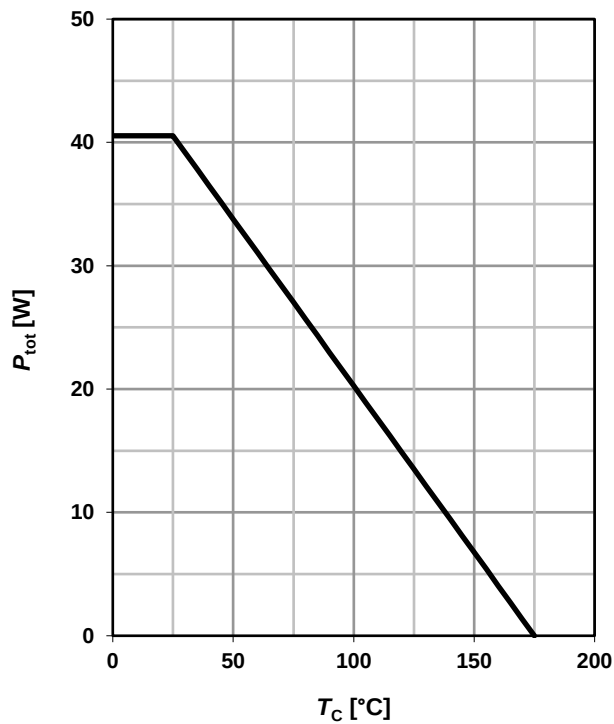
²⁾ The parameter is not subject to production test -specified by design.

³⁾ The product can operate at specified current based on best practice to minimize electromigration at the solder joint. For rare events and inrush currents the value may be exceeded.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

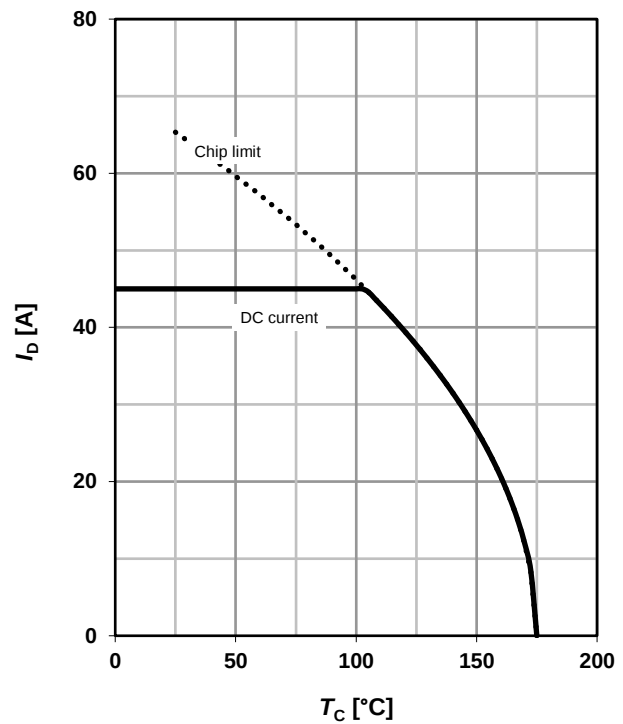
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

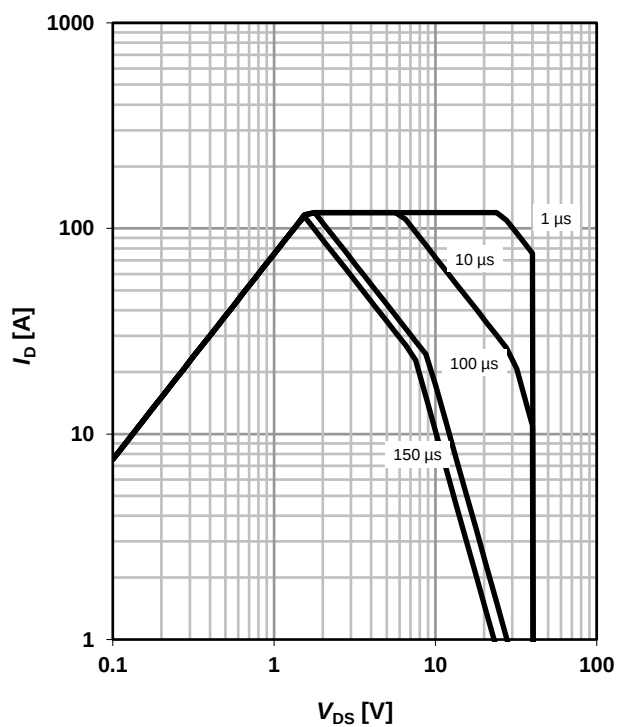
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

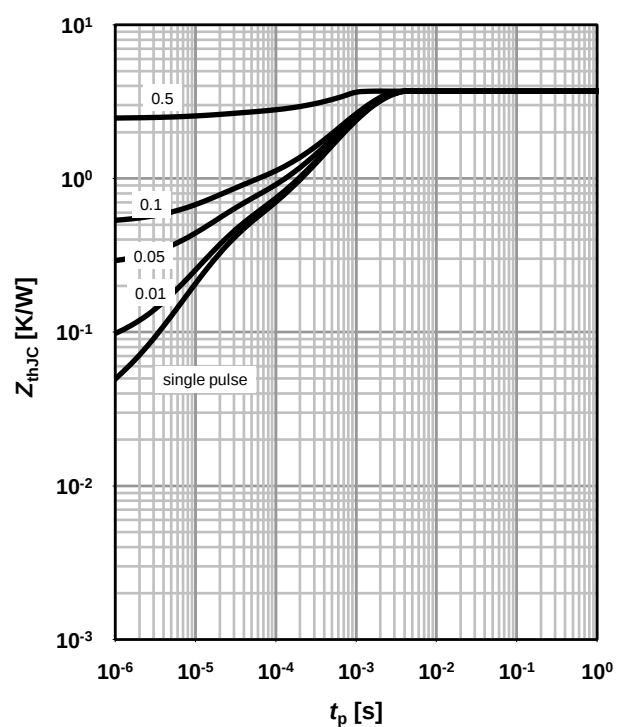
parameter: t_p



4 Max. transient thermal impedance

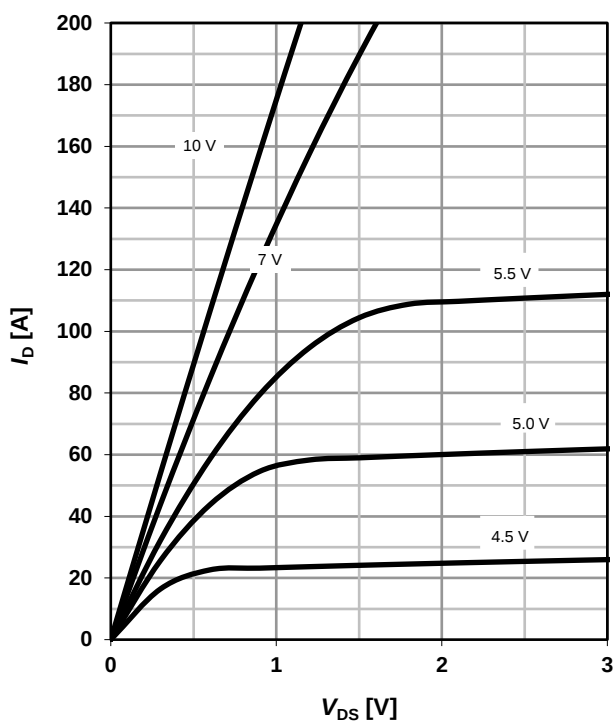
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



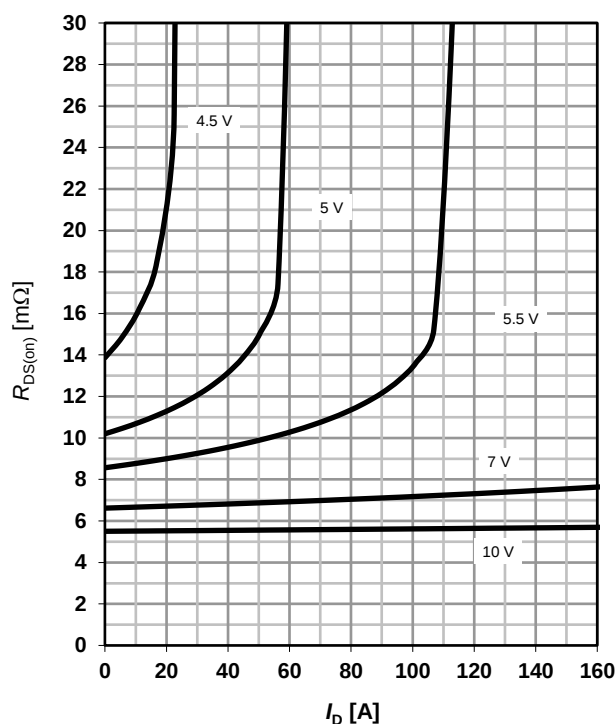
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


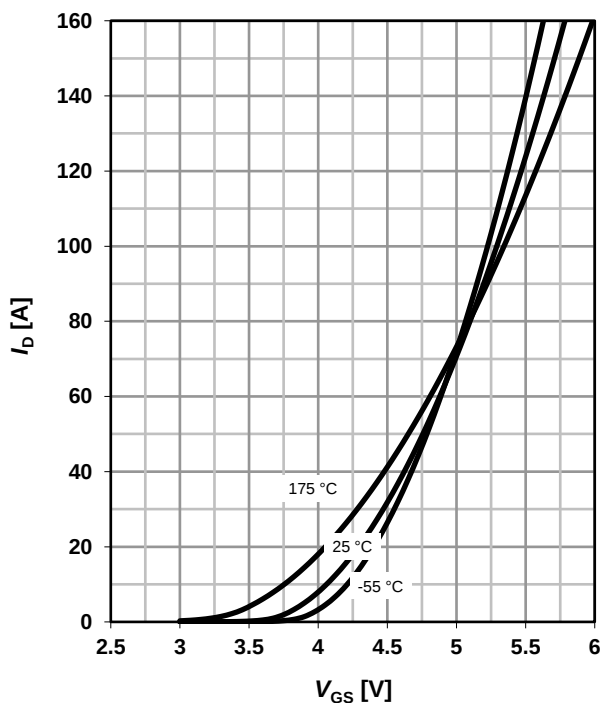
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

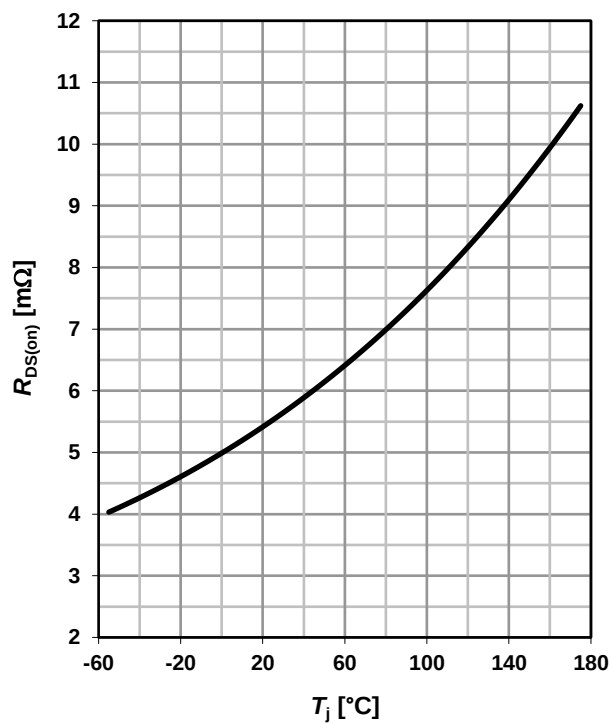
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j


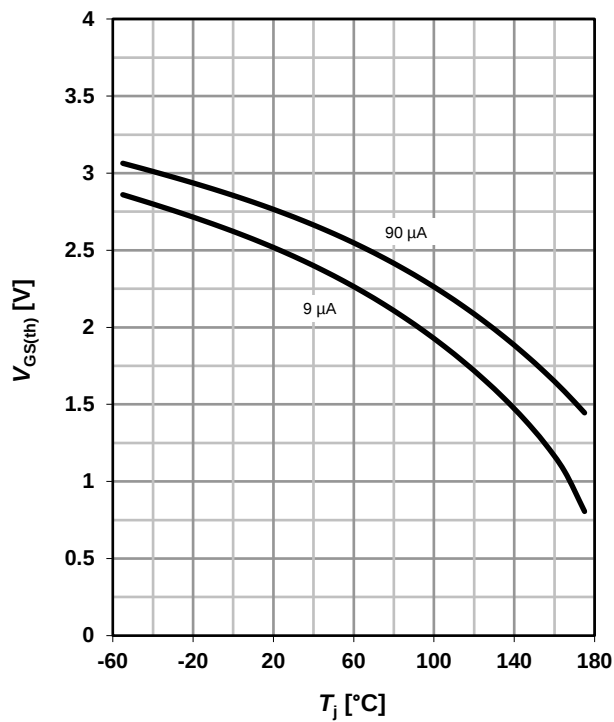
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 22\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

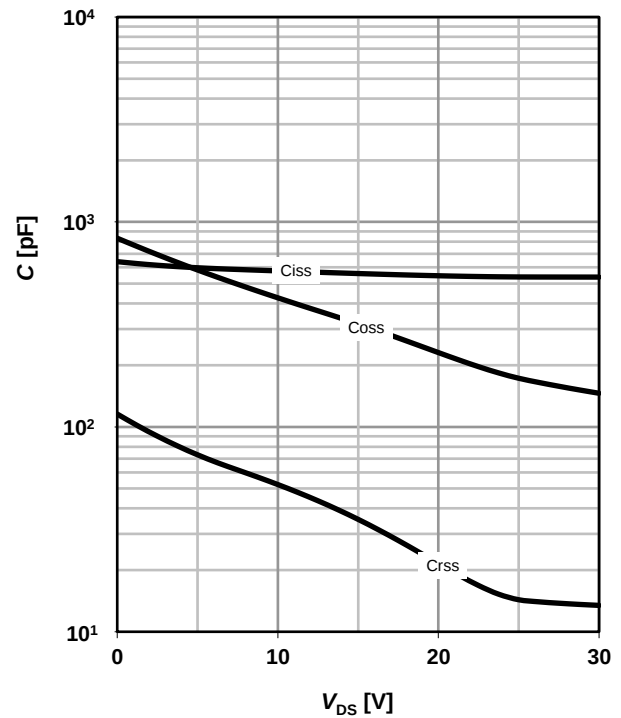
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

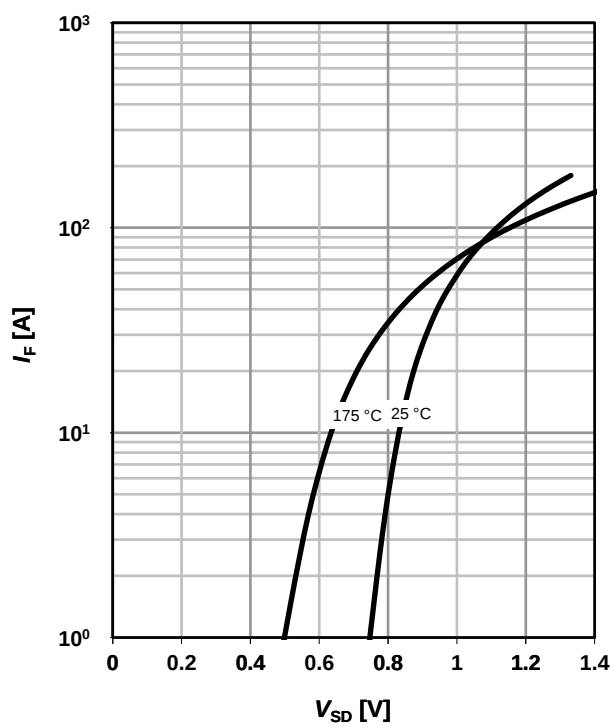
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

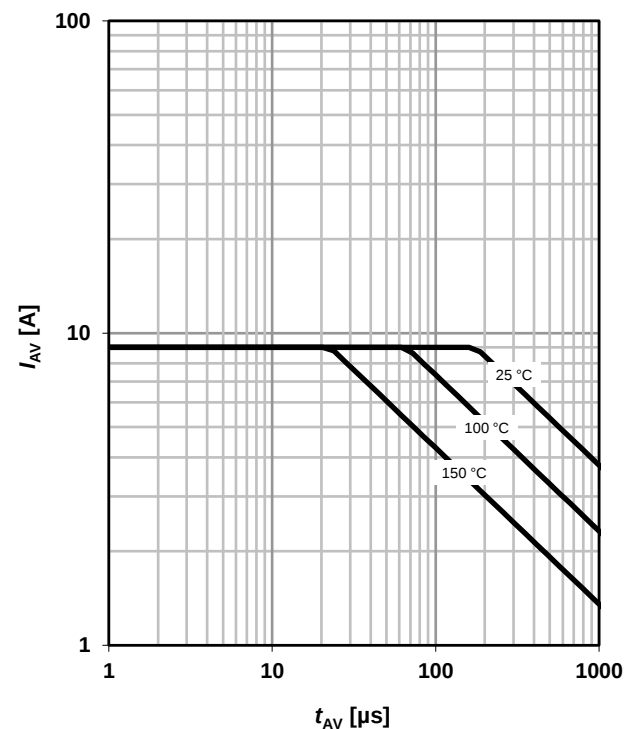
parameter: T_j



12 Avalanche characteristics

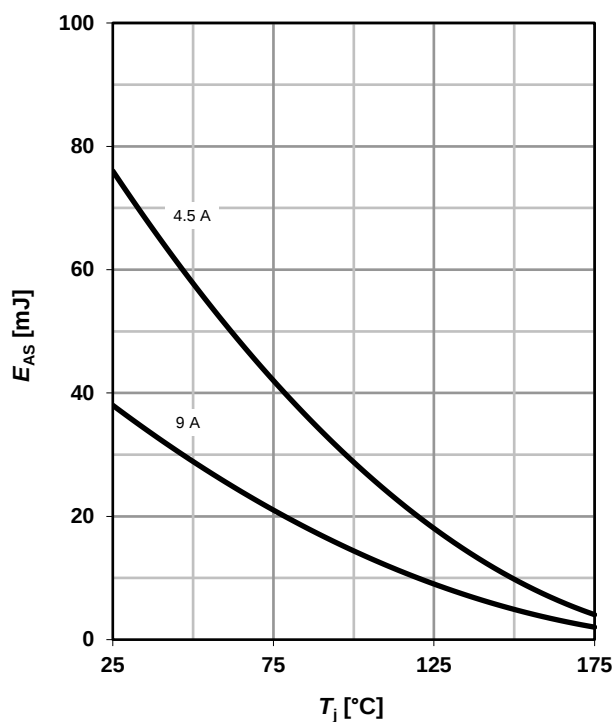
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



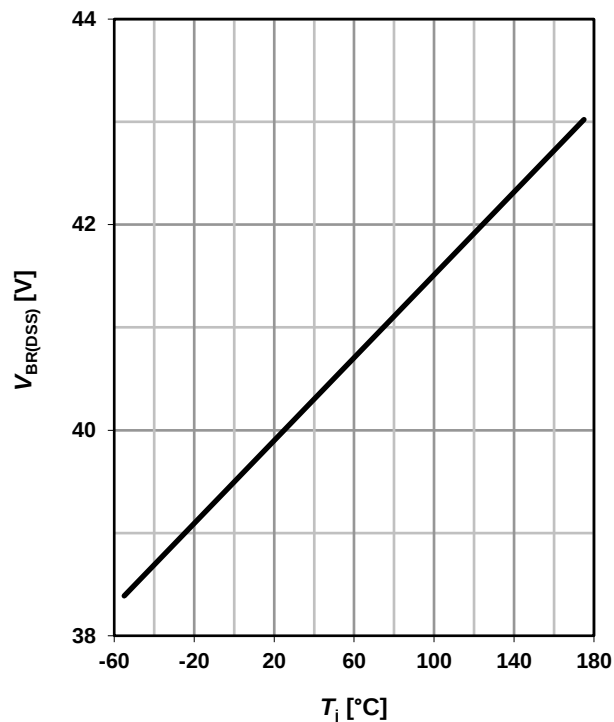
13 Avalanche energy

$$E_{AS} = f(T_j)$$



14 Drain-source breakdown voltage

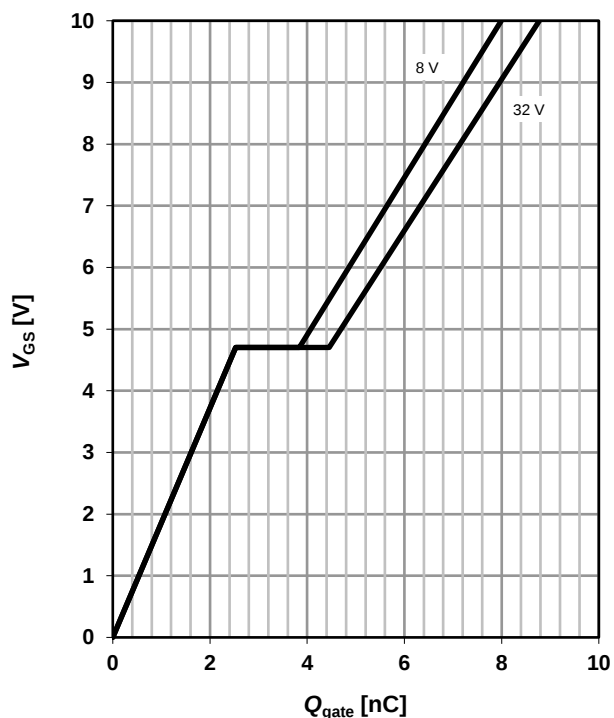
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



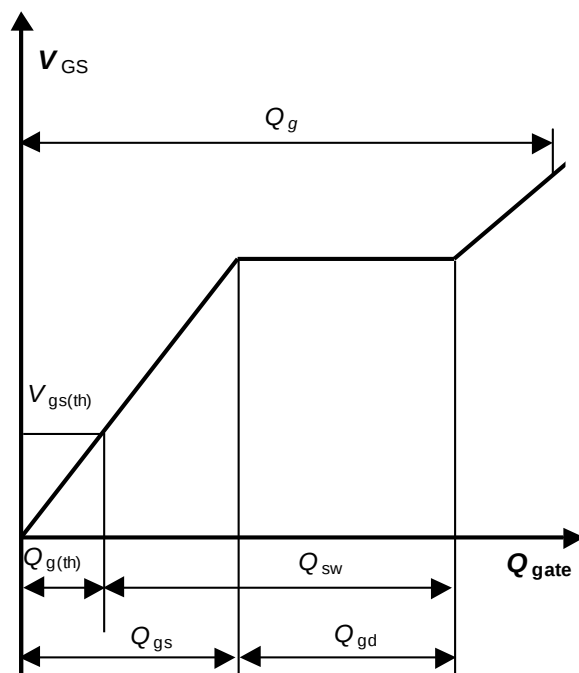
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 22 \text{ A pulsed}$$

parameter: V_{DD}



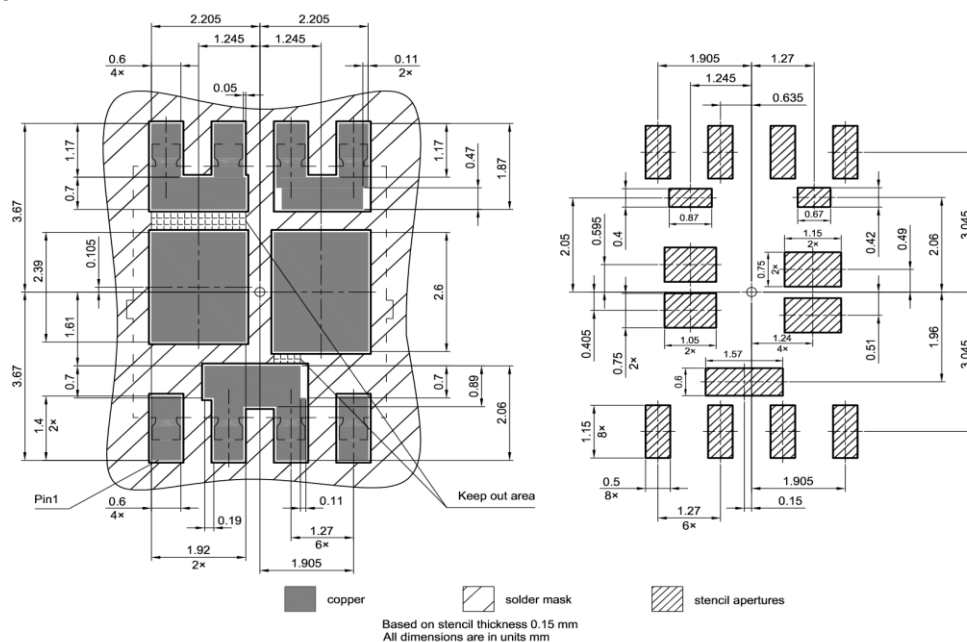
16 Gate charge waveforms



The drawing includes the following views and dimensions:

- Top View:** Shows the package footprint with a width of 5.15 mm and a height of 6.44 mm. Pin 1 is marked with a circle and the letter 'A'. A circular feature is labeled 'Pin1 Marking'. A surface texture symbol indicates a roughness of 0.03 mm.
- Side View:** Shows the package height of 5.48 mm and a lead thickness of 0.25 mm. A dimension of 0.13 mm is shown for the lead width at the base.
- Detail View:** Provides a cross-sectional view of the package with numerous dimensions:
 - Overall width: 4.45 mm
 - Lead width at base: 1.69 mm
 - Lead thickness: 0.43 mm
 - Lead height: 0.9 mm
 - Package body height: 2.85 mm
 - Package body width: 4.23 mm
 - Package body thickness: 0.55 mm
 - Package body width at base: 1.98 mm
 - Package body thickness at base: 0.56 mm
 - Package body width at top: 1.27 mm
 - Package body thickness at top: 0.74 mm
 - Package body width at bottom: 0.91 mm
 - Package body thickness at bottom: 0.42 mm
 - Package body width at top: 0.55 mm
 - Package body thickness at top: 0.25 mm
 - Package body width at bottom: 0.55 mm
 - Package body thickness at bottom: 0.25 mm
 - Package body width at top: 0.55 mm
 - Package body thickness at top: 0.25 mm
 - Package body width at bottom: 0.55 mm
 - Package body thickness at bottom: 0.25 mm

- ## Footprint



Dimensions in mm

1000 Series PCB Mounting Dimensions

Technical drawing showing the top and side views of the component. The top view dimensions are 12 (width) and 5.5 (height). The center-to-center distance between the first two mounting holes is 8, and the distance between the next two is 4. A PIN 1 INDEX MARKING is indicated. The side view shows a thickness of 0.3.

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History

Version	Date	Changes
Revision 1.0	22.09.2020	Final Datasheet

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