15 W auxiliary SMPS for air-conditioner using ICE5AR4770BZS

REF_5AR4770BZS_15W1

About this document

Scope and purpose

This document is a reference design for a 15 W auxiliary SMPS for air-conditioner with the latest Infineon fifth-generation fixed-frequency CoolSET™ ICE5AR4770BZS. The power supply is designed with a universal input compatible with most geographic regions and isolated output (+12 V/1.25 A) as typically employed in most home appliances.

Highlights of the auxiliary power supply for air-conditioner:

- High efficiency under light-load conditions to meet ENERGY STAR requirements
- Simplified circuitry with good integration of power and protection features
- Auto-restart protection scheme to minimize interruption and enhance end-user experience

Intended audience

This document is intended for power supply design or application engineers, etc. who want to design auxiliary power supplies for air-conditioners that are efficient under light-load conditions, reliable and easy to design.

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1 System introduction

With the growing household trend for internet-connected devices, the new generation of home appliances such as air-conditioners are equipped with advanced features such as wireless control and monitoring capability, smart sensors and touch screen displays. These will transform a static product into an interactive and intelligent home appliance, capable of adapting to the smart-home theme. To support this trend, Infineon has introduced the latest fifth-generation fixed-frequency CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules and sensors, which typically operate from a stable DC voltage source. The Infineon CoolSET™ (as shown in Figure 1) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

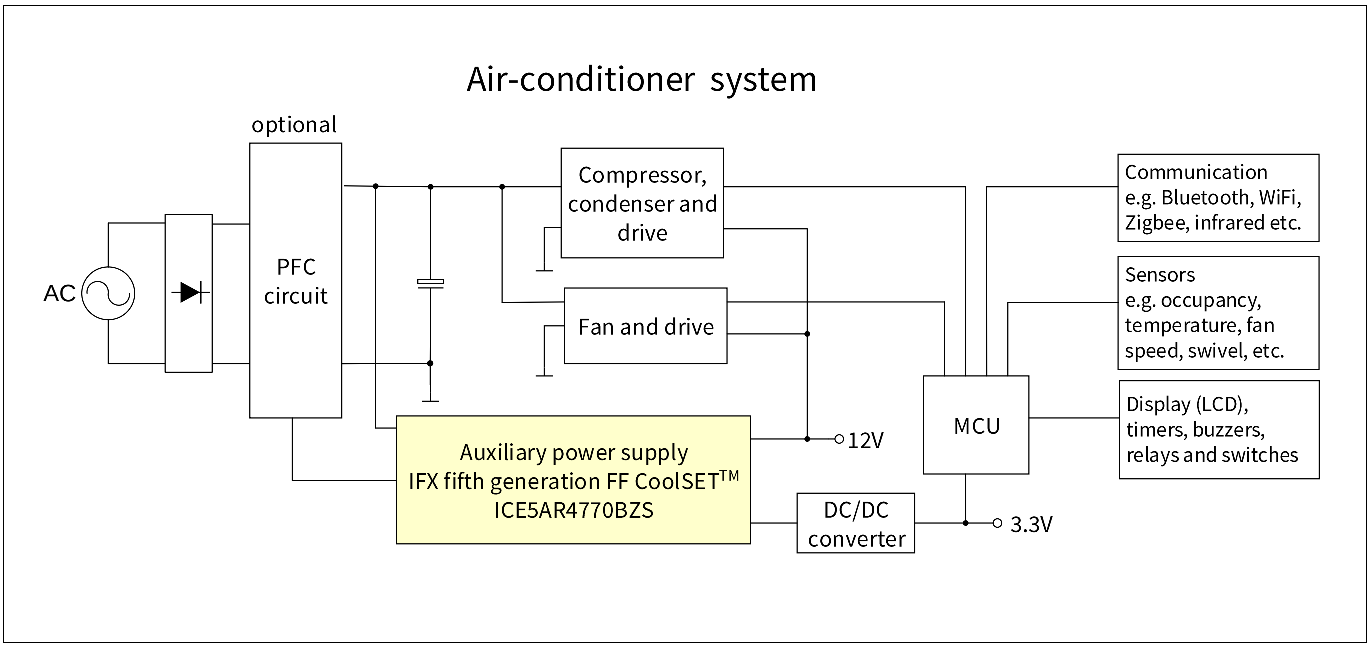


Figure 1 Simplified air-conditioner system block diagram

Table 1 lists the system requirements for an air-conditioner, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for air -conditioner	Infineon solution – ICE5AR4770BZS
1	High efficiency under light-load conditions to meet ENERGY STAR requirements	New fixed-frequency control and Active Burst Mode (ABM)
2	Simplified circuitry with good integration of power and protection features	Embedded 700 V MOSFET and controller in DIP-7 package
3	Auto-restart protection scheme to minimize interruption to enhance end-user experience	All abnormal protections are in auto restart

1.1 High efficiency under light-load conditions to meet ENERGY STAR requirements

During typical air-conditioner operation, the power requirement fluctuates according to various use cases. However, in most cases where room temperature is already stabilized, the air-conditioner will reside in an idle state in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for most of the period. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency play a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5AR4770BZS was primarily chosen due to its frequency reduction switching scheme. Compared with a traditional fixed-frequency flyback, the CoolSET™ reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, CoolSET™ is a highly integrated device with both a controller and HV MOSFET integrated into a single, space-saving DIP-7 package. These certainly help the designer to reduce component count as well as simplifying the layout into a single-layer PCB design for ease of manufacturing, using the traditional cost-effective wave-soldering process.

1.3 Auto-restart protection scheme to minimize interruption to enhance end-user experience

For an air-conditioner, it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the CoolSET™ implements auto-restart mode for all abnormal protections.

2 Reference design board

This document provides complete design details including specifications, schematics, Bill of Materials (BOM), and PCB layout and transformer design and construction information. This information includes performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans, etc.

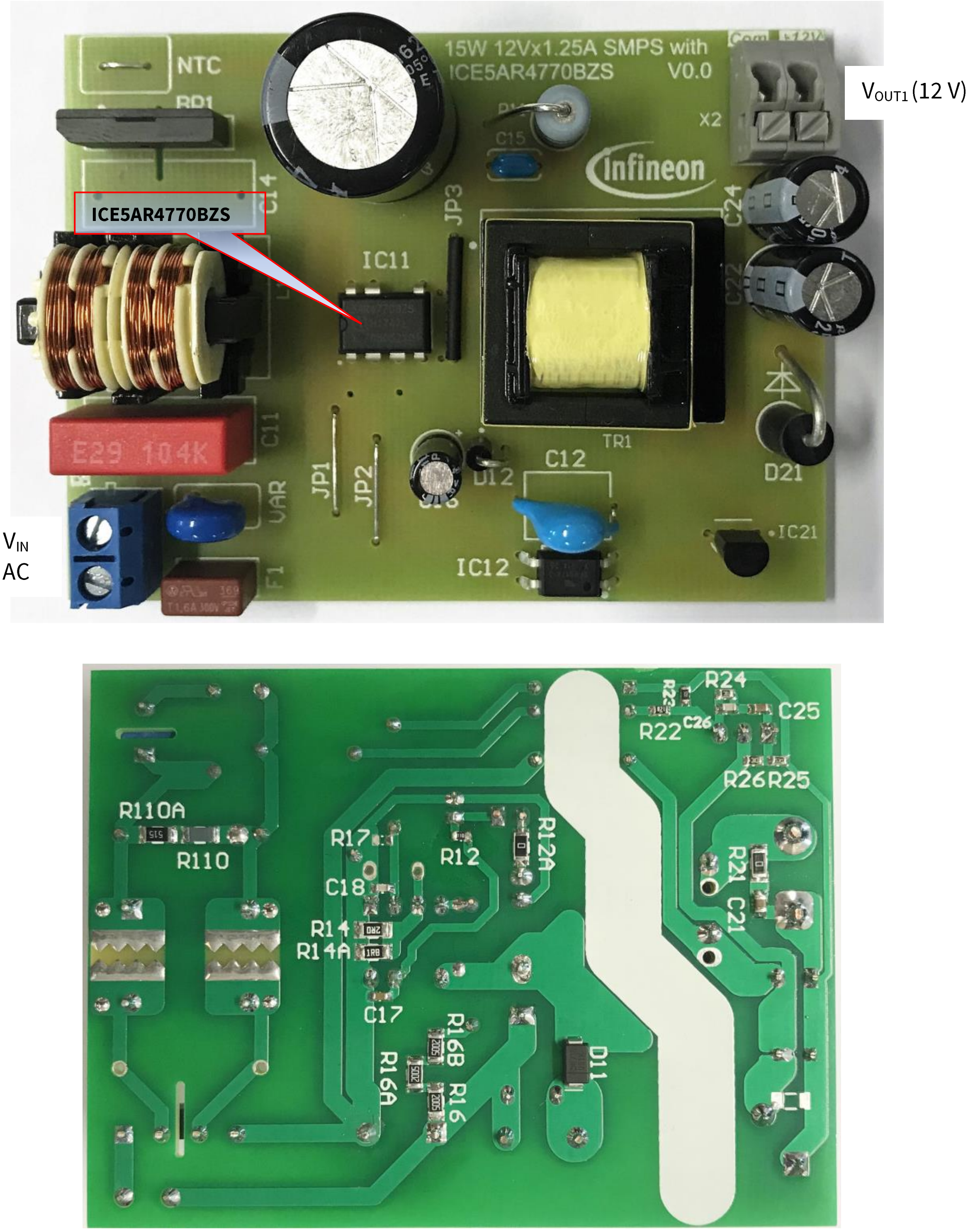


Figure 2 **REF_5AR4770BZS_15W1**

3 Power supply specifications

The table below represents the minimum acceptance performance of the design. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5AR4770BZS_15W1

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	90	–	264	V AC	Two wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	–	0.06	W	220 V AC
360 mW load input power	P_{stby_ML}	–	–	0.55	W	220 V AC
Output						
Output voltage	V_{OUT}	–	12	–	V	±3 percent
Output current	I_{OUT}	0.030	0.625	1.25	A	
Output voltage ripple	V_{RIPPLE}	–	–	240	mV	20 MHz BW
Max. power output	P_{OUT_Max}	–	–	15	W	
Output Over Voltage Protection (OVP)		-	18	-	V	Short R26 resistor during system operation at no load
Efficiency						
Max. load	η	–	83	–	Percent	115 V AC/220 V AC
Average efficiency at 25 percent, 50 percent, 75 percent and 100 percent of P_{OUT_Max}	η_{avg}	84	–	–	Percent	115 V AC/220 V AC
Environmental						
Conducted EMI		7	–	–	dB	Margin, CISPR 22 class B
ESD		8	–	–	kV	EN 61000-4-2
Surge immunity						EN 61000-4-5
Differential Mode (DM)		2	–	–	kV	
Common Mode (CM)		4	–	–	kV	
Ambient temperature	T_{amb}	0	–	50	°C	Free conviction, sea level
Form factor		60 × 80 × 32			mm^3	L × W × H

4 Circuit diagram

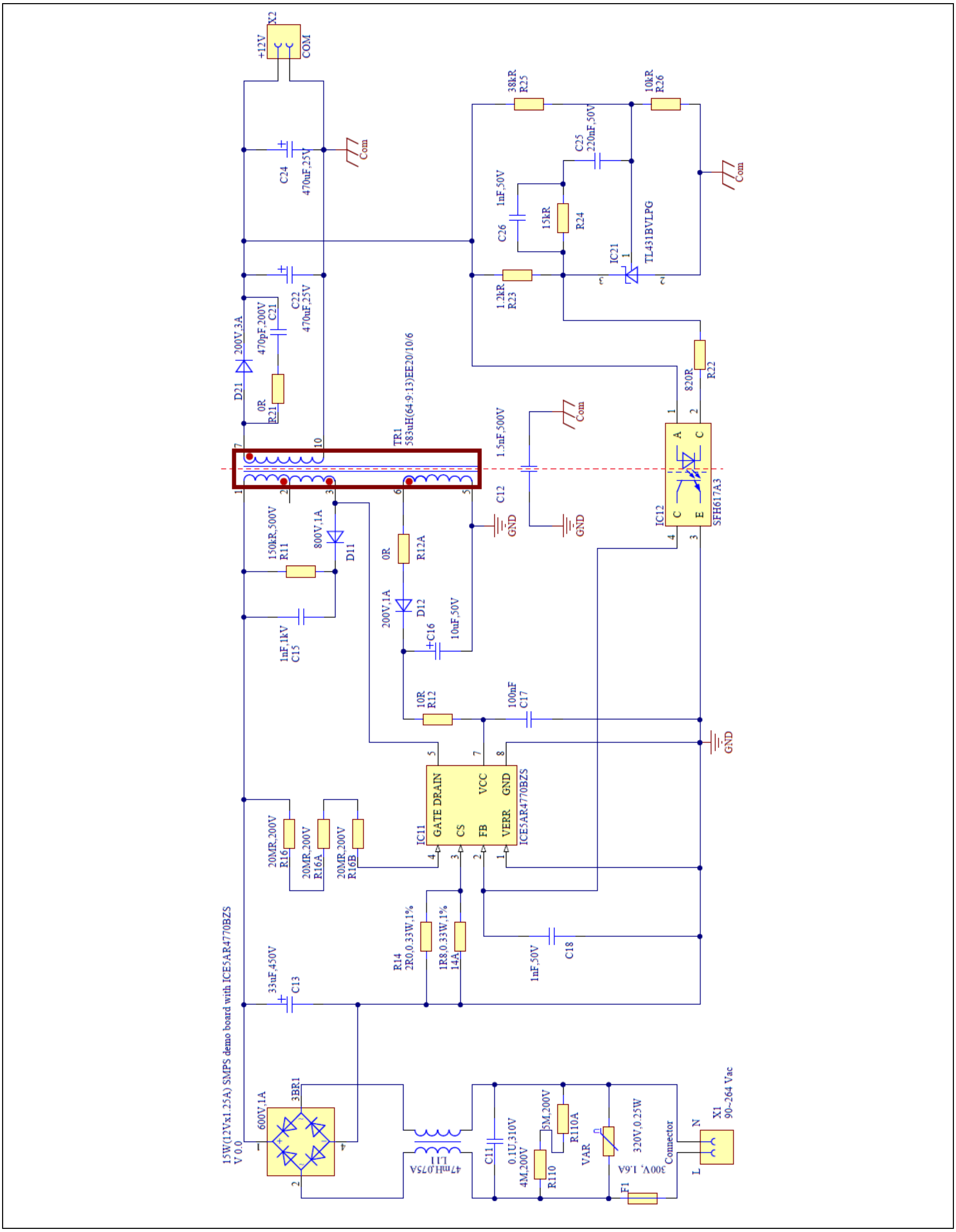


Figure 3 Schematic of REF_5AR4770BZS_15W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide [2] and calculation tool [3].

5.1 EMI filtering and line rectification

The input of the power supply unit is taken from the AC power grid, which is in the range of 90 V AC ~ 264 V AC. The fuse F1 is right at the entrance to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR, which is connected across L and N to absorb the line surge transient. Inductors L11 and C11 form a filter to attenuate the DM and CM conducted EMI noise. C11 must be X-capacitor grade. There are optional spark-gap devices SA1 and SA2 to absorb further higher surge level transient if required by the system. Resistors R110 and R110A are used to discharge the X-capacitor when the AC is off in order to fulfill the IEC61010-1 and UL1950 safety requirements. The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the bulk capacitor, C13.

5.2 Flyback converter power stage

The flyback converter power stage consists of C13, transformer TR1, a primary HV MOSFET (integrated into ICE5AR4770BZS), secondary rectification diodes D21 and secondary output capacitors C22 and C24.

When the primary HV MOSFET turns on, some energy is stored in the transformer. When it turns off, the stored energy is released to the output capacitors and the output loading through the output diode D21.

Sandwich winding structure for the transformer TR1 is used to reduce the leakage inductance, and so the loss in the clamper circuit is reduced. TR1 has single output windings, the V_{OUT} (12 V). The output rectification of V_{OUT} is provided by the diode D21 through filtering of C22 and C24. All the secondary capacitors must be the low-ESR type, which can effectively reduce the switching ripple. Together with the Y-capacitor C12 across the primary and secondary side, the EMI noise can be further reduced to comply with CISPR 22 specifications.

5.3 Control of flyback converter through fifth-generation fixed-frequency CoolSET™ ICE5AR4770BZS

5.3.1 Integrated HV power MOSFET

The ICE5AR4770BZS CoolSET™ is a seven-pin device in a DIP-7 package. It has been integrated with the new fixed-frequency PWM controller and all necessary features and protections, and most importantly the 700 V power MOSFET, Infineon Superjunction (SJ) CoolMOS™. Hence, the schematic is much simplified and the circuit design is made much easier.

5.3.2 Current Sensing (CS)

The ICE5AR4770BZS is a current mode controller. The peak current is controlled cycle-by-cycle through the CS resistors R14 and R14A in the CS pin (pin 3) and so transformer saturation can be avoided and the system is more robust and reliable.

5.3.3 Feedback and compensation network

Resistor R25 is used to sense the V_{OUT} and feedback (FB) to the reference pin (pin 1) of error amplifier IC21 with reference to the voltage at resistor R26. A type 2 compensation network C25, C26 and R24 is connected between the output pin (pin 3) and the reference pin (pin 2) of the IC21 to stabilize the system. The IC21 further connects to pin 2 of the optocoupler, and IC12 with a series resistor R22 to convert the control signal to the primary side through the connection of pin 4 of the IC12 to ICE5AR4770BZS FB pin (pin 2) and complete the control loop. Both the optocoupler IC12 and the error amplifier IC21 are biased by V_{OUT}; IC12 is a direct connection while IC21 is through an R23 resistor.

The FB pin of ICE5AR4770BZS is a multi-function pin which is used to select the entry burst power level (there are three levels available) through the resistor at the FB pin (R17) and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth-generation fixed-frequency CoolSET™ ICE5AR4770BZS to support the requirements of air-conditioner auxiliary power

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC start-up uses the cascode structure integrated into the package to charge up the V_{CC} capacitor during the start-up stage [2]. The GATE pin (pin 4) is a multi-function pin and it serves as the start-up pin with the connection of pull-up resistors R16, R16A and R16B, which has the other end connecting to the bus voltage during the start-up phase. The device is implemented with two steps of charging current: the smaller current 0.2 mA (V_{VCC_typ} = 0 V ~ 1.1 V) and the larger current 3.2 mA (V_{VCC_typ} = 1.1 V ~ 16 V). The start-up time is the sum of those two charging times. With the V_{CC} capacitor C16 at 10 µF, the start-up time is shortened to around 0.15 s.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer TR1, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.) through the rectifier circuit D12, R12, R12A and C16.

5.4.2 CCM, DCM operation with frequency reduction

ICE5AR4770BZS can be operated in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) with frequency-reduction features. This reference board is designed to operate in DCM. When the system is operating at maximum power, the controller will switch at the fixed frequency of 100 kHz. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented, and the reduction curve is shown in Figure 4. The V_{CS} is clamped by the current limitation threshold or by the PWM op-amp while the switching frequency is reduced. After the maximum frequency reduction, the minimum switching frequency is f_{OSC2_MIN} (43 kHz).

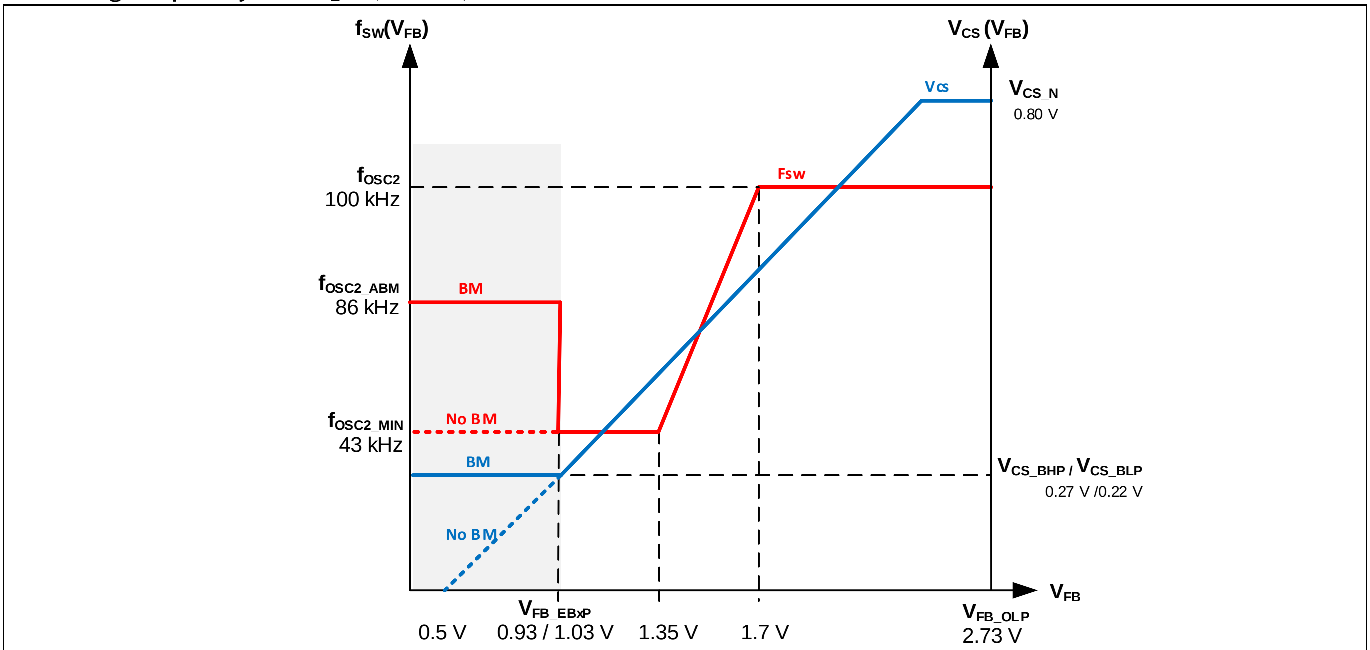


Figure 4 Frequency-reduction curve

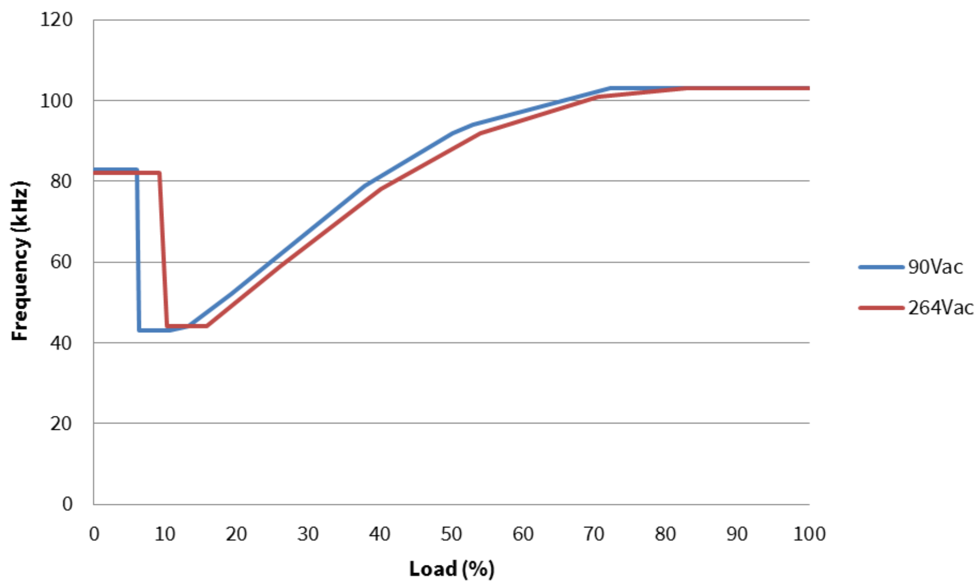


Figure 5 Frequency-reduction curve of REF_5AR4770BZS_15W1

The measured frequency-reduction curve of REF_5AR4770BZS_15W1 is shown in Figure 5.

5.4.3 Frequency jittering with modulated gate drive

The ICE5AR4770BZS has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 100 kHz (±4 kHz), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5AR4770BZS provides comprehensive protection to ensure the system is operating safely. This includes V_{CC} OV and Under Voltage (UV), over-load, over-temperature (controller junction), CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions is shown in the table below.

Table 3 Protection functions of ICE5AR4770BZS

Protection function	Failure condition	Protection mode
V_{CC} OV	V_{VCC} greater than 25.5 V	Odd-skip auto restart
V_{CC} UV	V_{VCC} less than 10 V	Auto restart
Over-load	V_{FB} greater than 2.75 V and lasts for 54 ms	Odd-skip auto restart
Over-temperature (junction temperature of controller chip only)	T_J greater than 140°C	Non-switch auto restart
CS short-to-GND	V_{CS} less than 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto restart
V_{CC} short-to-GND (V_{VCC} = 0 V, start-up = 50 MΩ and V_{DRAIN} =	V_{VCC} less than 1.1 V, $I_{VCC\_Charge1}$ ≈ -0.2 mA	Cannot start up

Protection function	Failure condition	Protection mode
90 V)		

5.5 Clamper circuit

A clamper network, D11, C15 and R11, is used to reduce the switching spikes for the drain pin, which are generated from the leakage inductance of the transformer TR1. This is a dissipative circuit and the selection of the R11 and C15 needs to be fine-tuned.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The power loop needs to be as small as possible (see Figure 6). There are two power loops in the demo design; one from the primary side and one from the secondary side. For the primary side, it starts from the bulk capacitor (C13) positive to the bulk capacitor negative. The power loop components include C13, the main primary transformer winding (pin 1 and pin 1 of TR1), the DRAIN pin and the CS pin of the CoolSET™ IC11 and CS resistors R14 and R14A. For the secondary side, the 12 V output starts from the secondary transformer windings (pin 7 of TR1), output diode D21 and output capacitors C22 and C24.
- Star ground concept should be used to avoid unexpected HF noise coupling affecting control. The ground of the small-signal components, e.g. C17 and C18, and the emitter of the optocoupler (pin 3 of IC12) etc. should connect directly to the IC ground (pin 8 of IC11). Then it connects to the negative terminal of the C13 capacitor directly.

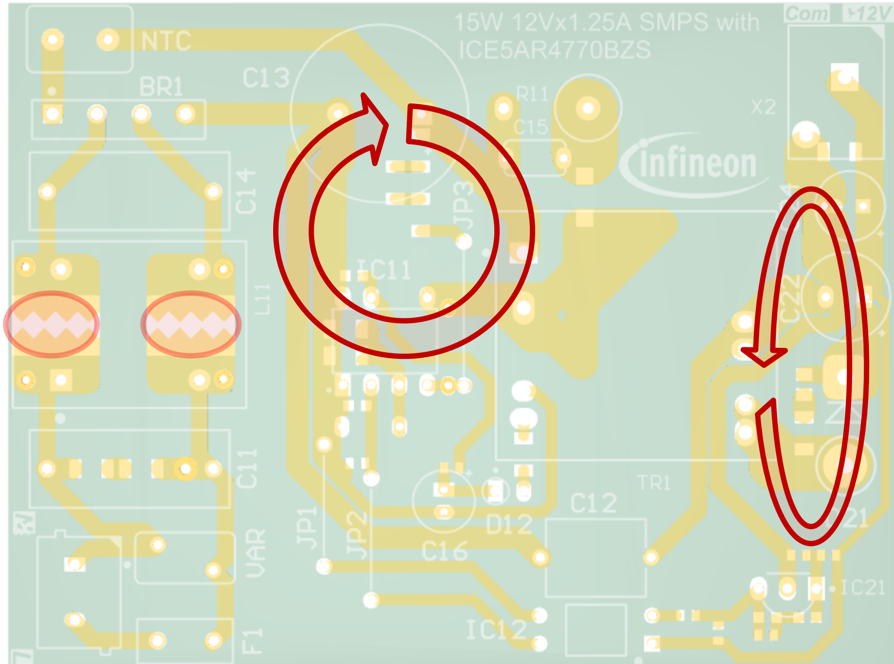


Figure 6 **PCB layout tips**

- Adding the spark-gap (PCB saw-tooth, 0.5 mm separation) pattern under the input CM Choke (CMC) L11 can increase the system input line surge capability.
- Separating the HV components and LV components, e.g. the clamper circuit (D11, R11 and C15) at the top part of the PCB (see Figure 6) and the other LV components at the lower part of the PCB, can reduce the spark-over chance of the high energy surge during ESD or a lightning surge test.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve satisfactory EMI performance.

- Good transformer winding coupling is very important. Without this there would be high leakage inductance and a lot of switching spike and HF noise. The most effective method is to adopt sandwich winding (see Figure 10) where the secondary winding is in the middle of the winding and covered by the primary winding on the bottom and top layer. Shielding the transformer can reduce the HF noise. The outermost shield wrapped around the transformer cores with copper foil can help to reduce leakage flux and reduce the noise coupling to nearby components. The inner shield (copper foil or copper wire winding) between the transformer windings can help to reduce the parasitic capacitance and reduce the HF noise coupling. Both shields need to tie to the negative of C13 to achieve the best performance, but note that the inner shield approach would result in more energy loss.
- Short power loop design in PCB (as described in section 5.6) and terminate to the low ESR capacitor such as C13 for primary-side loop and C22 and C24 for the secondary-side loop. It can help to reduce the switching ripple which comes out to the input terminals V_{IN}. In addition, adding a low-ESR ceramic capacitor in parallel to the C13/C22/C24 can help to further reduce the switching ripple.
- Sufficient input LC (L11 and C11) filter design is important to pass the EMI requirement. Note that the most effective capacitor is C11, which has the best filtering capability to the switching ripple.
- The Y-capacitor C12 has a function to return the HF noise to the source (negative of C13) and reduce the overall HF noise going out to the input terminals. The larger capacitance is more effective. However, larger values would introduce larger leakage current and may fail the safety requirements.

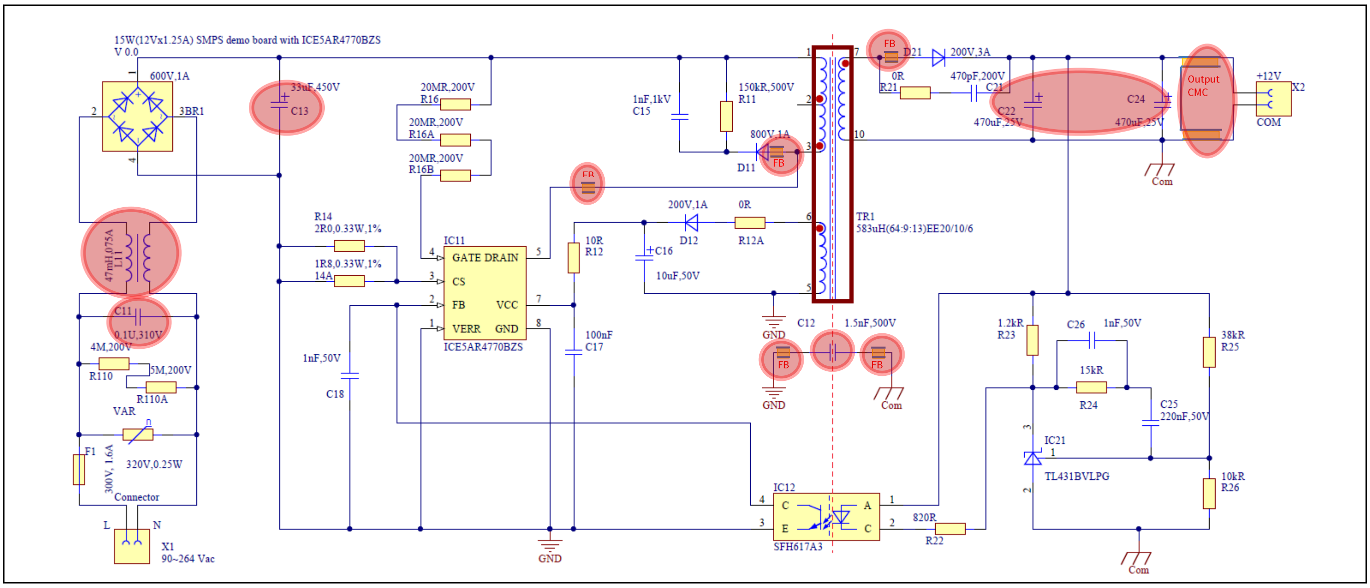


Figure 7 EMI reduction tips

- Adding DRAIN to CS pin capacitor for the MOSFET of the CoolSET™ can reduce the high switching noise. However, it also reduces efficiency.
- Adding a ferrite bead to the critical nodes of the circuit can help to reduce the HF noise, such as the connecting path between the transformer and the drain pin, clamper diode D11, output diode D21, Y-capacitor C12, etc.
- Adding additional output CMC can also help to reduce the HF noise.

6 PCB layout

6.1 Top side

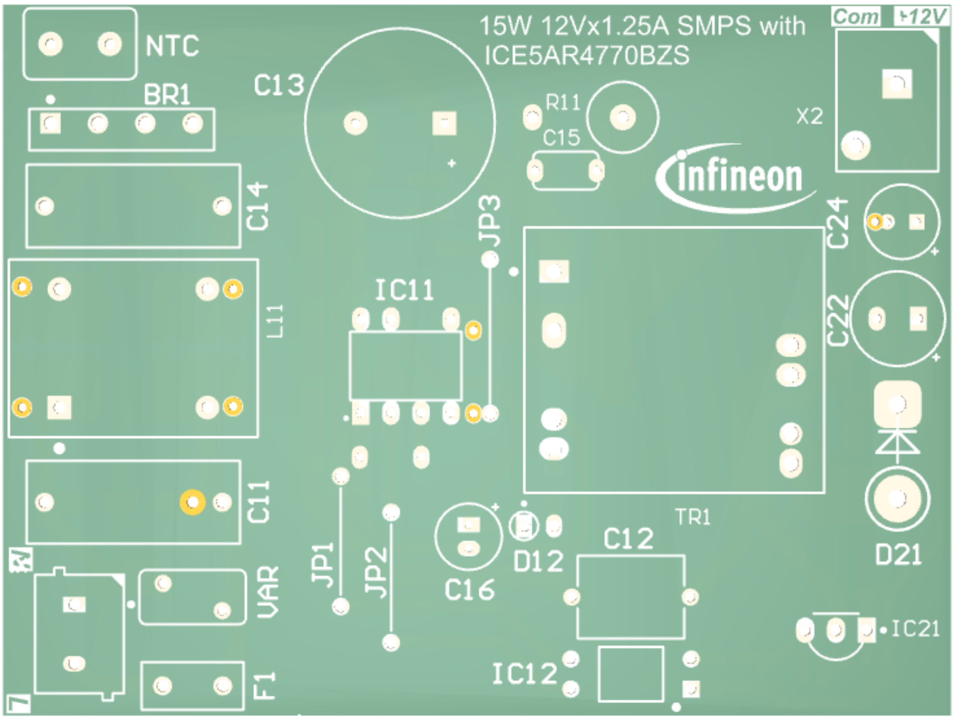


Figure 8 Top-side component legend

6.2 Bottom side

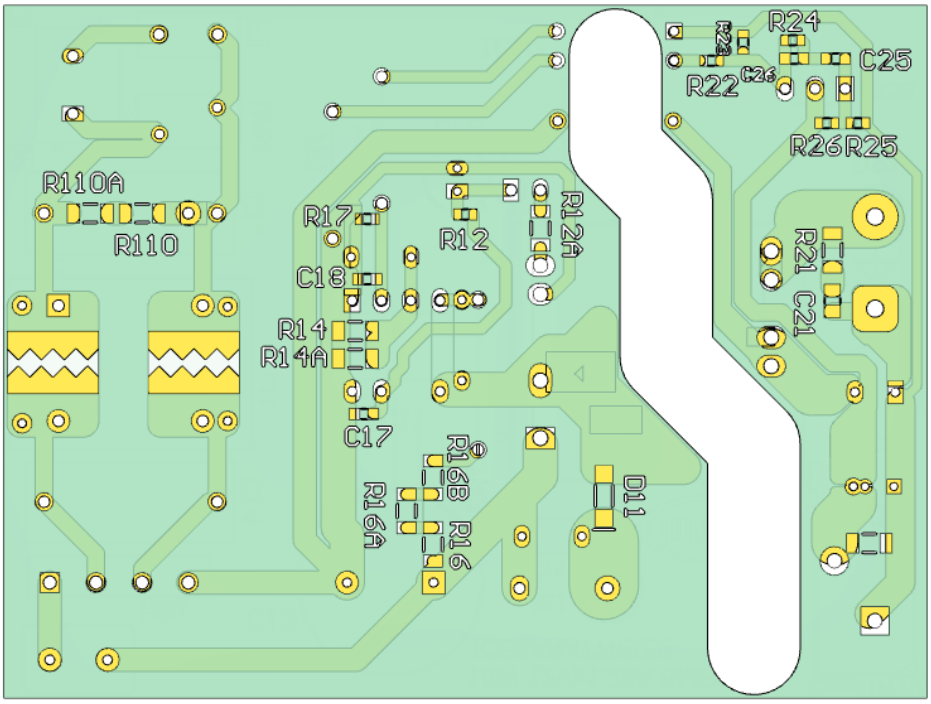


Figure 9 Bottom-side copper and component legend

7 BOM

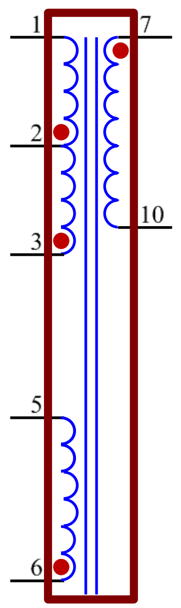
Table 4 BOM (V 0.0)

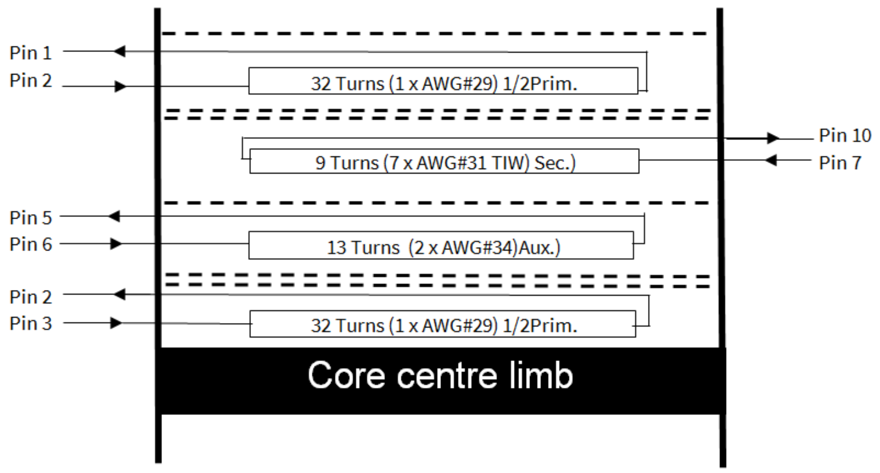
No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V,1 A	S1VBA60	Shindengen	1
2	C11	0.1 U, 310 V	890334025017	Wurth Electronics	1
3	C12	1.5 nF, 500 V	DE1E3RA152MA4BQ01F	Murata	1
4	C13	33 µF, 450 V	450BXC33MEFC16X25	Rubycon	1
5	C15	1 nF, 1000 V	RDE7U3A102J2K1H03	Murata	1
6	C16	10 µF, 50 V	50PX10MEFC5X11	Rubycon	1
7	C17	100 nF	GRM188R71H104KA93D	Murata	1
8	C18, C26	1 nF, 50 V	GRM1885C1H102GA01D	Murata	2
9	C21	470 pF, 250 V	GRM21A5C2E471JWA1#	Murata	1
10	C22, C24	470 µF, 25 V	25ZLG470MEFC8X20	Rubycon	2
11	C25	220 nF, 50 V	GRM188R71H224KAC4D	Murata	1
12	D11	800 V, 1 A	US1K		1
13	D12	200 V, 1 A	1N4003		1
14	D21	200 V, 3 A	UF5402		1
15	F1	300 V, 1.6 A	36911600000		1
16	IC11	ICE5AR4770BZS	ICE5AR4770BZS	Infineon	1
17	IC12	Optocoupler, CTR 100 ~ 200 percent DIP-4	SFH617A-3X006		1
18	IC21	2.5 V shunt regulator, TO92	TL431BVLPG		1
19	JP1, JP2, NTC	Jumper			3
20	JP3	Inulated jumper			1
21	L11	47 mH, 0.75 A	750342434	Wurth Electronics	1
22	R11	150 kR	MO2CT631R154J		1
23	R12	10 R	0603 Resistor		1
24	R12A, R21	0 R	1206 Resistor		2
25	R14	2R0, 0.33 W, 1 percent	ERJ8BQF2R0V		1
26	R14A	1R8, 0.33 W, 1 percent	ERJ-8BQF1R8V		1
27	R16, R16A, R16B	20 MR, 200 V	1206 Resistor		3
28	R22	820 R	0603 Resistor		1
29	R23	1.2 kR	0603 Resistor		1
30	R24	15 kR	0603 Resistor		1
31	R25	38 kR	0603 Resistor		1
32	R26	10 kR	0603 Resistor		1
33	R110	4 M, 200 V	1206 Resistor		1
34	R110A	5 M, 200 V	1206 Resistor		1
35	TR1	583 µH (64:9:13) EE20/10/6	750343814 (Rev. 03)	Wurth Electronics	1
36	VAR	320 V, 0.25 W	B72207S2321K101	Epcos	1
37	X1	Connector	691 102 710 002	Wurth Electronics	1
38	X2	Connector	691 412 120 002B	Wurth Electronics	1

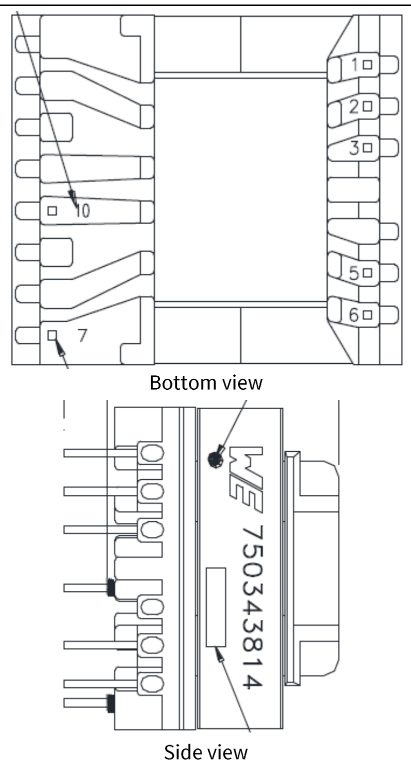
8 Transformer specification

(Refer to Appendix A for transformer design and Appendix B for WE transformer specification.)

- Core and materials: EE20/10/6, TP4A (TDG)
- Bobbin: 070-5643 (14-pin, THT, horizontal version)
- Primary inductance: L_p = 583 µH (±10 percent), measured between pin 4 and pin 6
- Manufacturer and part number: Wurth Electronics Midcom (750343814) Rev. 03







Start	Stop	Turns	Wire size	Layer
3	2	32	1 × AWG#29	½ primary
6	5	13	2 × AWG#34	Auxiliary
7	10	9	7 × AWG#31 TIW	Secondary
2	1	32	1 × AWG#29	½ primary

Figure 10 Transformer structure

9 Measurement data and graphs

Table 5 Measurement data

Input (V AC/Hz)	Description	P_{in} (W)	V_{OUT1} (V DC)	I_{OUT1} (A)	P_{out} (W)	η (percent)	$η_{avg}$ (percent)	P_{in_OLP} (W)	I_{out1_OLP} (A)
90/60	No load	0.05	12.09	0.000				25.70	1.69
	Min. load	0.51	12.09	0.030	0.36	71.12			
	1/20 load	0.99	12.09	0.063	0.76	76.33			
	1/10 load	1.90	12.09	0.125	1.51	79.54			
	1/4 load	4.53	12.09	0.313	3.78	83.40	83.01		
	Typ. load	9.03	12.09	0.625	7.56	83.68			
	3/4 load	13.61	12.09	0.938	11.33	83.28			
	Max. load	18.50	12.09	1.250	15.11	81.69			
115/60	No load	0.05	12.09	0.000				25.30	1.72
	Min. load	0.50	12.09	0.030	0.36	72.54			
	1/20 load	0.98	12.09	0.063	0.76	77.10			
	1/10 load	1.89	12.09	0.125	1.51	79.96			
	1/4 load	4.49	12.09	0.313	3.78	84.15	84.41		
	Typ. load	8.90	12.09	0.625	7.56	84.90			
	3/4 load	13.37	12.09	0.938	11.33	84.77			
	Max. load	18.03	12.09	1.250	15.11	83.82			
220/50	No load	0.06	12.09	0.000				25.02	1.77
	Min. load	0.50	12.09	0.030	0.36	72.54			
	1/20 load	1.00	12.09	0.063	0.76	75.56			
	1/10 load	1.93	12.09	0.125	1.51	78.30			
	1/4 load	4.48	12.09	0.313	3.78	84.33	85.48		
	Typ. load	8.82	12.08	0.625	7.55	85.60			
	3/4 load	13.17	12.08	0.938	11.33	85.99			
	Max. load	17.56	12.08	1.250	15.10	85.99			
264/50	No load	0.06	12.09	0.000				25.20	1.79
	Min. load	0.50	12.09	0.030	0.36	72.54			
	1/20 load	1.01	12.09	0.063	0.76	74.81			
	1/10 load	1.96	12.09	0.125	1.51	77.10			
	1/4 load	4.52	12.08	0.313	3.78	83.52	85.18		
	Typ. load	8.89	12.08	0.625	7.55	84.93			
	3/4 load	13.16	12.08	0.938	11.33	86.06			
	Max. load	17.50	12.07	1.250	15.09	86.21			

- No-load condition (no load) : 12 V at 0 A
- Minimum load condition (min. load) : 12 V at 30 m A
- 1/20 load condition (1/20 load) : 12 V at 62.5 mA
- 1/10 load condition (1/10 load) : 12 V at 125 mA
- 1/4 load condition (1/4 load) : 12 V at 0.3125 A
- Typical load condition (typ. load) : 12 V at 0.625 A
- 3/4 load condition (3/4 load) : 12 V at 0.9375 A
- Maximum load condition (max. load) : 12 V at 1.25 A

9.1 Load regulation

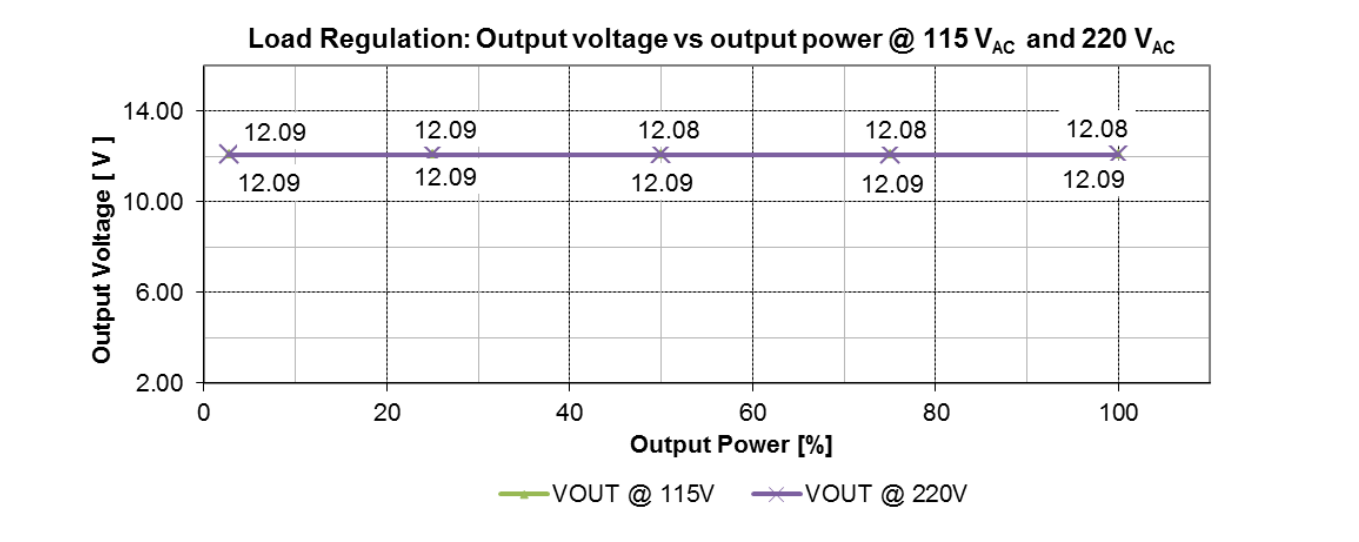


Figure 11 Load regulation V_{OUT} vs output power

9.2 Line regulation

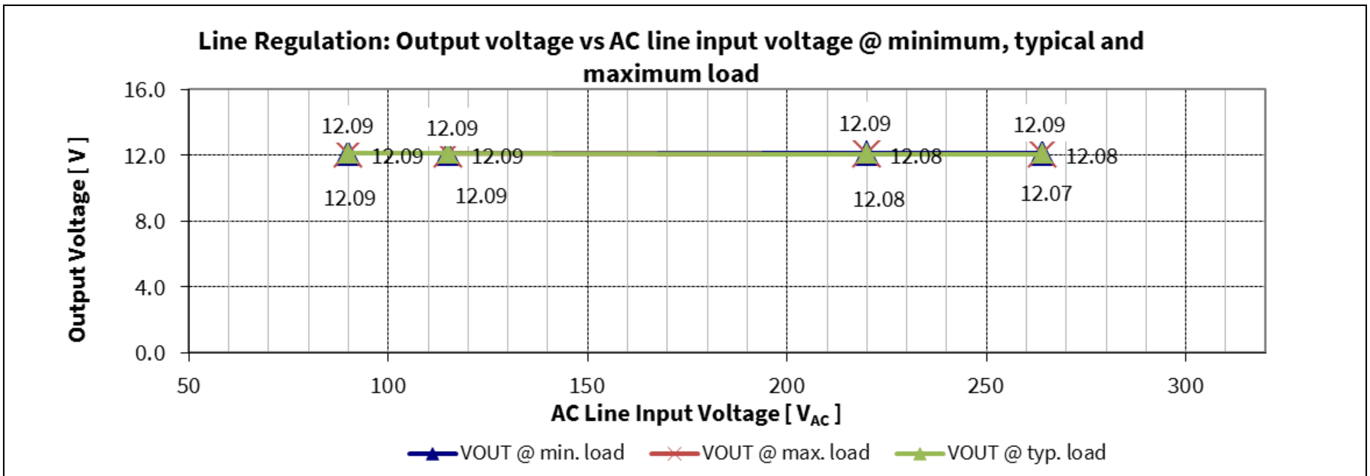


Figure 12 Line regulation: V_{OUT} vs AC-line input voltage

9.3 Efficiency vs AC-line input voltage

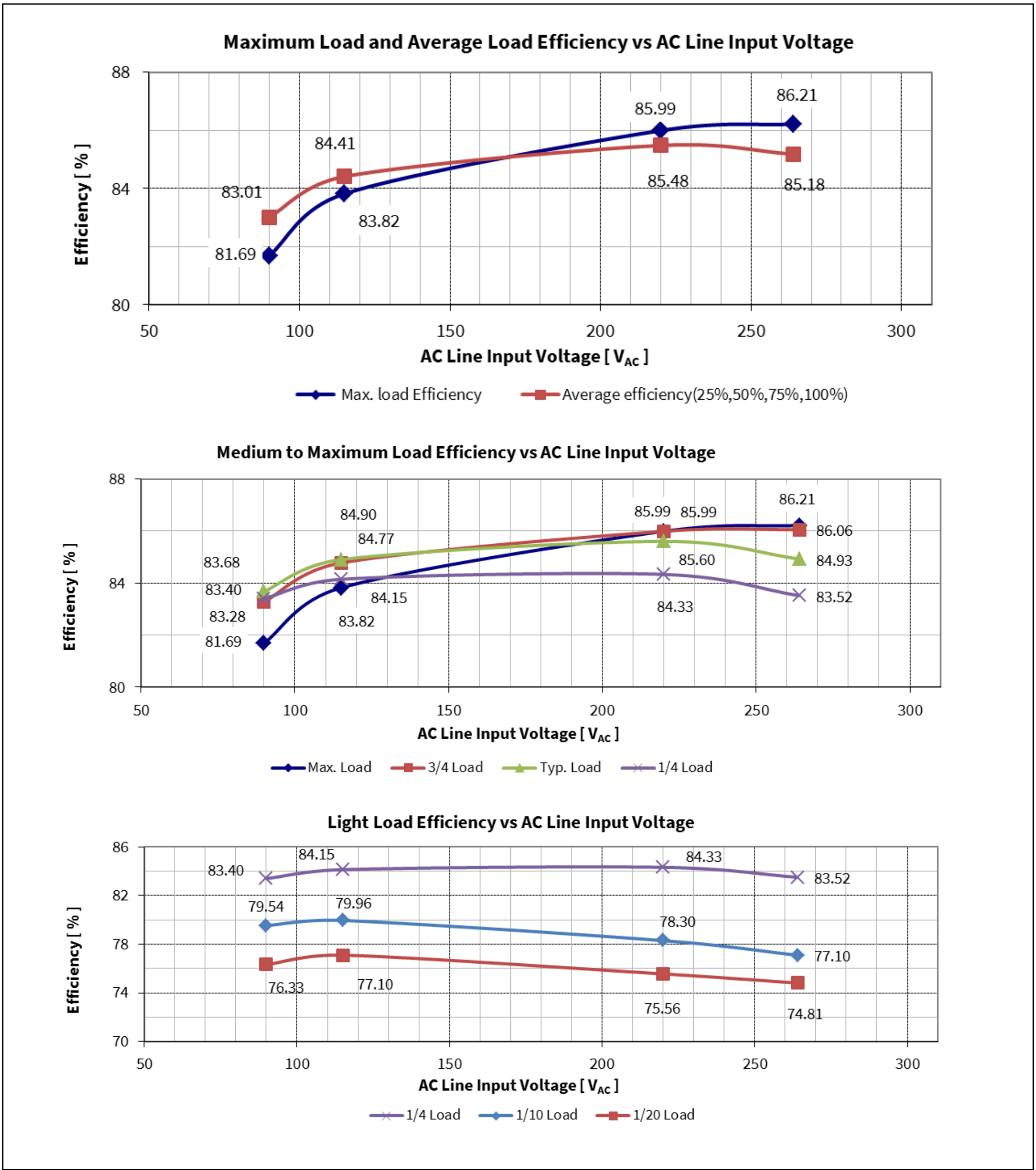


Figure 13 Efficiency vs AC-line input voltage

9.4 Standby power

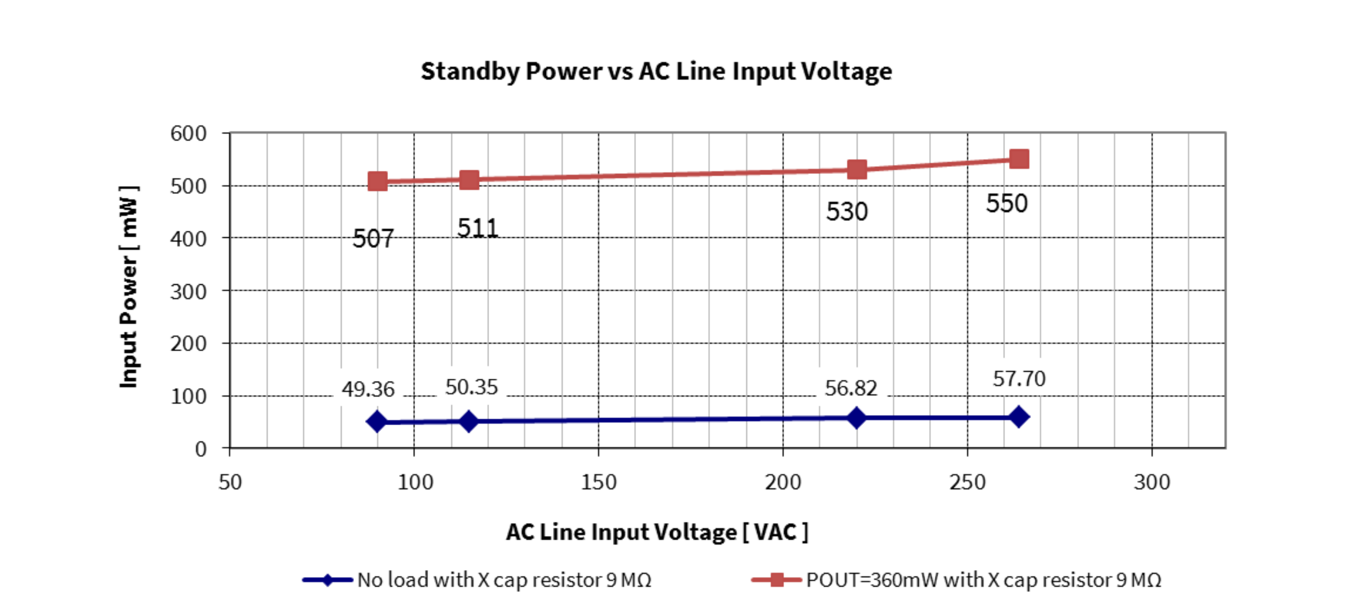


Figure 14 **Standby power at no load (P_{stby_NL}) and 360 mW load (P_{stby_ML}) vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)**

9.5 Maximum output current

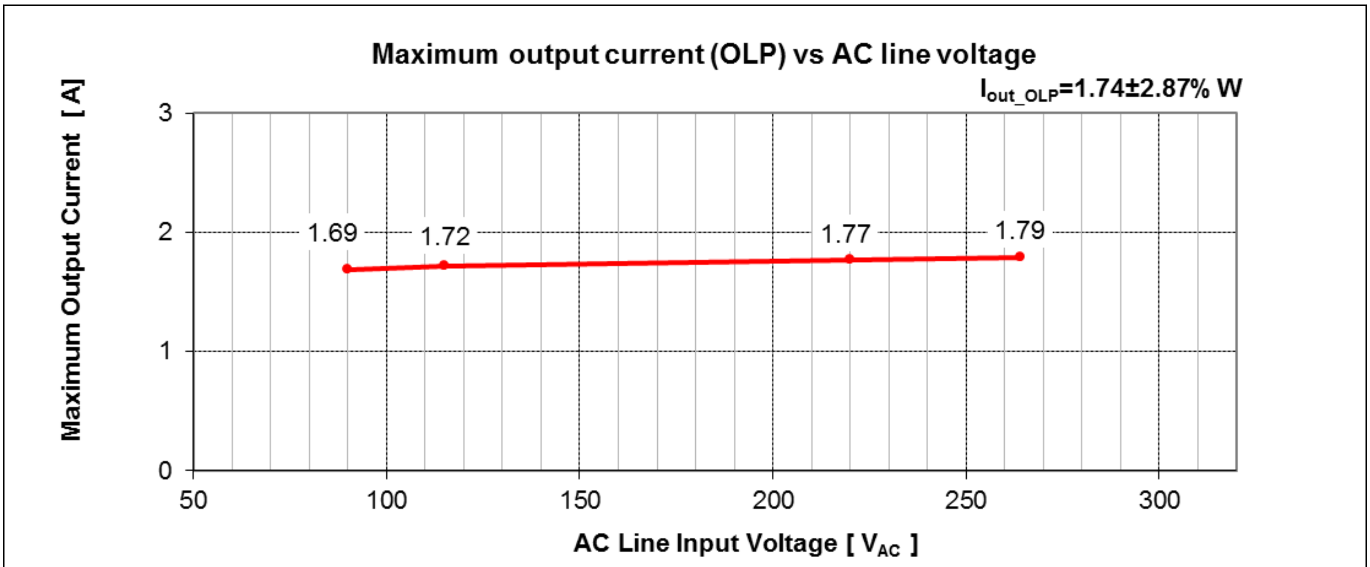


Figure 15 **Maximum output current (before over-load protection) vs AC-line input voltage**

10 Thermal measurement

The thermal testing of the demo board was done in the open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of particular components. The measurements were taken at the maximum load running for one hour. The tested input voltage was 90 V AC and 264 V AC.

Table 6 Component temperature at full load (12 V 1.25 A) under T_{amb} = 25°C

Circuit code	Major component	90 V AC (°C)	264 V AC (°C)
IC11	ICE5AR4770BZS	80.8	62.3
R14	CS resistor	55.1	47.2
TR1	Transformer	57.2	58.2
BR1	Bridge diode	47.2	33.6
R11	Clamper resistor	45.5	42.5
L11	Input CMC	47.1	32.3
D21	+12 V output diode	76.8	76.1
	Ambient	25.0	25.0

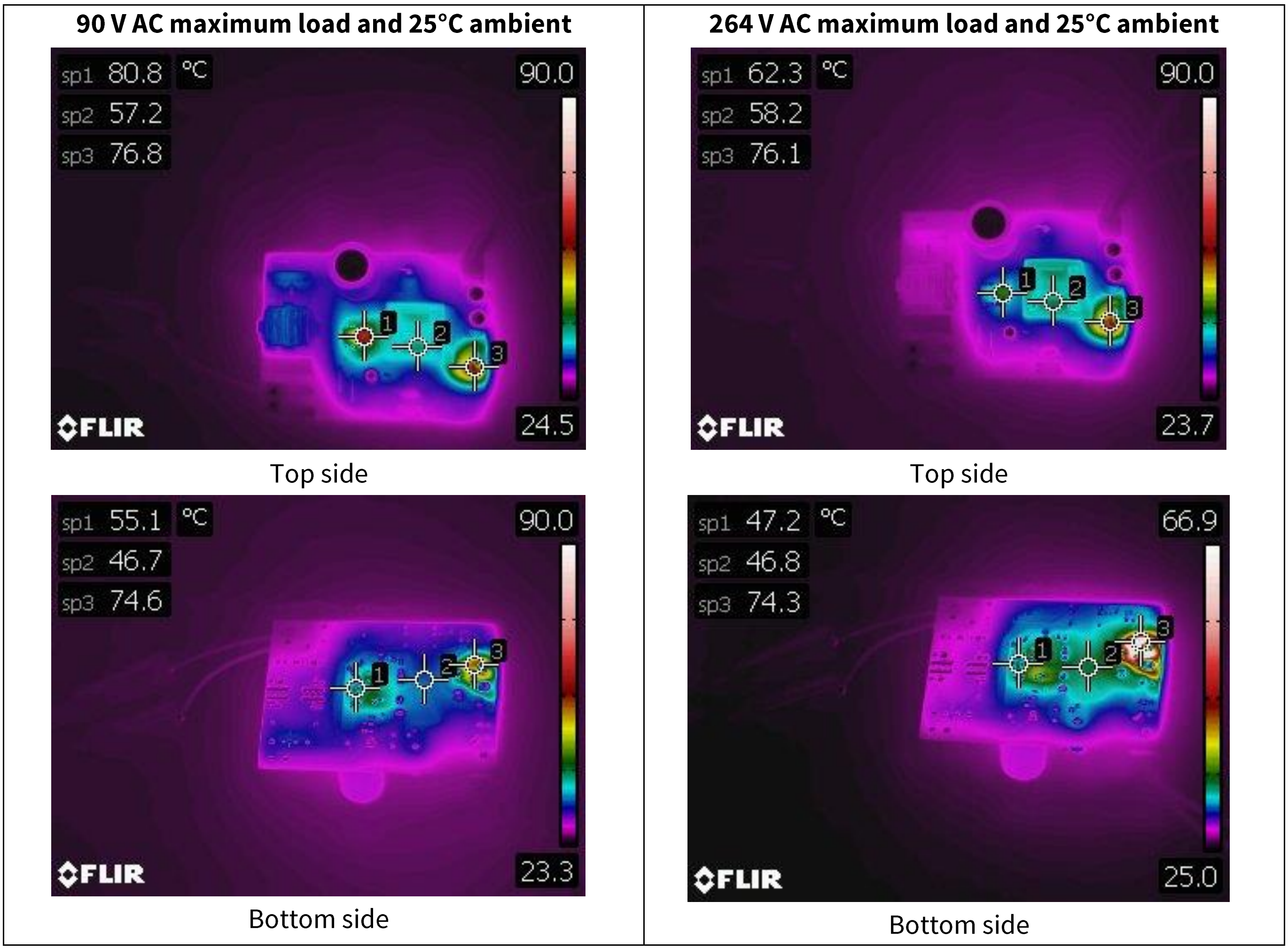
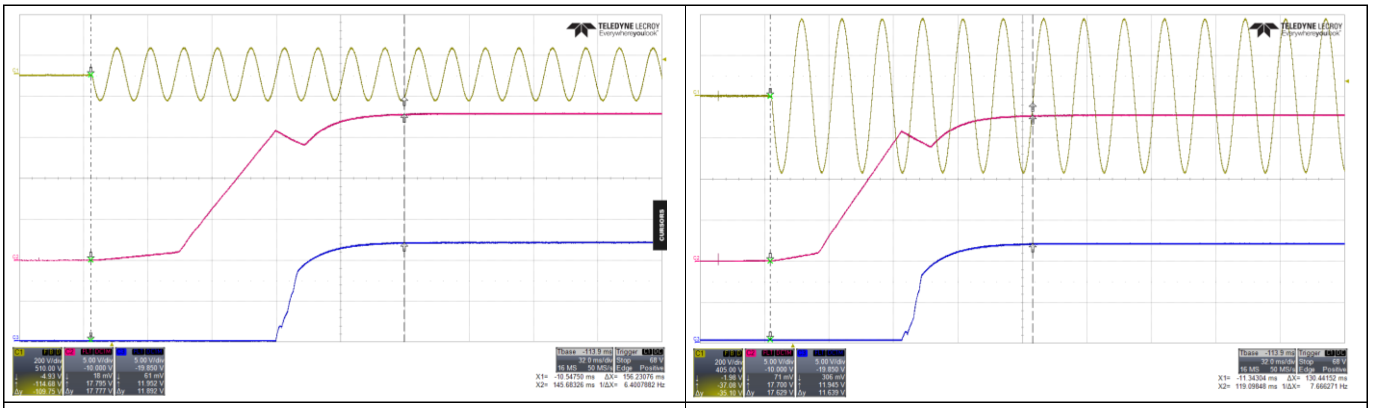


Figure 16 Infrared thermal image of REF_5AR4770BZS_15W1

11 Waveforms

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

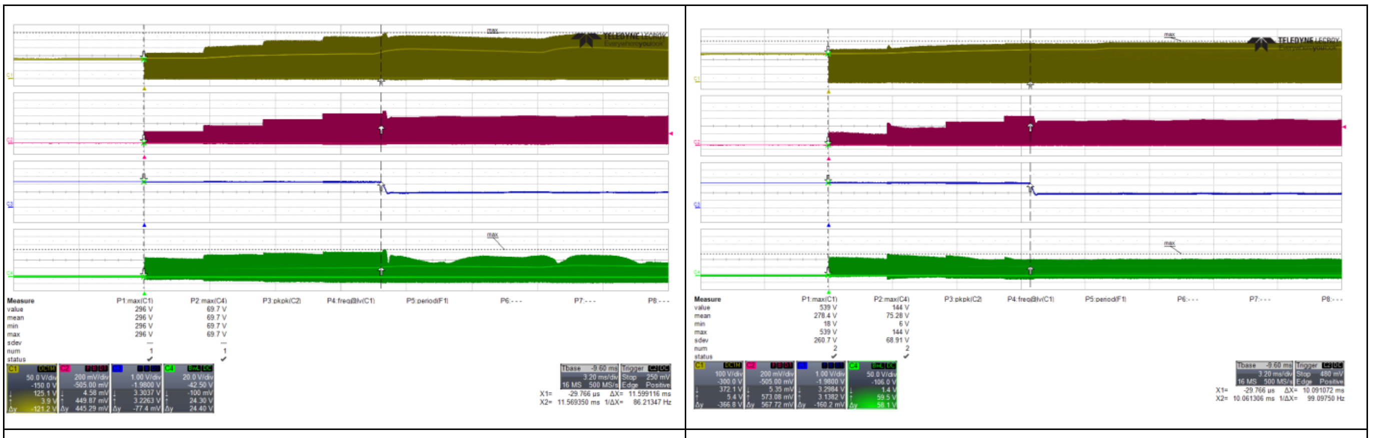
11.1 Start-up at low/high AC-line input voltage with maximum load



C1 (yellow): V AC; C2 (purple): V_{VCC}; C3 (blue): V_{OUT1} (12 V)	C1 (yellow): V AC; C2 (purple): V_{VCC}; C3 (blue): V_{OUT1} (12 V)
V_{IN} = 90 V AC, max. load; start-up time: ≈ 156 ms	V_{IN} = 264 V AC, max. load; start-up time: ≈ 130 ms

Figure 17 Start-up

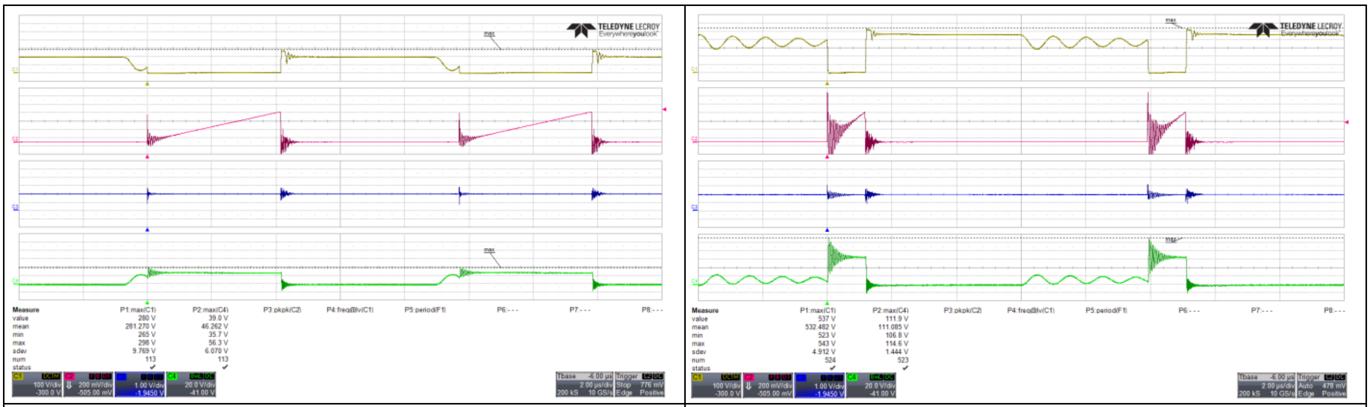
11.2 Soft-start



C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}	C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}
V_{IN} = 90 V AC, max. load; soft-start time: ≈ 11 ms	V_{IN} = 264 V AC, max. load; soft-start time: ≈ 10 ms

Figure 18 Soft-start

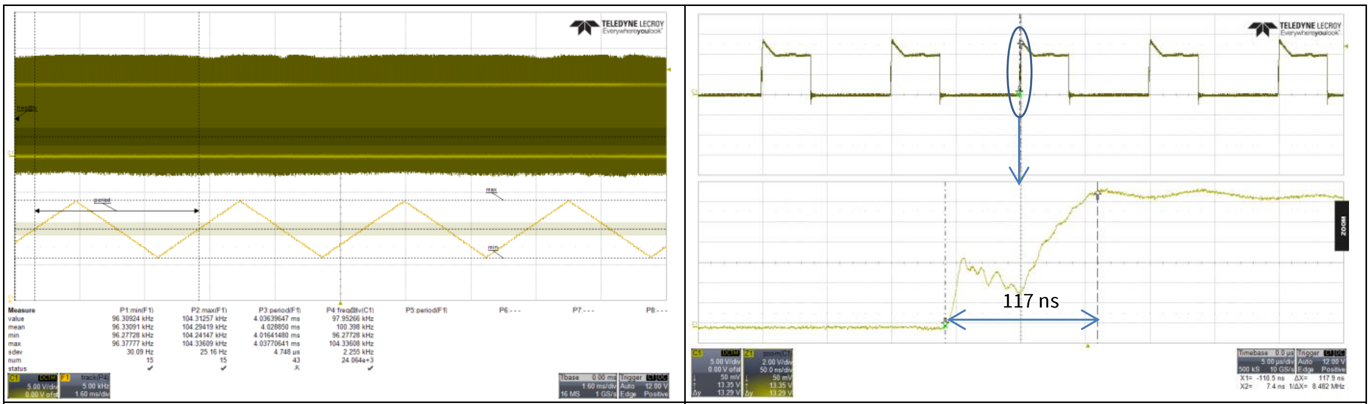
11.3 Switching waveform at maximum load



C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}	C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}
V_{IN} = 90 V AC, max. load; V_{Drain_max}: 289 V DC and V_{D21_max}: 56 V DC	V_{IN} = 264 V AC, max. load; V_{Drain_mzx}: 543 V DC and V_{D21_max}: 114 V DC

Figure 19 Drain and CS voltage at maximum load

11.4 Frequency jittering and modulated gate drive



C1 (yellow): V_{GATE}; F1 (orange): Frequency track of V_{GATE}	C1 (yellow): V_{GATE}; Z1 (orange): Zoom of V_{GATE}
V_{IN} = 90 V AC, 100 percent load; jittering frequency ≈ 96 kHz ~ 104kHz and period ≈ 4.4 ms	V_{IN} = 90 V AC, 100 percent load; modulated gate drive rising up time ≈ 117 ns

Figure 20 Frequency jittering and modulated gate drive

11.5 Output ripple voltage at maximum load

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW

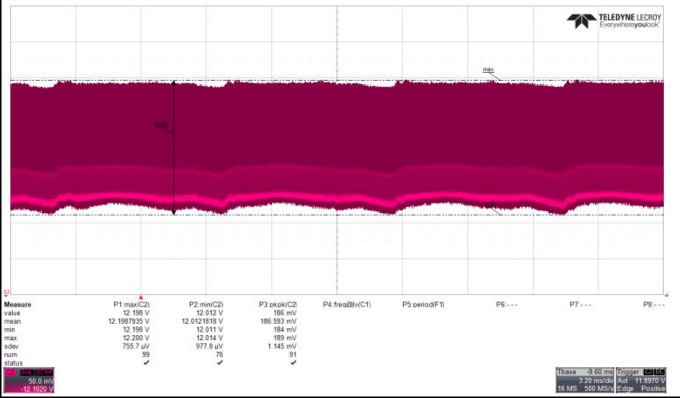
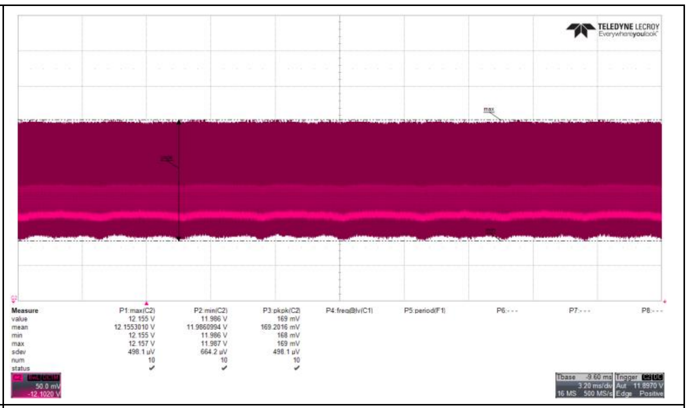
	
C2 (purple): $V_{RIPPLE1}$ (12 V)	C2 (purple): $V_{RIPPLE1}$ (12 V)
V_{IN} = 90 V AC, max. load; $V_{RIPPLE1}$ (12 V): 189 mV	V_{IN} = 264 V AC, max. load; $V_{RIPPLE1}$ (12 V): 169 mV

Figure 21 Output ripple voltage at maximum load

11.6 Output ripple voltage in ABM 1 W load

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW
- Load: 1 W (12 V, 83 mA)

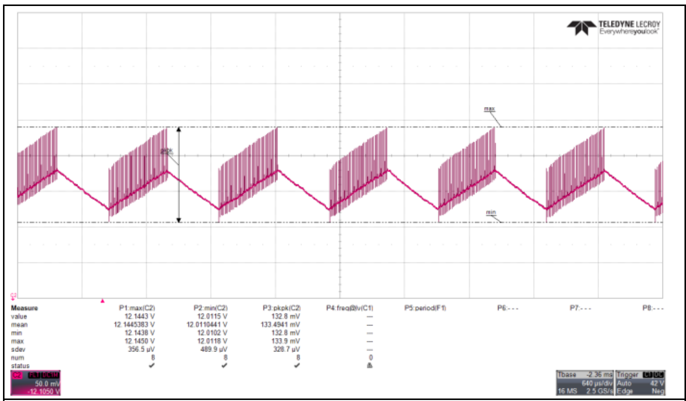
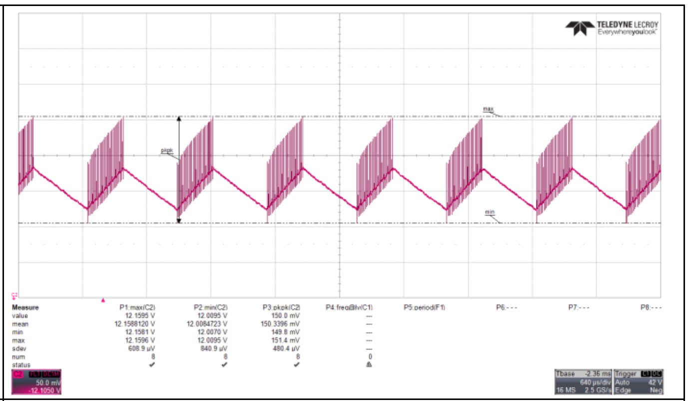
	
C2 (purple): $V_{RIPPLE1}$ (12 V)	C2 (purple): $V_{RIPPLE1}$ (12 V)
V_{in} = 90 V AC, 1 W load; $V_{RIPPLE1}$ (12 V): 133 mV	V_{in} = 264 V AC, 1 W load; $V_{RIPPLE1}$ (12 V): 151 mV

Figure 22 Output ripple voltage in ABM 1 W load

11.7 Load transient response (dynamic load from 10 percent to 100 percent)

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW
- 12 V load change from 10 percent to 100 percent, 100 Hz, 0.4 A/µs slew rate

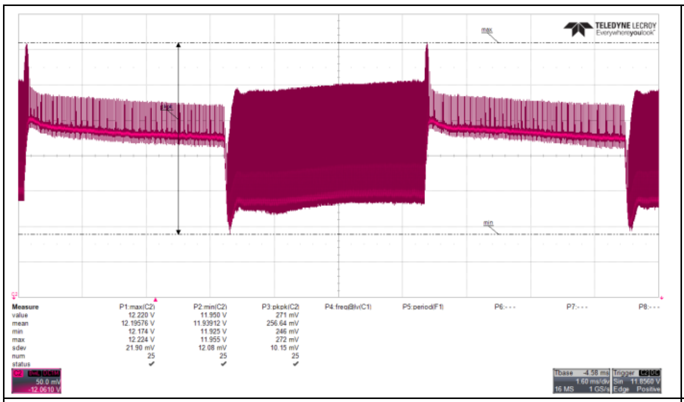
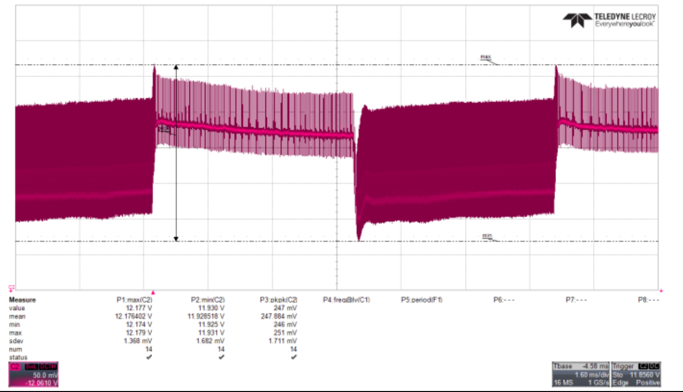
	
C2 (purple): $V_{RIPPLE1}$ (12 V)	C2 (purple): $V_{RIPPLE1}$ (12 V)
V_{in} = 90 V AC, 10 percent to 100 percent load; $V_{RIPPLE1}$ (12 V): 272 mV	V_{in} = 264 V AC, 10 percent to 100 percent load; $V_{RIPPLE1}$ (12 V): 251 mV

Figure 23 Load transient response

11.8 Entering ABM

- Load change from 15 W (12 V, 1.25 A) to 0.5 W (12 V, 0.041 A)

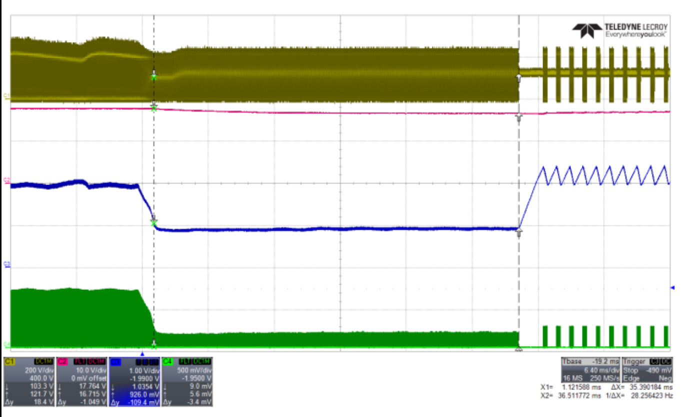
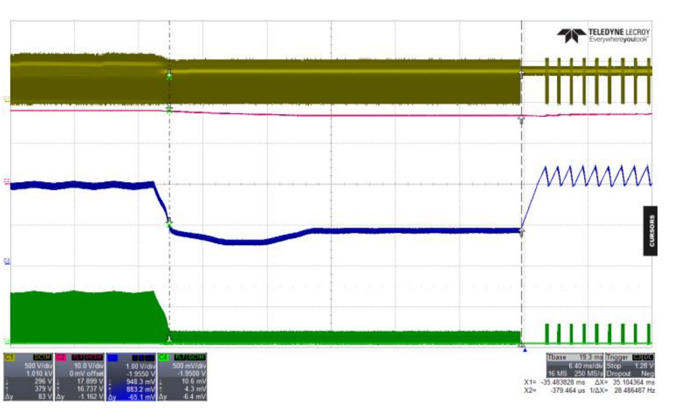
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 90 V AC; system enters burst mode option 3: V_{FB} less than 1.03 V and $t_{blanking}$ = 36 ms	V_{IN} = 264 V AC; system enters burst mode option 3: V_{FB} less than 1.03 V and $t_{blanking}$ = 36 ms

Figure 24 Entering ABM

11.9 During ABM

- Load: 1 W (12 V, 0.083 A)

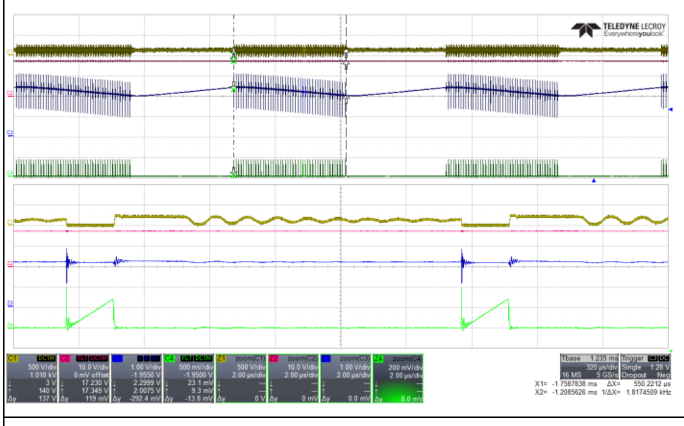
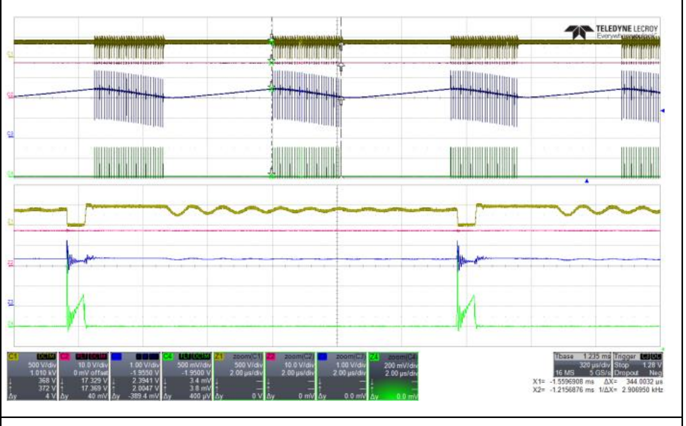
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 90 V AC; burst mode option 3: V_{FB_BOn} = 2.35 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.27 V, f_{OSC4_ABM} = 83 kHz	V_{IN} = 264 V AC; burst mode option 3: V_{FB_BOn} = 2.35 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.27 V, f_{OSC4_ABM} = 83 kHz

Figure 25 During ABM

11.10 Leaving ABM

- Load change from 0.5 W (12 V, 0.041 A) to full load

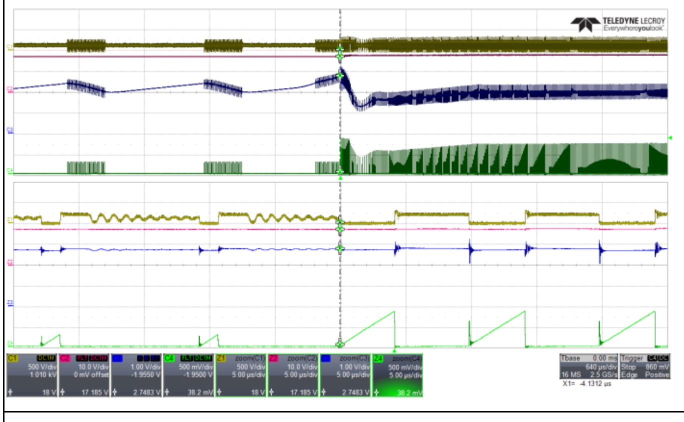
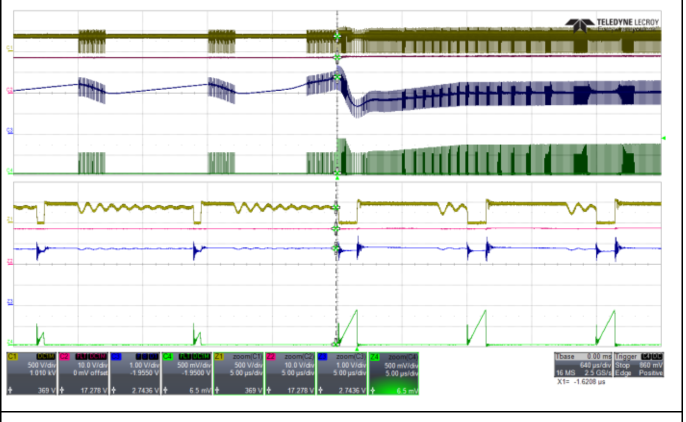
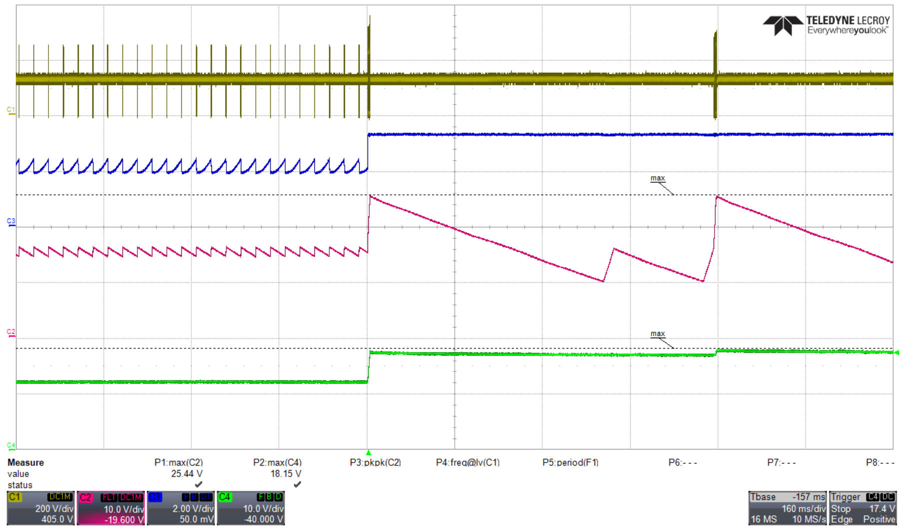
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 90 V AC; system leaves burst mode: V_{FB} greater than 2.73 V	V_{IN} = 264 V AC; system leaves burst mode: V_{FB} greater than 2.73 V

Figure 26 Leaving ABM

11.11 Output OVP by utilizing V_{CC} OVP (odd-skip auto restart)

- Short R26 resistor during system operation at no load



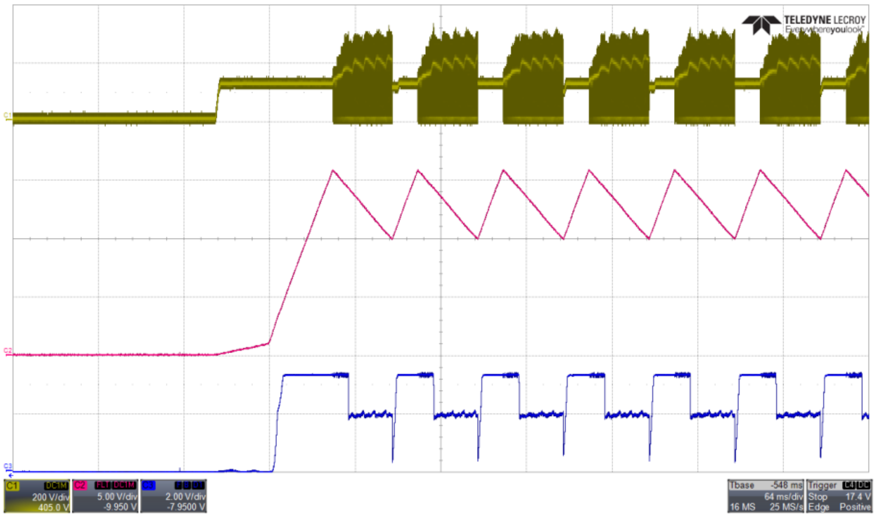
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB} (12 V); C4 (green): V_{CS}

V_{IN} = 90 V AC; system enters output OVP by using V_{CC} OVP: V_{Out} greater than 18 V (V_{CC} greater than 25.5 V)

Figure 27 V_{CC} OVP

11.12 V_{CC} UVP (auto restart)

- Remove R12A and power on the system with full load



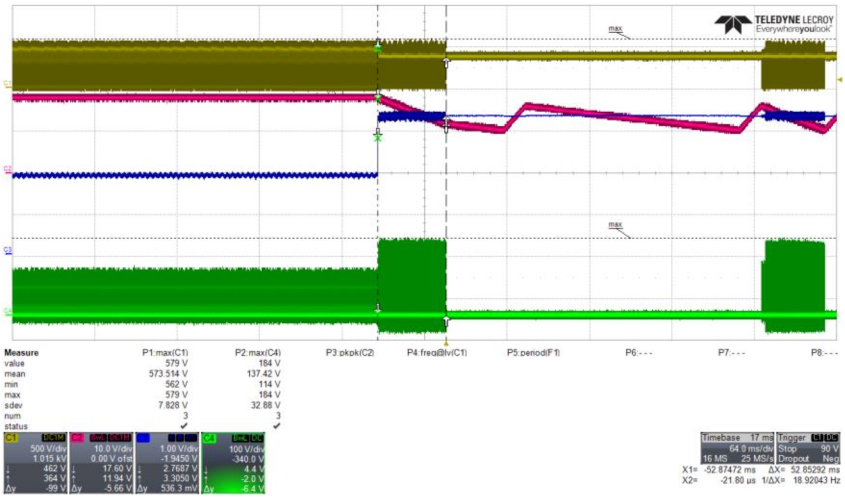
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}

V_{IN} = 90 V AC; system enters V_{CC} UVP: V_{CC} less than 10 V

Figure 28 V_{CC} UVP

11.13 Over-load protection (odd-skip auto restart)

- V_{OUT1} (12 V) short-to-GND at 264 V AC



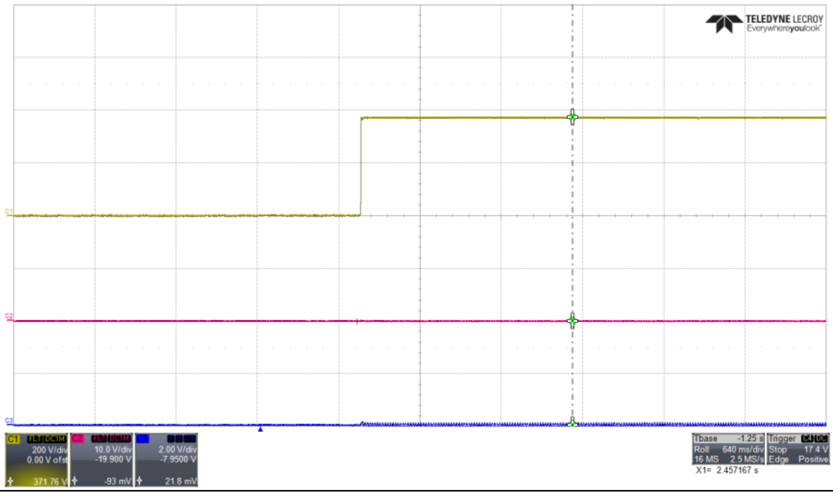
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB};C4 (green): V_{D21}

V_{IN} = 264 V AC; system enters over-load protection: V_{FB} greater than 2.73 V and lasts for ≈ 53 ms blanking time: V_{Drain_max}: 579 V DC and V_{D21_max}: 184 V DC

Figure 29 Over-load protection and max. voltage stress for MOSFET and output diode (D21)

11.14 V_{CC} short-to-GND protection

- Short V_{CC} pin-to-GND with current meter before system start-up



C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}

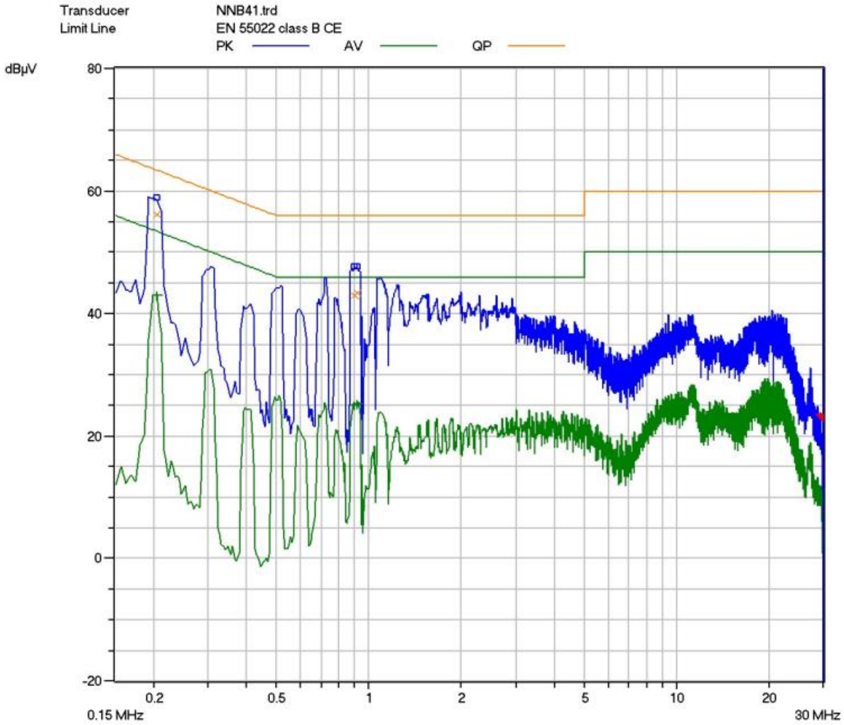
V_{IN} = 264 V AC; system enters V_{CC} short-to-GND: V_{CC} less than V_{VCC_SCP} → I_{VCC} = 439 µA (input power ≈ 160 mW)

Figure 30 V_{CC} short-to-GND protection

11.15 Conducted emissions (EN 55022 class B)

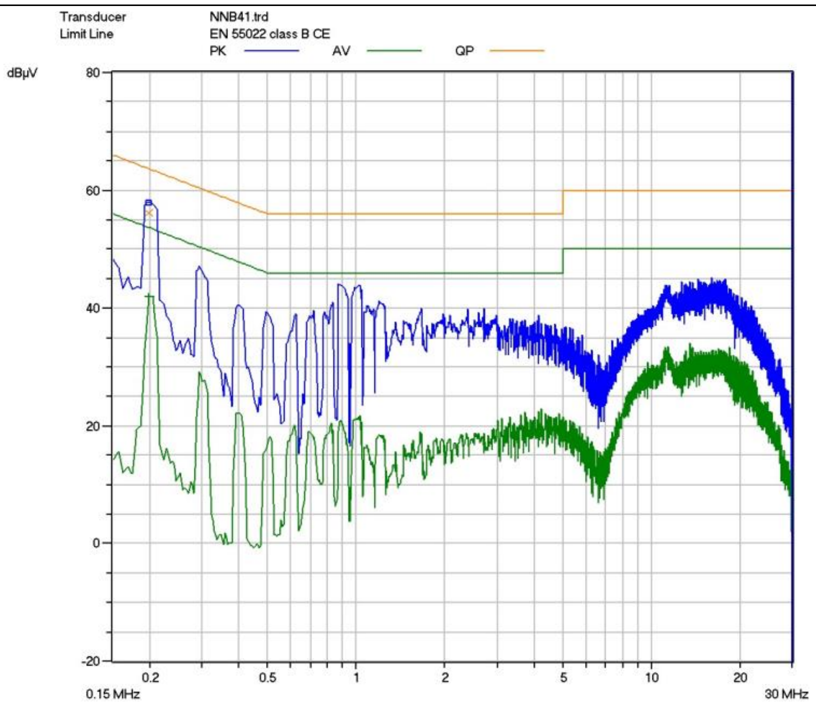
Equipment: Schaffner SMR4503 (receiver); standard: EN 55022 (CISPR 22) class B; test conditions: V_{IN} = 115 V AC and 220 V AC, load: 15 W (12 V 9.6 Ω).

- Pass conducted emissions EN 55022 (CISPR 22) class B with greater than 7 dB margin for quasi-peak measurement at low-line (115 V AC) and greater than 10 dB margin for quasi-peak measurement at high-line (220 V AC).



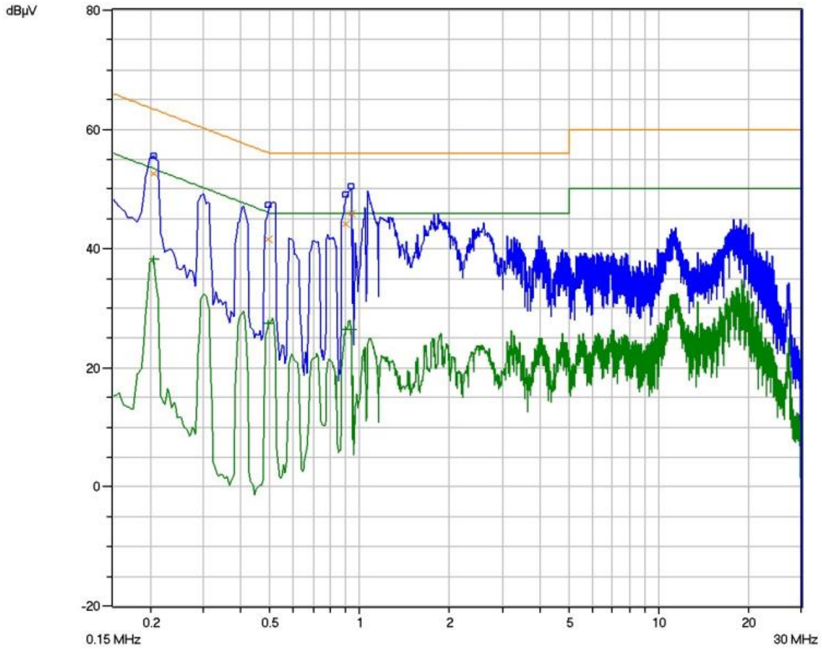
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2040	L	59.0	L	43.0	L	56.1	53.4	63.4
0.9000	L	47.8	L	25.2	L	43.0	46.0	56.0
0.9180	L	47.7	L	25.3	L	43.5	46.0	56.0

Figure 31 Conducted emissions at 115 V AC-line and 15 W load – greater than 7 dB margin



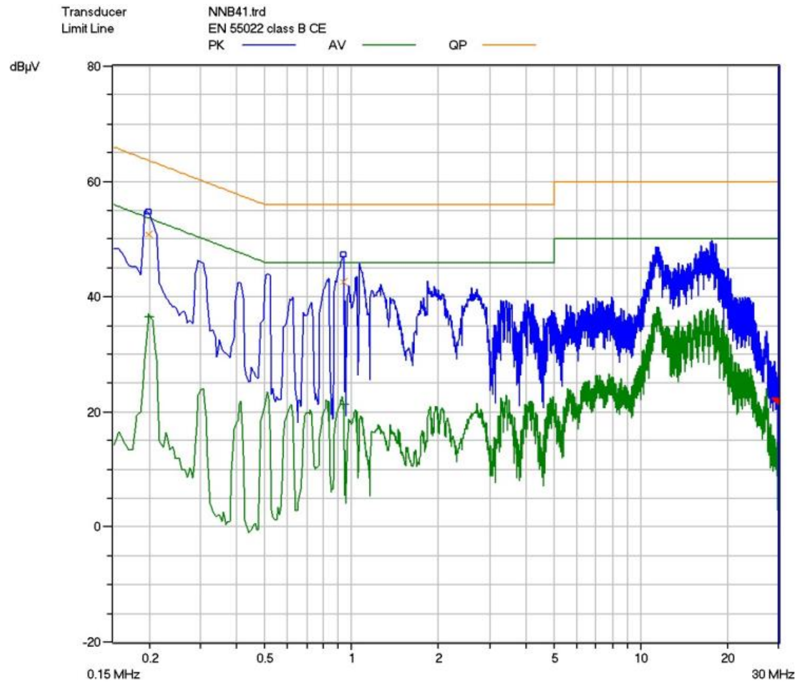
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.1980	N	58.0	N	42.0	N	56.2	53.7	63.7

Figure 32 Conducted emissions at 115 V AC-neutral and 15 W load – greater than 7 dB margin



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2040	L	55.5	L	38.3	L	52.6	53.4	63.4
0.4920	L	47.2	L	27.4	L	41.6	46.1	56.1
0.9000	L	49.0	L	26.4	L	44.1	46.0	56.0
0.9360	L	50.5	L	26.4	L	46.0	46.0	56.0

Figure 33 **Conducted emissions at 220 V AC-line and 15 W load – greater than 10 dB margin**



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.1980	N	54.7	N	36.4	N	50.8	53.7	63.7
0.9360	N	47.3	N	21.3	N	42.6	46.0	56.0

Figure 34 **Conducted emissions at 220 V AC-neutral and 15 W load – greater than 12 dB margin**

11.16 ESD immunity (EN 61000-4-2)

This system was subjected to a ±8 kV ESD test according to EN 61000-4-2 for both contact and air discharge. A test failure was defined as non-recoverable.

- Air discharge: pass ±8 kV; contact discharge: pass ± 8 kV.

Table 7 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			$+V_{OUT}$	$-V_{OUT}$	
115 V AC, 15 W (12 V 9.6 Ω)	Contact	+8 kV	10	10	PASS
		-8 kV	10	10	PASS
	Air	+8 kV	10	10	PASS
		-8 kV	10	10	PASS
220 V AC, 15 W (12 V 9.6 Ω)	Contact	+8 kV	10	10	PASS
		-8 kV	10	10	PASS
	Air	+8 kV	10	10	PASS
		-8 kV	10	10	PASS

11.17 Surge immunity (EN 61000-4-5)

This system was subjected to a surge immunity test (±2 kV DM and ±4 kV CM) according to EN 61000-4-5. A test failure was defined as a non-recoverable.

- DM: pass ±2 kV; CM: pass ±4 kV.

Table 8 System surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
115 V AC, 15 W (12 V 9.6 Ω)	DM	+2 kV	L → N	3	3	3	3	PASS
		-2 kV	L → N	3	3	3	3	PASS
	CM	+4 kV	L → G	3	3	3	3	PASS
		+4 kV	N → G	3	3	3	3	PASS
		-4 kV	L → G	3	3	3	3	PASS
		-4 kV	N → G	3	3	3	3	PASS
220 V AC, 15 W (12 V 9.6 Ω)	DM	+2 kV	L → N	3	3	3	3	PASS
		-2 kV	L → N	3	3	3	3	PASS
	CM	+4 kV	L → G	3	3	3	3	PASS
		+4 kV	N → G	3	3	3	3	PASS
		-4 kV	L → G	3	3	3	3	PASS
		-4 kV	N → G	3	3	3	3	PASS

12 Appendix A: Transformer design and spreadsheet [3]

Design procedure for fixed-frequency flyback converter using CoolSET™ 5xRxxxxAG/BZS (version 1.0)

Project	**ICE5AR4770BZS**
Application	**90 ~ 264 V AC and 15 W (12 V, 1.25 A) single-output, isolated flyback**
CoolSET™	**ICE5AR4770BZS**
Date	**12 Jan 2018**
Revision	**0.1**

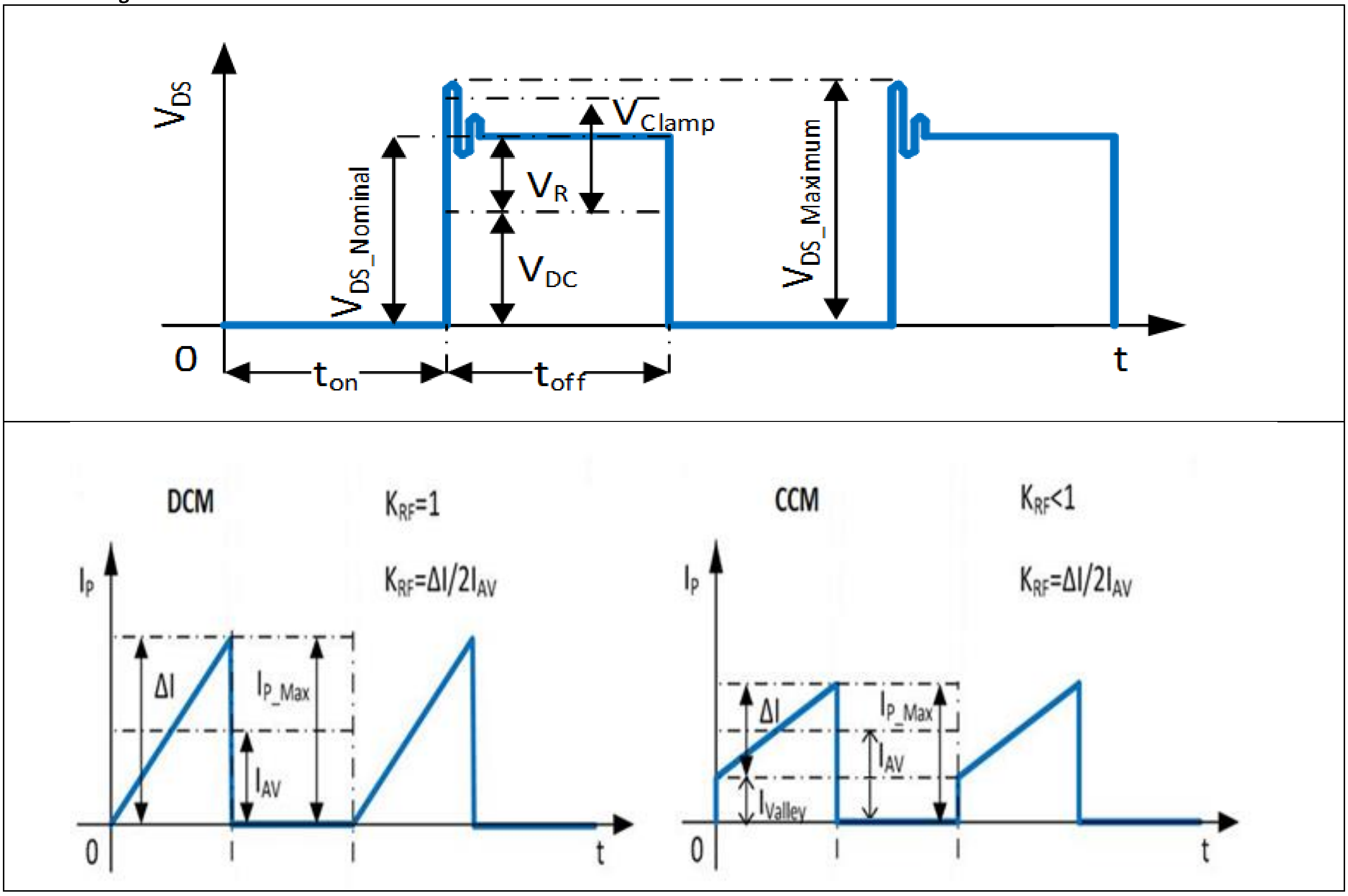
Enter design variables in orange colored cells
Read design results in green colored cells

	Description	Eq. #	Parameter	Unit	Value
Input, output, CoolSET™ specs					
Line input					
Input	Minimum AC input voltage		$V\ AC_{Min}$	[V]	90
Input	Maximum AC input voltage		$V\ AC_{Max}$	[V]	264
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V\ DC_{Ripple}$	[V]	31.5
Output 1 specs					
Input	Output voltage 1		V_{Out1}	[V]	12
Input	Output current 1		I_{Out1}	[A]	1.25
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.6
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	0.24
Result	Output power 1	Eq. 001	P_{Out1}	[W]	15
Auxiliary					
Input	V_{CC} Voltage		V_{Vcc}	[V]	18
Input	Forward voltage of V_{CC} diode(D2)		$V_{F\ Vcc}$	[V]	0.6
Power					
Input	Efficency		η		0.82
Result	Nominal output power	Eq. 003	P_{OutNom}	[W]	15.00
Input	Maximum output power for over-load protection		P_{OutMax}	[W]	15
Result	Maximum input power for over-load protection	Eq. 006	P_{InMax}	[W]	18.29
Input	Minimum output power		P_{OutMin}	[W]	1.5
Controller/CoolSET™					
	CoolSET™ -				ICE5AR4770BZS
Input	Switching frequency		f_S	[Hz]	100000
Input	Targeted max. drain source voltage		V_{DSMax}	[V]	550
Input	Max. ambient temperature		T_{amax}	[°C]	50
Diode bridge and input capacitor					
Diode bridge					
Input	Power factor		cosφ		0.6
Result	Maximum AC input current	Eq. 007	I_{ACRMS}	[A]	0.339
Result	Peak voltage at $V\ AC_{Max}$	Eq. 008	$V\ DC_{MaxPk}$	[V]	373.35
Input capacitor					
Result	Peak voltage at $V\ AC_{Min}$	Eq. 009	$V\ DC_{MinPk}$	[V]	127.28
Result	Selected minimum DC input voltage	Eq. 010	$V\ DC_{MinSet}$	[V]	95.78
Result	Discharging time at each half-line cycle	Eq. 011	T_D	[ms]	6.43
Result	Required energy at discharging time of input capacitor	Eq. 012	W_{In}	[Ws]	0.12
Result	Calculated input capacitor	Eq. 013	C_{INCal}	[µF]	33.46
Input	Select input capacitor (C1)		C_{in}	[µF]	33
Result	Calculated minimum DC input voltage	Eq. 015	$V\ DC_{Min}$	[V]	95.27

Appendix A: Transformer design and spreadsheet [3]

Transformer design

Drain voltage and current waveform



Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	89.6
Result	Maximum duty cycle	Eq. 016	D_{Max}		0.48
Input	Select current ripple factor		K_{RF}		1
Result	Primary inductance	Eq. 017	L_P	[H]	5.83E-04
Result	Primary turn-on average current	Eq. 018	I_{AV}	[A]	0.40
Result	Primary peak-to-peak current	Eq. 019	ΔI	[A]	0.79
Result	Primary peak current	Eq. 020	I_{PMax}	[A]	0.79
Result	Primary valley current	Eq. 021	I_{Valley}	[A]	0.00
Result	Primary RMS current	Eq. 022	I_{PRMS}	[A]	0.318

Select core type

Input	Select core type				1
Result	Core type				EE20/10/6
Result	Core material				TP4A (TDG)
Result	Maximum flux density		B_{Max}	[T]	0.25
Result	Cross-sectional area		A_e	[mm^2]	32
Result	Bobbin width		BW	[mm]	11
Result	Winding cross-section		A_N	[mm^2]	34
Result	Average length of turn		l_N	[mm]	41.2

Winding calculation

Result	Calculated minimum number of primary turns	Eq. 023	N_{PCal}	Turns	57.72
Input	Select number of primary turns		N_P	Turns	64
Result	Calculated number of secondary 1 turns	Eq. 024	N_{S1Cal}	Turns	9.00
Input	Select number of secondary 1 turns		N_{S1}	Turns	9
Result	Calculated number of auxiliary turns	Eq. 026	N_{VccCal}	Turns	13.29
Input	Select number of auxiliary turns		N_{Vcc}	Turns	13

Appendix A: Transformer design and spreadsheet [3]

Result	Calculated V_{CC} voltage	Eq. 027	V_{VccCal}	[V]	17.60
Post calculation					
Result	Primary to secondary 1 turns ratio	Eq. 028	N_{PS1}		7.11
Result	Post calculated reflected voltage	Eq. 030	V_{RPost}	[V]	89.60
Result	Post calculated maximum duty cycle	Eq. 031	$D_{MaxPost}$		0.48
Result	Duty cycle prime	Eq. 032	D_{Max}'		0.52
Result	Actual flux density	Eq. 033	B_{MaxAct}	[T]	0.225
Result	Maximum DC input voltage for CCM operation	Eq. 034	$V\ DC_{maxCCM}$	[V]	95.27
Transformer winding design					
Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.3
Result	Effective bobbin window	Eq. 035	BW_E	[mm]	11.0
Result	Effective winding cross-section	Eq. 036	A_{Ne}	[mm^2]	34.0
Input	Primary winding area factor		AF_{NP}		0.50
Input	Secondary 1 winding area factor		AF_{NS1}		0.45
Input	Auxiliary winding area factor		AF_{NVcc}		0.05
Primary winding					
Result	Calculated wire copper cross-sectional area	Eq. 037	A_{PCal}	[mm^2]	0.0797
Result	Calculated maximum wire size	Eq. 038	AWG_{PCal}		28
Input	Select wire size		AWG_P		29
Input	Select number of parallel wire		nw_P		1
Result	Wire copper diameter	Eq. 039	d_P	[mm]	0.29
Result	Wire copper cross-sectional area	Eq. 040	A_P	[mm^2]	0.0652
Result	Wire current density	Eq. 041	S_P	[A/mm^2]	4.89
Input	Insulation thickness		INS_P	[mm]	0.02
Result	Turns per layer	Eq. 042	NL_P	Turns/layer	33
Result	Number of layers	Eq. 043	Ln_P	Layers	2
Secondary 1 winding					
Result	Calculated wire copper cross-sectional area	Eq. 044	A_{NS1Cal}	[mm^2]	0.5100
Result	Calculated maximum wire size	Eq. 045	AWG_{S1Cal}		20
Input	Select wire size		AWG_{S1}		31
Input	Select number of parallel wire		nw_{S1}		7
Result	Wire copper diameter	Eq. 046	d_{S1}	[mm]	0.2287
Result	Wire copper cross-sectional area	Eq. 047	A_{S1}	[mm^2]	0.2874
Result	Peak current	Eq. 048	I_{S1Max}	[A]	5.6345
Result	RMS current	Eq. 049	I_{S1RMS}	[A]	2.3353
Result	Wire current density	Eq. 050	S_{S1}	[A/mm^2]	8.12
Input	Insulation thickness		INS_{S1}	[mm]	0.02
Result	Turns per layer	Eq. 051	NL_{S1}	Turns/layer	5
Result	Number of layers	Eq. 052	Ln_{S1}	Layers	2
RCD clamper and CS resistor					
RCD clamper circuit					
Input	Leakage inductance percentage		$L_{LK\%}$	[Percent]	0.84
Result	Leakage inductance	Eq. 062	L_{LK}	[H]	4.89E-06
Result	Clamping voltage	Eq. 063	V_{Clamp}	[V]	87.05
Result	Calculated clamping capacitor	Eq. 064	$C_{ClampCal}$	[nF]	0.20
Input	Select clampingcapacitor value (C2)		C_{clamp}	[nF]	1
Result	Calculated clamping resistor	Eq. 065	$R_{clampCal}$	[kΩ]	150.8
Input	Select clampingresistor value (R4)		R_{clamp}	[kΩ]	150
CS resistor					
Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated CS resistor (R8A, R8B)	Eq. 066	R_{sense}	[Ω]	1.01

Ouput rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq. 067	$V_{RDiode1}$	[V]	64.50
Result	Diode RMS current		I_{S1RMS}	[A]	2.34
Input	Max voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.5
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq. 068	$I_{Ripple1}$	[A]	1.97
Result	Calculated minimum output capacitor	Eq. 069	$C_{Out1Cal}$	[uF]	500
Input	Select output capacitor value (C152)		C_{Out1}	[uF]	470
Input	ESR (Zmax) value from datasheet @ 100kHz		R_{ESR1}	[Ω]	0.02
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq. 070	f_{ZCOut1}	[Khz]	16.93
Result	First stage ripple voltage	Eq. 071	$V_{Ripple1}$	[V]	0.112691
Input	Select LC filter inductor value (L151)		L_{out1}	[uH]	0.2
Result	Calculated LC filter capacitor	Eq. 072	C_{LCCal1}	[uF]	441.8
Input	Select LC filter capacitor value (C153)		C_{LC1}	[uF]	470
Result	LC filter frequency	Eq. 073	f_{LC1}	[Khz]	16.42
Result	Second stage ripple voltage	Eq. 074	$V_{2ndRipple1}$	[mV]	2.96

V_{CC} diode and capacitor

V_{CC} diode and capacitor

Result	Auxiliary diode reverse voltage (D2)	Eq. 083	$V_{RDiodeVCC}$	[V]	93.44
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Charge3}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	3
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq. 084	C_{VCCCal}	[uF]	6.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[uF]	10
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq. 085	$t_{StartUp}$	[ms]	104.667

Calculation of losses

Input diode bridge

Input	Diode bridge forward voltage		V_{FBR}	[V]	1
Result	Diode bridge power loss	Eq. 086	P_{DIN}	[W]	0.68

Transformer copper

Result	Primary winding copper resistance	Eq. 087	R_{PCu}	[mΩ]	695.89
Result	Secondary 1 winding copper resistance	Eq. 088	R_{S1Cu}	[mΩ]	22.19
Result	Primary winding copper loss	Eq. 090	P_{PCu}	[mW]	70.59
Result	Secondary 1 winding copper loss	Eq. 091	P_{S1Cu}	[mW]	121.00
Result	Total transformer copper loss	Eq. 093	P_{Cu}	[W]	0.1916

Output rectifier diode

Result	Secondary 1 diode loss	Eq. 094	P_{Diode1}	[W]	1.40

RCD clamper circuit

Result	RCD clamper loss	Eq. 096	$P_{Clamper}$	[W]	0.31

CS resistor

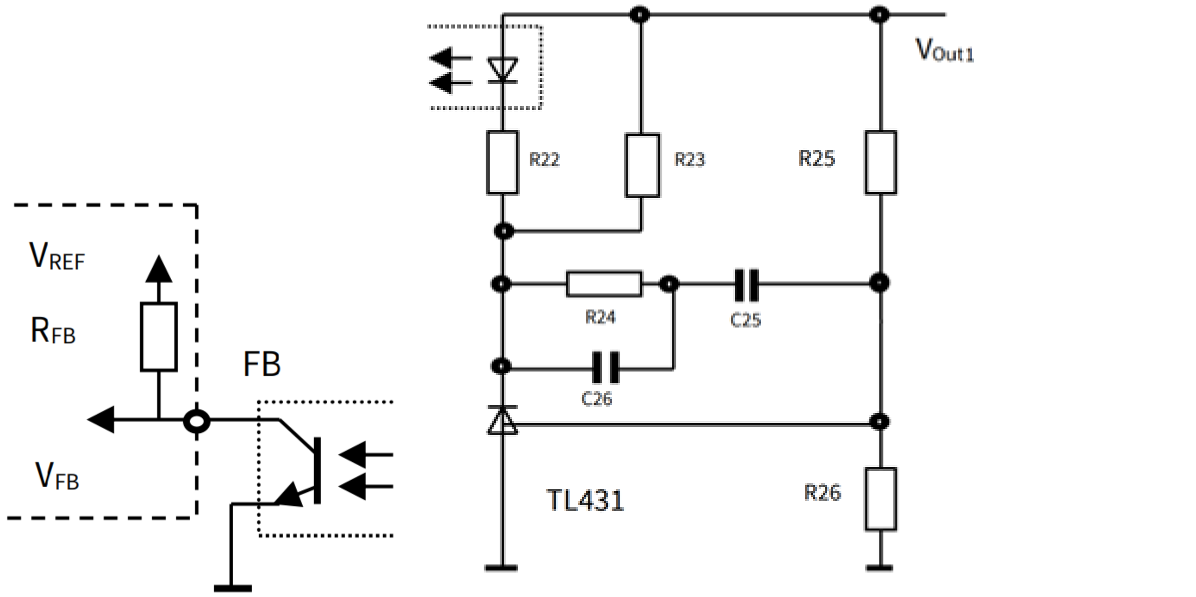
Result	CS resistor loss	Eq. 097	P_{CS}	[W]	0.10

MOSFET

Input	R_{DSON} from datasheet		R_{DSON} @ T_J=125°C	[Ω]	8.73
Input	Co(er) from datasheet		$C_{o(er)}$	[pF]	3.4
Input	External drain to source capacitance		C_{DS}	[pF]	0
Result	Switch on loss at minimum AC input voltage	Eq. 098	$P_{SONMinAC}$	[W]	0.0058
Result	Conduction loss at minimum AC input voltage	Eq. 099	$P_{condMinAC}$	[W]	0.8855
Result	Total MOSFET loss at minimum AC input voltage	Eq. 100	$P_{MOSMinAC}$	[W]	0.8913
Result	Switch on loss at maximum AC input voltage	Eq. 101	$P_{SONMaxAC}$	[W]	0.0364
Result	Conduction loss at maximum AC input voltage	Eq. 102	$P_{condMaxAC}$	[W]	0.2259
Result	Total MOSFET loss at maximum AC input voltage	Eq. 103	$P_{MOSMaxAC}$	[W]	0.2624

Appendix A: Transformer design and spreadsheet [3]

Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	0.8913
Controller					
Input	Controller current consumption		I_{VCC_Normal}	[mA]	0.9
Result	Controller loss	Eq. 104	P_{Ctrl}	[W]	0.0158
Efficiency after losses					
Result	Total power loss	Eq. 105	P_{Losses}	[W]	3.59
Result	Post calculated efficiency	Eq. 106	η_{Post}	Percent	80.68 percent
CoolSET™/MOSFET temperature					
CoolSET™/MOSFET temperature					
Input	Enter thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	82.0
Result	Temperature rise	Eq. 107	ΔT	[°K]	73.1
Result	Junction temperature at T_{amax}	Eq. 108	Tjmax	°C	123.1
Output regulation (isolated using TL431 and optocoupler)					
Isolated FB circuit					



Output regulation					
Input	TL431 reference voltage		V_{REF_TL}	[V]	2.5
Input	Current for voltage divider resistor R26		I_{R26}	[mA]	0.25
Result	Calculated voltage divider resistor	Eq. 111	$R26_{Cal}$	[kΩ]	10
Input	Select voltage divider resistor value		R26	[kΩ]	10
Result	Calculated voltage divider resistor	Eq. 112	$R25_{Cal}$	[kΩ]	38.00
Input	Select voltage divider resistor value		R25	[kΩ]	38.0
Optocoupler and TL431 bias					
Input	Current Transfer Ratio (CTR)		G_C	[Percent]	100 percent
Input	Optocoupler diode forward voltage		V_{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I_{Fmax}	[mA]	10
Input	Minimum current for TL431		I_{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance	Eq. 114	$R22_{Cal}$	[kΩ]	0.8250
Input	Select optocoupler bias resistor		R22	[kΩ]	0.82
Input	FB pull-up reference voltage V_{REF} from datasheet		V_{REF}	[V]	3.3
Input	V_{FB_OLP} from datasheet		V_{FB_OLP}	[V]	2.75
Input	R_{FB} from datasheet		R_{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance	Eq. 115	$R23_{Cal}$	[kΩ]	1.28
Input	Selected TL431 bias resistor		R23	[kΩ]	1.2
Regulation loop					
Result	FB transfer characteristic	Eq. 116	K_{FB}		18.29
Result	Gain of FB transfer characteristic	Eq. 117	G_{FB}	[db]	25.25
Result	Voltage divider transfer characteristic	Eq. 118	K_{VD}		0.208333

Result	Gain of voltage divider transfer characteristic	Eq. 119	G_{VD}	[db]	-13.62
Result	Resistance at maximum load pole	Eq. 120	R_{LH}	[Ω]	9.60
Result	Resistance at minimum load pole	Eq. 121	R_{LL}	[Ω]	96.00
Result	Poles of power stage at maximum load pole	Eq. 122	f_{OH}	[Hz]	70.55
Result	Poles of power stage at minimum load pole	Eq. 123	f_{OL}	[Hz]	7.05
Result	Zero frequency of the compensation network	Eq. 124	f_{OM}	[Hz]	22.31
Input	Zero dB crossover frequency		fg	[kHz]	3
Input	PWM-OP gain from datasheet		A_V		2.03
Result	Transient impedance	Eq. 117	Z_{PWM}	[V/A]	2.6
Result	Power stage at crossover frequency	Eq. 118	$\lvert F_{PWR}(fg)\rvert$		0.139
Result	Gain of power stage at crossover frequency	Eq. 119	$G_{PWR}(fg)$	[db]	-17.14
Result	Gain of the regulation loop at fg	Eq. 120	Gs(ω)	[db]	-5.521
Result	Separated components of the regulator	Eq. 121	Gr(ω)	[db]	5.521
Result	Calculated resistance value of compensation network	Eq. 122	$R24_{Cal}$	[kΩ]	14.95
Input	Select resistor value of compensation network		R24	[kΩ]	15
Result	Calculated capacitance value of compensation network	Eq. 123	$C26_{Cal}$	[nF]	3.537
Input	Select capacitor value of compensation network		C26	[nF]	1
Result	Calculated capacitance value of compensation network	Eq. 124	$C25_{Cal}$	[nF]	474.61
Input	Select capacitor value of compensation network		C25	[nF]	220

Output regulation (non-isolated)

Final design

Electrical

Minimum AC voltage			[V]	90
Maximum AC voltage			[V]	264
Maximum input current			[A]	0.20
Minimum DC voltage			[V]	95
Maximum DC voltage			[V]	373
Maximum output power			[W]	15.0
Output voltage 1			[V]	12.0
Output ripple voltage 1			[mV]	3.0
Transformer peak current			[A]	0.79
Maximum duty cycle				0.48
Reflected voltage			[V]	90
Copper losses			[W]	0.19
MOSFET losses			[W]	0.89
Sum losses			[W]	3.59
Efficiency			[Percent]	80.68 percent

Transformer

Core type				EE20/10/6
Core material				TP4A(TDG)
Effective core area			[mm²]	32
Maximum flux density			[mT]	225
Inductance			[µH]	583
Margin			[mm]	0
Primary turns			Turns	64
Primary copper wire size			AWG	29
Number of primary copper wires in parallel				1
Primary layers			Layer	2
Secondary 1 turns (N_{S1})			Turns	9
Secondary 1 copper wire size			AWG	31
Number of secondary 1 copper wires in parallel				7
Secondary 1 layers			Layer	2
Auxiliary turns			Turns	13
Leakage inductance			[µH]	4.9

Components

Input capacitor (C1)			[µF]	33.0
Secondary 1 output capacitor (C152)			[µF]	470.0

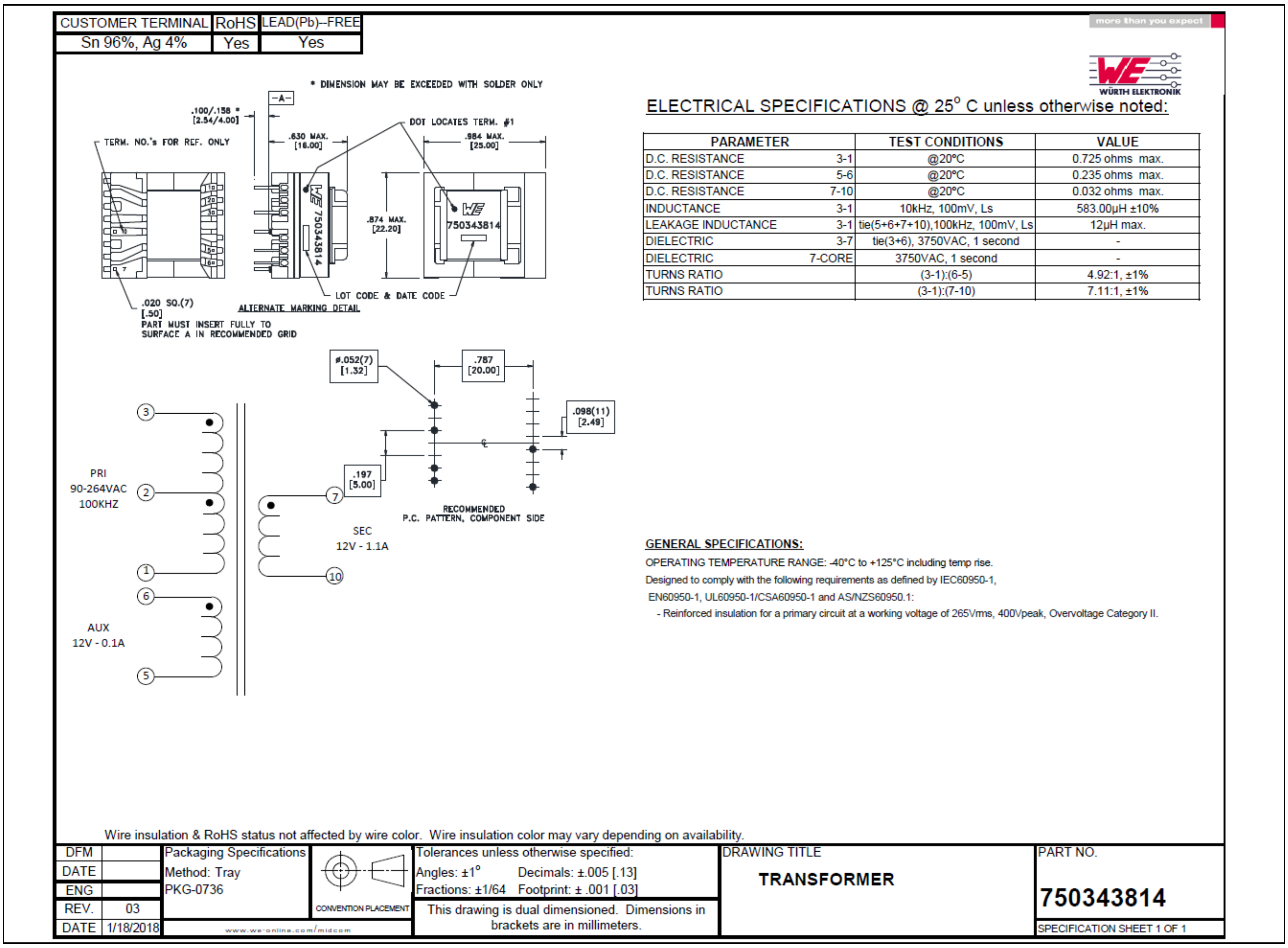
Appendix A: Transformer design and spreadsheet [3]

Secondary 1 output capacitor in parallel				1.0
Secondary 1 LC filter inductor (L151)			[µH]	0.2
Secondary 1 LC filter capacitor (C153)			[µF]	470.0
V_{CC} capacitor (C3)			[µF]	10.0
Sense resistor (R8A, R8B)			[Ω]	1.01
Clamping resistor (R4)			[kΩ]	150.0
Clamping capacitor (C2)			[nF]	1
High-side DC input voltage divider resistor (R3A, R3B, R3C)			[MΩ]	0
Low-side DC input voltage divider resistor (R7)			[kΩ]	0

Regulation components (isolated using TL431 and optocoupler)

Voltage divider		R26	[kΩ]	10.0
Voltage divider (V_{OUT1} sense)		R25	[kΩ]	38.0
Optocoupler bias resistor		R22	[kΩ]	0.82
TL431 bias resistor		R23	[kΩ]	1.2
Compensation network resistor		R24	[kΩ]	15.0
Compensation network capacitor		C26	[nF]	1.00
Compensation network capacitor		C25	[nF]	220.0

13 Appendix B: WE transformer specification



PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	3-1	@20°C	0.725 ohms max.
D.C. RESISTANCE	5-6	@20°C	0.235 ohms max.
D.C. RESISTANCE	7-10	@20°C	0.032 ohms max.
INDUCTANCE	3-1	10kHz, 100mV, Ls	583.00µH ±10%
LEAKAGE INDUCTANCE	3-1	tie(5+6+7+10),100kHz, 100mV, Ls	12µH max.
DIELECTRIC	3-7	tie(3+6), 3750VAC, 1 second	-
DIELECTRIC	7-CORE	3750VAC, 1 second	-
TURNS RATIO		(3-1):(6-5)	4.92:1, ±1%
TURNS RATIO		(3-1):(7-10)	7.11:1, ±1%

Figure 35 WE transformer specification

14 References

[1] ICE5AR4770BZS datasheet, Infineon Technologies AG

[2] 5th-Generation Fixed-Frequency Design Guide

[3] Calculation Tool Fixed-Frequency CoolSET™ Generation 5

Revision history

Document version	Date of release	Description of changes
V1.0	8 Feb 2018	First release

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Edition 2018-02-08

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
AN_1801_PL83_1802_091238