Half-bridge evaluation board with 100 V CoolGaN™ power transistor and EiceDRIVER™ 1EDN7136U gate driver user guide

About this document

Scope and purpose

This user guide provides an overview and detailed feature description of the EVAL_7136U_100V_GaNc general purpose half-bridge evaluation board with the CoolGaN™ power transistor IGC033S10S1 and EiceDRIVER™ 1EDN7136U truly differential input (TDI) gate driver. The board can be used for testing and assessing the performance of the products in half-bridge applications such as DC-DC conversion or motor drives. It provides a flexible platform for evaluating and optimizing the switching performance of these products under different operating conditions. Additionally, it gives a reference for the recommended PCB layout for a half-bridge and gate driving circuit with these products.

EVAL_7136U_100V_GaNc Evaluation Board is designed to showcase the performance of the IGC033S10S1 transistor when used with the 1EDN7136U gate driver in a half-bridge configuration. For that purpose, it provides optimized waveform measurement points as well as other features enabling easy lab bench usage.

A detailed description of the gate driver 1EDN7136U is available online [1] as well as the datasheet for the IGC033S10S1 [2].

Intended audience

This document is for power electronic engineers, technicians, and developers of power electronic systems who are interested in evaluating the performance of the CoolGaN™ power transistor 100 V IGC033S10S1 as and EiceDRIVER™ 1EDN7136U gate driver.

Table of contents

1 Introduction

EVAL_7136U_100V_GaNc Evaluation Board shown in Figure 1 is for general-purpose evaluation of CoolGaN™ power transistor 100 V IGC033S10S1 in a PQFN package, along with EiceDRIVER™ 1EDN7136U TDI gate driver. This board includes an optimized layout for a hard-switching half-bridge, as well as waveform measurement points and other useful features to enable easy lab bench characterization of these transistors and drivers. It is preconfigured as a buck or boost converter but can easily be reconfigured for a double-pulse test or any half-bridge topology with external connections.

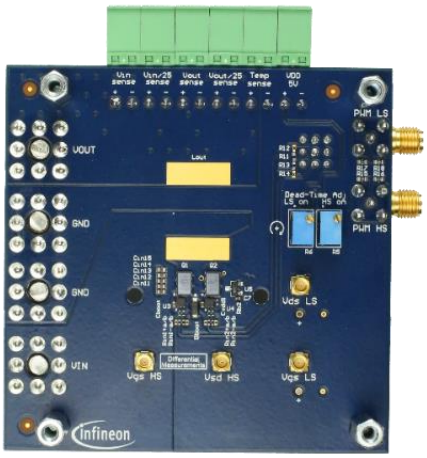


Figure 1 EVAL_7136U_100V_GaNc Evaluation Board

1.1 EiceDRIVER™ 1EDN7136U gate driver

EiceDRIVER™ 1EDN7136U is an optimized gate driver IC that is designed for driving CoolGaN™ power transistors. It features a truly differential input (TDI), active Miller clamp, bootstrap voltage clamp, and low-inductance TSNP package, which are all essential for a high-performance system design with fast-switching transistors. TDI allows the gate driver output state to be controlled solely by the voltage difference between the two inputs. This is regardless of the driver's reference potential, as long as the common-mode voltage remains below 150 V (static) and 200 V (dynamic). This feature eliminates the risk of false triggering caused by ground bounce in low-side driving and enables 1EDN7136U to be used as a high-side driver.

The driver can be used with gate resistors (R_{GON}/R_{GOFF}) on the split source and sink outputs, but this board instead offers an optimized gate loop with no provision for gate resistors. To change the driving strength and switching speed, the driver variant can be changed instead. In Section 5.4, example results are shown to demonstrate the influence of changing the gate driver variant.

The board comes with two 1EDN7136U assembled. These are a variant of the EiceDRIVER™ 1EDN71x6U family. It has four variants with different driving strengths available in the same package type and footprint. An overview of the important parameters for all variants is given in Table 1.

Table 1 EiceDRIVER™ 1EDN7136U family variants

Part number	Peak source/sink current	Input pulse blanking time	Typical propagation delay
1EDN7116U	2.0 A	20 ns	55 ns
1EDN7126U	1.5 A	40 ns	75 ns
1EDN7136U	1.0 A	60 ns	105 ns
1EDN7146U	0.5 A	80 ns	125 ns

1.2 EVAL_7136U_100V_GaNc Evaluation Board

The main parts of the EVAL_7136U_100V_GaNc Evaluation Board are:

- CoolGaN™ power transistor IGC033S10S1 transistors in a half-bridge configuration
- EiceDRIVER™ 1EDN7136U gate driver

It can be controlled by two pulse width modulation (PWM) input signals. If only one PWM is available, the second PWM signal can be generated by using the on-board dead-time generation circuit. With the dead-time circuit, both dead-times can be set using onboard trimmers within a specified range.

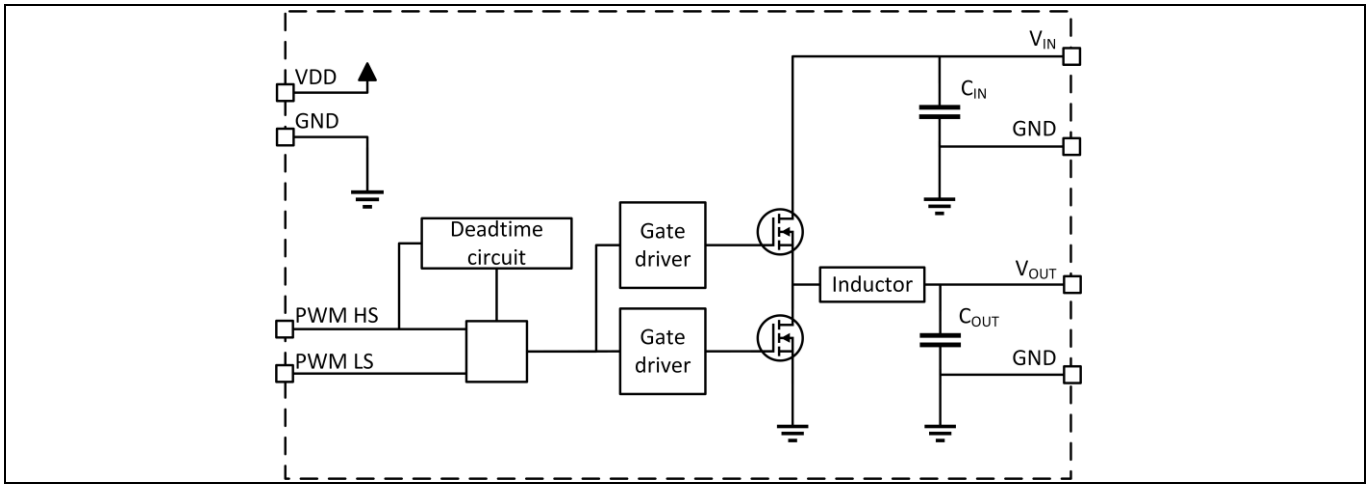


Figure 2 EVAL_7136U_100V_GaNc Evaluation Board

The board comes without a power inductor assembled but two large pads are available to solder any kind of power inductor. Input and output capacitors are assembled on-board, providing enough capacitance for most of the operating conditions. A DC power supply and load can be connected to the four power connectors labeled as “V_{IN}”, “V_{OUT}”, and “GND”.

1.3 Board specifications

Table 2 Recommended operating conditions

Parameter	Values			Unit	Note
	Min	Typ	Max		
V_{DD} supply voltage	4.5	5	5.5	V	–
V_{IN} to GND	–	–	80	V	–
V_{OUT} to GND	–	–	80	V	–
PWM voltage level	–	5	–	V	Rework needed for 3.3 V signals, see 4.1
DC input/output current	–	–	25	A	At 1 MHz and 48 V with bottom-side heatsink and 5 m/s airflow [1]

Table 3 Board characteristics

Parameter	Values			Unit	Note
	Min	Typ	Max		
V_{DD} supply current	–	20	–	mA	At 1 MHz switching frequency
V_{IN} to GND	–	–	100	V	Limited by capacitor ratings
V_{OUT} to GND	–	–	100	V	Limited by capacitor ratings
On-board dead-time adjustment range	7	–	100	ns	Limits depend on accuracy of trimmers
PWM pulse width	71	–	–	ns	Limited by gate driver

[1] The maximum DC current can be much higher at different switching frequencies and cooling conditions and is also limited by the saturation of the power inductor used.

1.4 Main board features

EVAL_7136U_100V_GaNc half-bridge evaluation board comes with additional features to support evaluation next to the half-bridge itself.

- There is an onboard dead-time generation circuit (mentioned in Section 1.1) can generate the second PWM control signal for the low-side gate driver when only one PWM signal is supplied to the board.
- Both dead-times between these two signals can be modified with the on-board trimmers. Rotating each trimmer clockwise will extend the respective dead-time within the specified range. The different options for PWM input can be selected with jumpers, as explained in Section 2.5.
- A custom heatsink is provided that can be mounted on either side of the board for cooling the half-bridge. Steps to assemble the heatsink are described in 2.6.
- There are options to measure DC voltages V_{IN} and V_{OUT} directly or attenuated, as well as the gate and drain-to-source waveforms of both switches. For detailed descriptions for all voltage measurements, see Section 3.
- An on-board temperature sensor, which is located close to the half-bridge. The sensor provides the temperature information of the board, not necessarily the device temperature. This can be used for a safety shutdown. If the specific component temperature is of interest, the use of a thermal infrared camera is recommended as explained in Section 3.3.
- The main feature of the 1EDN7136U gate driver is that the high-side switch is supplied via the BST pin of the low-side driver. This prevents overcharging of the bootstrap capacitor and the resulting overvoltage on the high-side gate. This is important because the maximum continuous gate voltage rating of the IGC033S10S1 is 5.5 V.
- The board also offers the possibility to supply the bootstrap voltage directly from V_{DD}, by implementing the rework instructions in Section 4.3. For conventional bootstrapping from V_{DD}, a Zener diode is highly recommended to prevent the applied gate voltage from exceeding the devices maximum rating of the device.

1.5 CoolGaN™ 100 V power transistor

The CoolGaN™ power transistor 100 V IGC033S10S1 comes in a PQFN package with very low inductance in the pH range, as well as dual-side cooling with an exposed thermal pad on the top-side of the transistor.

IGC033S10S1 can be operated at high switching frequencies and short dead-times due to its fast-switching transitions and low switching loss. This enables reducing the size of magnetics, capacitors, and heatsinks in the application to improve power density and overall system efficiency.

Alternatively, IGB110S10S1 can also be assembled on the board as described in Section 4.5. IGB110S10S1 comes in a 3 mm x 3 mm PQFN package with an exposed die for dual-side cooling [3]. Both packages are shown in Figure 3.

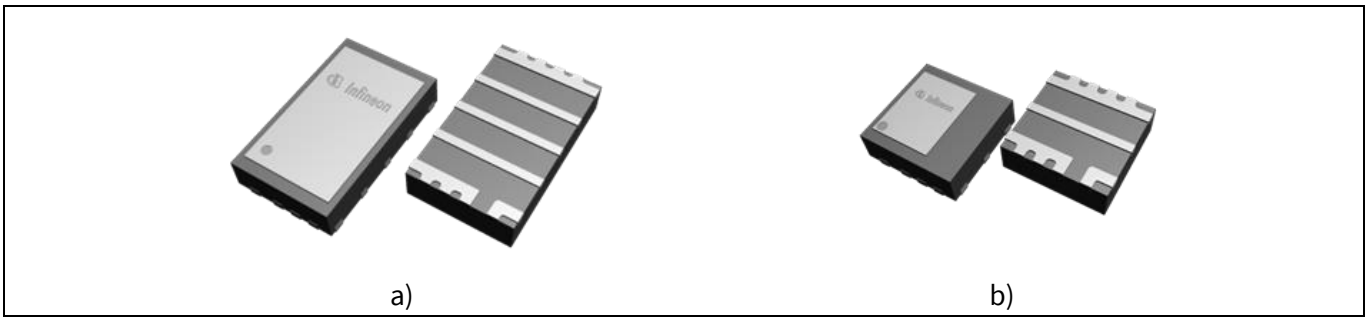


Figure 3 CoolGaN™ power transistors IGC033S10S1 (a) and IGB110S10S1 (b)

2 Test setup description

The design and connections of the EVAL_7136U_100V_GaNc Evaluation Board can be used in different test setups. It can be operated in the following configurations:

- Buck converter test
- Boost converter test
- Buck-mode double pulse test
- Boost-mode double pulse test

Recommended operating conditions

- **Input and output voltage:** Maximum 60 V input and output voltage with the switching frequency in the range of 200 kHz to 1 MHz.
- **Input/output current:** The maximum input/output currents are dependent on the thermal configuration and are in the range of 20 A to 30 A. However, if the voltage and temperature ratings of the board components are not violated, you can choose to exceed the voltage, frequency, and current at your own discretion.

The following sections describe how to connect the board for each configuration.

2.1 Buck converter test setup

For performance characterization as well as waveform measurements.

Next to performance evaluation, this setup can be used to measure the gate and drain voltage waveforms of the low-side switch when soft-switching as a synchronous rectifier, as well as hard switching waveforms of the high-side switch. In this configuration, the board must be connected with one of the PWM input options as shown in Figure 4 and described in Section 2.5.

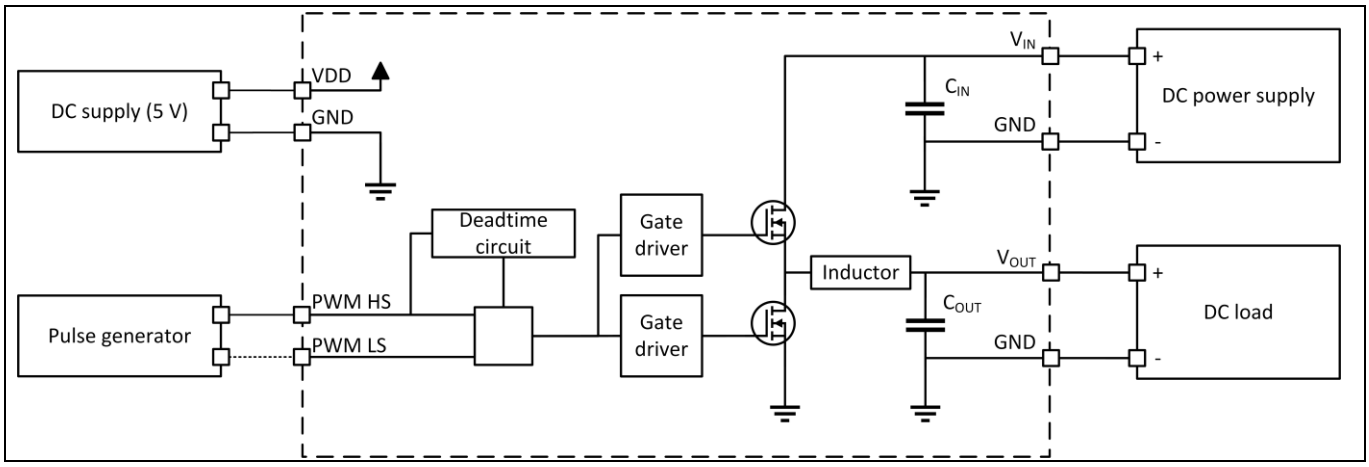


Figure 4 Block diagram of buck converter test setup

2.2 Boost converter test setup

For performance characterization as well as waveform measurements.

Next to performance evaluation, this setup can be used to measure the gate and drain voltage waveforms of the low-side switch when hard-switching, as well as the high-side waveforms when soft switching. To set up the board as a boost converter, the connections for V_{IN} and V_{OUT} must be reversed, with a voltage supply on V_{OUT} and a DC load on V_{IN} as shown in Figure 5.

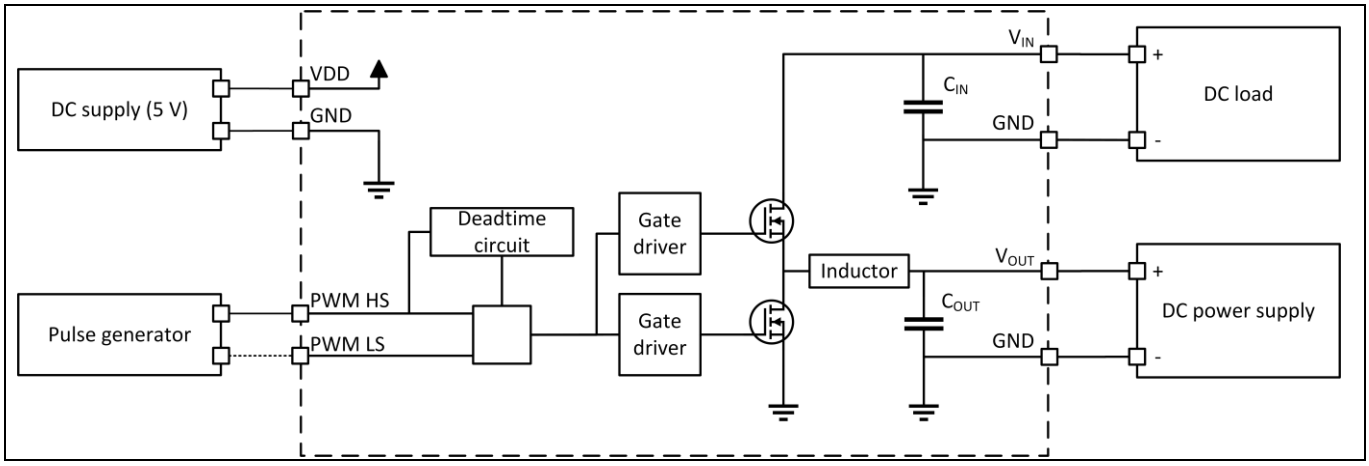


Figure 5 Block diagram of boost converter test setup

2.3 Buck-mode double pulse test setup

Two different types of double pulse tests can be performed, buck-mode and boost-mode. For both modes the inductor should have a high inductance value, typically in the range of 10 µH to 100 µH, often routed off-board with cables to allow inductor current measurement using a split-core current probe.

Buck-mode double pulse testing enables capturing soft-switching voltage waveforms without self-heating effects.

V_{OUT} should be connected to GND, and a DC power supply connected to V_{IN} as shown in Figure 6.

Two pulses are sent to the high-side PWM:

- One long pulse to raise the inductor current to the desired level
- One short pulse to view the turn-on and turn-off transitions, see [8] and [9].

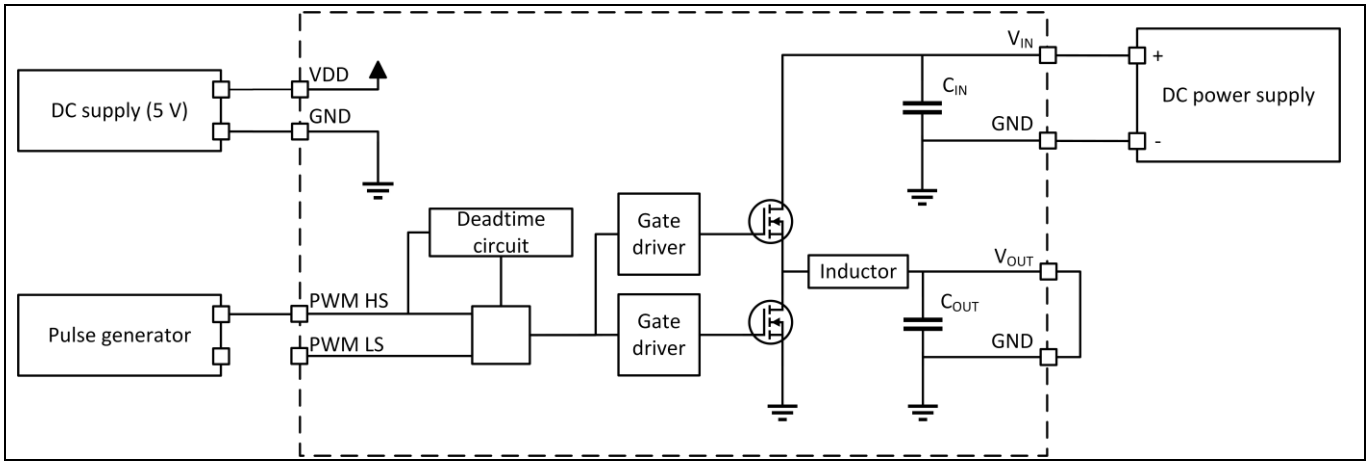


Figure 6 Block diagram of buck-mode double pulse test setup

Typically, the low-side PWM input should be manually set to 0 V for safety during this test. This can be implemented on jumper J3 as shown in Figure 9. As the high-side gate driver is per default supplied via bootstrapping from the low-side driver, it is mandatory for this setup to change the bootstrapping to come from V_{DD} directly as explained in 4.3.

2.4 Boost-mode double pulse test setup

For capturing hard-switching voltage waveforms without self-heating effects.

The V_{IN} to V_{OUT} connectors should be shorted together, with one DC voltage supply controlling both voltage nodes as shown in Figure 7.

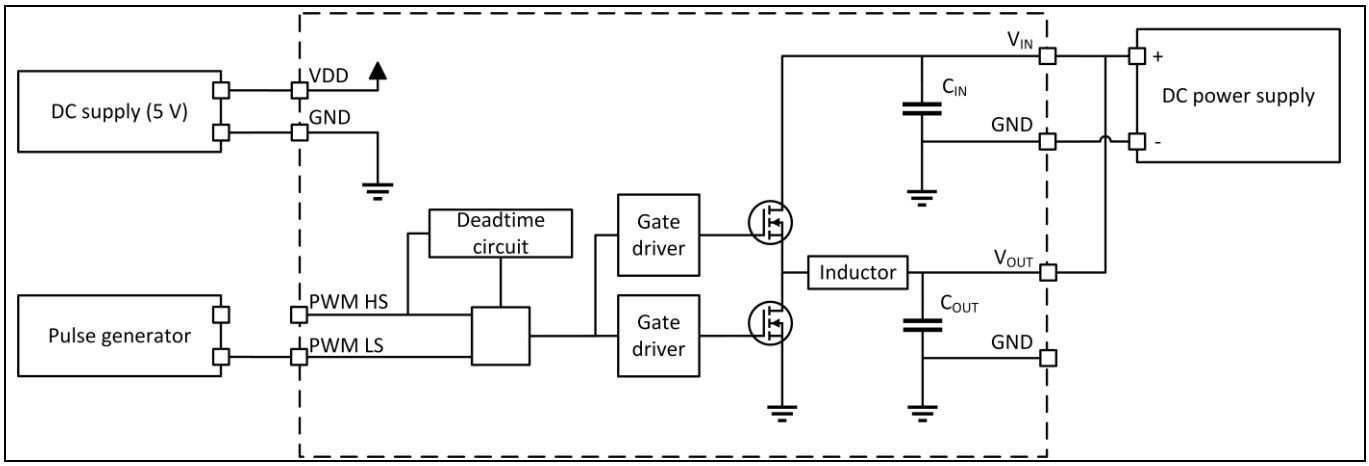


Figure 7 Block diagram boost converter double pulse test setup

For boost-mode double pulse testing, two pulses are sent to the low-side PWM:

- One long pulse to raise the inductor current to the desired level
- One short pulse to view the turn-on and turn-off transitions

The high-side PWM can be switched complementarily to the low-side, but this is typically not necessary in a double pulse test. In this case, the high-side PWM input should be manually set to 0 V for safety during this test. This can also be done on jumper J3 as shown in Figure 9.

2.5 PWM input options

There are different options for the PWM signals to control the half-bridge:

- Dual 5 V logic inputs with 50 Ω terminated SMA
- Dual 3.3 V logic inputs with 50 Ω terminated SMA (rework needed per Section 4.1)
- Dual 5 V logic inputs with high-Z terminated 3-pin header
- Dual 3.3 V logic inputs with high-Z terminated 3-pin header (rework needed per Section 4.1)
- Single high-side 5 V logic input with 50 Ω terminated SMA, using on-board dead-time generator

When using a two-channel benchtop function/waveform generator to supply both high-side and low-side PWM signals, connect them via the two SMA connectors “PWM HS” and “PWM LS”. Each SMA input is terminated with 50 Ω, and the function generator must be configured to drive a 50 Ω load. In the default configuration of the board, all logic signals must be based on 5 V, not 3.3 V. To configure the board for 3.3 V logic, the TDI resistors must be reworked per the instructions in Section 4.1.

A single high-side PWM signal can be connected from a waveform generator, with 5 V logic and 50 Ω terminated SMA. In this configuration, both PWM signals are generated using the on-board dead-time generation circuit with dead-time determined by trimmer resistors (R5 and R6). The outputs of this dead-time generating circuit are complementary 5 V logic signals. The maximum dead-time achievable with this circuit is approximately 100 ns per edge, but it is recommended to start with a value close to 10 ns per edge.

The third option is to supply dual PWM signals directly to the header J1, but with a high-Z termination rather than 50 Ω. The function generator or other signal source must be configured to drive a high impedance load, rather than 50 Ω.

Figure 8 demonstrates how to set the jumpers or connect to a high-Z source on connector J1.

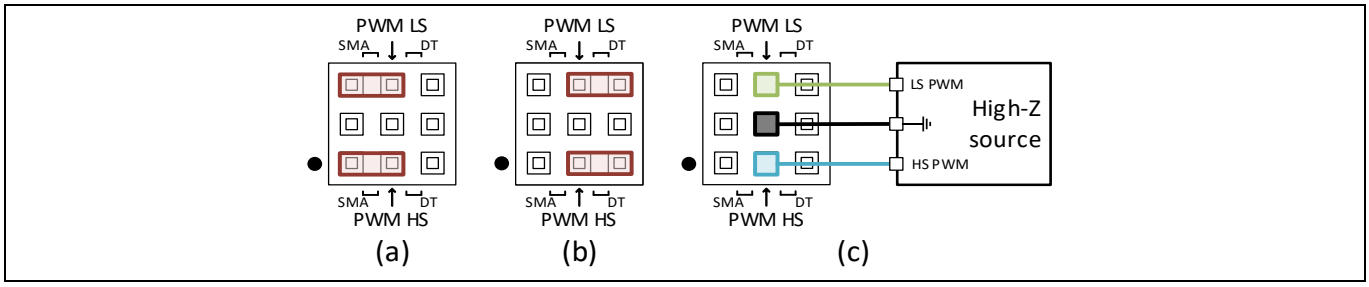


Figure 8 (a) Jumper J1 settings for dual 50 Ω logic inputs, (b) single high-side 5 V logic input, and (c) dual 5 V high-Z terminated logic inputs

The dead-time can only be adjusted with the trimmers on-board if the jumpers are set according to Figure 8(b). For the other options, the dead-time is defined by the dual PWM signals.

To perform double pulse tests, the jumper settings for buck-mode and boost-mode should be set as shown in Figure 9.

- For buck-mode, the low-side PWM channel is tied to GND, and pulses are sent only to the high-side PWM channel.
- For boost-mode, the high-side PWM channel is tied to GND, and the low-side PWM channel input is used to control the pulses.

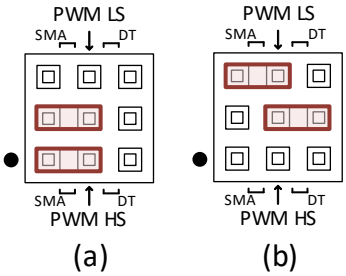


Figure 9 Double pulse test jumper settings for buck-mode (a) and boost-mode (b)

2.6 Heatsink attachment options

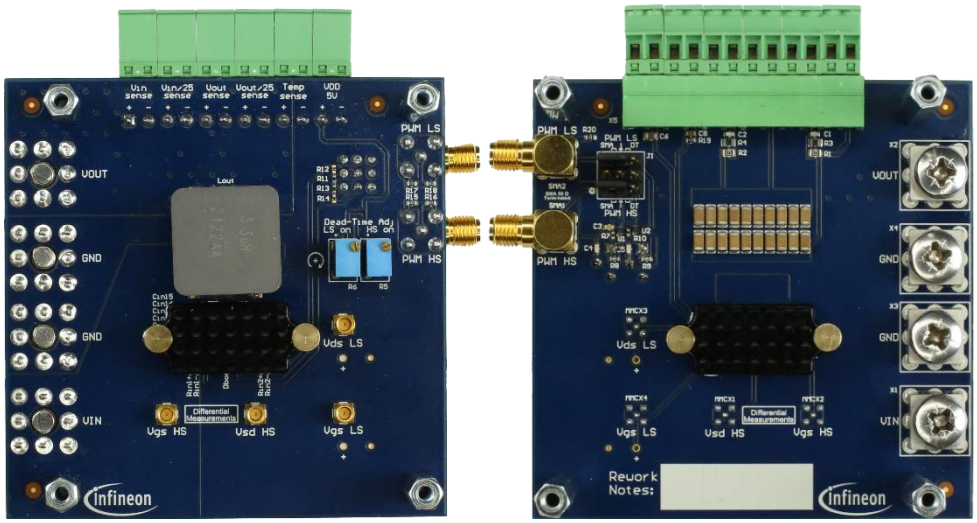
The provided heatsink comes with a preinstalled thermal interface material (TIM) pad of T-Global TG-A1780, which is an ultra-soft galvanically isolated TIM pad with a thermal conductivity of 17.8 W/m·K and a thickness of 0.5 mm. Recommended TIM pads from t-Global include TG-A1780, TG-A1660, TG-A1450, TG-A1250, depending on the preference for cost vs. performance.

The heatsink can be installed on the bottom-side of the PCB for bottom-side cooling or on top of the transistors for dual-sided cooling, as shown in Figure 10.

Install the heatsink

1. Remove the plastic protective tape from the TIM pad.
2. Position the heatsink at the desired location.
3. Press down on both the spring pins at the same time.

Note: Use two flathead (slotted) screwdrivers or similar tools to avoid finger injuries on the pin fins as shown in Figure 11.



(a) (b)

Figure 10 (a) Heatsink attachment top-side and (b) bottom side

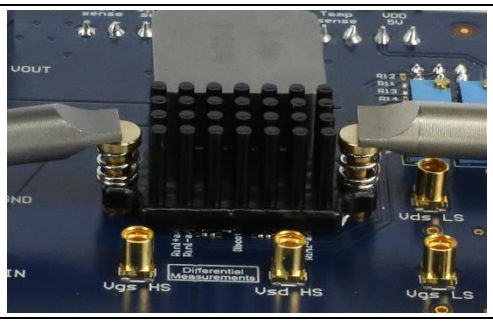
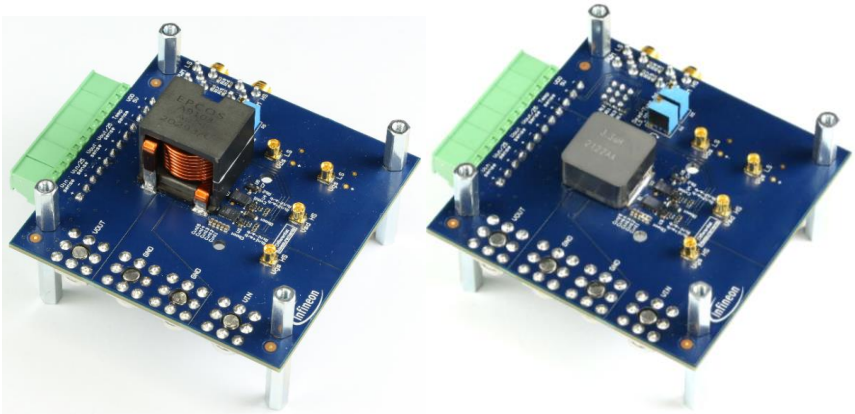


Figure 11 Heatsink attachment with two flathead screwdrivers to compress spring pins

2.7 Inductor mounting

Figure 12 shows two different inductors soldered to the board. A 10 µH inductor from TDK ERU series (a), and on the right a 3.3 µH inductor from Vishay's IHLP7575-JZ series (b).



(a) (b)

Figure 12 (a) Mounted inductors – TDK ERU series and (b) Vishay IHLP7575-JZ series

3 Measurement options

3.1 DC voltage measurements

The board is equipped with convenient screw terminal plugs for the DC measurements. Input and output voltage can be measured with or without 25x attenuation, making it compatible with a digital multimeter or datalogger for efficiency measurements, or alternatively for inputs to an external controller.

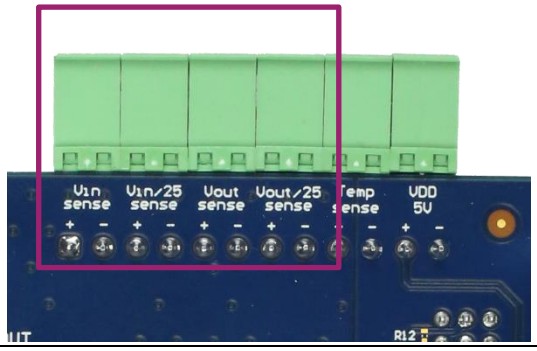


Figure 13 Screw terminal plugs for DC voltage measurement

3.2 Waveform measurements

The board offers multiple options to capture device switching waveforms, which are all circled in Figure 14.

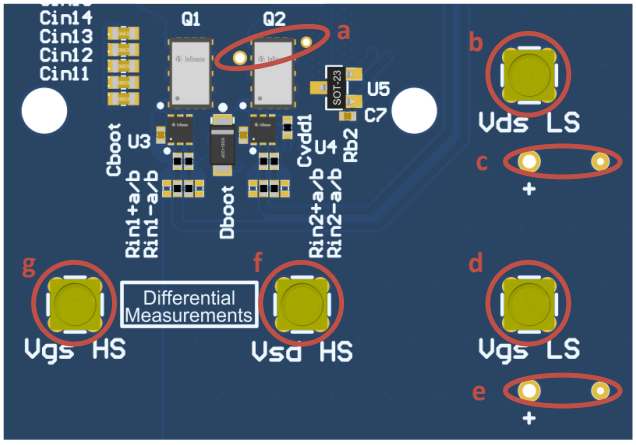


Figure 14 Device waveform measurements points

a) V_{DS} LS near device
b) V_{DS} LS MMCX
c) V_{DS} LS far
d) V_{GS} LS MMCX
e) V_{GS} LS far
f) V_{SD} HS MMCX
g) V_{GS} HS MMCX

The drain-to-source voltage of the low-side device (V_{DS} LS) can be measured at three different points, once with an MMCX tip and two times at vias with a spring clip probe. Once near the device (a) and the other is further away (c), next to the MMCX connector (b).

The low-side gate-to-source voltage (V_{GS} LS) can be measured with an MMCX tip (d) and a spring clip probe at vias (e) next to the MMCX connector.

The high-side device source-to-drain voltage (V_{SD} HS) and gate-to-source voltage (V_{GS} HS) can be measured with a differential probe with MMCX tips, (f) and (g), respectively.

Low-side single-ended voltage measurements

Any passive probe can be used to measure low-side voltage waveforms for CoolGaN™ power transistors, but they should have suitable bandwidth and connectivity. The recommended bandwidth for all voltage probes and oscilloscopes is a minimum 1 GHz. The loop between the probe tip and the measurement points (both + and – sides) should be within 10 mm, preferably shorter.

For example, the recommended probing solution is the Tektronix TPP1000 [4] with an MMCX tip adapter 206-0663-xx, which guarantees the tightest possible probing loop for this tip as shown in Figure 15. Alternative to the passive MMCX probe is the MMCX-A1025 probe from PMK [7]. As a second option, a “spring clip” probe tip solution may be employed at the provided vias, but this does degrade the measurement fidelity to some degree.

The V_{DS} LS waveform can be measured at three locations on the board: MMCX connector (b), two vias beside the MMCX connector (c), or two at the vias located close to the low-side switch (a). V_{GS} LS can be measured at the MMCX connector or at the vias beside it.

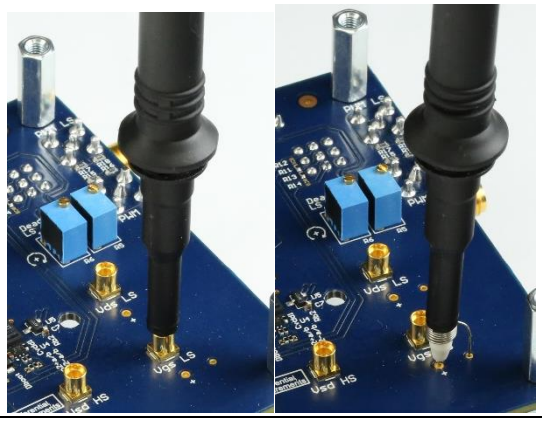


Figure 15 Low-side single ended voltage measurements options

High-side differential voltage measurements

In general, high-side voltage waveforms are challenging for a GaN-based half-bridge circuit, due to the extremely high dv/dt and di/dt involved. The most accurate measurement scheme comes from an extremely high-bandwidth optically isolated probing system, for example the IsoVu probe system from Tektronix [5] or the FireFly series from PMK [6].

Figure 16 High-side differential voltage measurements with high-bandwidth differential probes

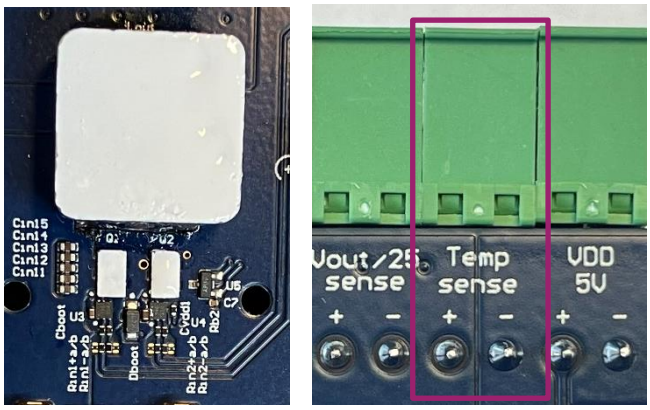
The high-side drain measurement connector is configured for V_{SD} rather than V_{DS}, because a measurement with a stable DC reference point typically results in more accurate measurements. However, most oscilloscopes allow for convenient inverting of measurement channels to translate V_{SD} into V_{DS}.

In addition to the bandwidth of the probing system, the probing loop connectivity is critical. An MMCX tip adapter for high-side differential measurements is very important for an accurate measurement with the highest fidelity and the lowest signal degradation.

3.3 Temperature measurements

The board is equipped with an on-board PCB temperature sensor, but it is recommended to use a contacting thermocouple solution or an infrared thermal camera to capture the temperature of the CoolGaN™ power transistor, as well as the power inductor.

When using a thermal camera, it is highly recommended to paint all target surfaces with a matte-finish paint (white or black is commonly used) to ensure the consistency of the emissivity for all temperature measurements. Reflections that can distort the temperature captured by a camera can also be avoided [10].



(a) (b)

Figure 17 (a) Exemplary painted surfaces for temperature measurement with a thermal infrared camera and (b) screw terminal plug connection to sense the output of the on-board temperature sensor

4 Rework options

4.1 TDI resistor adjustment for 3.3 V PWM input

EiceDRIVER™ 1EDN7136U gate driver utilizes a truly differential input (TDI) circuit for common-mode voltage rejection to level-shifting or galvanic isolation. Input resistor values must be selected based on the logic voltage level of the PWM inputs, for example, 5 V or 3.3 V. The default configuration of the board has a TDI resistance of 28 kΩ + 47 kΩ = 75 kΩ, which is required for a 5 V logic input.

To use dual 3.3 V logic inputs, for example, from an external control board, the input resistance must be reduced from 75 kΩ to 47 kΩ. To enable 3.3 V logic inputs, solder 0 Ω resistors or solder bridge the four empty 0402 footprints in parallel with the 28 kΩ resistors, leaving only 47 kΩ un-bypassed as shown in Figure 18.

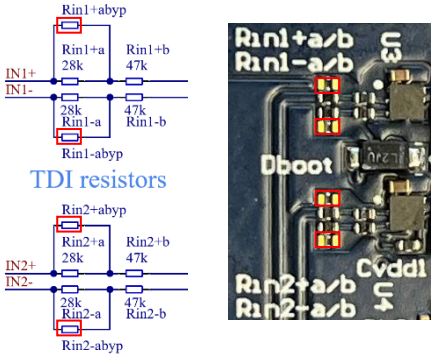


Figure 18 Rework option for 3.3 V input PWM signals

4.2 Cross-connected PWM inputs for overlap protection

By default, the input PWM signals can be overlapped to achieve very short dead-times. However, overlap protection can be enabled by cross-connecting the IN+ and IN– signals between the EiceDRIVER™ 1EDN7136U gate drivers. To implement this feature, the two 0 Ω resistors (R11 and R13) must be removed and instead soldered in positions R12 and R14, as shown in Figure 19. With this rework, the shortest achievable effective dead-time may be slightly higher.

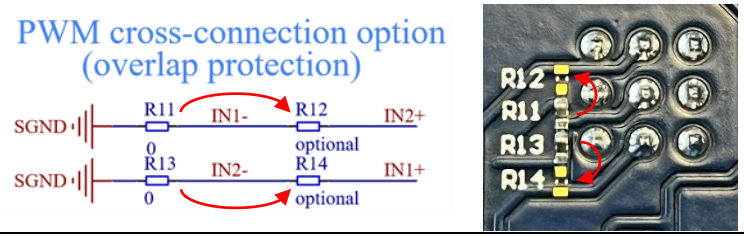


Figure 19 Rework option for overlap protection of the PWM input signals

4.3 Conventional bootstrapping direct from V_{DD} with Zener regulation

The EiceDRIVER™ 1EDN7136U gate driver provides a useful feature to avoid overcharging the bootstrap capacitor by connecting the bootstrap diode to the BST pin of the low side gate driver instead of directly feeding it from V_{DD}.

However, you can also use conventional bootstrapping. To change bootstrapping schemes, remove resistor R_{b2} and populate R_{b1} with a value in the range of 1 Ω to 4.7 Ω.

In such a configuration, it is recommended to populate position Dz with a 5.1 V~5.6 V Zener diode in an SOD523 package, for example, BZT585B5V6T-7. It may be more difficult to install a bottom-side heatsink with R_{b2} and Dz installed.

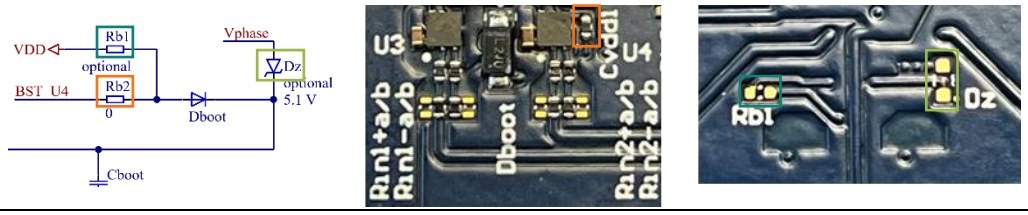


Figure 20 Rework instructions for conventional bootstrapping from V_{DD}

4.4 Split ground option

SGND and PGND are the two different grounds that exist on the board, as shown in the schematic in Section 6.1. By default, both grounds are connected with the resistor (R20). This is needed for the dead-time generation circuit to work properly. If the dead-time circuit is not used, then R20 can be removed to isolate the external PWM generator's reference from PGND.

4.5 Changing the CoolGaN™ power transistor

The evaluation board comes with the EiceDRIVER™ 1EDN7136U and the CoolGaN™ power transistor IGC033S10S1 assembled. As already mentioned in Section 1.1, the driver family has four variants with different driving strengths in the same package. Therefore, the change of the driver is a simple one to one replacement. It is not recommended to use different driver variants to drive the high-side and low-side transistors of the same half-bridge, due to propagation delay differences as shown in the table below.

The evaluation board comes with CoolGaN™ power transistor IGC033S10S1 in a 3 mm x5 mm PQFN package assembled. Alternatively, the IGB110S10S1 transistor can also be assembled on the board. The transistor's 3 mm x3 mm PQFN package can be soldered on the 3 mm x5 mm PQFN footprint, as shown in Figure 21.

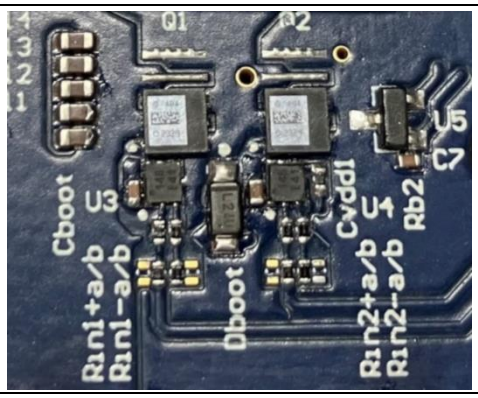


Figure 21 Reworked board with IGB110S10S1 assembled instead of IGC033S10S1

5 Example experimental results

In this section, the results shown have been measured with this board in different operating modes. Results are shown for buck and boost-mode operation, including example waveforms. To show the influence of changing the gate driver to another variant of the EiceDRIVER™ 1EDN71x6U family, efficiency results, and waveforms are shown in Section 5.4. Finally, example thermal images are shown in Section 5.5 for different cooling conditions.

5.1 Example experimental efficiency and power loss

The efficiency and power loss are determined by measuring the input and output voltage at the measurement connector, an input and output current between the board, the source/load, and the supply voltage and current of the auxiliary V_{DD}, then calculated as follows:

$$P_{LOSS} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT} + V_{DD} \cdot I_{DD}$$

Equation 1

$$\eta = \frac{V_{OUT} \cdot I_{OUT}}{(V_{IN} \cdot I_{IN}) + (V_{DD} \cdot I_{DD})}$$

Equation 2

The efficiency and power loss results are shown for the board operating in buck mode with an input voltage of 48 V, an output voltage of 12 V, at two different switching frequencies of 500 kHz and 1 MHz, and with three different cooling conditions.

First, the test was run without any heatsink attached or forced airflow, then with an airflow of 5 m/s and the heatsink attached to the bottom side of the board, and third with 5 m/s airflow and the heatsink on the top side of the board.

Figure 22 and Figure 23 show the results for a TDK ERU 10 µH inductor mounted on the board, whereas in Figure 24 and Figure 25 the results are shown for a Vishay IHLP7575-JZ 3.3 µH inductor.

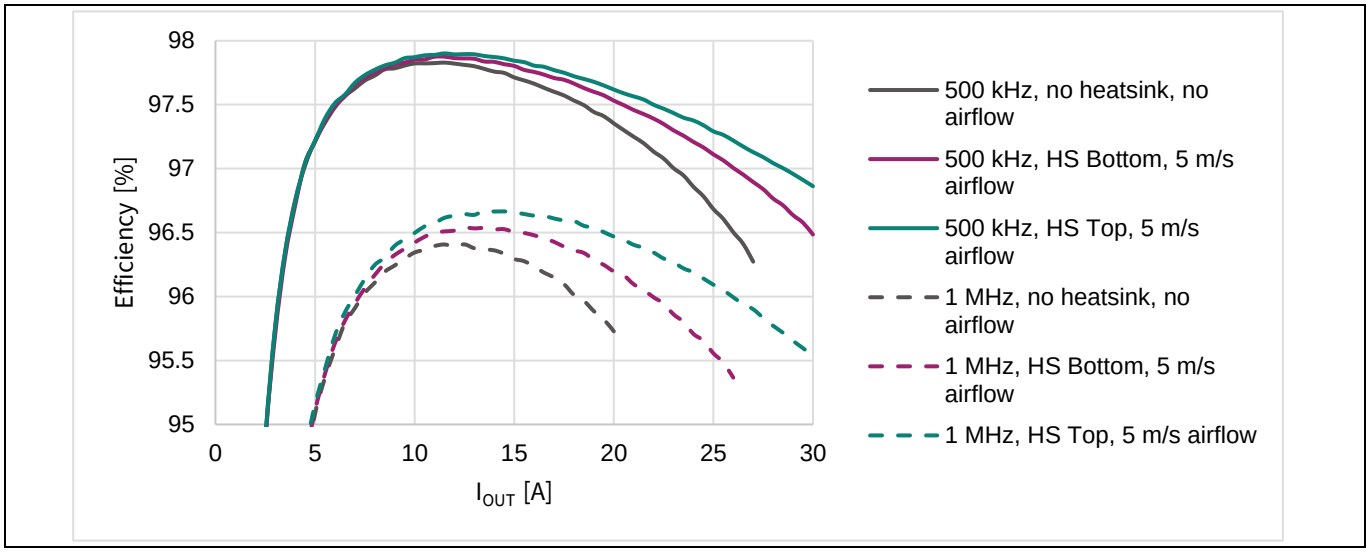


Figure 22 Example efficiency results with TDK ERU 10 µH inductor

Efficiency results are better for 500 kHz switching frequency, because of the lower switching loss. However, the results at 1 MHz still show a very good performance, due to the very low Q_{OSS} of IGC033S10S1 compared to conventional MOSFETs.

The influence of different cooling conditions is clearly visible. The best results can be achieved with the heatsink attached on top, because the IGC033S10S1 is a dual-side cooling package, and the heat flow is the best to the top side of the package with its large, exposed die area.

With the heatsink attached on bottom, the losses increase at higher currents compared to the top-side heatsink results because of the superior thermal performance of dual-side cooling.

The same behavior is visible for the condition with no heatsink and no airflow, where the losses are higher than the dual-side cooling scenario at an even lower output current.

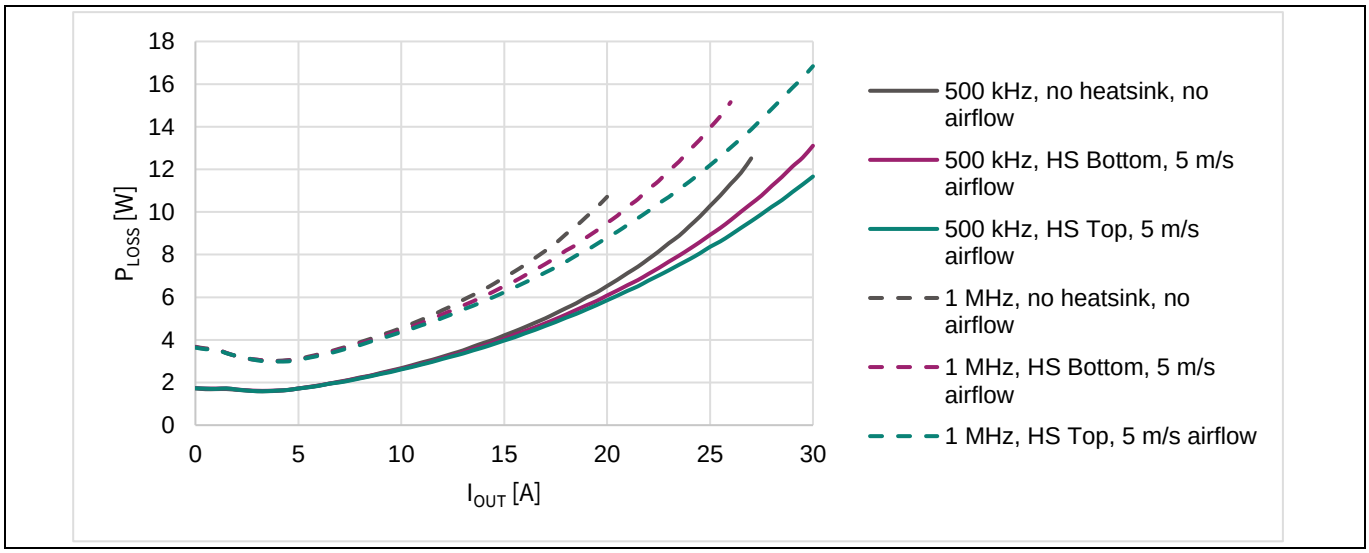


Figure 23 Example power loss results with TDK ERU 10 µH inductor

There is no data for some conditions at higher currents because the devices have reached a temperature of 120°C. This is only due to the selected cooling condition, which does not represent any specific application, and can always be improved with a different heatsink and/or airflow.

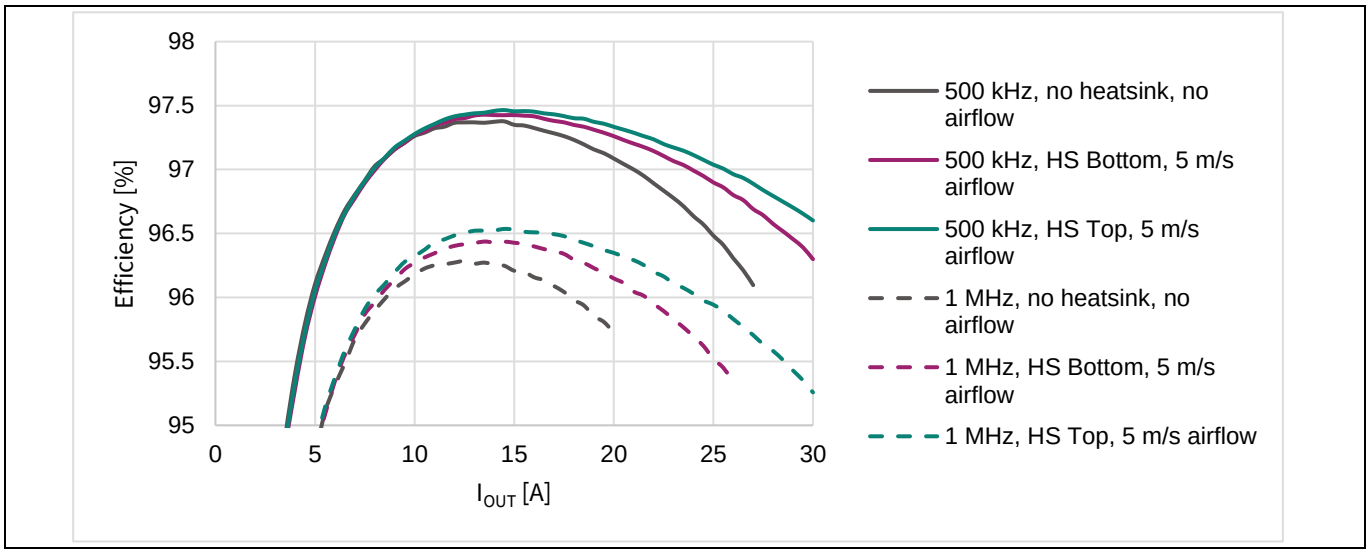


Figure 24 Example efficiency results with Vishay IHLP7575-JZ 3.3 µH inductor

The difference between the results for the two inductors is that the 3.3 µH inductor increases the overall losses due to the higher ripple current and corresponding core loss, which is a common compromise when using a physically smaller inductor such as this one.

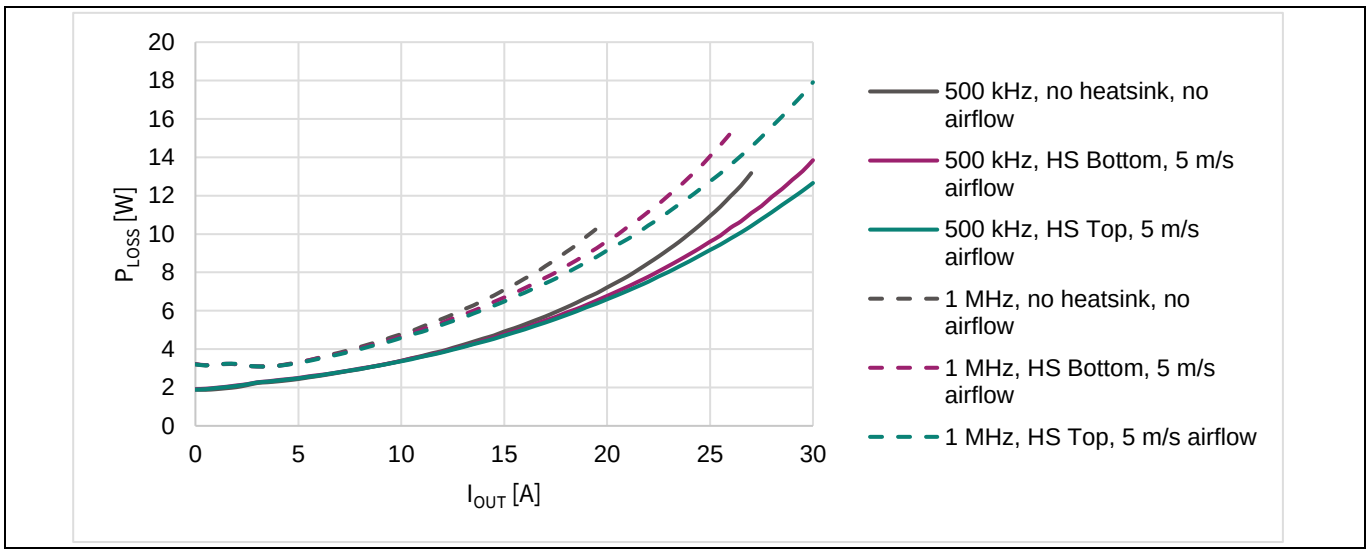


Figure 25 Example power loss results with Vishay IHLP7575-JZ 3.3 µH inductor

5.2 Example buck-mode waveforms

The board was set up to be used in buck-mode as described in Section 2.1. Waveforms at all points are shown in Figure 26 and Figure 27 for the turn-off of the high-side device. The results for turn-on of the high-side device are shown in Figure 28 and Figure 29. Operating conditions of the board in buck mode are 48 V input voltage, 12 V output voltage, 20 A output current, a 3.3µH power inductor, heatsink attached on the bottom side of the board, and an airflow of 5 m/s.

For the turn-off gate voltages shown in Figure 26, the V_{GS} LS waveforms are nearly identical at both measurement points. At 52 ns, there is a small (-1 V) negative gate voltage spike on the low-side switch, caused by the Miller effect when the high-side switch turning off causes a dv/dt in the low-side drain. It is also visible

that the high side gate voltage V_{GS} HS is approximately 4.7 V during on state, which is slightly below the supplied 5 V due to bootstrapping. Nevertheless, this voltage level is still sufficiently high to operate the high side switch in a safe manner. Next to the gate voltages, the three V_{DS} LS measurements overlap and show the same result in Figure 27.

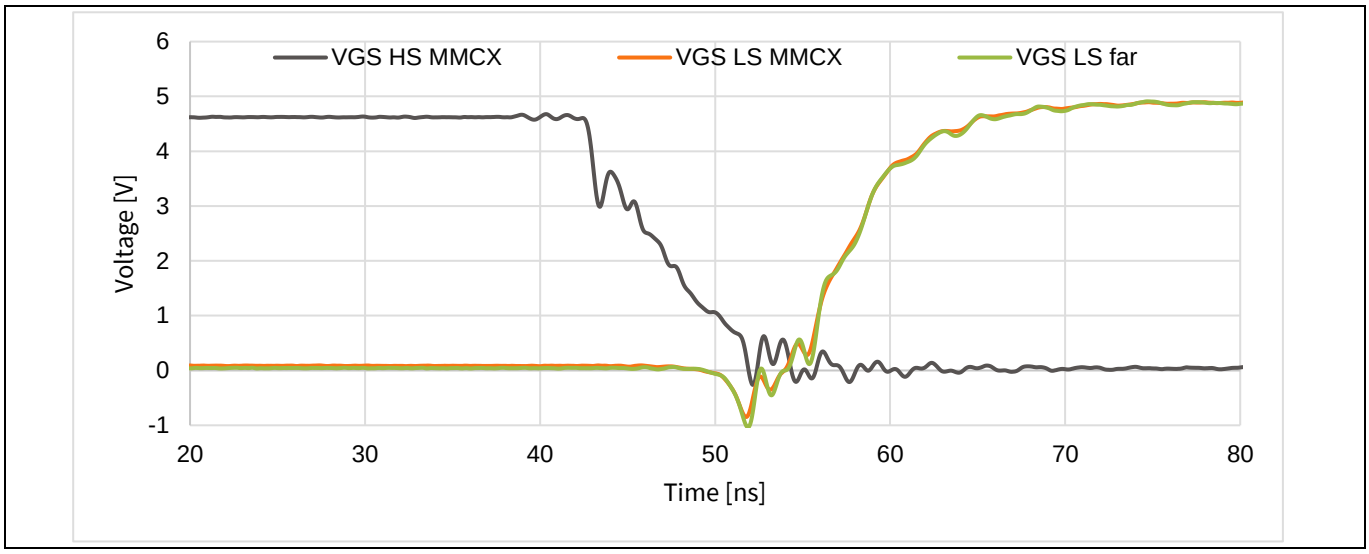


Figure 26 Buck mode example waveforms - gate voltages during high-side turn-off transition

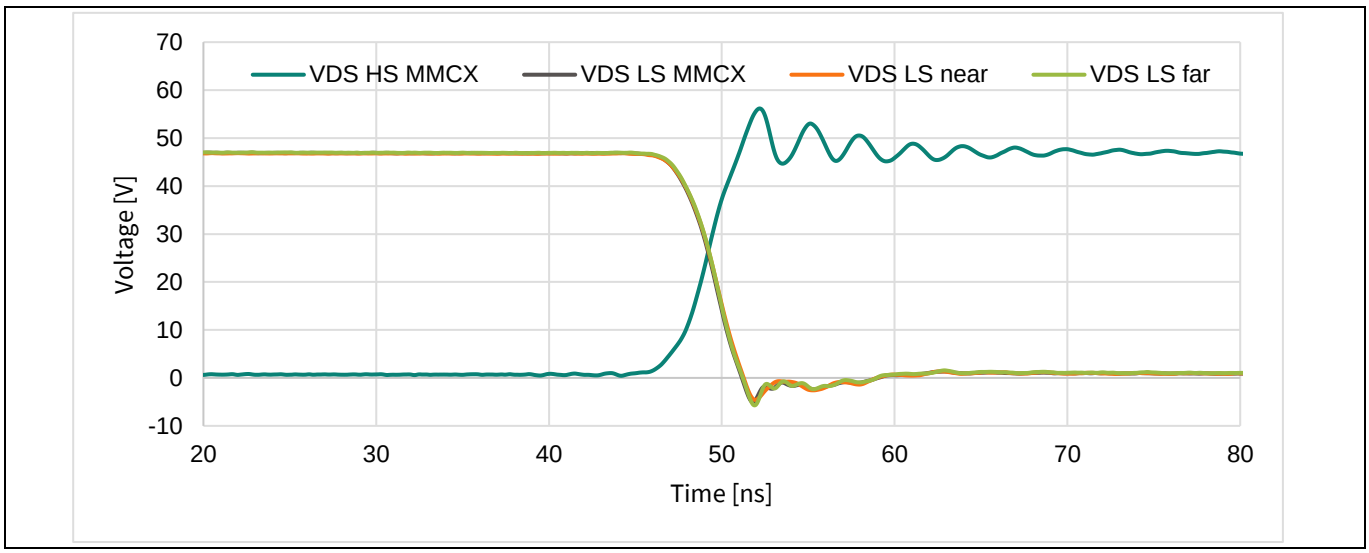


Figure 27 Buck-mode example waveforms - drain voltages during high-side turn-off transition

In Figure 28, the gate voltages for the low side device are again very similar. The "V_{GS} HS MMCX" turn-on waveform shows a high oscillation at the high-side gate where the gate voltage also drops to 2 V. Because there is no visible turn-off at this point in the rising edge of V_{DS} LS, this dip in V_{GS} HS is likely caused by the small resistance and/or inductance between the package and die of the CoolGaN™ power transistor, and it may be exaggerated by the response of the differential probe.

For the turn-on event of the high side device, the overshoot of V_{DS} LS is usually of most interest. This waveform is shown in Figure 29, measured at all three possible points on the board. All three results match in terms of switching speed and ringing frequency. Only the amplitude of the overshoot is slightly different by a maximum of 3 V in this measurement, as in most other operating conditions.

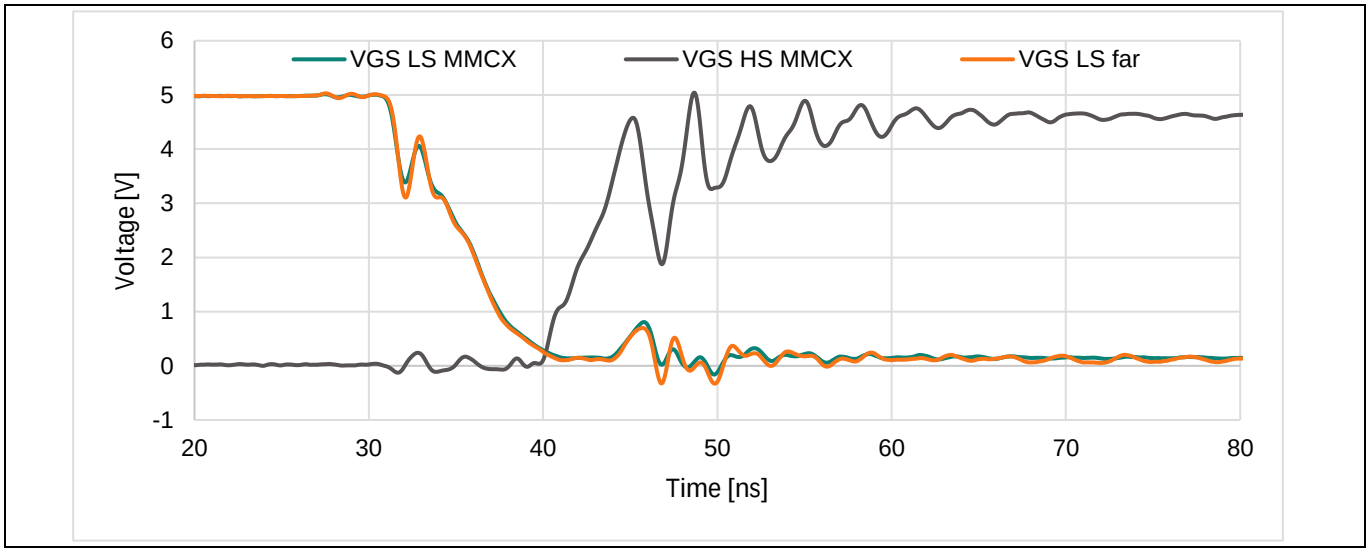


Figure 28 Buck-mode example waveforms - turn on gate voltages

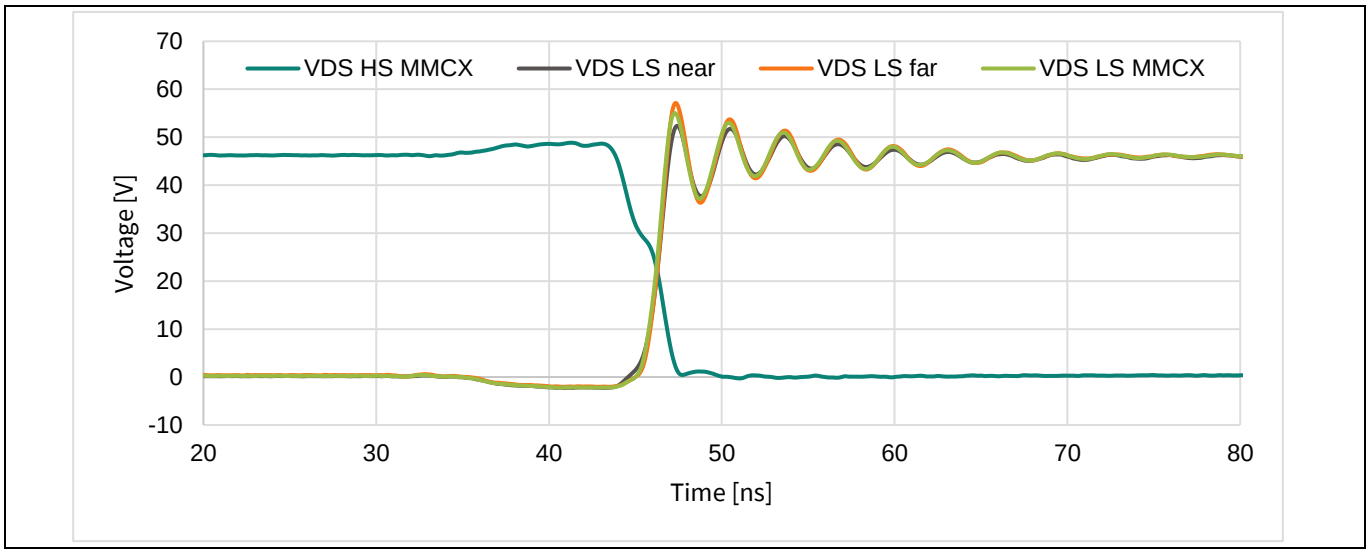


Figure 29 Buck-mode example waveforms - turn on drain voltages

5.3 Example boost-mode waveforms

In boost mode, the same waveforms are captured as in the previous section. The board is connected to the power supply and load as described in Section 2.2. It is operated with 12 V input voltage, 48 V output voltage, 20 A input current, a 3.3 µH power inductor, heatsink attached on the bottom side of the board, and an airflow of 5 m/s. For the turn-off event of the low side device, the gate and drain voltage waveforms are shown in Figure 30 and Figure 31. For the time when the low side device is turning on, the gate and drain waveforms are shown in Figure 32 and Figure 33.

As previously shown for the buck mode, the waveforms for V_{GS} LS and V_{DS} LS are nearly identical at all available measurement locations, and only a slight difference in the amplitude of the overshoot voltage of V_{DS} LS is visible between probing locations. For this reason, it is appropriate to choose whichever measurement point is most convenient for the test bench used.

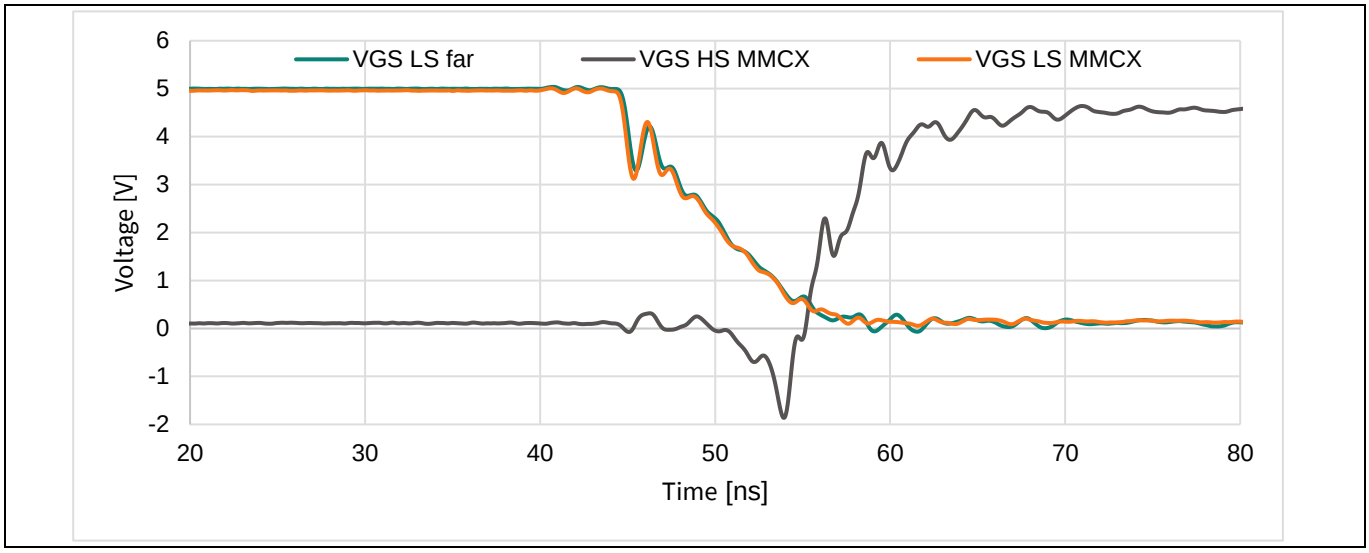


Figure 30 Boost-mode example waveforms - turn off gate voltages

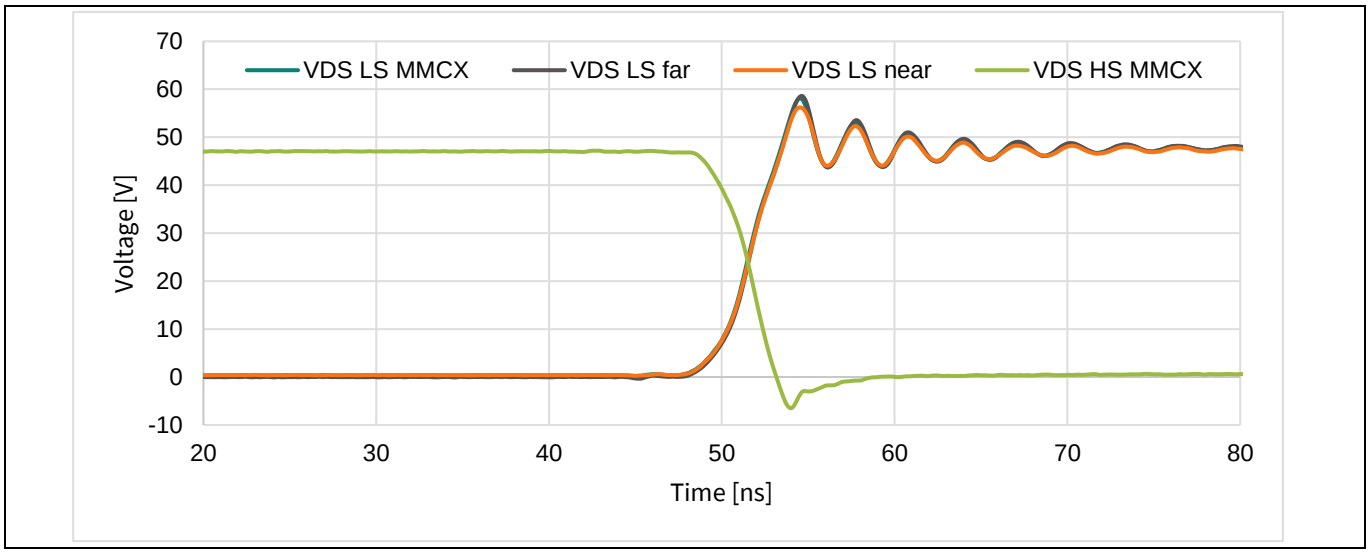


Figure 31 Boost-mode example waveforms – turn-off drain voltages

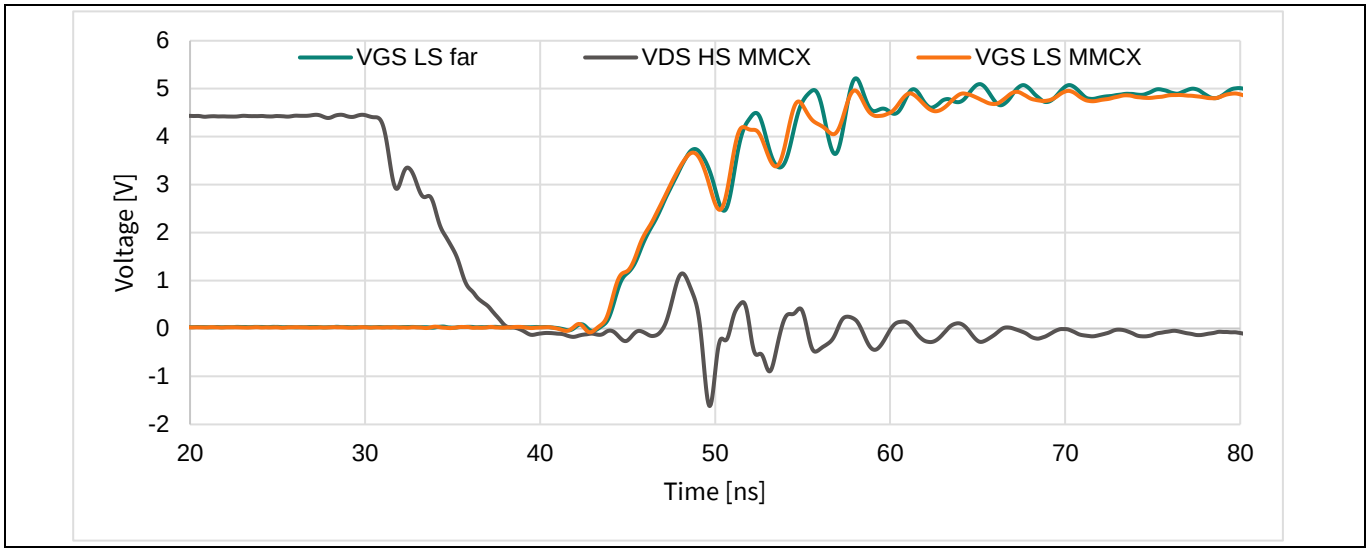


Figure 32 Boost-mode example waveforms - turn on gate voltages

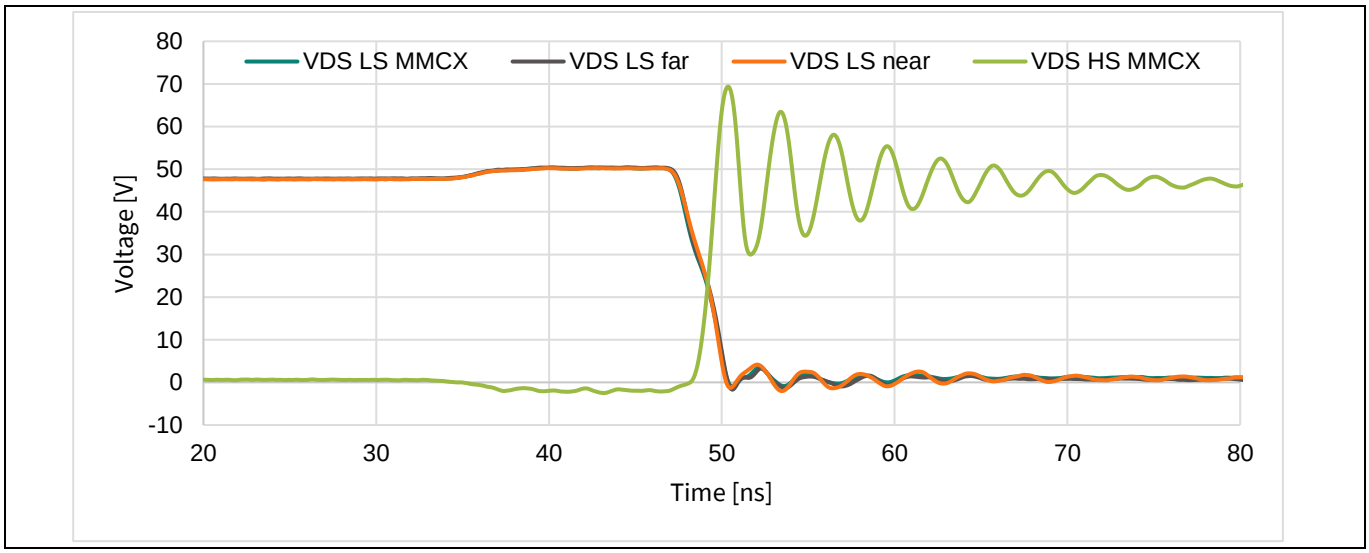


Figure 33 Boost-mode example waveforms - turn on drain voltages

5.4 Example results for different gate driver variants

As described in Section 1.1, the EiceDRIVER™ 1EDN71x6U family includes four variants with different peak gate current driving strengths. To demonstrate the difference between each variant, the board was tested with each variant at the same conditions for comparison: buck mode with 48 V input voltage, 12 V output voltage, 500 kHz switching frequency, a 3.3 µH inductor, heatsink attached on the bottom side of the board, and an airflow of 5 m/s.

Since mostly the low side drain voltage overshoot is affected by the different driving strength, only these waveforms are shown in Figure 34. As expected, the stronger the driver, the higher the overshoot of the drain voltage. Comparing the weakest driver 1EDN7146U to the 1EDN7136U (default for this board), the increase of switching speed is significant. When comparing the 1EDN7136U to the next stronger variants 1EDN7126U and 1EDN7116U, the difference in switching speed is still visible and the peak overshoot voltage also increases due to the higher dV/dt.

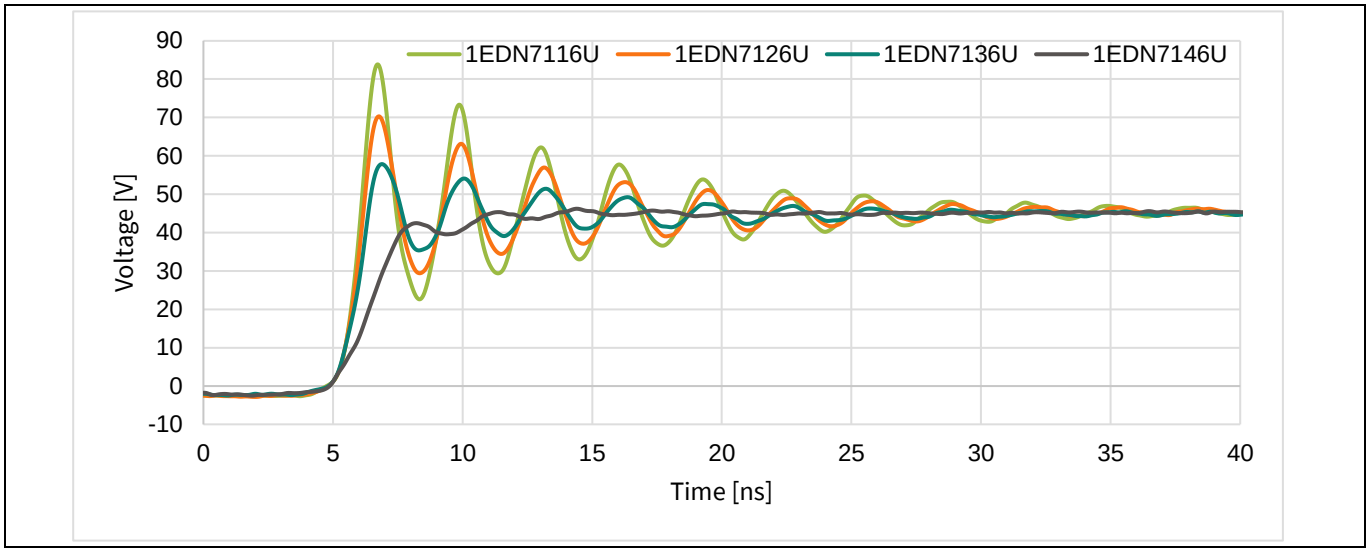


Figure 34 Buck-mode example V_{DS} LS waveform at 20 A I_{OUT} for all four gate driver variants

When looking at efficiency and power loss results in Figure 35 and Figure 36, the increase of overall efficiency with a stronger driver is shown. Nevertheless, the results show that there is no significant benefit in terms of losses and efficiency between 1EDN7116U and 1EDN7126U in this example. The weakest driver 1EDN7146U achieves a much lower efficiency because of higher switching losses. However, there may be applications requiring this slower switching transition to reduce overshoots and meet EMI/EMC requirements.

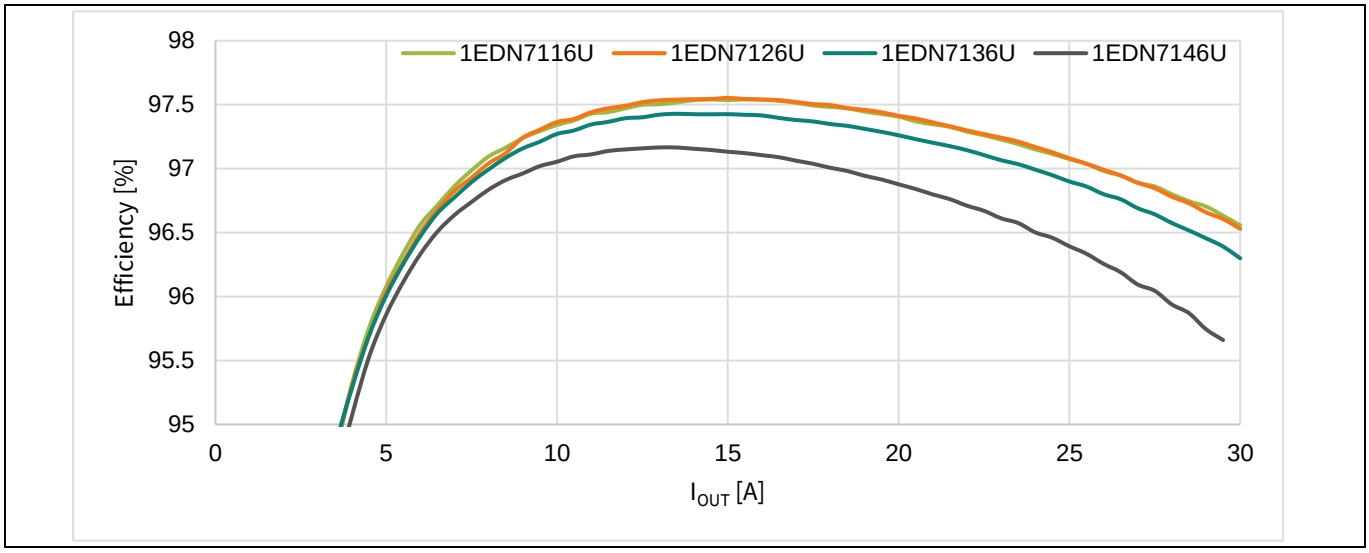


Figure 35 Buck-mode example efficiency results for all four gate driver variants

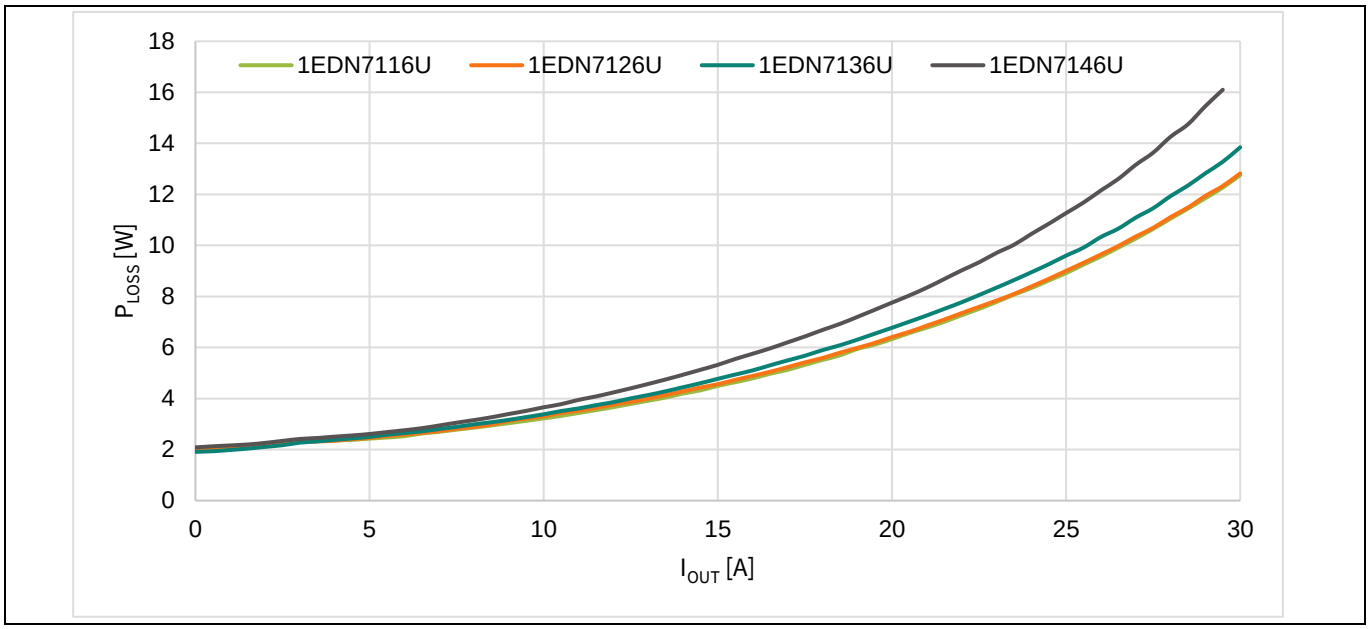


Figure 36 Buck-mode example power loss results for all four gate driver variants

5.5 Thermal images

To show the influence of different cooling to the temperature of the board, it is operated at 48 V input voltage, 12 V output voltage, 500 kHz switching frequency, 20 A output current, with a 3.3 µH inductor. The results for the heatsink attached on the bottom-side of the PCB are shown in Figure 36. For all three cooling conditions, which are the same as given in Section 5.1 for the example efficiency results.

At the given load condition, the influence of the different cooling is clearly visible. Without a heatsink and airflow, the high-side switch reaches a maximum temperature of about 90°C and the low-side switch reaches 81°C in steady state.

Applying the heatsink to the bottom side of the board with an airflow of 5 m/s, the devices stay cooler at a maximum temperature of 67°C for the high-side switch and 55°C for the low-side switch.

The best results can be achieved when the heatsink is attached to the top side of the switches, because the IGC033S10S1 is a dual-side cooled package. It is not possible to capture the surface temperature for each switch in a thermal image with the heatsink attached on top, but the maximum temperature across the whole board is 45°C in this case.

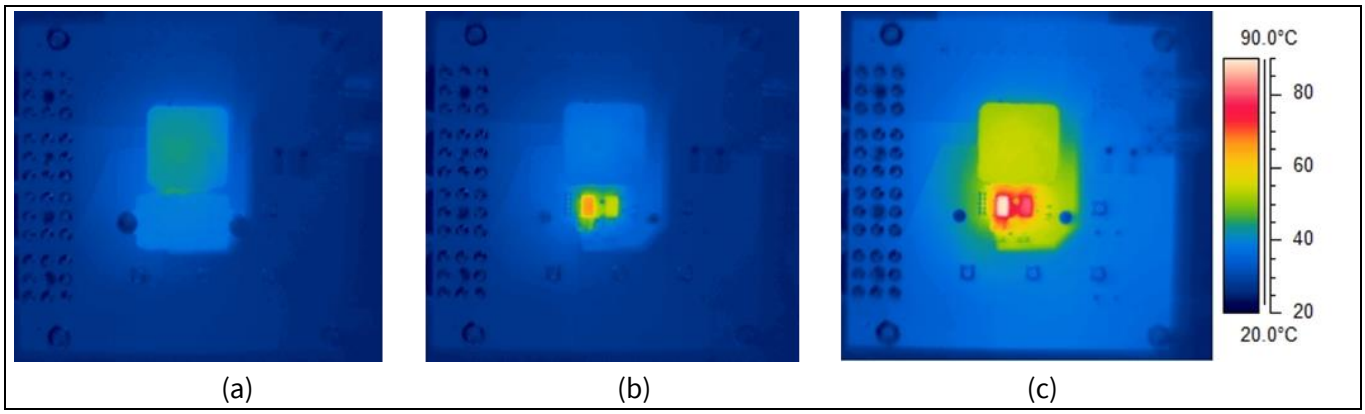


Figure 37 (a) Thermal imaging results for the board operated with heatsink on top and 5 m/s airflow, (b) with heatsink on bottom and 5 m/s airflow (c) and without heatsink and airflow

6 Board documentation

6.1 Schematic

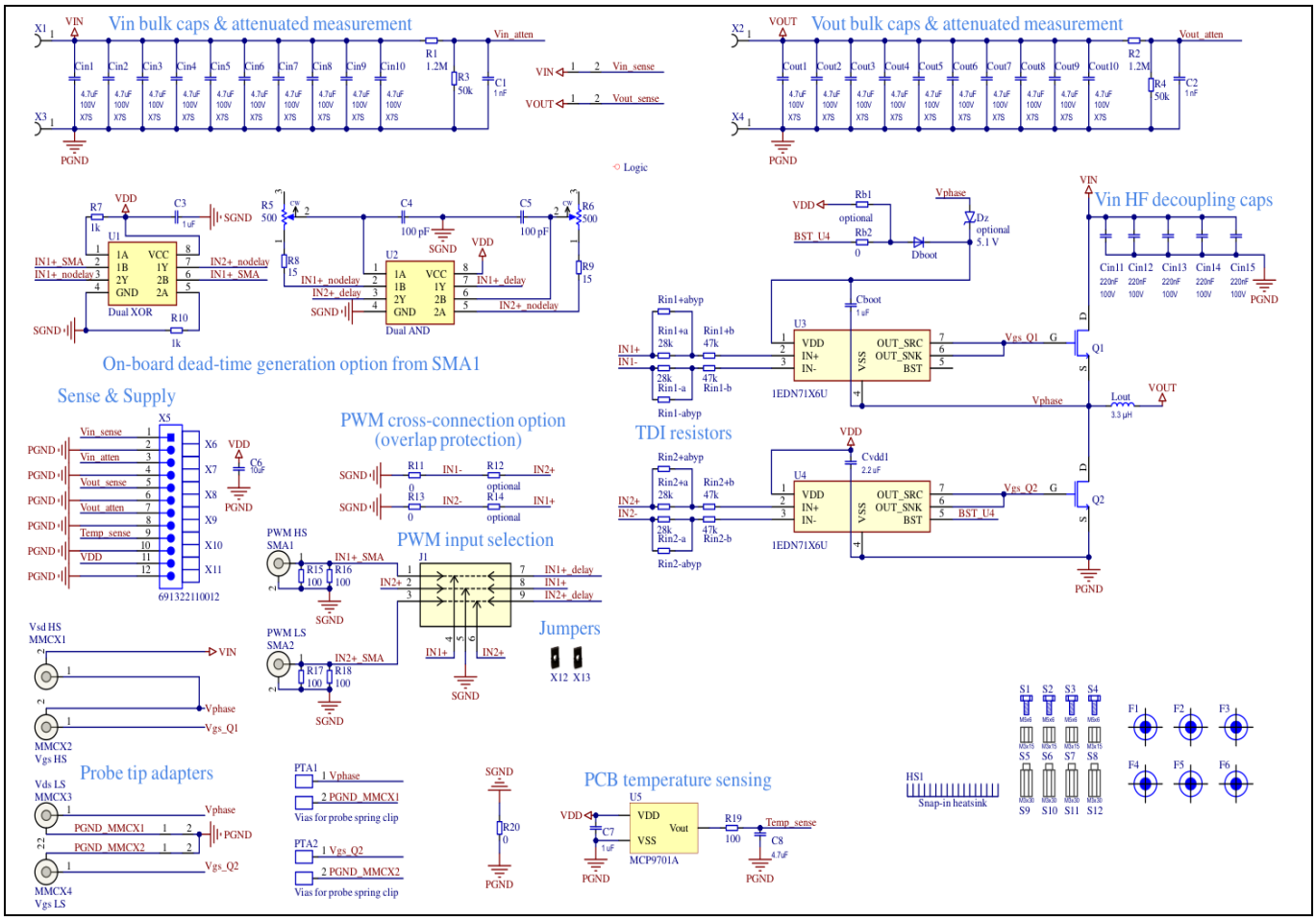


Figure 38 EVAL_7136U_100V_GaNc schematic

6.2 Layout

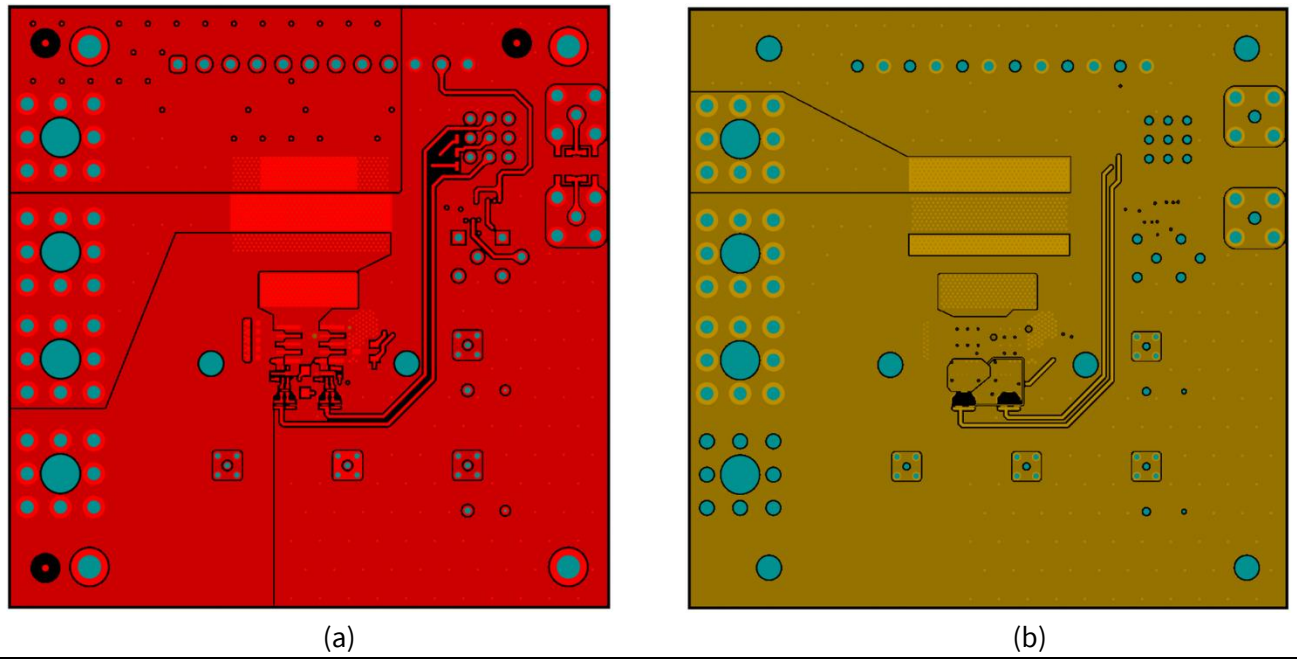


Figure 39 (a) PCB layout top-layer and (b) mid-layer 1

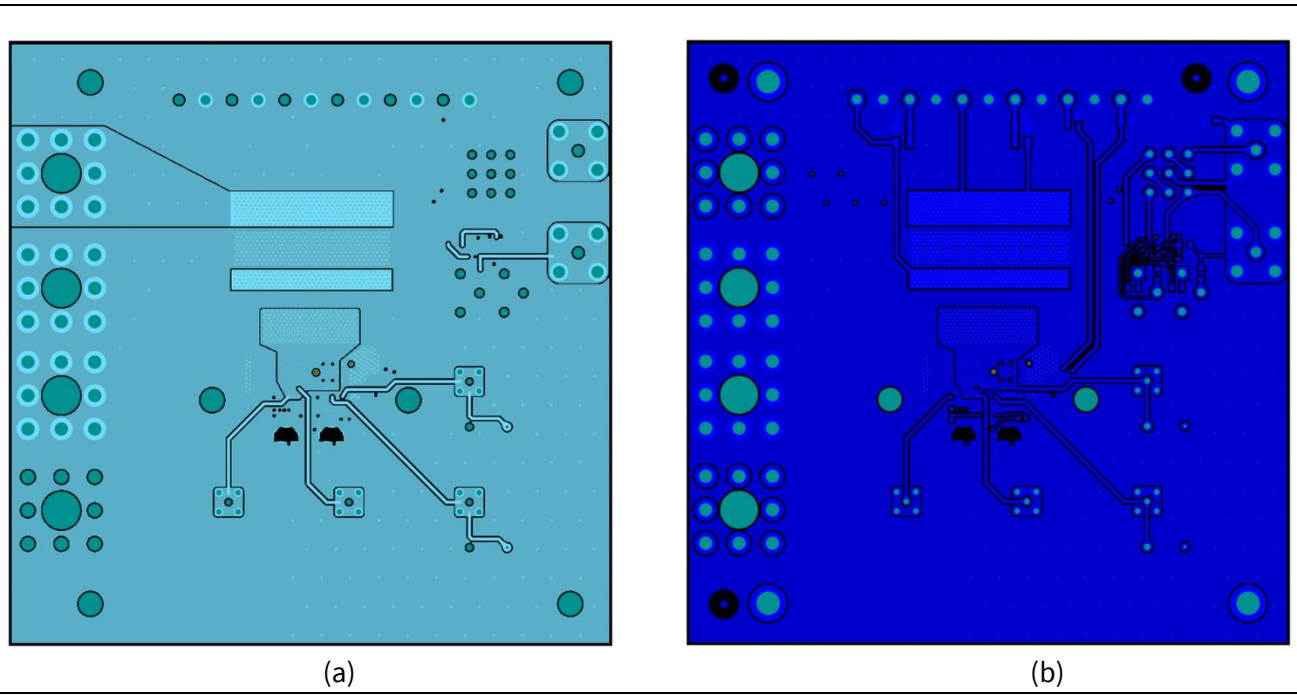


Figure 40 (a) PCB layout mid-layer 2 and (b) bottom layer

6.3 Bill of materials

Table 4 Bill of materials

#	Designator	Value	Manufacturer	Manufacturer part number
1	C1, C2	1 nF	Kemet	C0603C102K3GACTU
2	C3	1 µF	Murata	GCM188R71E105KA64D
3	C4, C5	100 pF	Würth Elektronik	885012006023
4	C6	10 µF	Murata	GRM21BC71E106ME11L
5	C7, Cboot	1 µF	Murata	GRT155C81E105KE13D
6	C8	4.7 µF	Murata	GRM188C81E475KE11D
7	Cin1 ~ Cin10, Cout1 ~ Cout10	4.7 µF	Murata	GRM31CC72A475ME11L
8	Cin11, Cin12, Cin13, Cin14, Cin15	220 nF	Taiyo Yuden	HMK107C7224KAHTE
9	Cvdd1	2.2 µF	Murata	GRM155C81E225ME11D
10	Dboot	Schottky diode	ON semi	MBR2H200SFT1G
11	Dz	optional	Diodes Inc	BZT585B5V6T-7
12	HS1	Heatsink	–	–
13	J1	Header	Samtec	TSW-103-07-G-T
14	Lout	3.3 µH	Vishay	IHLP7575JZERER3R3M5A
15	MMCX1 ~ MMCX4	MMCX vertical jack	Würth Elektronik	66012002111503
16	Q1, Q2	CoolGaN™ power transistor	Infineon	IGC033S10S1
17	R1, R2	1.2 MΩ	Susumu	RG2012P-125-B-T5
18	R3, R4	50 kΩ	Vishay	PTN0805E5002BST1
19	R5, R6	500 Ω	Vishay	T63YB501KT20
20	R7, R10	1 kΩ	Stackpole	RMCF0402FT1K00
21	R8, R9	0 Ω	Yageo	RC0603JR-070RL
22	R11, R13, Rb2	0 Ω	Stackpole	RMCF0402ZT0R00
23	R12, R14, Rb1	Optional	–	–
24	R15, R16, R17, R18, R19	100 Ω	Stackpole	RMCF0603FG100R
25	R20	0 Ω	Yageo	AC0603FR-070RL
26	Rin1+a, Rin1-a, Rin2+a, Rin2-a	28 kΩ	Panasonic	ERA-2APB2802X
27	Rin1+abyp, Rin1-abyp, Rin2+abyp, Rin2-abyp	Optional	–	–
28	Rin1+b, Rin1-b, Rin2+b, Rin2-b	47 kΩ	Panasonic	ERA-2APB473X
29	S1, S2, S3, S4	M5x6 mm	B&F	MPMS 005 0006 PH

#	Designator	Value	Manufacturer	Manufacturer part number
30	S5, S6, S7, S8	Spacer 15 mm fem. M3	Würth Elektronik	970150321
31	S9, S10, S11, S12	Spacer 30 mm male M3	Würth Elektronik	970300321
32	SMA1, SMA2	SMA jack	Würth Elektronik	60311002111526
33	U1	Dual XOR	Diodes Inc	74LVC2G86HK3-7
34	U2	Dual AND	Nexperia	74LVC2G08GS-Q100X
35	U3, U4	TDI EiceDriver™ for GaN	Infineon	1EDN7136U
36	U5	MCP9701AT-E/TT	Microchip Technology	MCP9701AT-E/TT
37	X1, X2, X3, X4	Redcube connector	Würth Elektronik	74655095R
38	X5	Screw terminal header	Würth Elektronik	691322110012
39	X6, X7, X8, X9, X10, X11	Screw terminal plugs	Würth Elektronik	691363110002
40	X12, X13	Jumpers	Würth Elektronik	609002115121

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Others

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Document revision	Date	Description of changes
V 1.0	2024-07-17	Initial release

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