# 65 W high power density quick-charger demo board using XDP™ digital power XDPS2201 and EZ-PD™ CCG3PA

**DEMO_XDPS2201_65W1**

## About this document

### Scope and purpose

Design information and measurement results of the 65 W high power density USB-PD demo board using XDP™ digital power XDPS2201 and EZ-PD™ CCG3PA.

### Intended audience

This document intended for users who wish to use the DEMO_XDPS2201_65W1 board.

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# 1 Introduction

As the mobile electronic devices, such as note book computer and smart phone, are getting increasingly popular, the market for the high power density quick-charger with USB power delivery (PD) capability is getting more and more attractive. Such an adapter operates with a wide input voltage range, typically from 90 V to 264 V, and a wide output range, from 5 V or even 3.3 V to 20 V. Besides light weight and small dimension, high system efficiency and low standby power are the key requirements for this application.

For a switching mode power supply below 75 W, where a power factor correction (PFC) is not required, the flyback topology is the most cost-effective solution. For this topology, many control methods are available with good performance, such as the quasi-resonant control and the active clamped control. With the quasi-resonant control method, the power MOSFET is turned on at the valley of the voltage across the MOSFET drain-source. In addition, it is hard to achieve the zero-voltage switching (ZVS) over the whole input and output voltage and current range. In addition, high voltage spike at the turn-off of the main switch causes high voltage stress for that switch. With additional components, the voltage stress of the main switch is reduced in the active clamped flyback converter. However, higher voltage stress than the bulk capacitor voltage still exists for the main switch. Besides this, more losses in the primary winding during the energy transferring and difficulty to achieve full ZVS over the whole load range impair the application by this control method.

In the hybrid-flyback (HFB) topology, the main switches automatically have a voltage clamping to the bulk capacitor voltage and, therefore, there is no stress of voltage spike as mentioned in the other two topologies. The low-side switch automatically has the ZVS turn-on, while a controlled negative current ensures ZVS turn-on for the high-side switch. The snubber circuit, as in the quasi-resonant converter and the active clamped flyback converter, is not required. In addition, both the transformer and the resonant capacitor of the HFB converter contribute to the intermediate energy storage and transferring, which enables a very compact design. All these features make HFB the most promising topology for high power density designs.

A 65 W demo board for USB-PD application, based on the HFB controller XDPS2201 [1] and the USB-PD controller CYPD3174-24LQXQ [2], is introduced in this document. This board is designed for a wide input application and provides PD output voltage profile of 5 V, 9 V, 12 V, 15 V and 20 V. In addition, the demo board supports PPS output from 5 V to 20 V with the voltage step defined by the PD device. The nominal continuous output current is 3.25 A.

While the design of the HFB converter with XDPS2201 is illustrated in the design guide [3] and the design excel sheet [4], this document focuses on the following topics:

- Board description (***Chapter 2***)
- Measurement result (***Chapter 3***)
- Summary (***Chapter 4***)
- Change history (***Chapter 6***)
- References (***Chapter 5***)

# 2 Board description

This chapter covers the following topics:

- Input and output specifications (***Chapter 2.1***)
- Board circuit, PCB and key components (***Chapter 2.2***)

## 2.1 Input and output specifications

For this demo board, the following specifications apply:

**Table 1 Specifications of the 65 W demo board for USB-PD/PPS application**

| Parameter | Symbol | Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | Minimum | Typical | Maximum | |
| Input RMS voltage | $V_{AC}$ | Maximum range | 90 | | 264 | V |
| Mains frequency | $f_{AC}$ | | 47 | | 63 | Hz |
| No load power consumption | $P_{stby}$ | 115 V/230 V input and 5 V output | | | 75 | mW |
| Continuous output current | $I_{outnom}$ | 20 V output | | 3.25 | | A |
| Output voltage [1)] | $V_{OUT}$ | | 5 | | 20 | V |
| Nominal output power | $P_{outnom}$ | | | 65 | | W |
| Peak power | $P_{out\_peak}$ | 95 W for 5 ms at 1 Hz, output voltage should be higher than 17 V for AC in range 100 V to 265 V and higher than 15 V for AC input at 90 V | | 95 | | W |
| System start-up time | $t_{startup}$ | From AC on to output voltage reaching 90% nominal value | | | 2.5 | s |
| Efficiency at nominal power | | At 115 V and 230 $V_{AC}$, 20 V output and 65 W output power | 93.5 | | | % |

The key components and dimension of the demo board are listed in the following table.

**Table 2 Key components, board dimension and power density**

| Item | Specification |
|---|---|
| HFB controller IC | XDPS2201 |
| PD controller | CYPD3174-24QXQ |
| MOSFETs | IPD60R180C7, IPP60R180C7, BSC093N15NS5, BSZ086P03NS3 |
| Dimension (L x W x H) uncased | 46 mm x 37 mm x 20.2 mm |
| Power density (uncased) | 31 W/inch$^3$, 1.9 W/cm$^3$ |

1 The USB port controller is programmed for the output voltages of 5 V, 9 V, 12 V, 15 V and 20 V, and PPS from 5 V to 20 V.

## 2.2 Board circuit, PCB and key components

This chapter provides the following information:

- Schematic (***Chapter 2.2.1***)
- PCB design (***Chapter 2.2.2***)
- Component list (***Chapter 2.2.3***)
- Magnetic components (***Chapter 2.2.4***)
- Board view (***Chapter 2.2.5***)

### 2.2.1 Schematic

The circuit consists of the following three main portions:

- Input stage
- Main stage
- PD control circuit

The schematic of the demo board is shown in ***Figure 1***.

#### 2.2.1.1 Input stage

The input stage includes a common mode EMI filter, a bridge rectifier, a differential mode filter and a main energy storage capacitor. In this stage, the common mode choke (CMC) (***Figure 20***) is made out of bifilar wires for a low leakage inductance that helps for the better common mode noise attenuation.

#### 2.2.1.2 Main stage

Two power switches Q1 and Q2 build up a half-bridge. One terminal of the transformer primary winding is connected to the switching node of the half-bridge, while the other one is connected to the resonant capacitor, which is out of the six pieces of SMD ceramic capacitors C11 to C16. These SMD capacitors enable a compact design. The secondary side power circuitry is the same as in a conventional flyback converter. Synchronous rectifier (SR) is employed for a high power conversion efficiency. The PD controller U4 CYPD3174 senses the output voltage and generates a control signal. This control signal is transferred via the opto-coupler to the primary side controller U1 XDPS2201 for the output voltage regulation.

There are three sources to supply the controller IC U1: the start-up cell inside the controller XDPS2201, the rectified voltage from the auxiliary winding, and the voltage Vcr from the resonant capacitors (Cr). For the third source, a linear regulator consisting of the depletion N-channel MOSFET Q4, the zener diode ZD1 and the resistor R19 is required. While the first one is utilized to power-up the IC at AC turn-on, either one of the latter two supplies the IC XDPS2201 during its operation. At any time, only one channel delivers power to the IC depending on the output voltage level. In case the output voltage is high enough and, therefore, the rectified voltage from the auxiliary winding is higher than the zener diode breakthrough voltage, the linear regulator transistor Q4 is blocked since its gate-source voltage is negative. Otherwise, the linear regulator is active and supplies the control IC with power. The capacitor C18 is an intermediate energy storage device. Its voltage has the peak value of the voltage across the resonant capacitors via the components D3 and R18. Considering the power losses and thermal design for the MOSFET Q4, the level of the output voltage where the linear regulator begins to be active must be as low as possible. Due to the small package of the transistor Q4 and its high thermal resistance, the thermal pad is required for the transistor Q4. In addition, the zener diode breakthrough voltage must be higher than the depletion cell turn-on threshold $V_{VCCslpHVon}$, to avoid activation of the start-up cell during burst mode operation which leads to high standby power.

#### 2.2.1.3 PD control circuit

On this demo board, the 24-pin device CYPD3174-24LQXQ is used. This PD controller gives feedback signal to the HFB controller via the opto-coupler U3 based on the sensed output voltage of the HFB converter. The current flowing through the CATH path, which is the current through the opto-coupler diode, is proportional to the potential difference between the sensed converter output voltage (FB pin of this device) and the internal

bandgap reference voltage for 5 V output or the internal IDACs and error amplifier for other voltage levels. In this way, the output voltage is regulated to the set target voltage level.

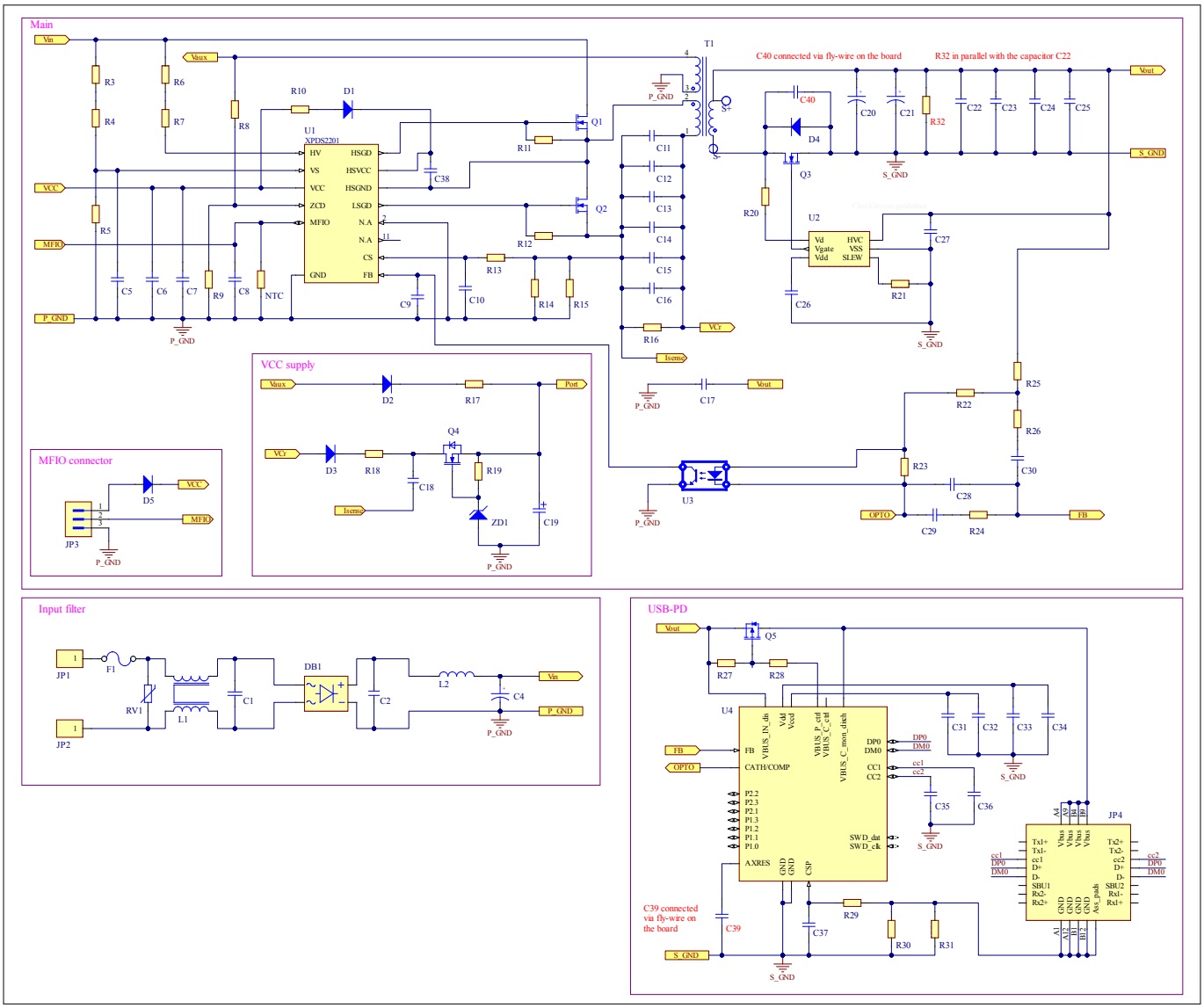


**Figure 1 Schematic of the board**

*Note: The capacitors C39 and C40, and the resistor R32 are connected via fly-wire on this board.*

On this demo board, the output voltage is set to 5 V, 9 V, 12 V, 15 V with a continuous output current of 3 A and 20 V with a continuous current of 3.25 A. In addition, PPS from 5 V to 20 V with a continuous current of 3 A is supported, as well.

*Note: This demo board can deliver a continuous load current of 3.25 A at the type-C connector, but does not support the current negotiation per e-marking cable for an output current higher than 3 A.*

## 2.2.2 PCB design

The PCB of the demo board consists of the following four layers.

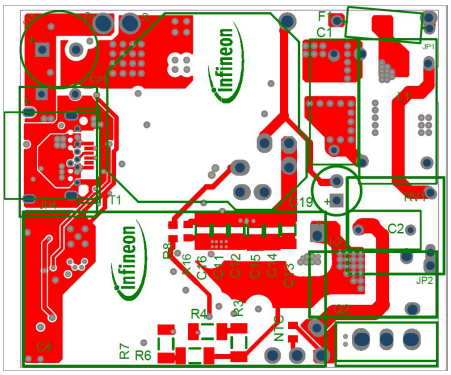

**Figure 2 Top layer**

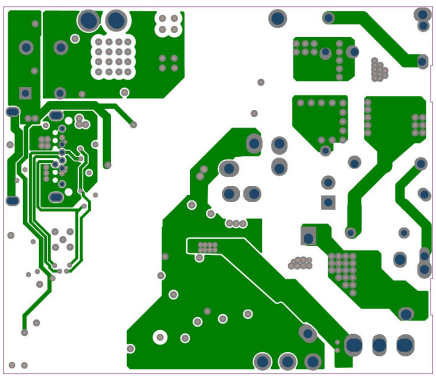

**Figure 3 Top inner layer**

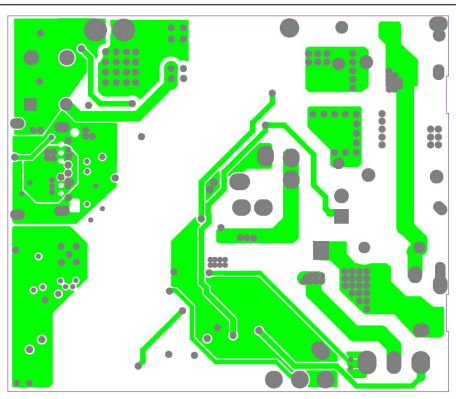

**Figure 4 Bottom inner layer**

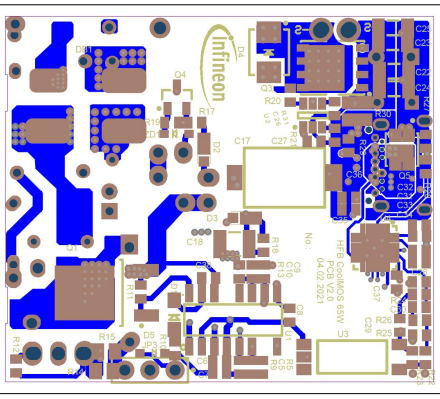

**Figure 5 Bottom layer**

The PCB layer stack, which results in a total PCB thickness of around 0.97 mm, is as follows:

| # | Name | Material | Type | Weight | Thickness | DK |
|---|---|---|---|---|---|---|
| | Top overlay | | Overlay | | | |
| | Top solder | Solder resist | Solder mask | | 0.01016 mm | 3.5 |
| 1 | Top layer | | Signal | 2 oz | 0.07 mm | |
| | Dielectric 2 | PP-006 | Prepreg | | 0.07112 mm | 4.1 |
| 2 | Inner layer top | | Signal | 1 oz | 0.035 mm | |
| | Dielectric 1 | RF-4 | Dielectric | | 0.6 mm | 4.8 |
| 3 | Inner layer bottom | | Signal | 1 oz | 0.035 mm | |
| | Dielectric 3 | PP-006 | Prepreg | | 0.07112 mm | 4.1 |
| 4 | Bottom layer | | Signal | 2 oz | 0.07 mm | |
| | Bottom solder | Solder resist | Solder mask | | 0.01016 mm | 3.5 |
| | Bottom overlay | | Overlay | | | |

**Figure 6 PCB layer stack**

### 2.2.3 Component list

The following table lists the bill of material (BOM) of the board.

**Table 3 System BOM**

| # | Designator | Description | Quantity | Manufacturer | Manufacturer part number |
|---|---|---|---|---|---|
| 1 | C1 | 100 nF, 310 $V_{AC}$, Box_5x13, 20% | 1 | KEMET | R463F310050M1M |
| 2 | C2 | 1.2 uF, 450 V, Box_4x7.5, 20% | 1 | muRata | RDED72W125MUB1H03B |
| 3 | C4 | 100 uF, 400 V, cyl_16_30_5_hor, 20% | 1 | Rubycon | 400BXW100MEFR16X30 |
| 4 | C5 | 330 pF, 50 V, 0603, X7R, 10% | 1 | muRata | GRM188R71H331JA01 |
| 5 | C6 | 100 nF, 50 V, 0603, X7R, 10% | 1 | TAIYO YUDEN | UMK107B7104KAHT |
| 6 | C7 | 1 uF, 50 V, 0603, X7R, 10% | 1 | muRata | GRM188R71E105KA12 |
| 7 | C8, C28 | 100 pF, 50 V, 0603, C0G, 5% | 2 | AVX | 06035A101JAT2A |
| 8 | C9 | 150 pF, 50 V, 0603, C0G, 5% | 1 | muRata | GCM1885C1H151JA16 |
| 9 | C10 | 22 pF, 50 V, 0603, C0G, 5% | 1 | muRata | GRM1885C1H220JA01 |
| 10 | C11, C12, C13, C14, C15, C16 | 0.15 uF, 200 V, 1206, 10% | 6 | KEMET | C1206C154K2RACTU |
| 11 | C17 | 1.5 nF, 250 $V_{AC}$, Y_cap_SMD, 5% | 1 | muRata | DK1E3EA152M86RAH01 |
| 12 | C18 | 4.7 uF, 100 V, 1210m_C, 20% | 1 | TDK | C3225X7S2A475M200AB |
| 13 | C19 | 47 uF, 35 V, Rad 5x11, 20% | 1 | Rubycon | 35PX47MEFC5X11 |
| 14 | C20, C21 | 470 uF, 25 V, CAPPRD350W60D800H1300B, 20% | 2 | ILLINOIS CAPACITOR | 477AVG025MFBJ |
| 15 | C22, C23, C24, C25 | 22 uF, 25 V, 1206m_C, 10% | 4 | AVX | 12063D226KAT2A |
| 16 | C26 | 1 uF, 25 V, 0603, C0G, 5% | 1 | AVX | 06033D105KAT2A |
| 17 | C27, C31, C33, C38, C39 | 100 nF, 50 V, 0603, X7R, 10% | 5 | muRata | GRM188R71H104KA93 |
| 18 | C29 | 47 nF, 50 V, 0603, X7R, 10% | 1 | muRata | GRM188R71H473KA61 |
| 19 | C30 | 4.7 nF, 50 V, 0603, C0G, 5% | 1 | muRata | GRM1885C1H102JA01 |
| 20 | C32, C34 | 1 uF, 25 V, 0603, X7R, 10% | 2 | muRata | GRM188R71E105KA12 |
| 21 | C35, C36 | 390 pF, 50 V, 0603, X7R, 5% | 2 | muRata | GRM188R71H391JA01 |
| 22 | C37 | 0603, X7R, 10% | 0 | muRata | GRM188R71H104KA93 |
| 23 | C40 | 1 nF, 200 V, 0603, X7R, 10% | 1 | KEMET | C0603C102K2RACTU |
| 24 | D1 | ES1GL R3G, 400 V, SUB_SMA | 1 | TAIWAN SEMICONDUCTOR | ES1GL R3G |
| 25 | D2, D3 | RF05VAM2STR, 200 V, MicroSMP | 2 | ROHM | RF05VAM2STR |
| 26 | D4 | STPS3150U, 150 V, SMBflat_diode | 1 | STMicroelectronics | STPS3150U |
| 27 | D5 | NA, 150 V, SOD323_d | 1 | MULTICOMP | 1N4148WS |

**Table 3 System BOM (continued)**

| | | | | | |
|---|---|---|---|---|---|
| 28 | DB1 | Z4DGP406L, CD-DF4xxS_v3 | 1 | Comchip | Z4DGP406L-HF |
| 29 | F1 | Fuss 2 A, 250 V, cyl_13_3.6_hor | 1 | MULTICOMP | MST 2A 250V |
| 30 | JP3 | HTSW-103-07-G-S, CONN3_v2 | 1 | samtec | HTSW-103-07-G-S |
| 31 | JP4 | USB3.1F, SB_C_24_multiComp | 1 | MULTICOMP | MC001002 |
| 32 | L1 | 2 x 5.5 mH | 1 | ItaCoil | TOR178 |
| 33 | L2 | 68 u, L 12X6 | 1 | Würth Electronic | 74447033 |
| 34 | NTC, R9 | 51 K, 75 V, 0603, 1% | 2 | VISHAY | CRCW060351K0FK |
| 35 | Q1 | IPD60R180C7, DPAK (TO-252) | 1 | Infineon | IPD60R180C7 |
| 36 | Q2 | IPP60R180C7, I2PAK (TO-262) | 1 | Infineon | IPP60R180C7 |
| 37 | Q3 | BSC093N15NS5, SuperSO8 | 1 | Infineon | BSC093N15NS5 |
| 38 | Q4 | BSS169, PG-SOT23 | 1 | Infineon | BSS169H6327XTSA1 |
| 39 | Q5 | BSZ086P03NS3, INF-PG- TSDSON-8-FL | 1 | Infineon | BSZ086P03NS3 |
| 40 | R3, R4 | 2.4 MEG, 400 V, 0805, 1% | 2 | VISHAY | CRCW08052M40FK |
| 41 | R5 | 28.7 K, 75 V, 0603, 1% | 1 | VISHAY | MCWR06X2872FTL |
| 42 | R6, R7 | 56 K, 200 V, 1206, 1% | 2 | VISHAY | CRCW120656K0FK |
| 43 | R8 | 560 K, 75 V, 0603, 1% | 1 | VISHAY | CRCW0603470KFK |
| 44 | R10 | 2.7 R, 75 V, 0603, 1% | 1 | VISHAY | CRCW06032R70FK |
| 45 | R11, R12 | 22 K, 75 V, 0603, 1% | 2 | VISHAY | CRCW060322K0FK |
| 46 | R13, R29 | 1 K, 75 V, 0603, 1% | 2 | VISHAY | CRCW06031K00FK |
| 47 | R14 | 200 mR, 150 V, 0805, 1% | 1 | BOURNS | CRL0805-FW-R200ELF |
| 48 | R15 | 180 mR, 150 V, 0805, 1% | 1 | BOURNS | CRL0805-FW-R200ELF |
| 49 | R16 | 1 MEG, 75 V, 0603, 1% | 1 | VISHAY | CRCW06031M00FK |
| 50 | R17, R18 | 0 R, 75 V, 0603, 0R | 2 | VISHAY | CRCW06030000Z0 |
| 51 | R19, R27 | 47 K, 75 V, 0603, 1% | 2 | VISHAY | CRCW060347K0FK |
| 52 | R20, R26 | 1 K, 75 V, 0603, 1% | 2 | VISHAY | CRCW06031K00FK |
| 53 | R21 | 100 K, 75 V, 0603, 1% | 1 | VISHAY | CRCW0603100KFK |
| 54 | R22 | 4.7 K, 75 V, 0603, 1% | 1 | VISHAY | CRCW06034K70FK |
| 55 | R23 | 6.8 K, 75 V, 0603, 1% | 1 | VISHAY | CRCW06036K80FK |
| 56 | R24 | 27 K, 75 V, 0603, 1% | 1 | VISHAY | CRCW060327K0FK |
| 57 | R25 | 47 R, 75 V, 0603, 1% | 1 | VISHAY | CRCW060347R0FK |
| 58 | R28 | 2.7 K, 75 V, 0603, 1% | 1 | VISHAY | CRCW06032K70FK |
| 59 | R30, R31 | 10 mR, 150 V, 0805, 1% | 2 | YAGEO | RL0805FR-7W0R01L |
| 60 | R32 | 9.1 K, 75 V, 0603, 1% | 1 | Panasonic | ERJ-UP3F9101V |
| 61 | RV1 | TVS 275 V, Varistor_10x5mm_lay | 1 | EPCOS | B72207S0271K101 |
| 62 | T1 | Npri:Nsec:Naux=17:6:5, RM8_v2 | 1 | Würth Electronic | 750344351r07 |

**Table 3 System BOM (continued)**

| | | | | | |
|---|---|---|---|---|---|
| 63 | U1 | XPDS2201, SOIC127P600X175-14-66 | 1 | Infineon | XPDS2201 |
| 64 | U2 | MP6908A, SOT23_6 | 1 | MPS | MP6908AGJ-P |
| 65 | U3 | TCLT1103, Opto_TCLT1103 | 1 | VISHAY | TCLT1103 |
| 66 | U4 | CYPD3174-24LQXQ, QFN24 | 1 | Infineon | CYPD3174-24LQXQ |
| 67 | ZD1 | TDZ12J, 12 V, SOD323_d | 1 | Nexperia | TDZ12J,115 |

*Note: Based on the operating voltage range, a 5 V rating is sufficient for the capacitors C5, C6, C7, C8, C10, C28, C29 and C30. Instead, the 50 V type capacitors are assembled on the board due to the lower price.*

### 2.2.4 Magnetic components

In the following sub-chapters, the transformer and CMC are described in detail.

#### 2.2.4.1 Transformer

The transformer T1 has the following specifications [4]:

- Turns ratio Np:Ns:Naux = 17:6:5
- Core material 3C95
- Bobbin RM8
- Main inductance $L_p$ = 53 µH
- Leakage inductance $L_r$ = 1.5 µH
- One inner shielding layer

The construction, wires used and winding arrangement, and bobbin pin assignment are shown in ***Figure 7***.

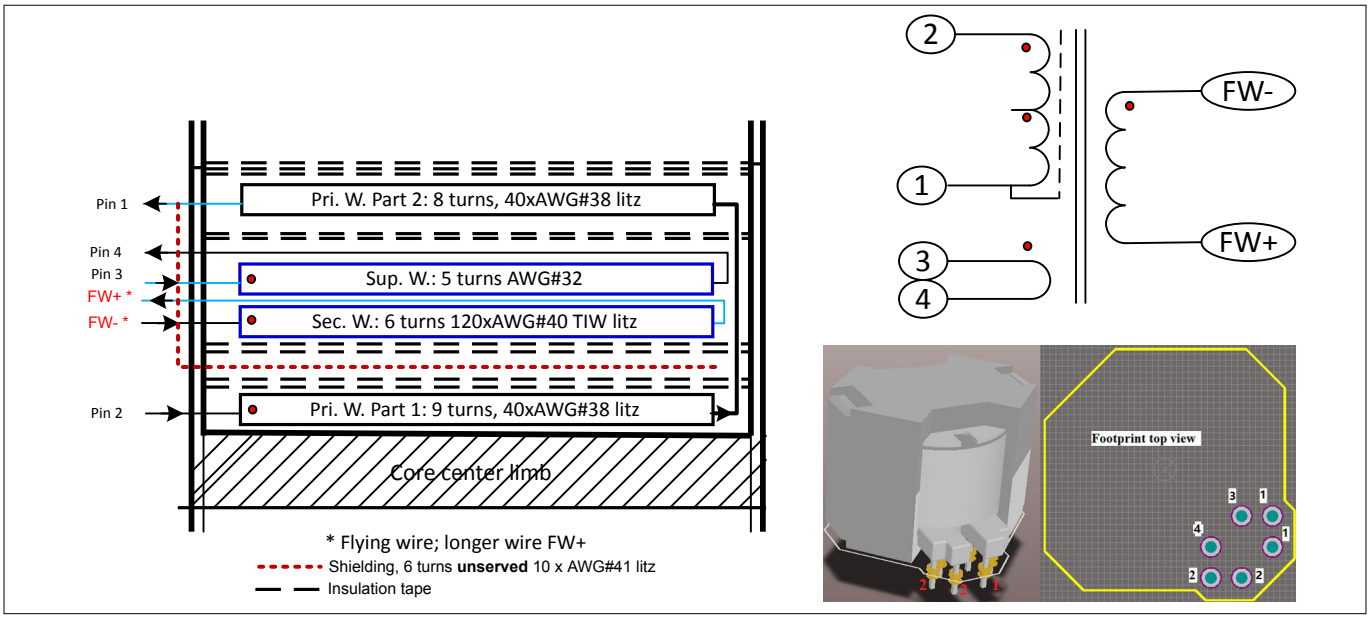


**Figure 7 Transformer winding arrangement and pin assignment**

One inner shielding layer is implemented in this transformer to improve the EMI performance. For the best attenuation of the coupling, the unserved litz wire out of 10 strands of AWG 41 is used. In addition, the 10 strands wire must be evenly distributed and cover the whole wiring layer space to maximize the shielding effect. The wiring process is proposed as shown in the following figures.

Figure 8 Bobbin preparation

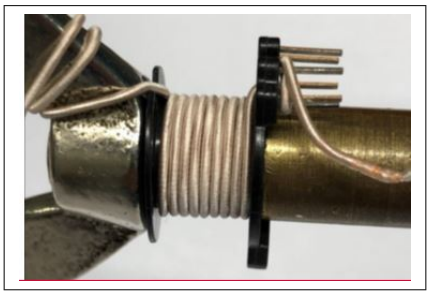

Figure 9 First part of the primary winding

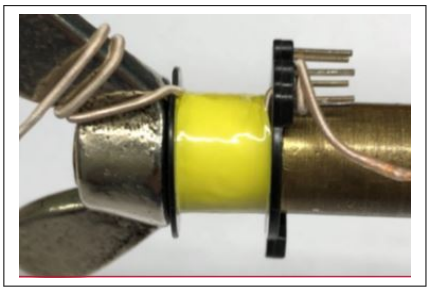

Figure 10 Insulation layer 1

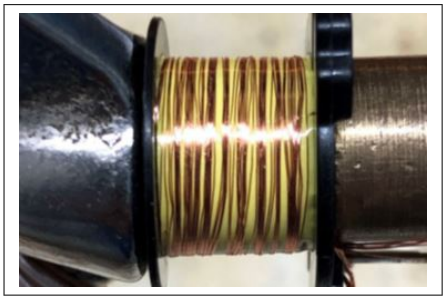

Figure 11 Shielding layer

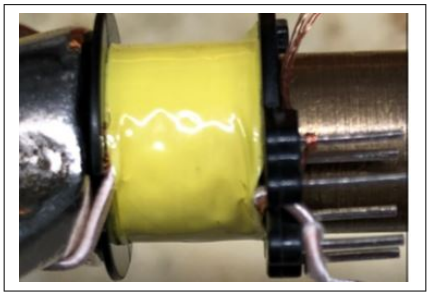

Figure 12 Insulation layer 2

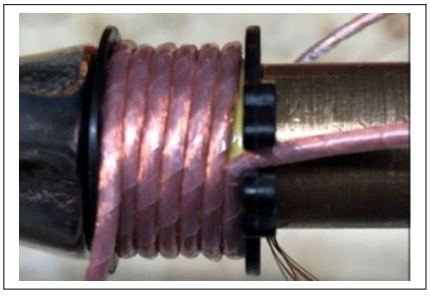

Figure 13 Secondary side winding

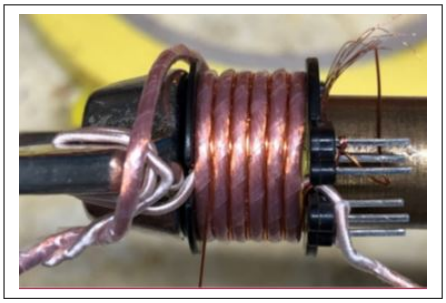

Figure 14 Auxiliary winding

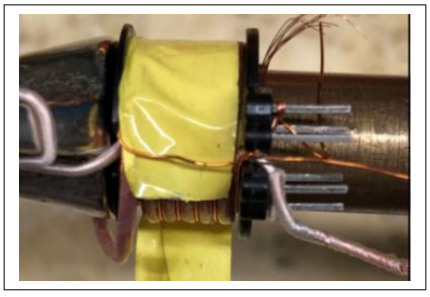

Figure 15 Insulation layer 3a

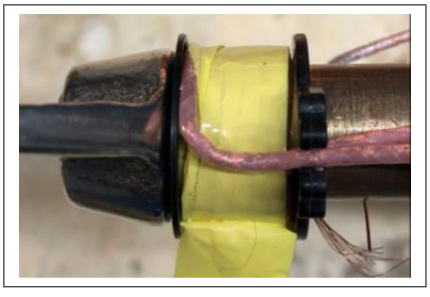

Figure 16 Insulation layer 3b

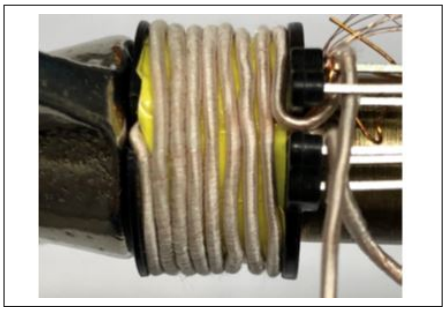

Figure 17 Secondary part of the primary winding

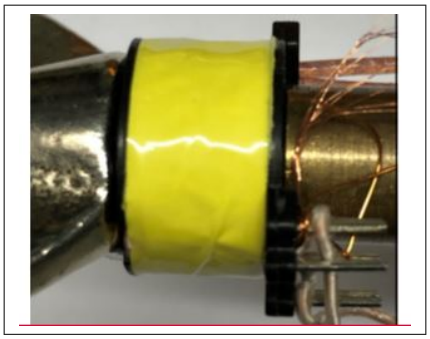

Figure 18 Insulation layer 4

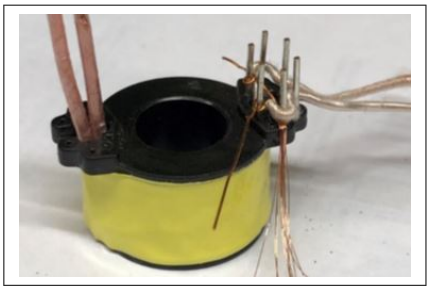

Figure 19 Bottom-side view of the wires

### 2.2.4.2 Common mode choke

*Figure 20* shows the CMC used on the board. Here, the bifilar wires are utilized to minimize the picked-up noise from the components around it.

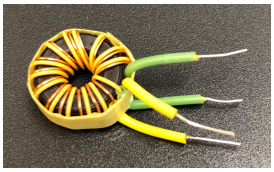

**Figure 20 Common mode choke**

The specifications of CMC are as follows:

- 2 x 5.5 mH
- DCR 41 mΩ
- Dielectric strength 2 $kV_{AC}$/2 s
- Turns ratio 1:1
- Core: T60006-L2012-W902, 12 x 8 x 4.5 mm; 28 µH@10 kHz
- Wire: bifilar; 0.4 mm diameter; one with varnish isolation and the other with varnish isolation plus plastic
- Terminals with insulation tube

## 2.2.5 Board view

The following images illustrate the demo board.

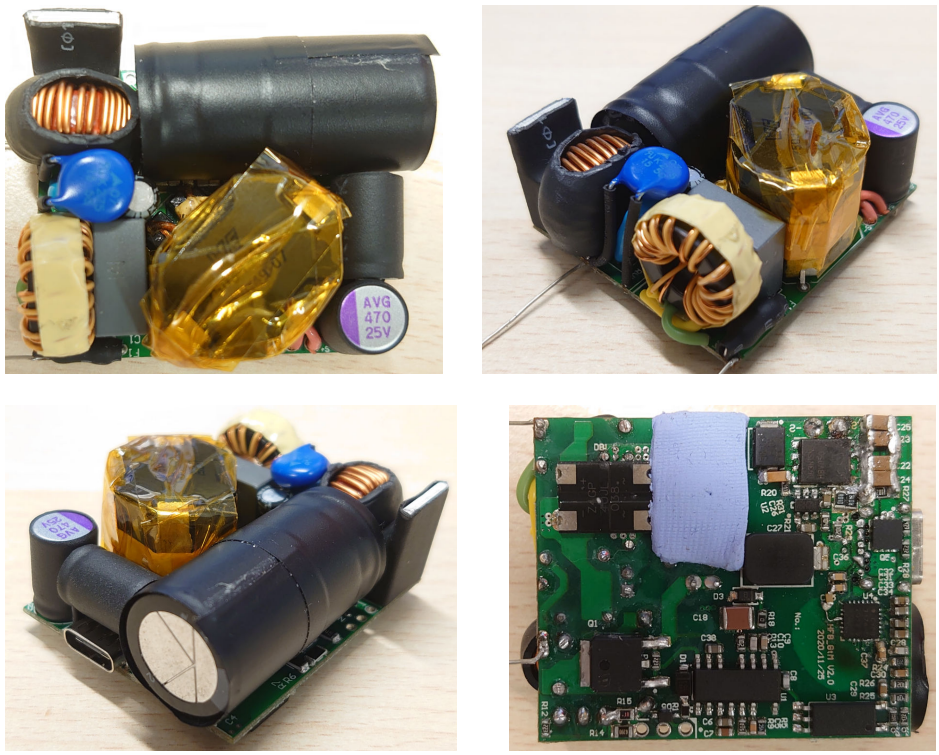


**Figure 21 Board view**

# 3 Measurement results

The measurement results are summarized in the following sub-chapters:

- Efficiency (***Chapter 3.1***)
- EMI (***Chapter 3.2***)
- Thermal image (***Chapter 3.3***)
- Output ripple (***Chapter 3.4***)
- Line and load transient (***Chapter 3.5***)
- Output voltage level transient (***Chapter 3.6***)
- Switching waveform (***Chapter 3.7***)

Depending on the measured items, either the HFB output or the source of the safety switch or the board output is taken as the output reference point. This will be described in the measurement items.

## 3.1 Efficiency and standby power

The efficiency of the board is measured at the source terminal of the safety switch Q5 (***Figure 1***). The full load current is set to 3.25 A for 20 V output voltage and 3 A for the other voltage levels. The measurement efficiency and standby power are shown below.

**Table 4 Efficiency measurement**

| $V_{OUT}$ | $V_{IN}$\Load(%) | 10 | 25 | 50 | 75 | 100 |
|---|---|---|---|---|---|---|
| 20 | 90 $V_{AC}$ | 87.6% | 90.5% | 92.1% | 92.9% | 91.9% |
| | 115 $V_{AC}$ | 88.7% | 91.5% | 92.9% | 93.7% | 93.5% |
| | 230 $V_{AC}$ | 88.8% | 91.6% | 92.5% | 93.0% | 93.8% |
| | 264 $V_{AC}$ | 88.4% | 91.2% | 92.0% | 92.7% | 93.7% |
| 15 | 90 $V_{AC}$ | 81.8% | 87.1% | 90.1% | 91.3% | 91.6% |
| | 115 $V_{AC}$ | 82.4% | 87.7% | 90.6% | 91.4% | 92.3% |
| | 230 $V_{AC}$ | 81.5% | 87.1% | 90.1% | 90.4% | 92.2% |
| | 264 $V_{AC}$ | 80.8% | 86.6% | 89.7% | 90.2% | 91.9% |
| 12 | 90 $V_{AC}$ | 81.7% | 86.8% | 89.7% | 91.2% | 91.4% |
| | 115 $V_{AC}$ | 82.0% | 87.5% | 90.3% | 91.2% | 92.0% |
| | 230 $V_{AC}$ | 80.6% | 87.1% | 89.8% | 90.1% | 91.8% |
| | 264 $V_{AC}$ | 80.1% | 86.1% | 89.3% | 90.7% | 91.8% |
| 9 | 90 $V_{AC}$ | 84.4% | 86.7% | 88.6% | 89.4% | 87.6% |
| | 115 $V_{AC}$ | 84.4% | 87.5% | 89.8% | 90.5% | 90.8% |
| | 230 $V_{AC}$ | 82.2% | 87.9% | 89.8% | 90.6% | 91.6% |
| | 264 $V_{AC}$ | 81.2% | 87.0% | 88.8% | 90.2% | 91.3% |
| 5 | 90 $V_{AC}$ | 84.5% | 86.2% | 87.8% | 87.8% | 87.2% |
| | 115 $V_{AC}$ | 84.6% | 86.4% | 88.1% | 88.3% | 88.1% |
| | 230 $V_{AC}$ | 82.2% | 85.9% | 87.2% | 87.7% | 88.3% |
| | 264 $V_{AC}$ | 81.4% | 85.0% | 86.4% | 87.1% | 88.0% |

## 3 Measurement results

**Table 5 Average efficiency**

| $V_{IN}$\$V_{OUT}$(V) | 5 | 9 | 12 | 15 | 20 |
|---|---|---|---|---|---|
| 90 $V_{AC}$ | 86.6% | 88.1% | 89.8% | 90.0% | 91.8% |
| 115 $V_{AC}$ | 86.9% | 89.6% | 90.2% | 90.5% | 92.9% |
| 230 $V_{AC}$ | 85.8% | 90.0% | 89.7% | 89.9% | 92.7% |
| 264 $V_{AC}$ | 85.0% | 89.3% | 89.5% | 89.6% | 92.4% |

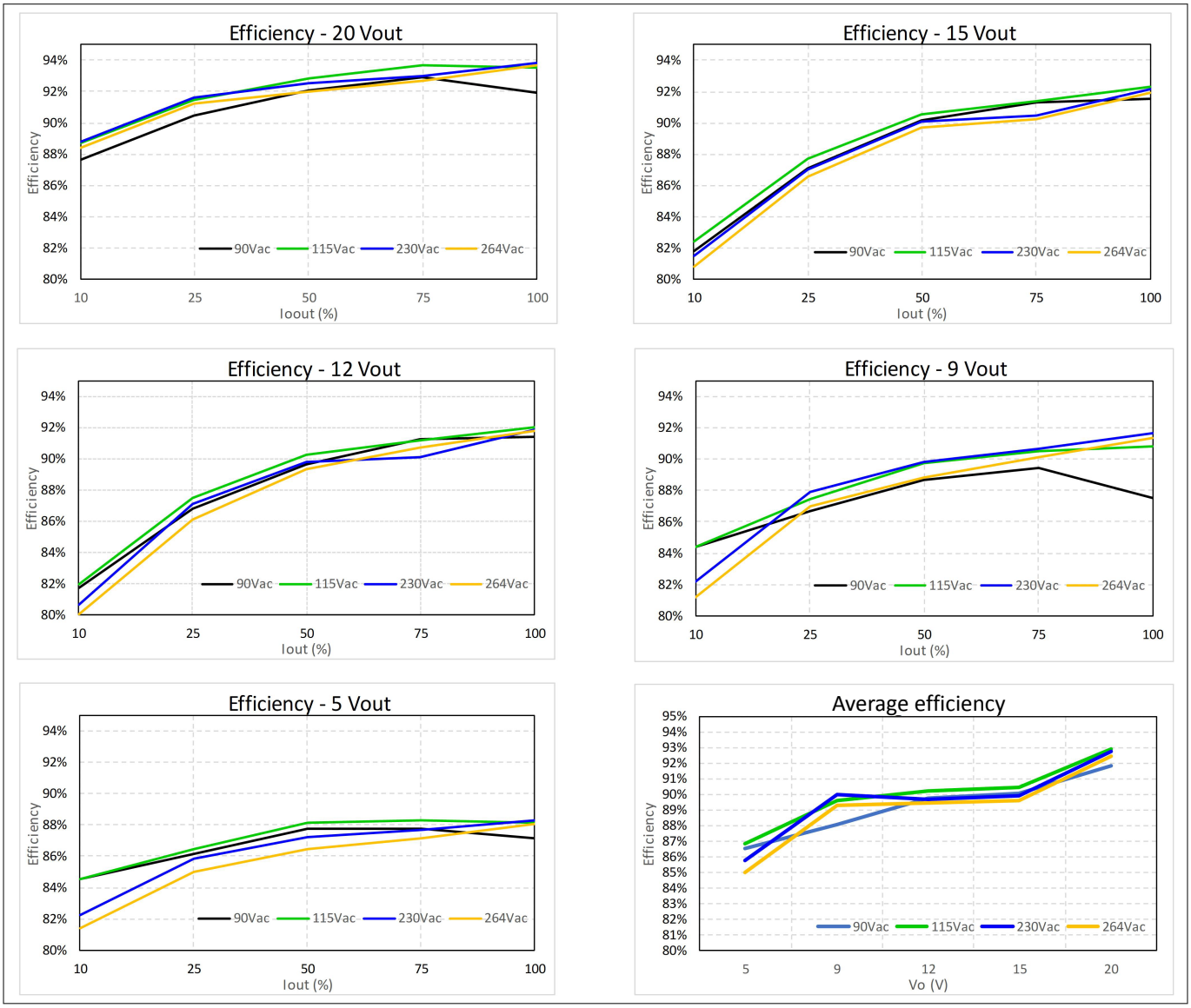


**Figure 22 Efficiency curves**

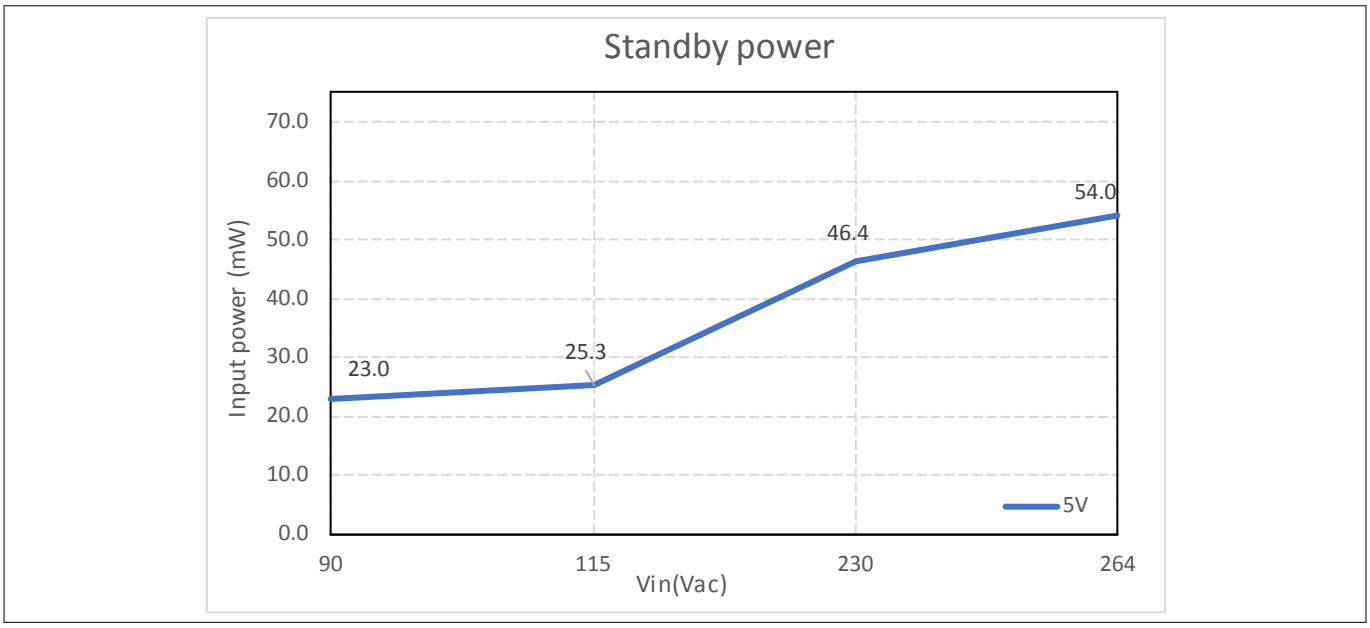


**Figure 23 Standby power**

## 3.2 EMI

The board passes the EMI test with at least -3 dBµV margin for the peak value measurement. The following figures show the results of different measurements.

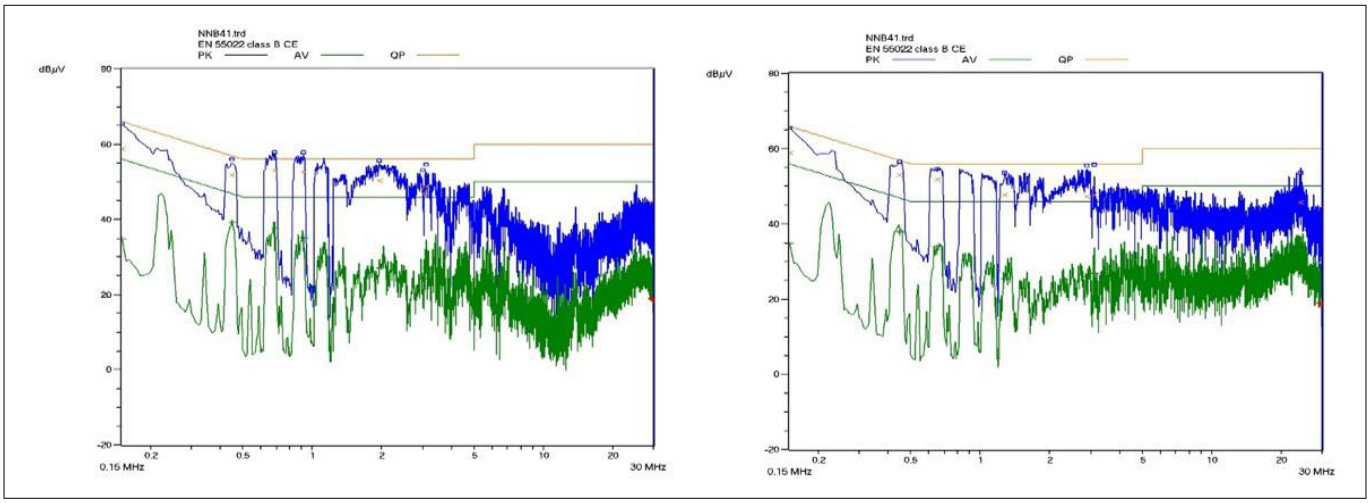


**Figure 24 Measurement at 230 V, output at 20 V and 3.25 A: line (left) and neutral (right)**

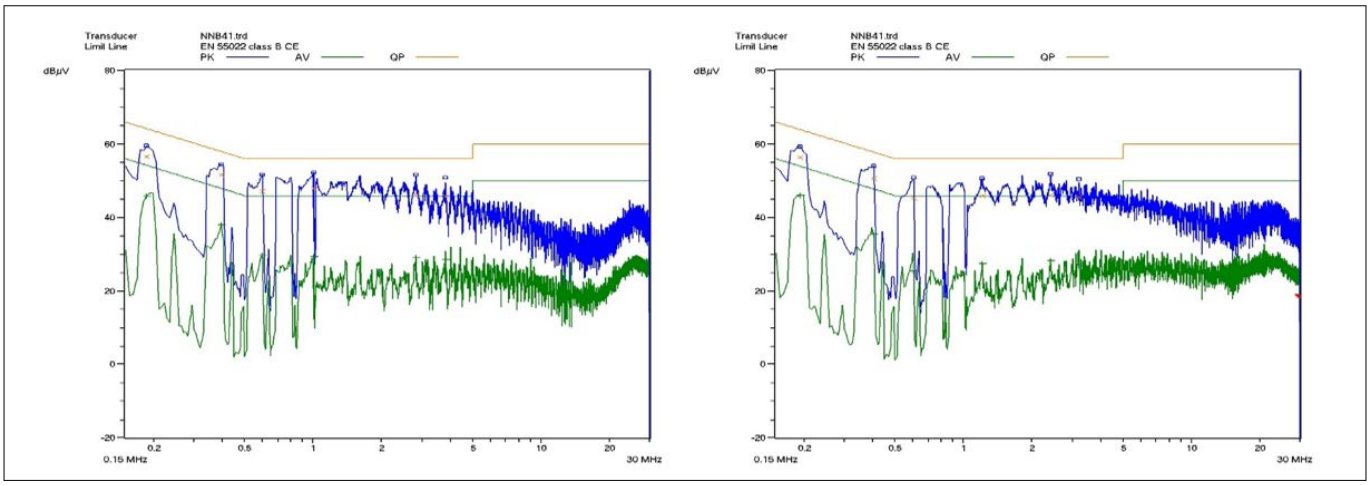


**Figure 25 Measurement at 115 V, output at 20 V and 3.25 A: line (left) and neutral (right)**

## 3.3 Thermal image

The following images show the thermal performance of the board. The highest temperature of 87.1°C is measured at the bridge rectifier at low line and 86.4°C at the SR controller at high line.

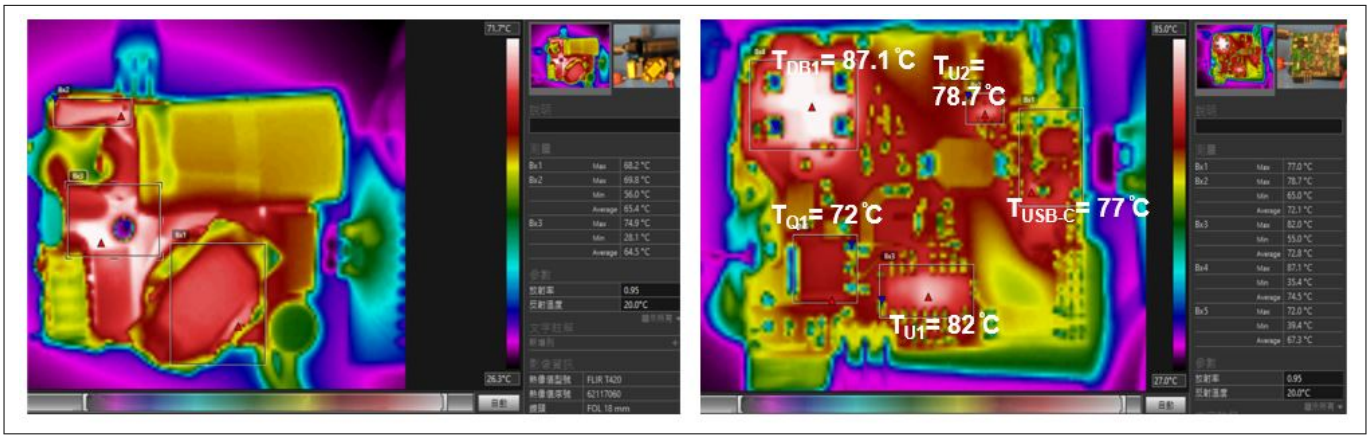


**Figure 26 Thermal image at AC of 115 V, output 20 V and 3 A: top (left) and bottom (right)**

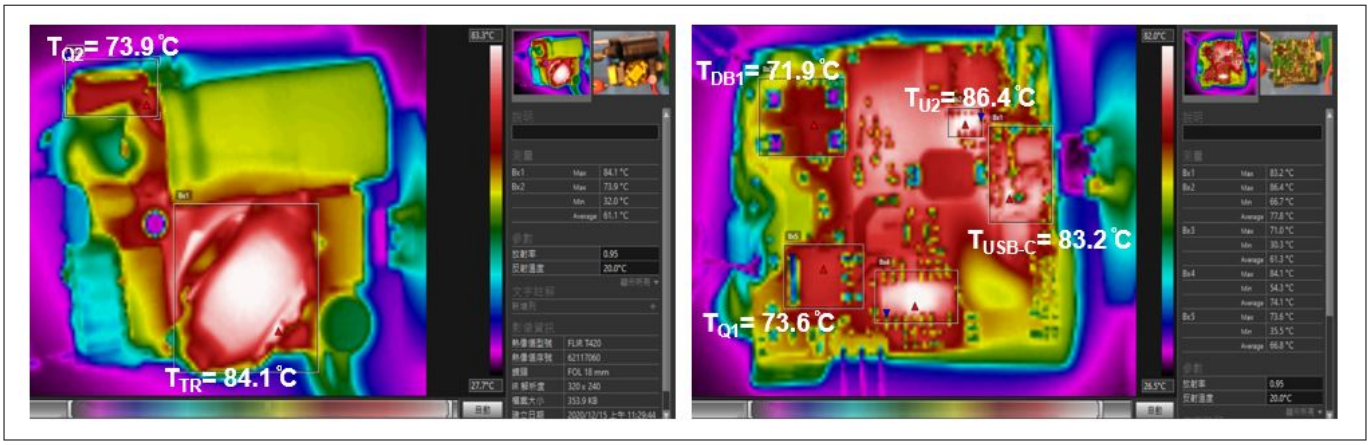


**Figure 27 Thermal image at AC of 230 V, output 20 V and 3 A: top (left) and bottom (right)**

## 3.4 Output ripple

The output voltage ripple during the steady-state operation is measured at the output capacitors of the HFB stage.

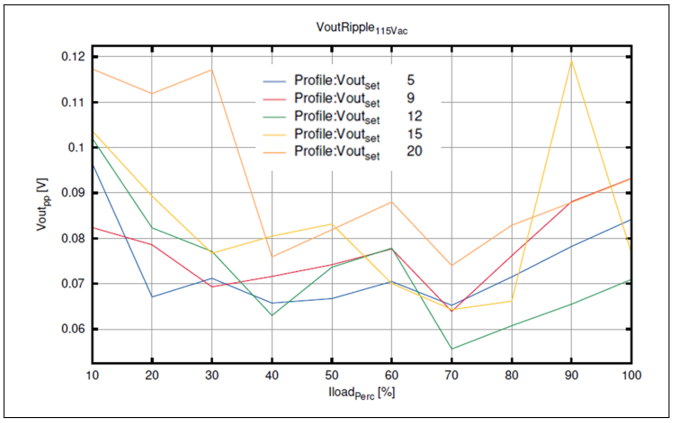


**Figure 28 Output voltage ripple at 115 V**

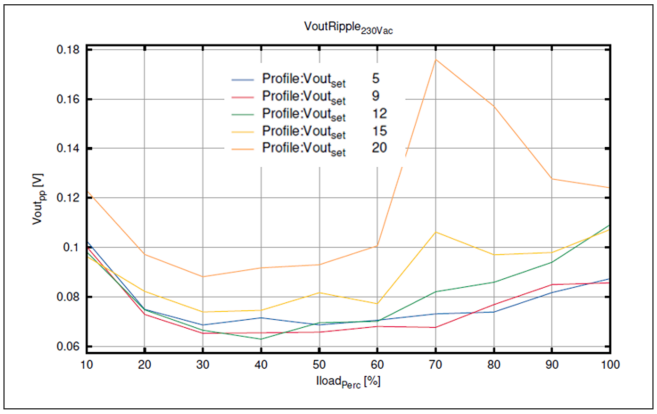


**Figure 29 Output voltage ripple at 230 V**

## 3.5 Line and load transient

The following figures show the HFB output voltage at line and load transient. As usual, a 10 µF electrolytic capacitor and a 100 nF ceramic capacitor are placed at the probe input.

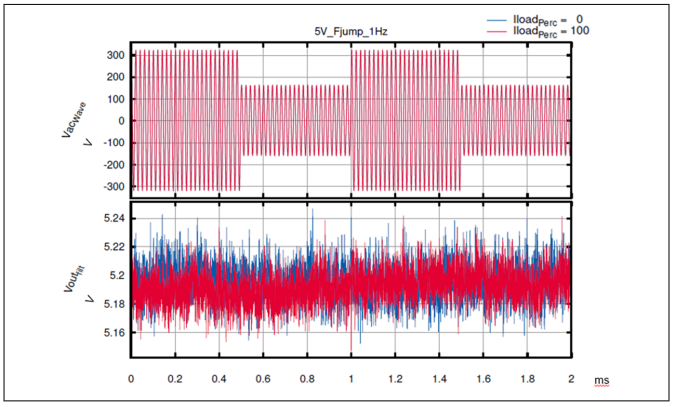


**Figure 30 Line transient between 115 V and 230 V at 1 Hz**

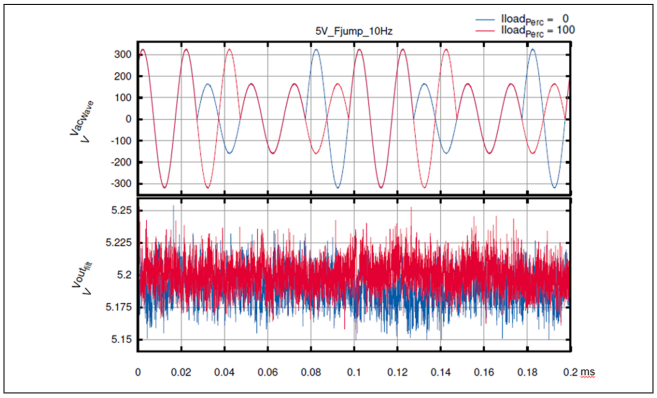


**Figure 31 Line transient between 115 V and 230 V at 10 Hz**

## 3 Measurement results

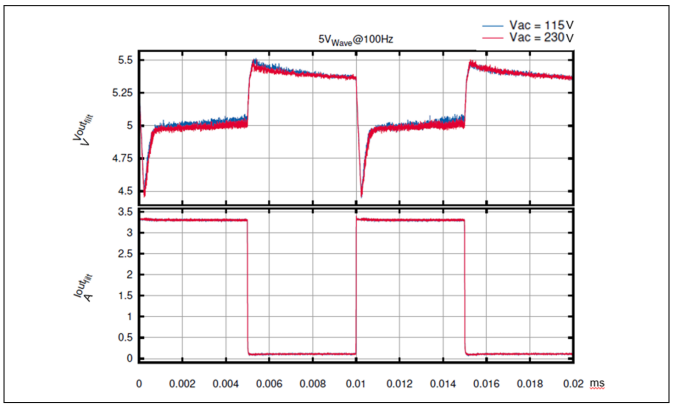


**Figure 32** **Load transient between 10% and 100% of 3.25 A at 5 V output**

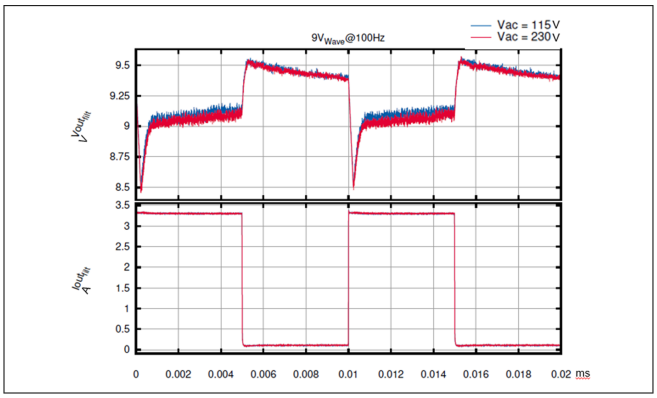


**Figure 33** **Load transient between 10% and 100% of 3.25 A at 9 V output**

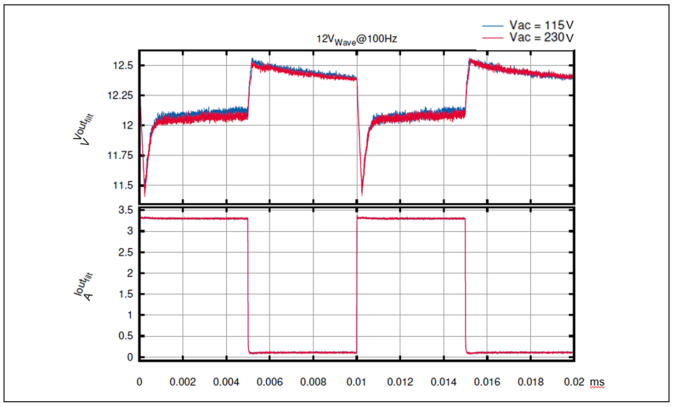


**Figure 34** **Load transient between 10% and 100% of 3.25 A at 12 V output**

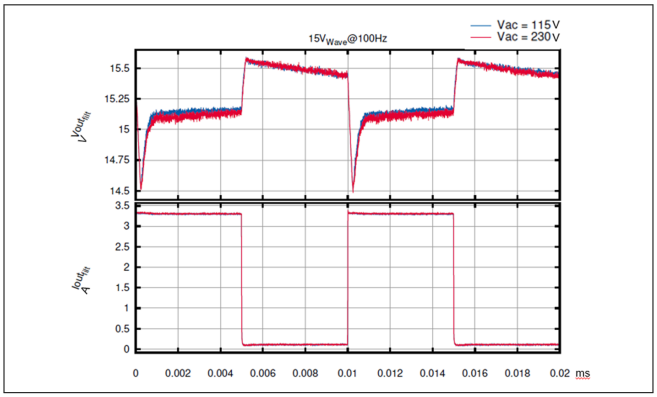


**Figure 35** **Load transient between 10% and 100% of 3.25 A at 15 V output**

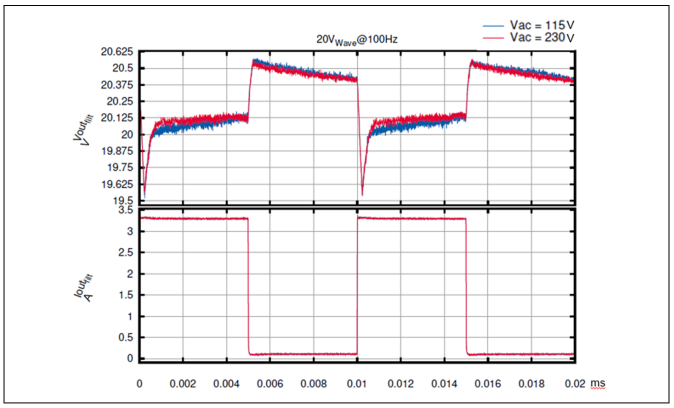


**Figure 36** **Load transient between 10% and 100% of 3.25 A at 20 V output**

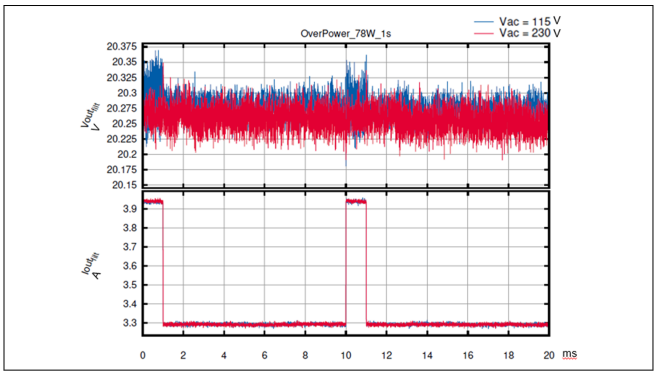


**Figure 37** **Overload: 78 W for 1 s**

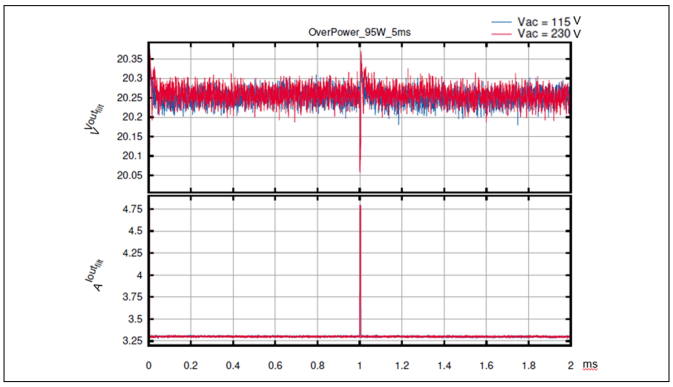


**Figure 38 Peak load: 95 W for 5 ms**

## 3.6 Output voltage level transient

The following figures show the HFB output voltage at the output level changes between 5 V and 20 V at 115 V and 230 $V_{AC}$ input voltage. The other output voltage level transients show similar waveforms, but are not shown here.

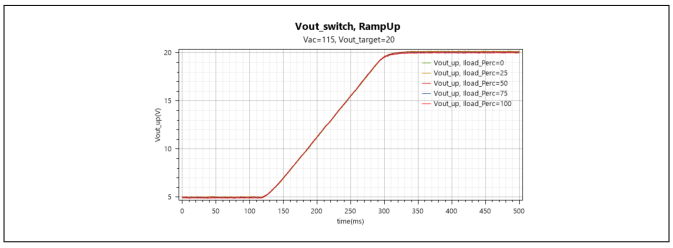


**Figure 39 Output from 5 V to 20 V at 115 $V_{AC}$**

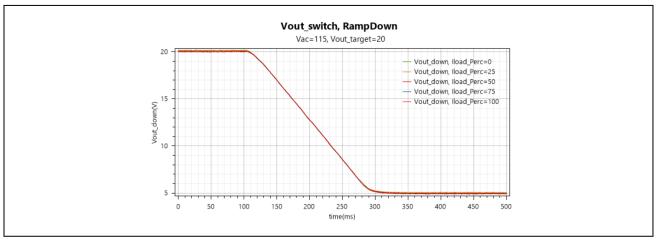


**Figure 40 Output from 20 V to 5 V at 115 $V_{AC}$**

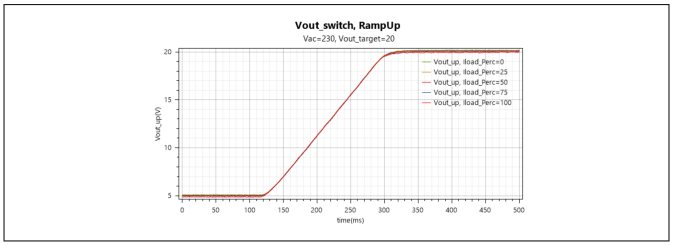


**Figure 41 Output from 5 V to 20 V at 230 $V_{AC}$**

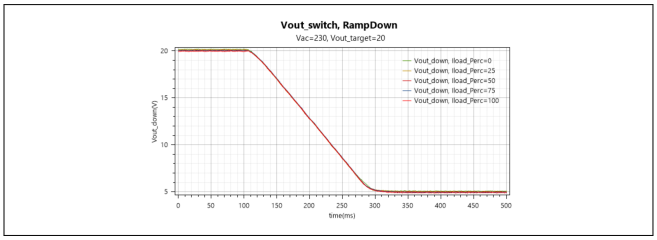


**Figure 42 Output from 20 V to 5 V at 230 $V_{AC}$**

## 3.7 Switching waveforms

The following switching waveforms are shown in this sub-chapter:

- Start-up (***Chapter 3.7.1***)
- Operation mode (***Chapter 3.7.2***)
- Jitter (***Chapter 3.7.3***)
- Protection (***Chapter 3.7.4***)

### 3.7.1 Start-up

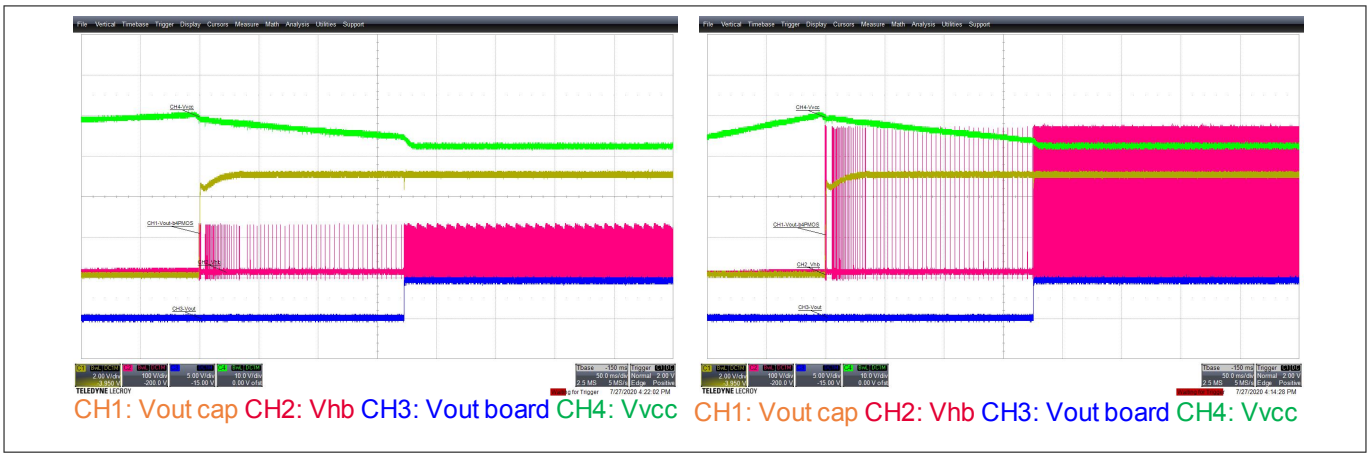


**Figure 43 Cold start-up at full load, and input 90 V (left) and 264 V (right)**

Figure 43 depicts the start-up at full load while the load is connected at the board output. The voltage at the HFB output (CH1, yellow) rises in short time after the beginning of the operation, but the PD device needs some time for initialization. The rising edge of the board output voltage (CH3, blue) shows a time delay. During this delay time, HFB operates in the burst mode, as shown by the voltage at the HB switching node Vhb (CH2, pink). Once the PD device is active, a well-regulated output voltage is available for the end device.

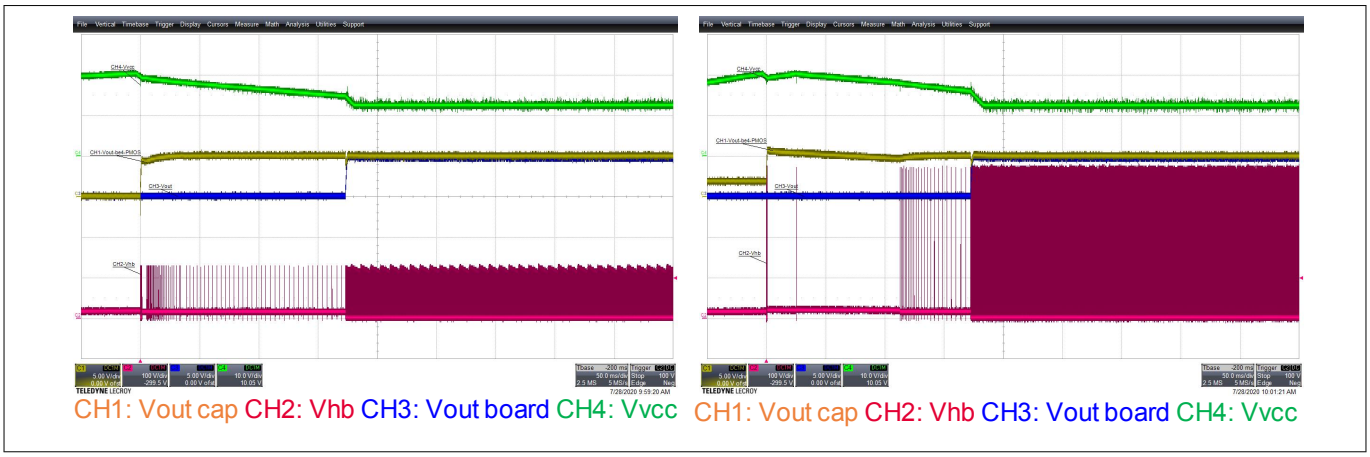


**Figure 44 Cold start-up with an additional 470 µF capacitor at the board output at full load, and input 90 V (left) and 264 V (right)**

These waveforms show the capacitive load performance where a 470 µF electrolytic capacitor is added at the input of the load module. Once the PD device is active, a well-regulated output voltage is available for the end device.

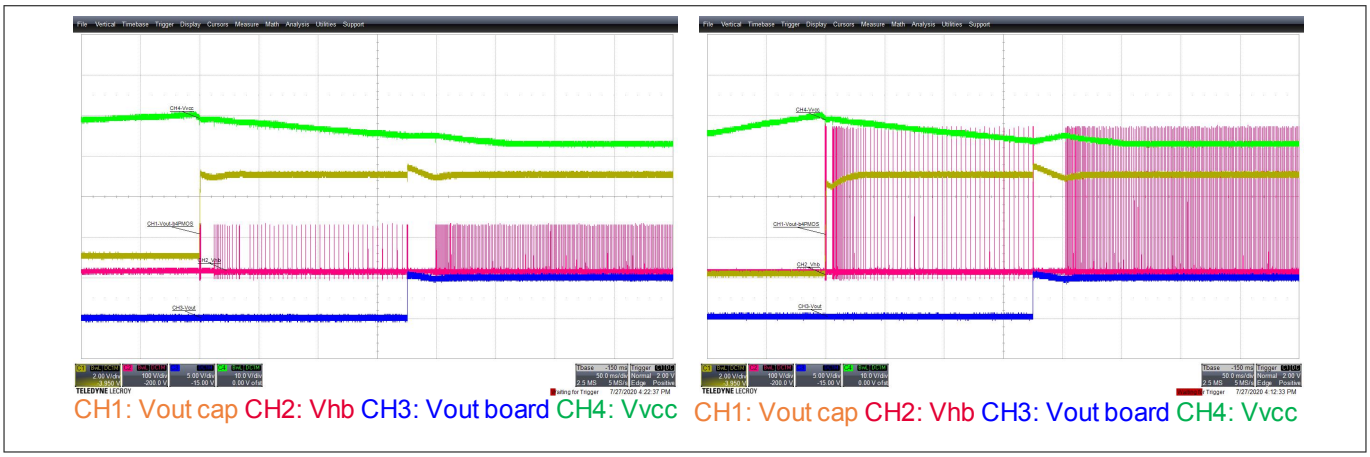


**Figure 45 Cold start-up at 0 A load current, and input 90 V (left) and 264 V (right)**

These waveforms show the behavior at 0 A load current. At 0 A loading, the system operates in the burst mode. For the start-up at 0 A, the used DC load module has some impact on the output voltage. The input capacitance of the load module leads to a relatively long burst time and, therefore, a slightly increased voltage. The same effect applies to the next test case of 0 A and with a 470 µF capacitive load.

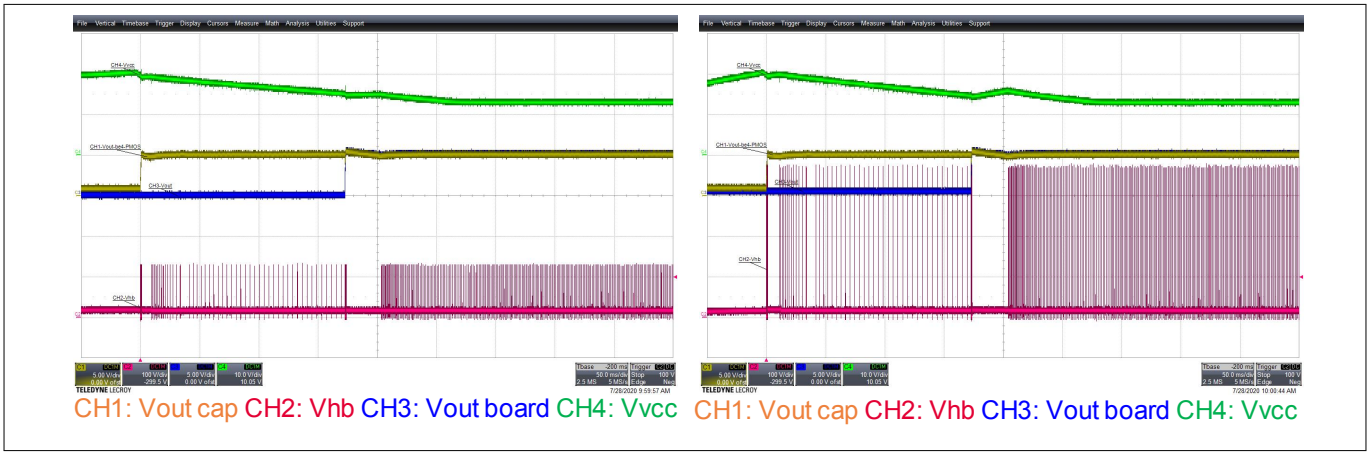


**Figure 46 Cold start-up with an additional 470 µF capacitor at the board output at 0 A, and input 90 V (left) and 264 V (right)**

## 3.7.2 Operation mode

The operation mode at the following conditions are shown below:

- AC input voltage of 90 V and 264 V
- Output voltage of 5 V and 20 V
- Output current of 0 A, 0.2 A, 1.2 A and 3.25 A

**Modes during steady-state operation**

Depending on the configured parameter values and the set real output voltage and current, HFB operates in different modes. By default parameter configuration, only the burst mode and ZV-RVS mode are possible for 5 V and 9 V output voltage, while the burst mode, ZV-RVS and CRM operation are possible for 12 V, 15 V and 20 V output voltage. The burst mode operation is for the light load current, while CRM is for the high output load current. In the middle range of the load current, the ZV-RVS mode takes place. In Figure 47 to Figure 50, only the operating waveforms for 5 V and 20 V are shown.

***Figure 47*** shows the burst mode operation at 0 A and 0.2 A, and the ZV-RVS operation at 1.2 A and 3.25 A for the 5 V output voltage. At 0 A load current, as shown in the upper-left figure, the burst break time is longer than 1 ms. Therefore, a pre-charge pulse occurs before the ZVS pulse, which boosts the VCC supply for the high-side

driver. This can be seen at the first drop of the primary current (CH3, blue). At 0.2 A load current, the burst break time is less than 1 ms. In this condition, there is no pre-charge pulse available.

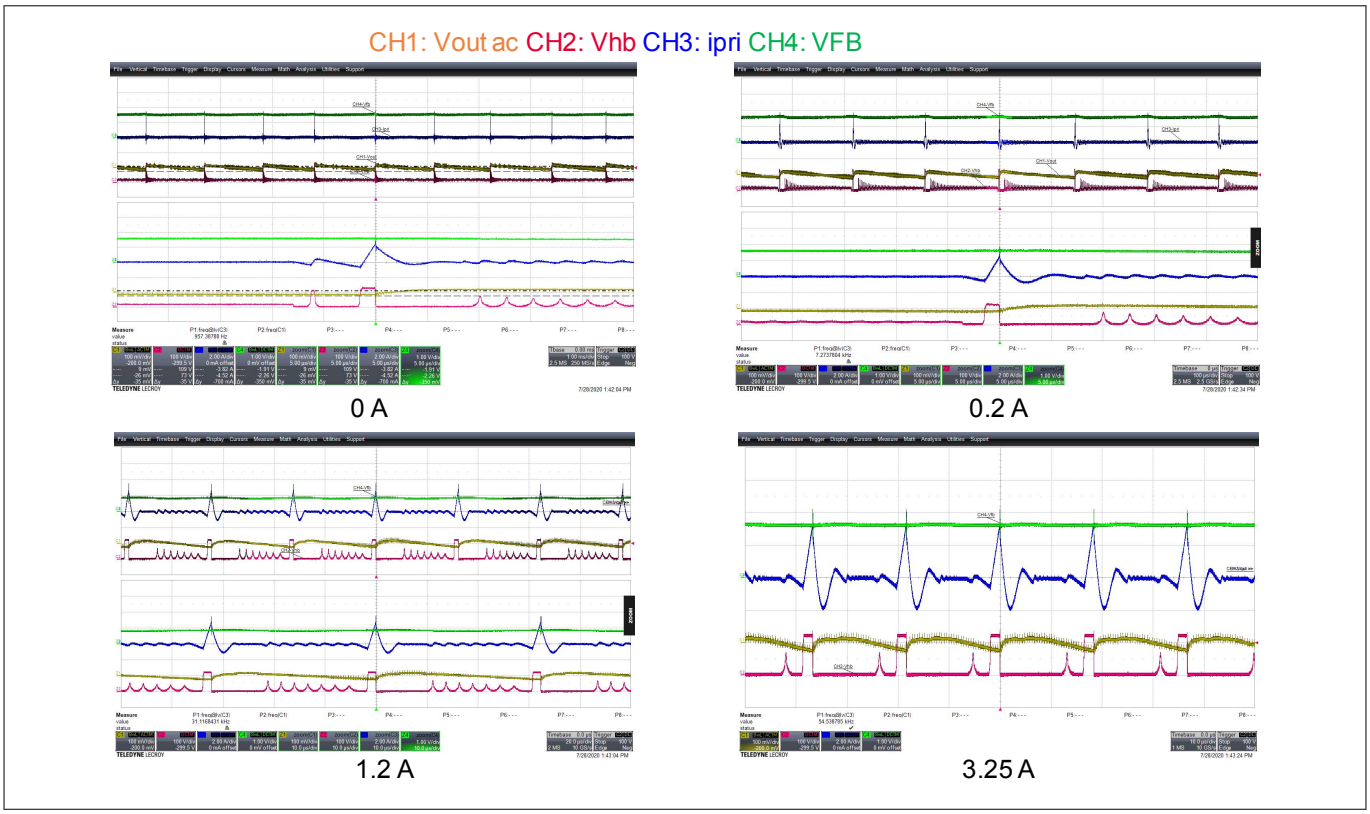


**Figure 47 Operation at 90 V input and 5 V output voltage**

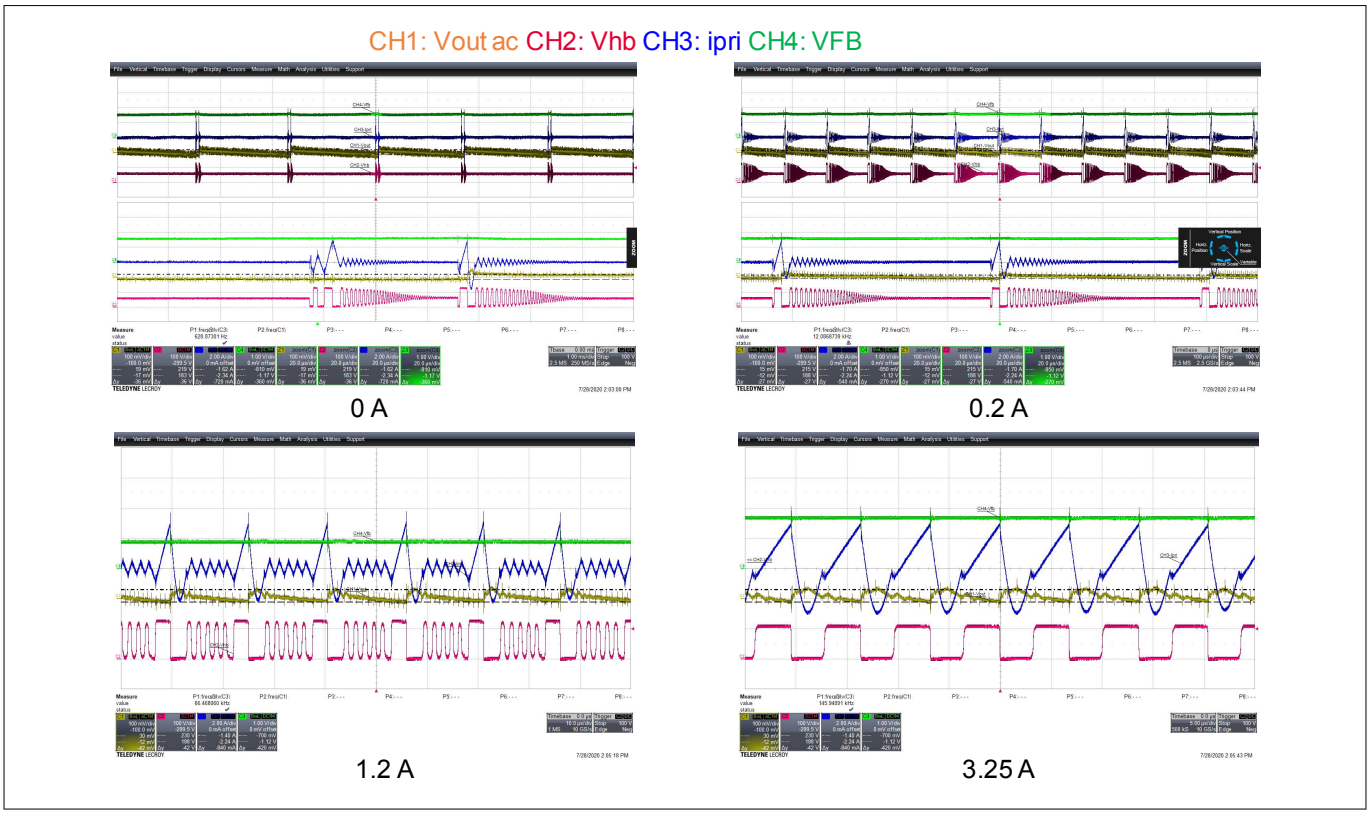


**Figure 48 Operation at 90 V input and 20 V output voltage**

## 3 Measurement results

At 20 V output voltage, the HFB converter operates in the burst mode for both 0 A and 0.2 A, ZV-RVS mode at 1.2 A and CRM at 3.25 A. At 0 A load current, the burst break is longer than 1 ms and the pre-charge pulse applies at the burst beginning.

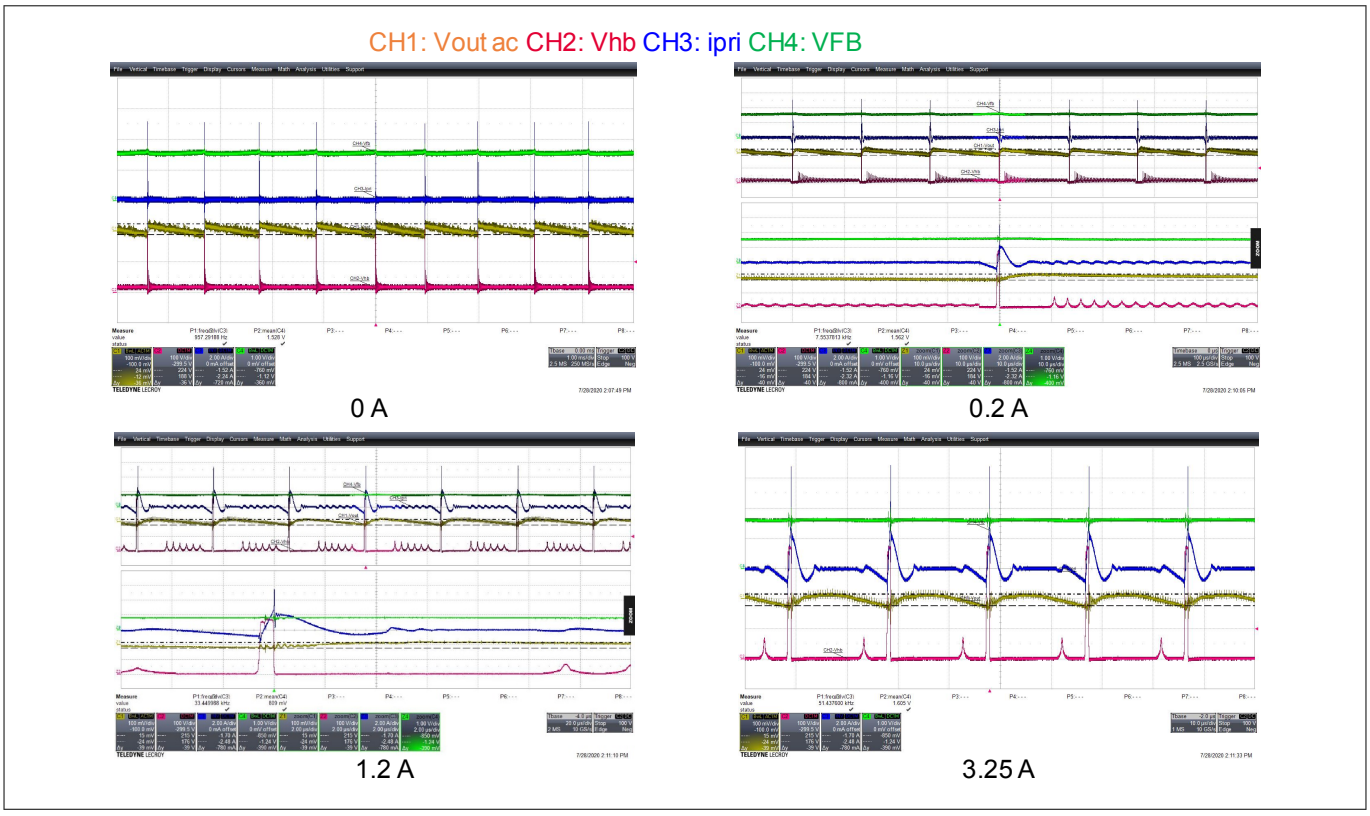


**Figure 49 Operation at 264 V input and 5 V output voltage**

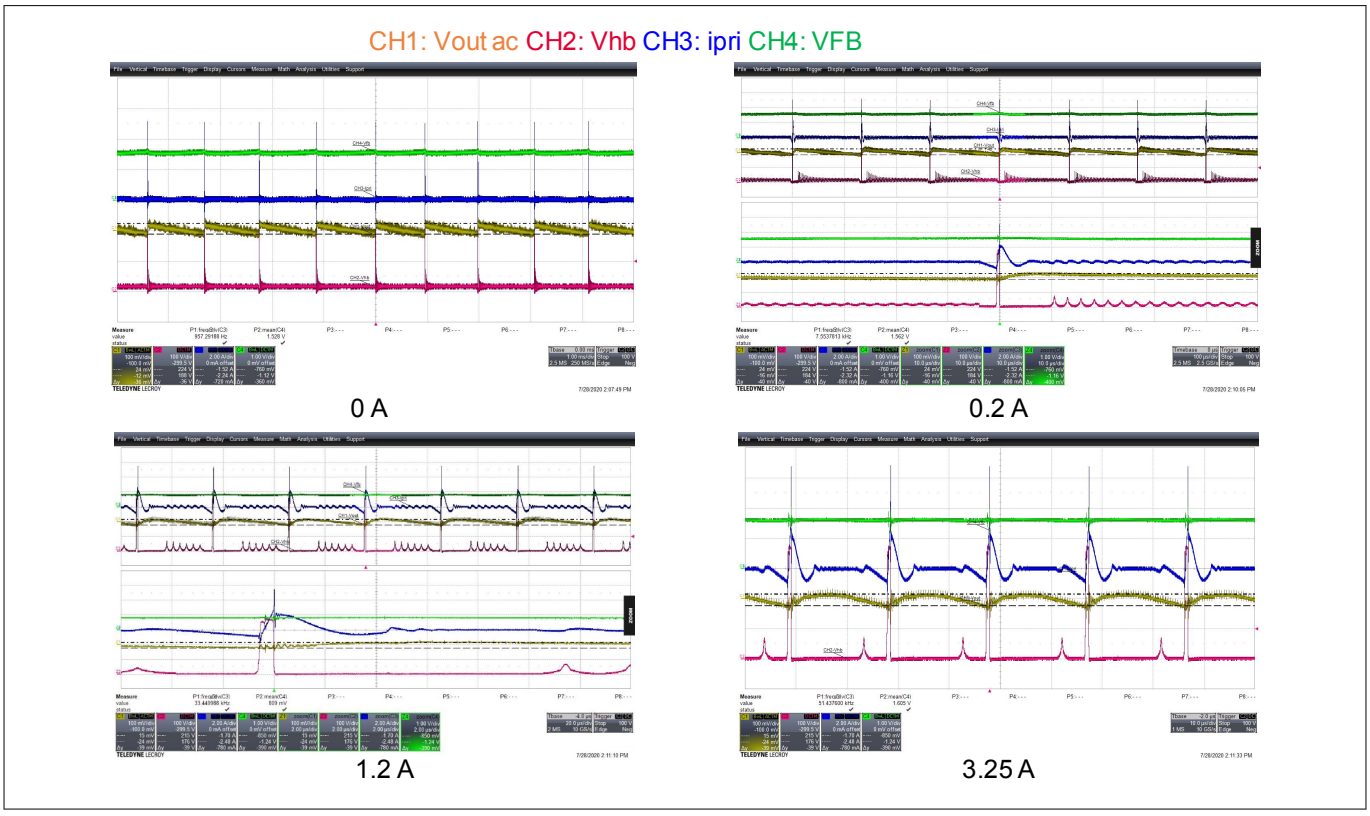


**Figure 50 Operation at 264 V input and 20 V output voltage**

Similar mode changes can be observed at the other operating conditions, such as at high line, as shown in ***Figure 49*** for the 5 V output and ***Figure 50*** for the 20 V output use cases at high line.

**Mode at load transient**

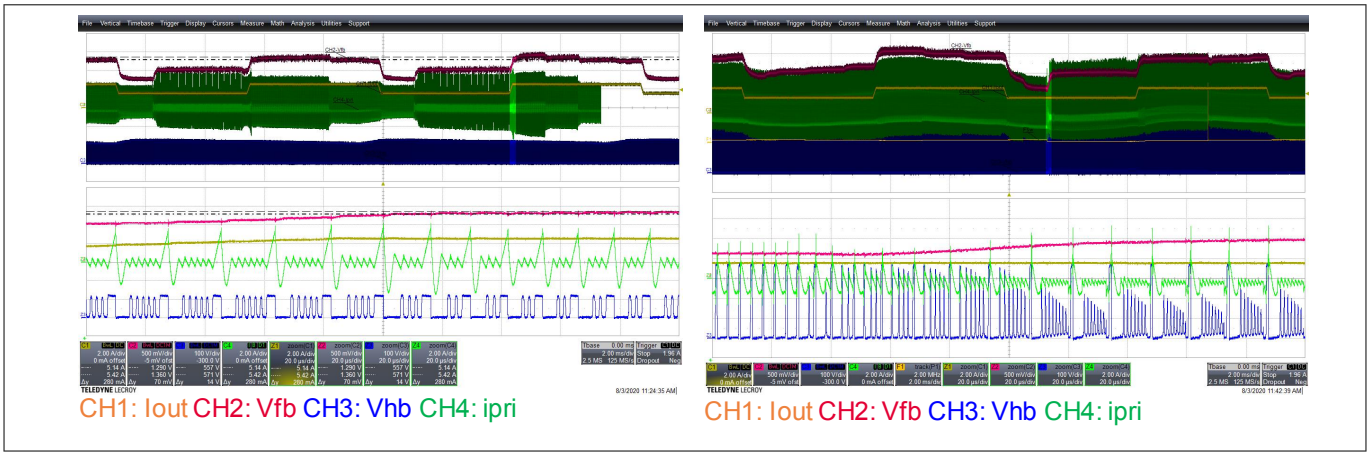


**Figure 51 Load transient between 2.5 A and 1.5 A, 113 Hz and 50% duty at input 90 V and 15 V output (left) and 264 V and 20 V output (right)**

The feedback voltage reacts on the output current change in time. Accordingly, the valley numbers change for the output voltage regulation, as shown in the left-side figure. The operation mode may change, as well. As shown in the right-side figure, the system changes from the CRM to ZV-RVS mode with increasing valley numbers. However, the operation mode change is not synchronized with the load steps. This is due to the fact that there are some other criteria for the operation mode change to ensure a stable operation at the load transition. This mode and the valley numbers change at the load transient can be observed at the other conditions, considering 12 V and 15 V output operating cases as examples (refer to ***Figure 52*** and ***Figure 53***).

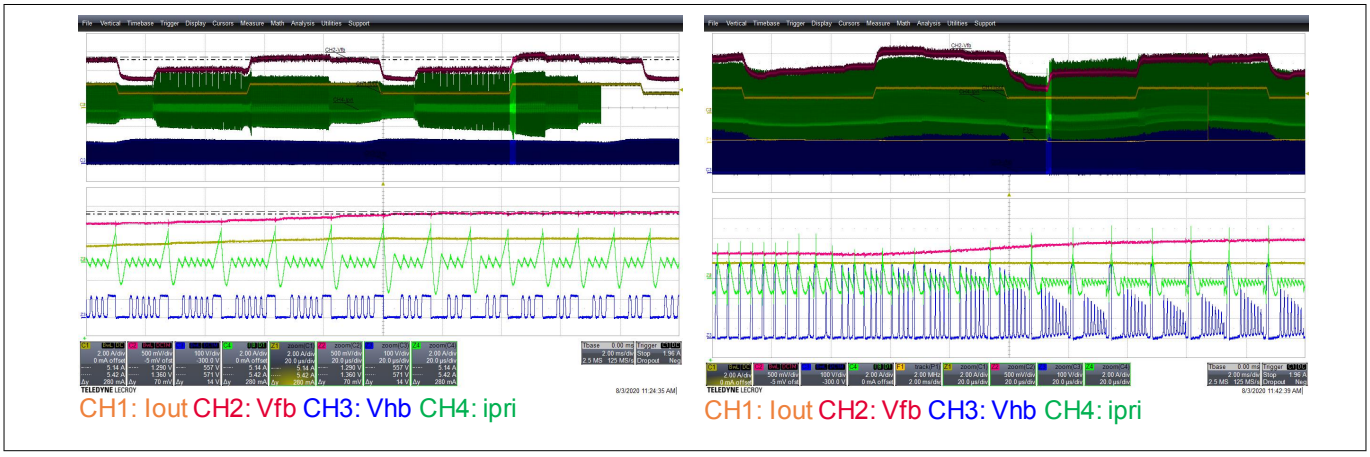


**Figure 52 Load transient between 2.5 A and 1.5 A, 113 Hz and 50% duty at input 90 V and output 15 V**

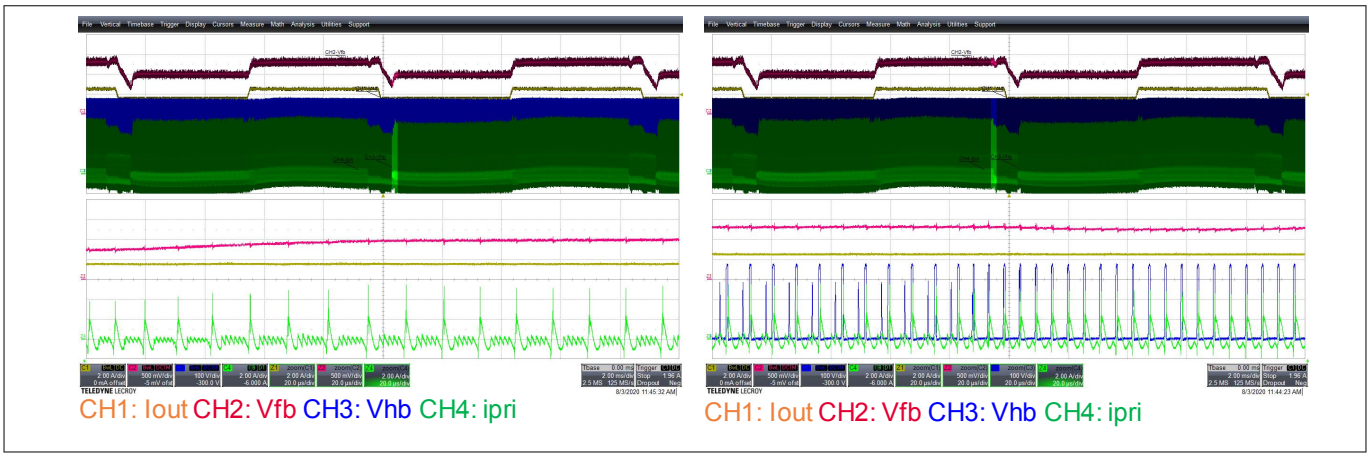


**Figure 53 Load transient between 2.5 A and 1.5 A, 113 Hz and 50% duty at input 264 V and output 15 V**

## 3.7.3 Jitter

The switching frequency jitter is implemented in the controller IC XDPS2201. The switching frequency jitters up a configurable voltage level across the bulk capacitor and in the CRM operation. The following figures show some of the measurement results.

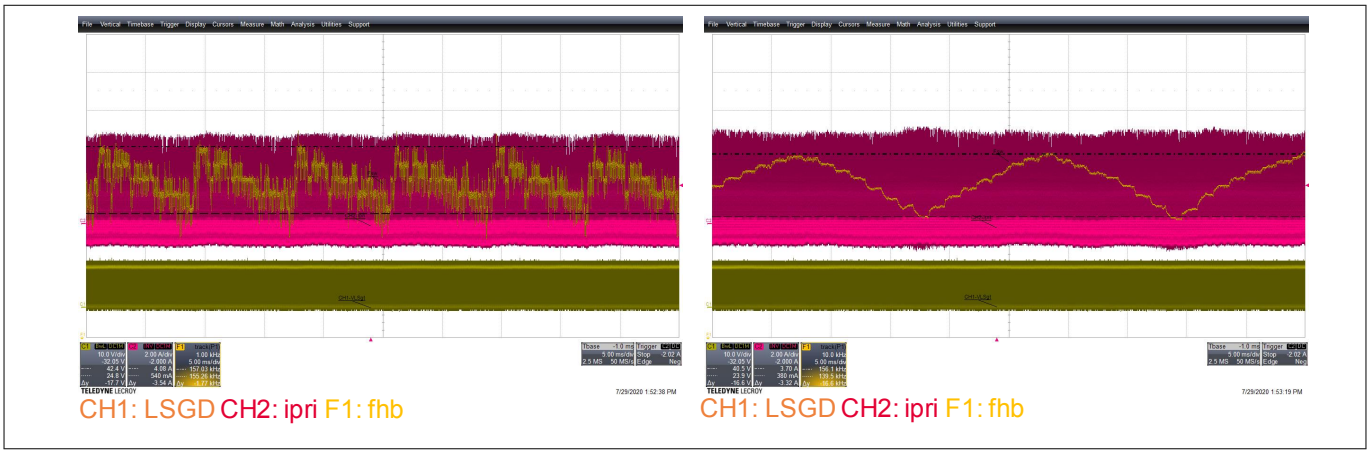


**Figure 54 Operation at 12 V and 3.25 A: no jitter at input 180 V (left) and jitter at input 185 V (right)**

There is no jitter of the switching frequency from the waveform at the left side, where the input voltage is 180 V rms and below the set threshold. The frequency changes irregularly and only the related voltage ripple across the bus capacitor. On the right side, the frequency changes according to the jitter setting and with a regular pattern.

Both time step of the frequency change and the span of the switching frequency jitter are configurable. The frequency jitter is only active at high output load, as shown in ***Figure 55*** and ***Figure 56***.

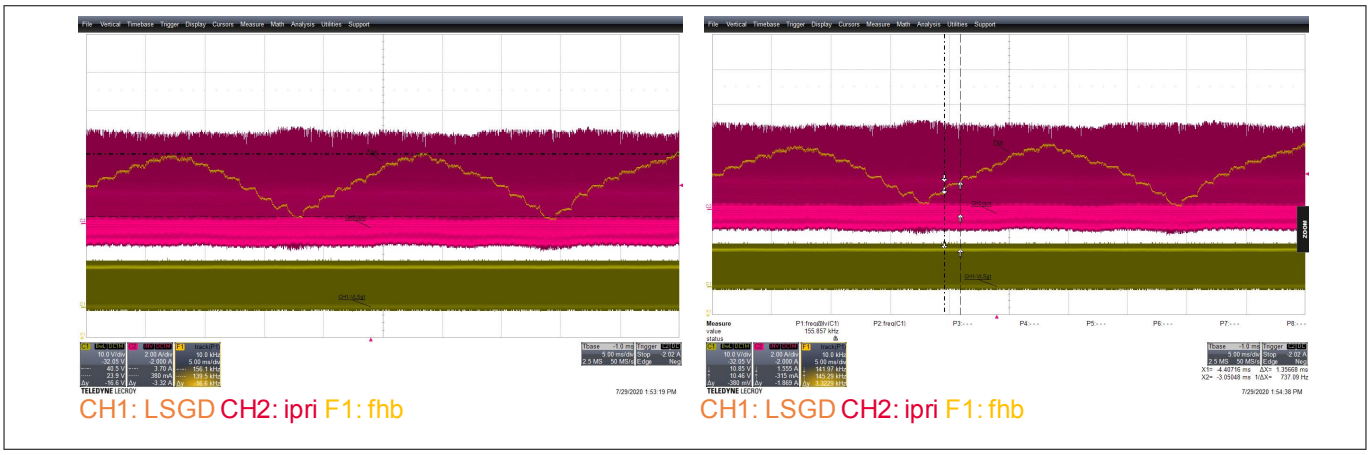


**Figure 55 Jitter frequency and update time at 185 V input, 12 V at 3.25 A**

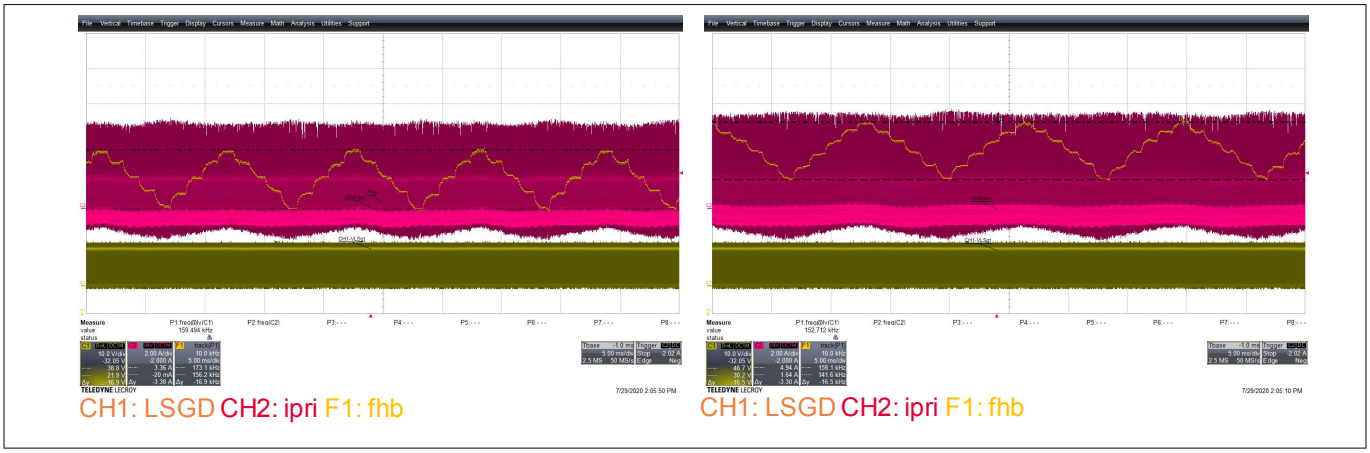


**Figure 56 Jitter frequency at 230 V, 12 V: 3.25 A (left) and 3 A (right)**

## 3.7.4 Protection

A comprehensive protection feature set is implemented in the controller XDPS2201. In the following sub-section, only some of them are illustrated.

**Overcurrent**

For the overcurrent tests, the load is connected to the main stage output across the capacitor C21 (***Figure 1***), to illustrate the functionality of the HFB controller XDPS2201.

Two types of overcurrent protection mechanisms are available: one is based on the output current estimation (including OCP1lev1, OCP1lev2 and OCP1max) and the other one is based on the hardware comparator (OCP2). The protection OCP1 has a lower threshold and longer blanking time and, therefore, reacts slower, while the protection OCP2 has a higher threshold and much shorter blanking time and reacts much faster. In addition, these two different protection mechanisms serve different purposes. While OCP1 is for the output load overcurrent protection, OCP2 is to avoid damage due to the hardware failure, such as short transformer winding. These are illustrated by the following test cases.

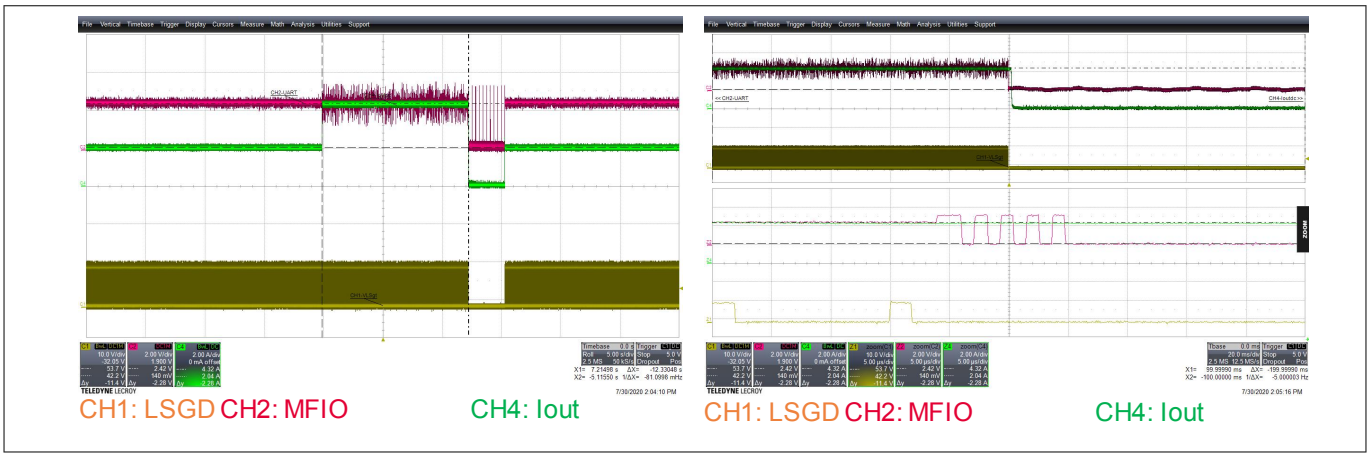


**Figure 57 OCP1 level 1 triggering at 90 $V_{AC}$ input**

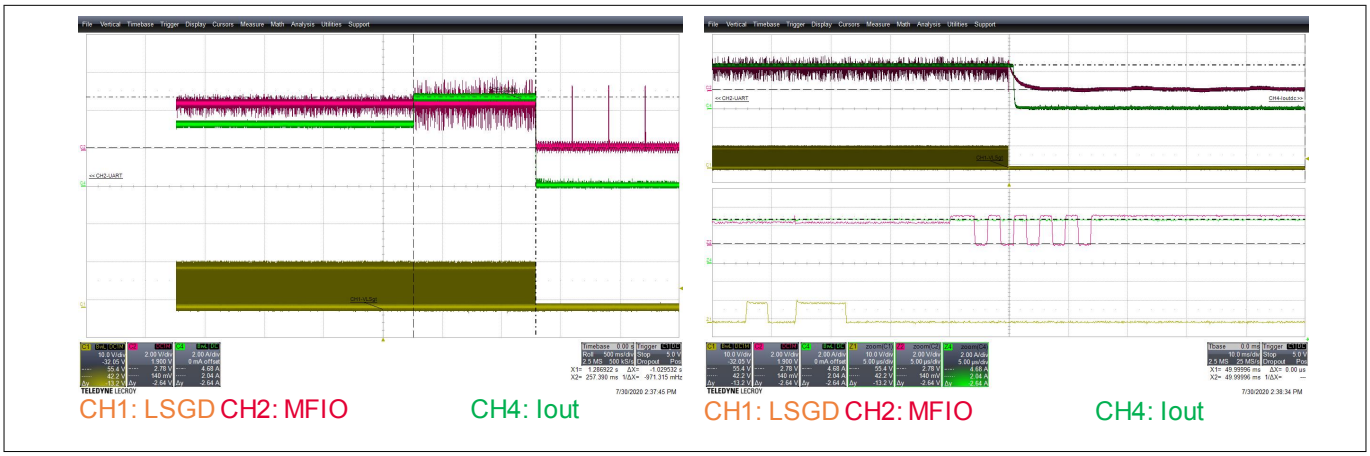


**Figure 58 OCP1 level 2 triggering at 90 $V_{AC}$ input**

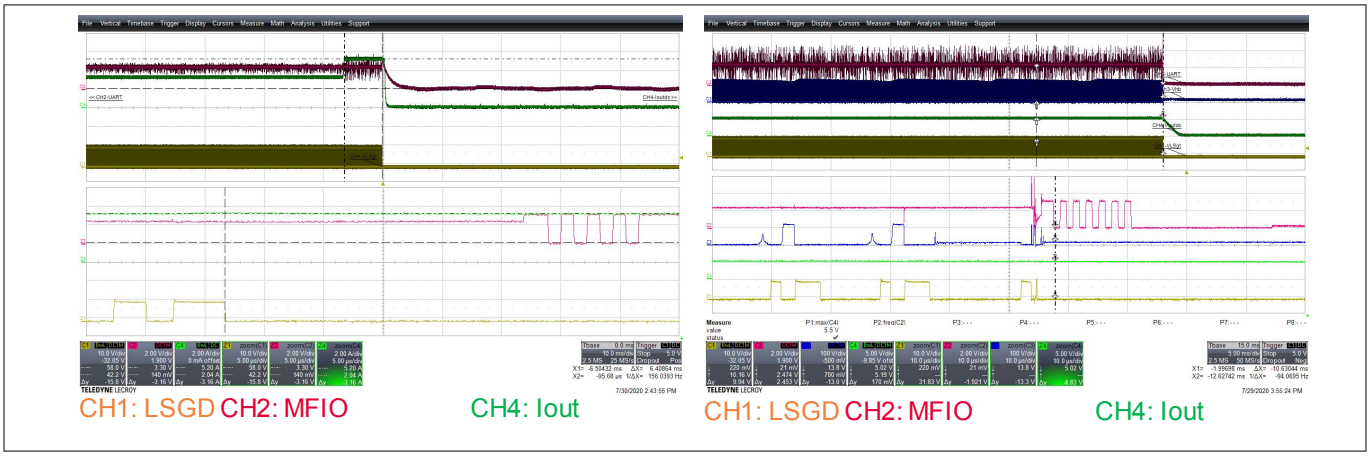


**Figure 59 OCP1 max (left) and OCP2 (right) at 90 $V_{AC}$**

Here, OCP2 is provoked by a direct short circuit at the secondary winding terminals on the board.

OCP1 will be triggered once a heavy load occurs during the normal operation. However, with the same root-cause but at other operating conditions, other protections may be triggered, for example, at start-up with the load current set to 10 A (***Figure 60***) or the shorted output before start-up. The start-up with heavy load causes no ZCD signal detectable within the given maximal HB switching cycles $N_{HBcyclemax}$ during the start-up process. The protection "no ZCD signal detected" is triggered, but not OCP1.

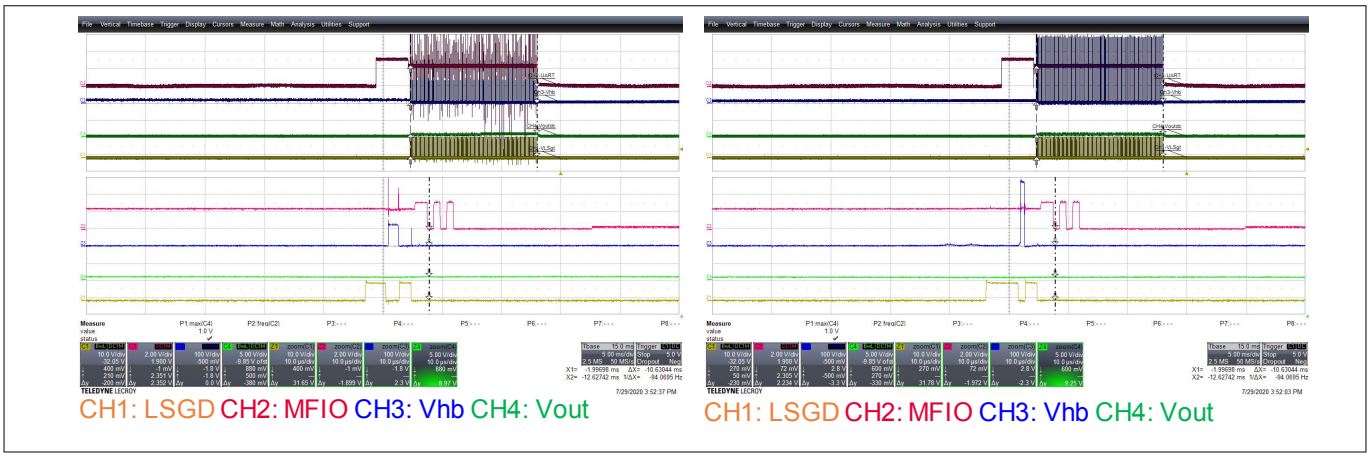


**Figure 60 Cold start-up with 10 A load current setting at 90 $V_{AC}$ (left) and 264 $V_{AC}$ (right)**

The controller XDPS2201 protects the system against possible serious failure on the board. In case of a shorted secondary winding, this failure can be detected by OCP2 anytime during its operation (***Figure 61***). In another case of shorted shunt resistor R14 or R15, this failure will be protected by the measured maximal on-time of the HS gate at system start-up (***Figure 62***).

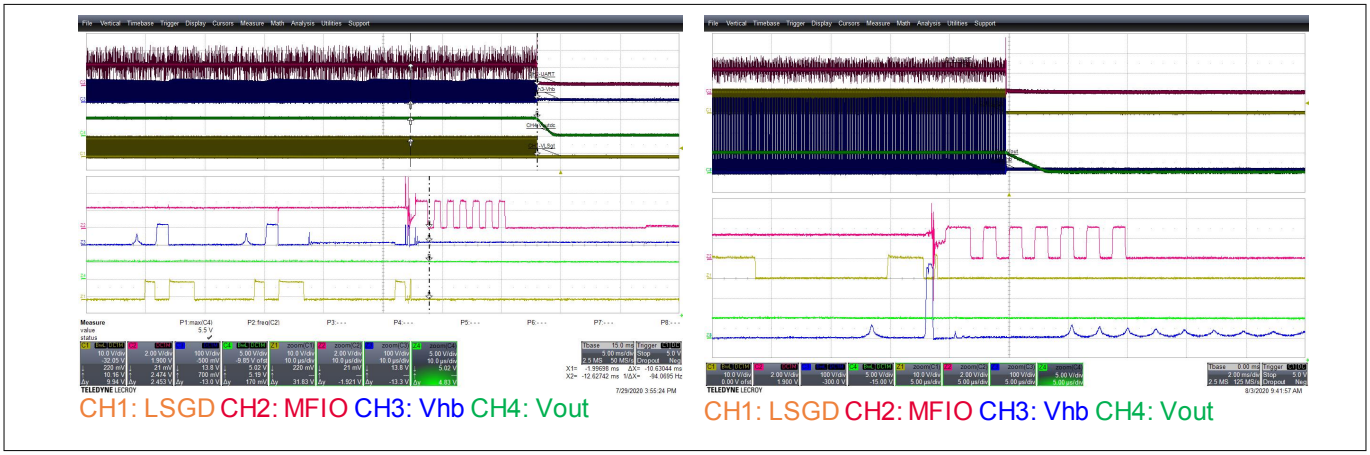


**Figure 61 OCP2 from secondary side winding terminals shorted during normal operation at 90 V (left) and 264 V (right)**

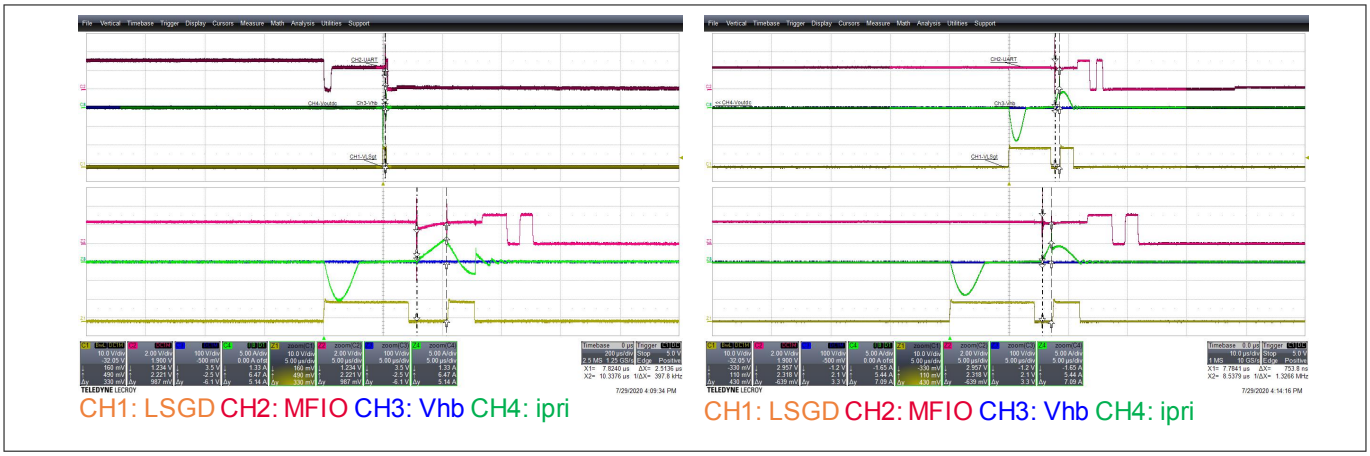


**Figure 62 Shorted shunt ad 90 $V_{AC}$ (left) and 264 $V_{AC}$ (right)**

Here, the maximal HS gate on-time, based on the configuration data, is elapsed before the HS switch is turned off by the current sensing signal, that is, 0 V with shorted shunt resistors. This failure will be detected by the maximal on-time check of the high-side gate pulse width.

### Output overvoltage protection (OVP)

To provoke an output overvoltage, the IC feedback pin of XDPS2201 is shorted to ground during its operation. For this test, the load is connected to the main stage output.

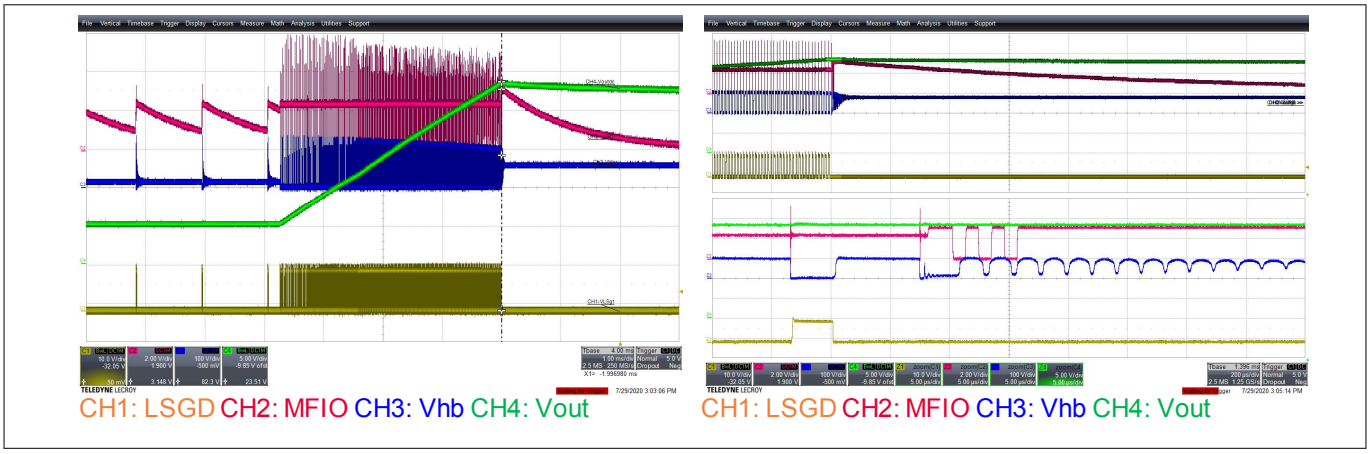


**Figure 63 Output overvoltage triggered at 90 $V_{AC}$, and 5 V and 0 A output**

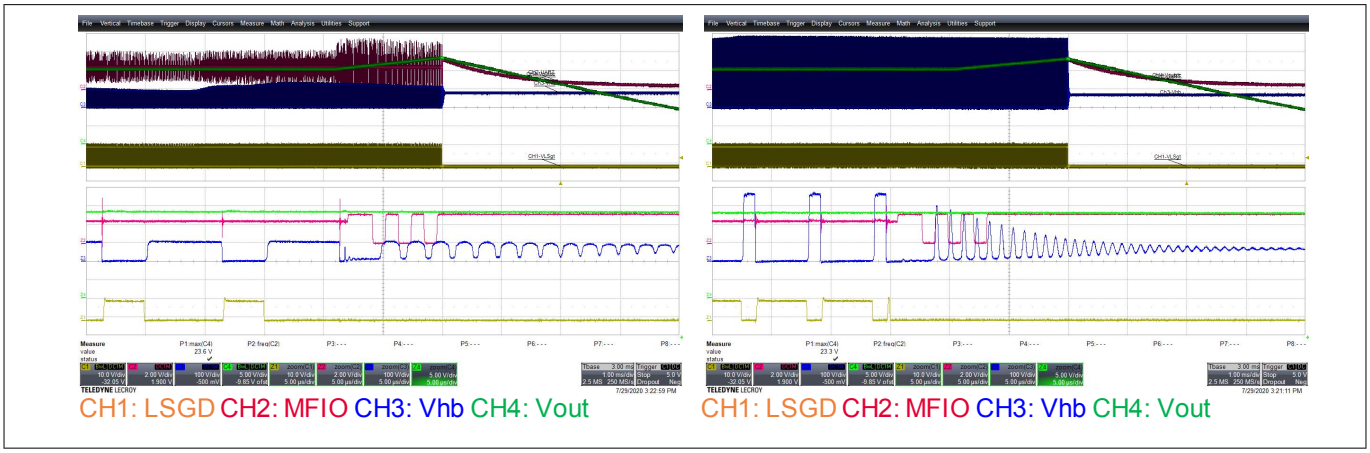


**Figure 64 Output OVP triggered at output of 20 V/3.25 A and 90 V (left) and 264 V (right) input**

### Overtemperature protection (OTP)

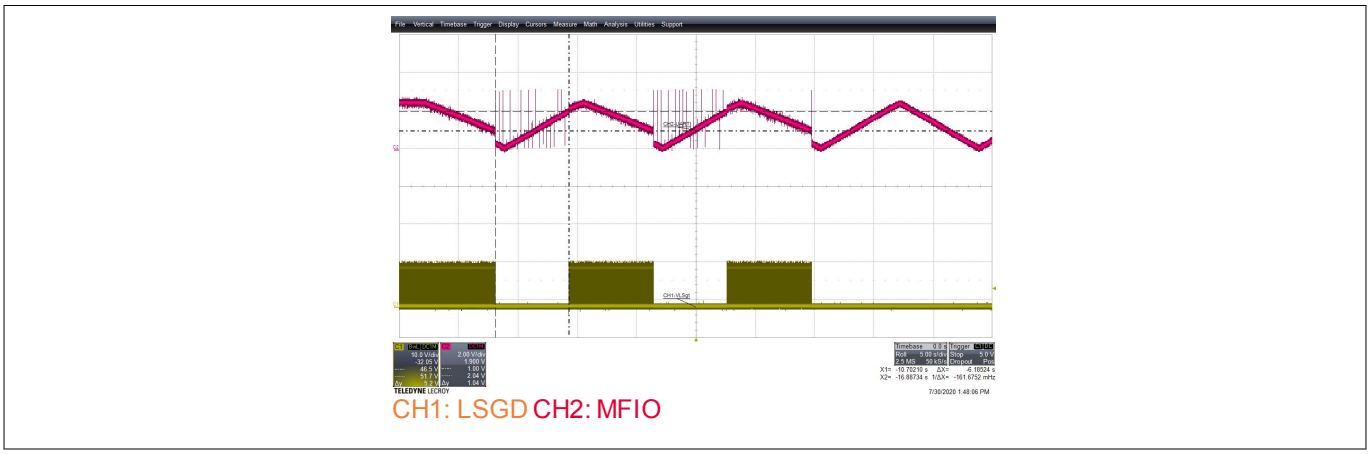


**Figure 65 OTP with emulated signal at the MFIO pin**

## 3 Measurement results

Currently, there is no NTC assembled on the board. The signal at the MFIO pin (CH2, pink) is emulated by a signal generator for demonstrating the functionality of the external OTP while the IC operation is indicated b ythe gate signal of the switch Q2 (CH1, yellow). A higher voltage at the MFIO means a lower temperature of NTC. Once the temperature is low enough (with high MFIO pin voltage), IC starts its operation. Once the tem perature is high enough (with low MFIO pin voltage), IC stops its operation. The hysteresis for the trigger and release of OTP ensures a reliable overtemperature protection.

# 4 Summary

This document comprises the design specifications, information about the board and components, and key measurement results of the high power density board using the HFB controller XDPS2201 and the USB-PD controller CYPD3174.

# 5 References

1. XDPS2201 data sheet: XDPS2201_DS_R1.1.pdf
2. http://www.cypress.com/part/cypd3174-24lqxq
3. XDPS2201 design guide: Hybrid-flyback_converter_design_with_XDPS2201.pdf
4. XDPS2201 design sheet: XDPS2201_HybridFlyback_PaperDesign_V1.0.xlsx

# 6 Change history

**Table 6 Change history**

| Date | Revision | Changes |
|---|---|---|
| 2021.04.21 | V1.0 | Initial Release |

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