EZ-PD™ PAG2S-QZ integrated USB PD and secondary-side QR-ZVS controller

General description

EZ-PD™ PAG2S-QZ CYPAS211 is an integrated secondary-side PWM controller and USB Power Delivery (USB PD) controller, PAG2S-QZ integrates secondary side synchronous rectifier (SR), pulse-width modulator (PWM) and zero voltage switching (ZVS) control. PAG2S-QZ is targeted towards USB-C power adapters; it fits well into high-efficiency AC-DC flyback designs with USB PD, Qualcomm Quick Charge, and other standard charging protocols. PAG2S-QZ CYPAS211 also supports USB PD Extended Power Range (EPR) mode.

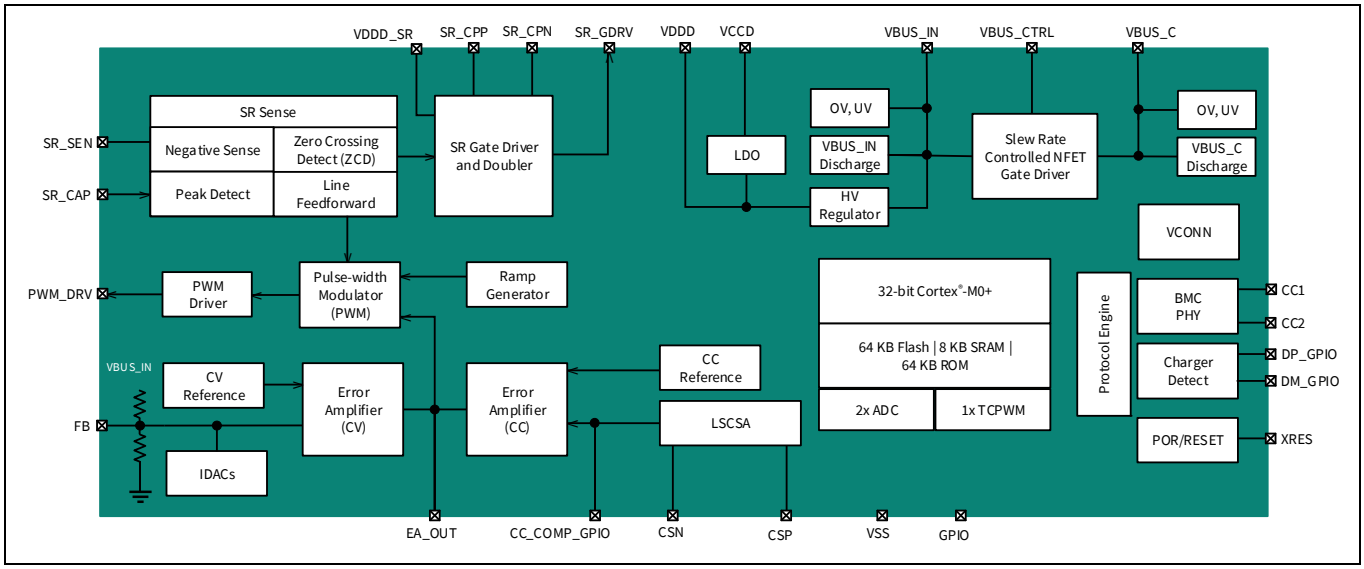
Applications

- USB-C chargers and adapters
- USB-C chargers and adapters with EPR
- Power adapters supporting both USB PD and legacy charging

Features

- Integrated secondary-side flyback controller and charging port controller
- Integrates secondary side synchronous rectifier (SR), PWM control with ZVS support
- Supports synchronous rectification in quasi-resonant (QR) or critical conduction mode (CrCM), valley switching, discontinuous conduction mode (DCM), and continuous conduction mode (CCM) and supports switching frequency up to 300 kHz
- Supports burst mode for light load operations
- SR driver works with both standard MOSFET and logic level MOSFET
- USB PD 3.1 compliant with EPR support of up to 28V VBUS
- Supports USB PD 2.0, PD 3.0 with Programmable Power Supply (PPS), QC5.0, QC4+, QC 4.0, QC 3.0, QC 2.0, Samsung AFC, Apple Charging, and BC v1.2 charging protocols
- Integrates low-side current sense amplifier (LSCSA), 2x VBUS discharge FETs, and an NFET gate driver to drive the load switch and VCONN FETs to support EMCA cables
- Configurable VBUS overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), short-circuit protection (SCP), and system overtemperature protection (OTP)
- Protects against accidental VBUS to CC short; electrostatic discharge (ESD) protection on CC, VBUS, and DP/DM lines and overvoltage on DP/DM lines
- Integrates a 32-bit Cortex®-M0+ with 64-KB flash, 8-KB SRAM, and 64-KB ROM
- 32-pin QFN package with –40°C to +150°C junction temperature range

Functional block diagram



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1 Application overview

1.1 USB PD adapter – Secondary-side flyback control

Figure 1 shows a power adapter application diagram implementing a secondary-side controlled synchronous flyback system. In this system, EZ-PD™ PAG2S-QZ modulates the pulse width of the primary MOSFET in voltage control mode. PAG2S-QZ engages the internal error amplifier (EA) and a programmable ramp generator to determine the pulse width of the PWM. This PWM signal is transferred from the secondary to the primary side through a pulse edge transformer. In this topology, PAG2S-QZ integrates three key features: secondary-side PWM control, charging protocol control, and fault protection. In the following example, EZ-PD™ PAG2P is used as the primary controller with PAG2S-QZ.

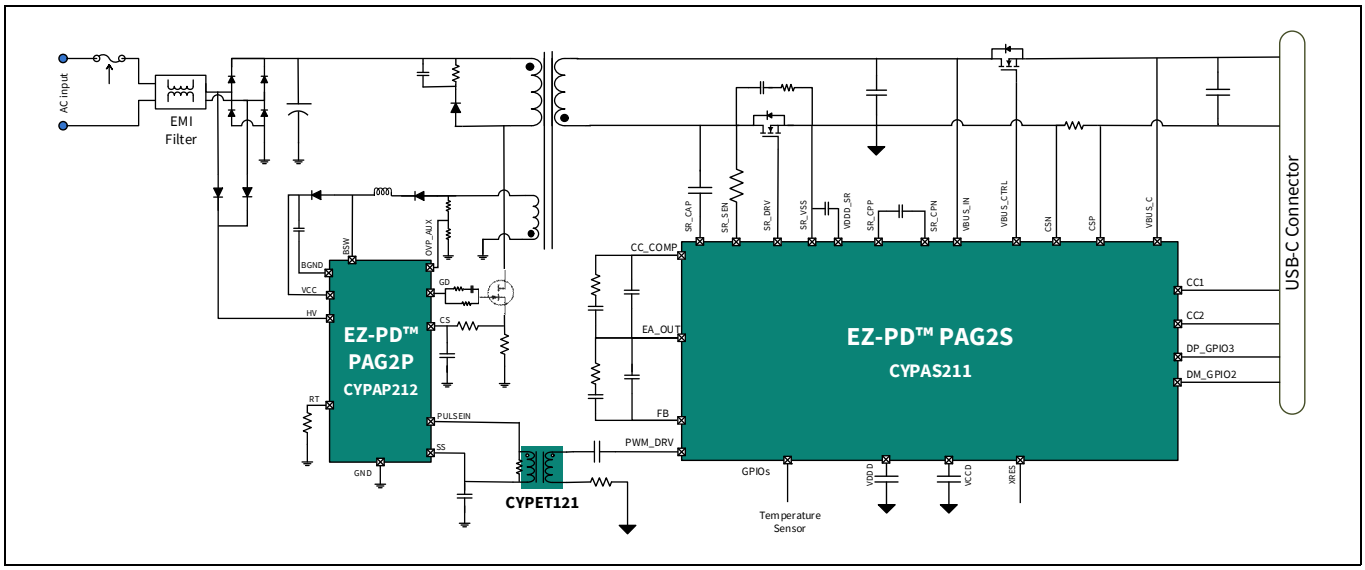


Figure 1 USB PD adapter with secondary-side flyback control

2 Pinouts

2.1 Pin definitions

Table 1 32-pin QFN pin description

Sl.#	Pin name	Pin description
1	VCCD	1.8-V core voltage LDO output
2	VDDD	3.0-V to 5.5-V internal LDO output
3	VSS	Ground
4	VDDD_SR	V_{DDD} supply for sync rectifier driver
5	SR_CPN	Synchronous rectification doubler capacitor negative pin
6	SR_CPP	Synchronous rectification doubler capacitor positive pin
7	VSS_SR	Ground for synchronous rectifier driver
8	SR_GDRV	Synchronous rectifier NFET gate driver
9	SR_SEN	Synchronous rectifier NFET drain terminal sensing
10	SR_CAP	Synchronous rectifier NFET drain sensing for resonance frequency > 4 MHz
11	PWM_DRV	Pulse-edge transformer driver
12	GPIO0	GPIO
13	GPIO1	
14	DM_GPIO2	USB D–/GPIO/SWD_DAT
15	DP_GPIO3	USB D+/GPIO/SWD_DAT
16	GPIO4	Not connected
17	XRES	External reset input
18	GPIO5	GPIO
19	GPIO6	GPIO/TCPWM
20	GPIO7	GPIO
21	CC2	Power Delivery Communication Channel 2
22	CC1	Power Delivery Communication Channel 1
23	CSN	Low-side current sense amplifier negative input
24	CSP	Low-side current sense amplifier positive input
25	VBUS_C	USB Type-C VBUS monitor input
26	VBUS_CTRL	Load switch NFET gate control
27	EA_OUT	EA output
28	FB	EA feedback
29	CC_COMP_GPIO8	Pin for constant current mode compensation capacitor/GPIO/TCPWM
30	CC_COMP_GPIO9	
31	VSS	Ground
32	VBUS_IN	3.3-V to 30-V power source input for regulator

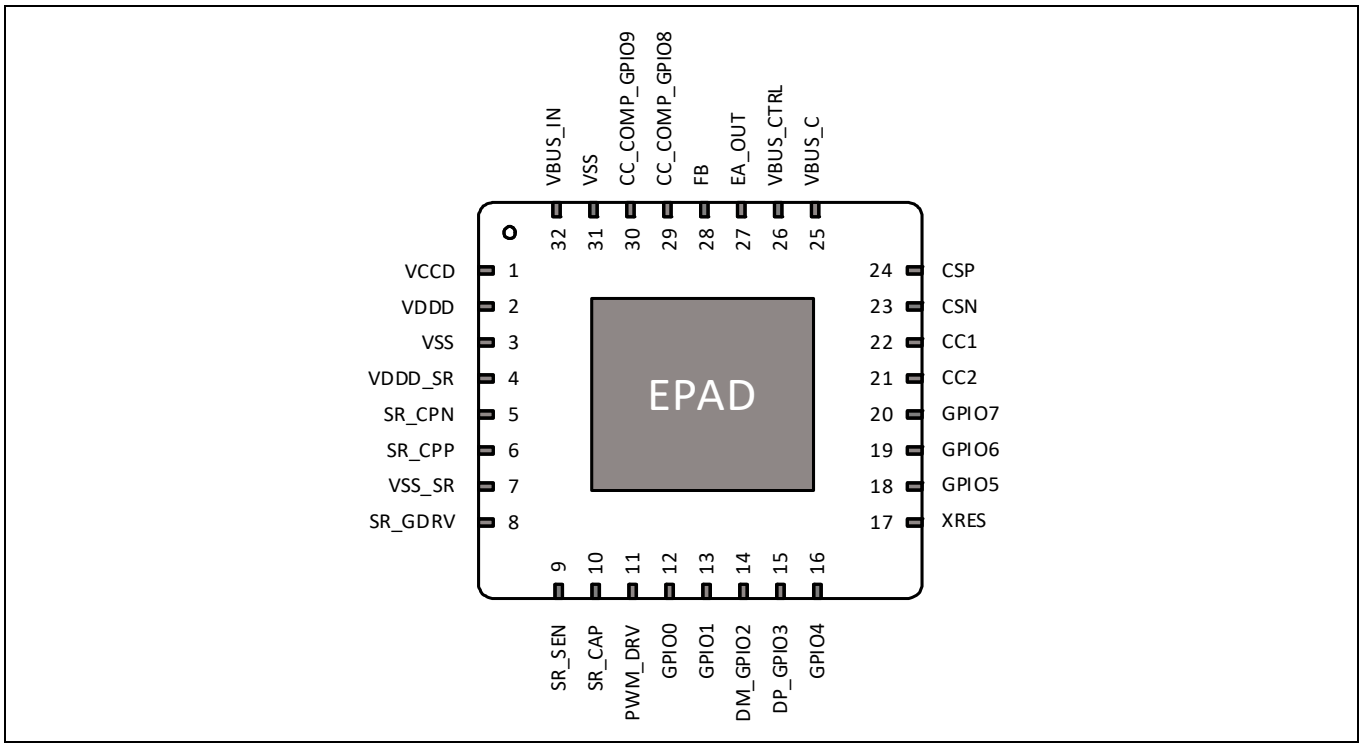


Figure 2 32-pin QFN pin map

2.2 Pin description

2.2.1 SR_GDRV, SR_VSS, SR_SEN, SR_CPP, SR_CPN, SR_CAP

EZ-PD™ PAG2S-QZ senses the voltage across the synchronous rectifier NFET and appropriately controls the gate driver to achieve optimum efficiency. It supports both standard NFET and logic-level NFET. PAG2S-QZ supports synchronous rectification in QR/CrCM, valley switching, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The SR sense block supports negative sense detect and ZCD. For solution having resonance frequency on SR_DRAIN > 4 MHz, peak-detect is sensed via the SR_CAP pin by coupling SR_DRAIN to SR_CAP via a 10-pF capacitor. If resonance frequency < 4 MHz, SR_CAP in must be left floating.

The gate driver (SR_GDRV) can be driven to internal VDDD or twice the VDDD to achieve lower $R_{DS(ON)}$ of the external NFET. The gate driver can be driven to twice the VDDD using an internal doubler circuit, with the doubler capacitor connected across the SR_CPP and SR_CPN pins. The source terminal of the SR FET must be connected to the SR_VSS pin. The voltage at the drain node of the external NFET is sensed via SR_SEN using a resistive divider.

2.2.2 FB, EA_OUT, CC_COMP_GPIOx

PAG2S-QZ integrates two error amplifier blocks which handle secondary-output sensing and regulation for both constant voltage and constant current modes of operation. The error-amplifier output feeds into the internal analog PWM block. The negative input of the error amplifier is the feedback (FB) pin and the positive input is an internal voltage reference. Based on the desired VBUS output, the voltage at the FB pin will be changed using internal current source/sink IDACs. An external compensation network is required between the FB and EA_OUT pins, as shown in the application diagram (see **Figure 1**). Constant current operation makes use of an internal LSCSA, the output of which feeds into an independent error amplifier as shown in functional block diagram. Constant current mode regulation requires an external compensation network between CC_COMP_GPIOx and EA_OUT as shown in **Figure 1**.

2.2.3 PWM_DRV

PAG2S-QZ supports an analog PWM generator, which modulates the pulse width of the primary-side FET in voltage control mode. It generates a programmable ramp which is compared against the output of the error amplifier to determine the PWM pulse width. The ramp is generated by sourcing current into an internal capacitor; the source current is a programmable combination of a certain fixed current and the feed-forward current. The PWM signal is transferred from the secondary side to the primary side through an external pulse edge transformer.

2.2.4 VBUS_IN, VDDD, VCCD

PAG2S-QZ integrates a high-voltage regulator, which is powered from the VBUS_IN rail, the output of the regulator powers the VDDD rail. The input to the regulator can range from 3.3-V minimum to 30-V maximum. This regulator is intended to deliver PAG2S-QZ current consumption and is not expected to drive any external loads or ICs. PAG2S-QZ also has an internal configurable discharge path for the VBUS_IN rail, which is used to discharge the VBUS rail during negative voltage transitions. The discharge resistor strength is configurable through firmware settings.

The regulated VDDD supply, is either used to directly power some internal analog blocks or further regulated down to 1.8-V VCCD, which powers the majority of the core. VDDD and VCCD are brought out on to pins to connect external capacitors for regulator stability; these are not meant to be used as power supplies.

2.2.5 VBUS_C, VBUS_CTRL

VBUS_C is used to monitor the voltage at the Type-C connector. VBUS_C has an internal configurable discharge path, which is used to discharge the VBUS_C rail during negative voltage transitions. The discharge resistor strength is configurable through firmware settings. The load switch is between VBUS_IN and VBUS_C. PAG2S-QZ integrates an NFET gate driver to control this load switch. VBUS_CTRL is the output of this gate driver. There is an optional slow turn-on feature which is meant to avoid sudden in-rush current.

2.2.6 CSP, CSN

PAG2S-QZ integrates a LSCSA to monitor the load current. CSP is the positive input pin for the LSCSA and CSN is the negative input. Suggested Rsense for LSCSA is 5 mΩ.

2.2.7 CC1, CC2

CC1 and CC2 are the communication channels for USB PD protocol. PAG2S-QZ integrates a USB PD transceiver consisting of a transmitter (TX) and receiver (RX) that communicate Biphase Mark Code (BMC)-encoded data over the Configuration Channel (CC) channels as per the USB PD standard. All communication is half-duplex. The physical layer implements collision avoidance to minimize communication errors on the channel. This block includes all termination resistors (Rp) and their switches as required by the USB PD specification.

To support active cable applications, PAG2S-QZ also integrates VCONN FETs to power the CC lines. An external 390-pF capacitor is required on both the CC1 and CC2 pins.

2.2.8 DP_GPIOx, DM_GPIOx

The DP and DM lines are the standard USB D+ and D- lines. PAG2S-QZ integrates a charge detect block, which handles legacy charging protocols such as BC 1.2, Quick Charge, Apple Charging, and Samsung AFC. This block integrates all the terminations required for these charging protocols; no external components are required. When legacy charging is not required in the system, the same DP and DM lines can be re-used as standard GPIOs. The charger detect block also supports impedance detection on DP/DM lines.

2.2.9 GPIOx, XRES

PAG2S-QZ has multiple GPIOs, out of which some are dedicated GPIOs and the rest are multiplexed with other functionalities. These GPIOs support multiple drive modes and configurable threshold options. During power-on and reset, the GPIOs are forced to the tristate so as not to crowbar any inputs and/or cause excess turn-on current.

The XRES pin can be used to initiate a reset; this pin is internally pulled HIGH and must be pulled LOW externally to trigger a reset.

3 Functional description

3.1 System start-up

On power-up, the primary side start-up controller must start controlling the primary switch using its soft start mechanism and provide sufficient current to charge the secondary-side output capacitor and the start-up current required for EZ-PD™ PAG2S-QZ. The secondary output voltage is the input power supply source of PAG2S-QZ. Once VBUS_IN voltage exceeds 3.3-V, PAG2S-QZ firmware will boot up and take control of the primary switch. The PAG2S-QZ firmware boot up time is in the order of a few milliseconds.

Once the boot-up is complete, the firmware configures the error-amplifier to achieve the 5-V secondary output and PAG2S-QZ will generate the PWM pulses accordingly. These pulses on PWM_DRV are coupled to the primary start-up controller through a pulse transformer. On receiving the PWM pulses, the primary side start-up controller is expected to synchronize its internal oscillator with the PWM pulses and switch from start-up mode to secondary control mode. In secondary control mode, the primary switch is directly controlled by the PWM pulses generated by PAG2S-QZ.

3.2 Modes of operation - SR

PAG2S-QZ supports synchronous rectification (SR) in both DCM and CCM modes. The SR sense block supports negative sense detect and ZCD. **Figure 3** through **Figure 5** show the SR_GDRV functionality in QR/CrCM, valley switching, and CCM modes. The SR controller has a turn-on propagation delay of 40 ns (typ) and a turn-off propagation delay of 25 ns (typ).

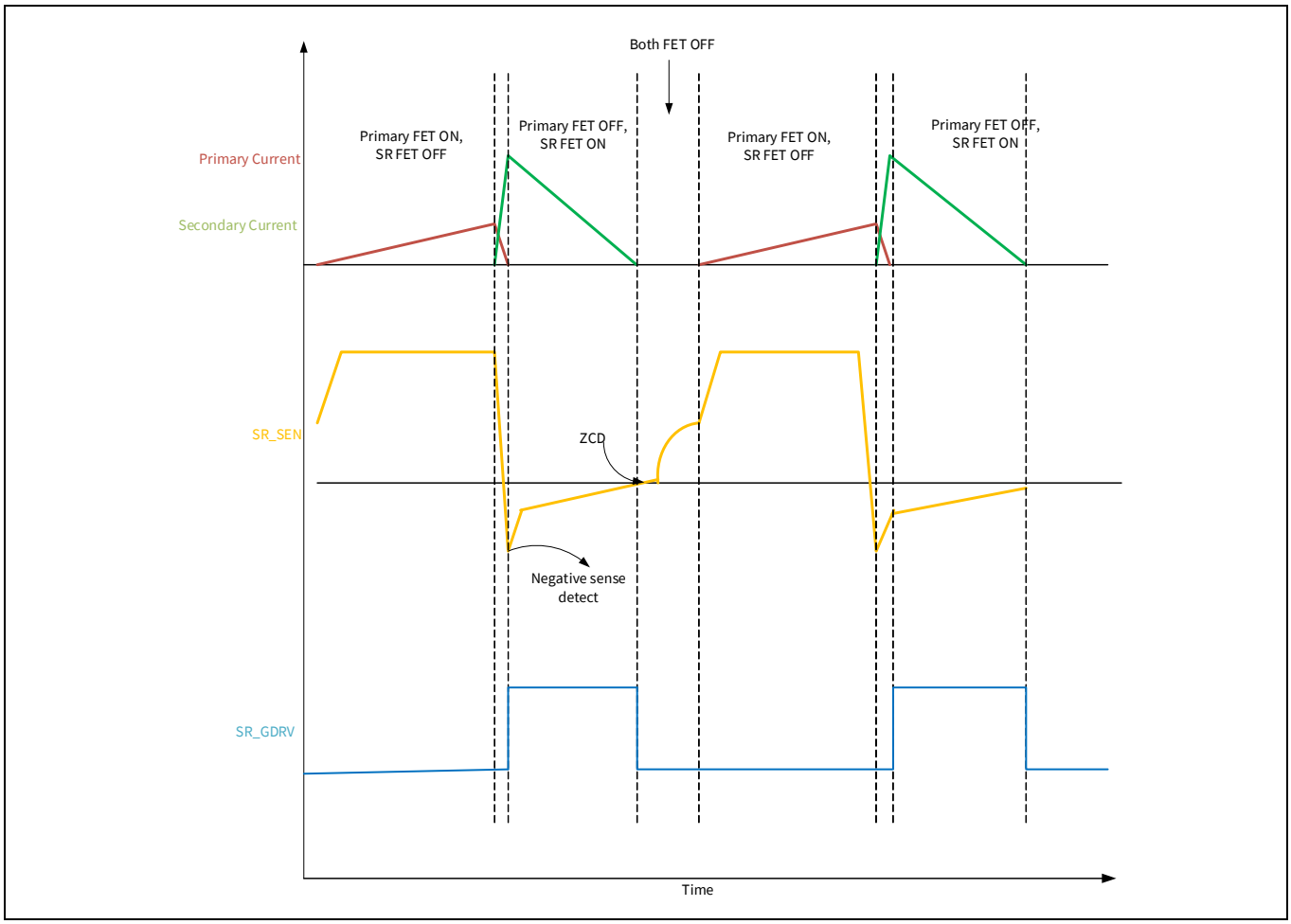


Figure 3 SR_SEN and SR_GDRV in QR/CrCM mode

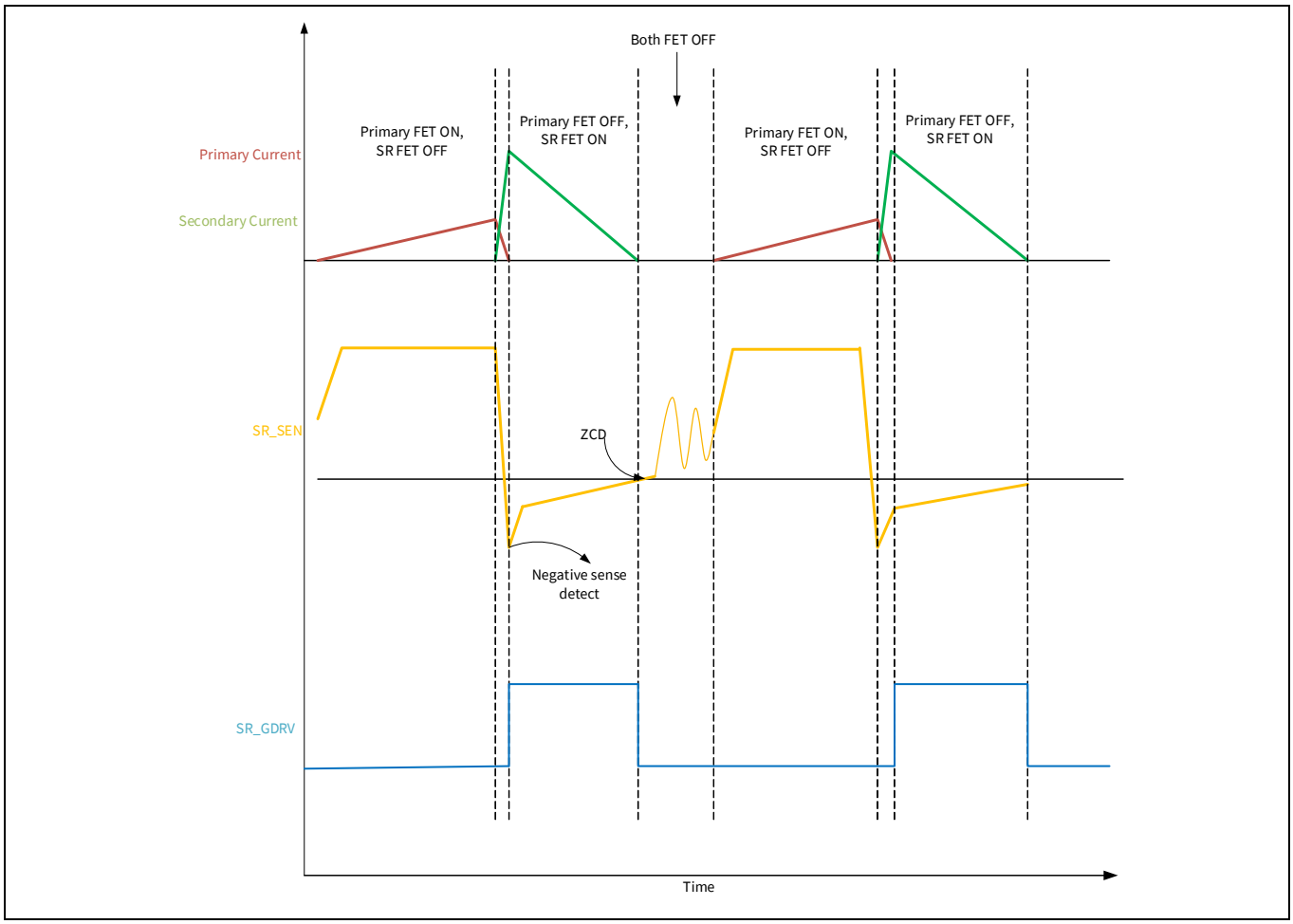


Figure 4 SR_SEN and SR_GDRV in DCM/valley switching mode

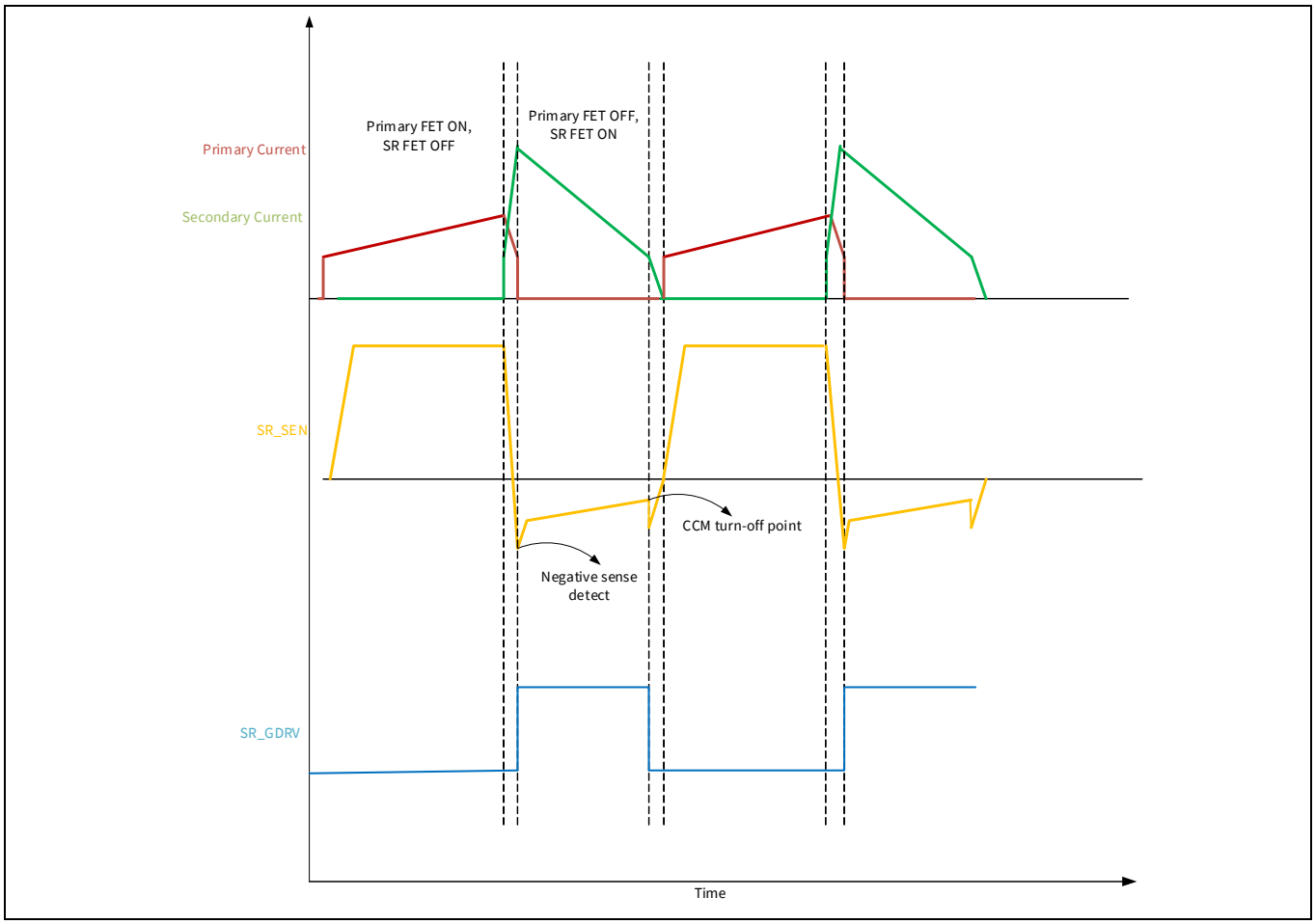


Figure 5 SR_SEN and SR_GDRV in CCM mode

The voltage at the drain node of the external NFET is sensed on the SR_SEN pin connected via an external resistor. The external resistor is required to restrict the voltage at the SR_SEN pin below 34 V. The external resistance on the SR_SEN pin depends on the turns ratio of the power transformer. **Table 2** provides the external resistor values required for different turns ratios.

Table 2 External resistance on SR_SEN vs. turns ratio

Primary: Secondary turns ratio	Rext (Ω)
3:1	20k
4:1	20k
5:1	20k
6:1	12k
7:1	12k
8:1	12k
9:1	12k
10:1	12k
11:1	12k
12:1	12k
13:1	12k
14:1	12k
15:1	12k

3.3 Modes of operation - PWM and ZVS

PAG2S-QZ supports multiple modes of operation: QR or CrCM, valley switching, DCM, CCM, and burst mode for light load operations. Firmware allows configurability for minimum/maximum pulse width, minimum/maximum period and pulse skip or burst levels. **Figure 6** through **Figure 8** show the PWM_DRV functionality in QR/CrCM, valley switching, and CCM modes.

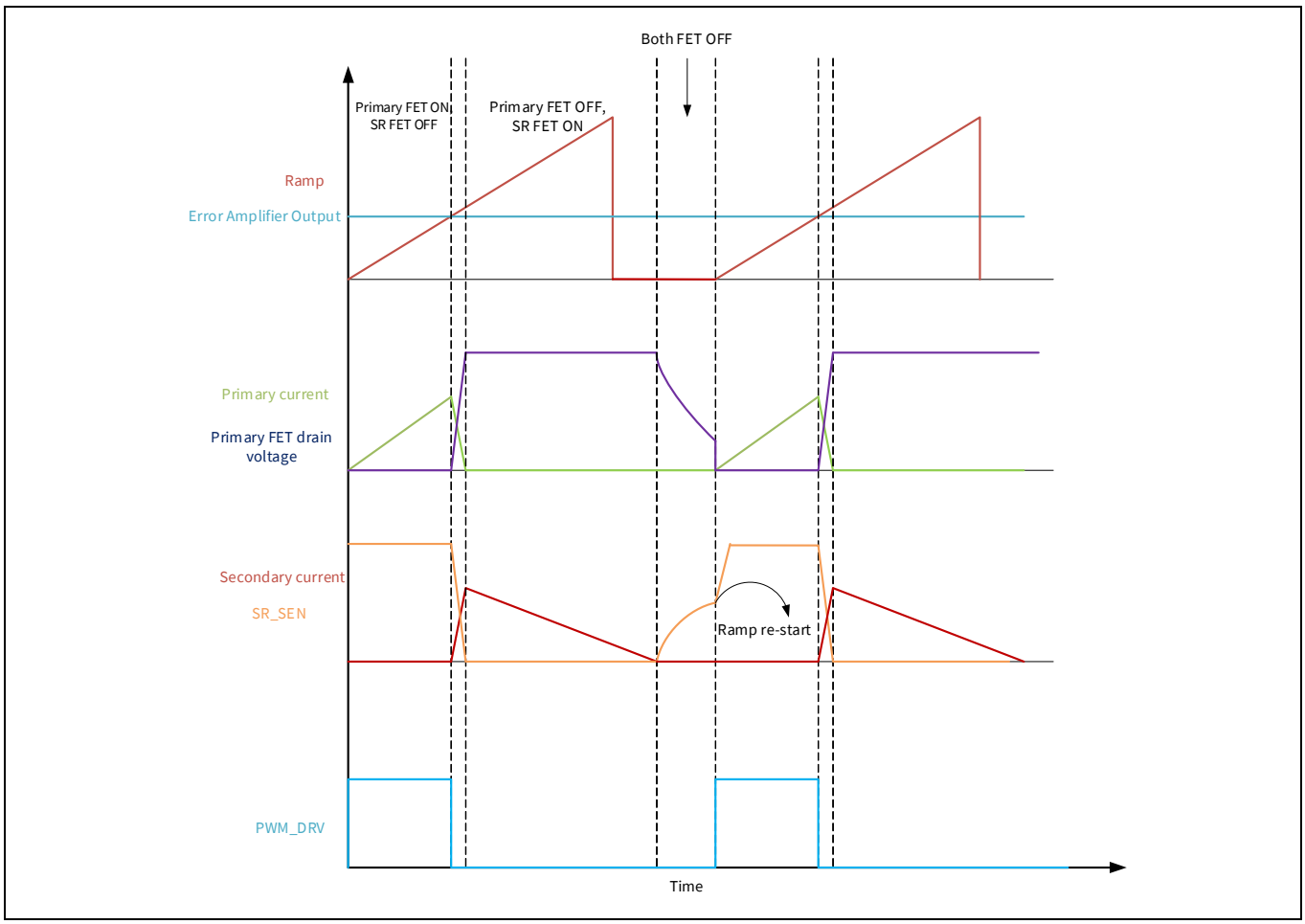


Figure 6 PWM_DRV in QR/CrCM mode

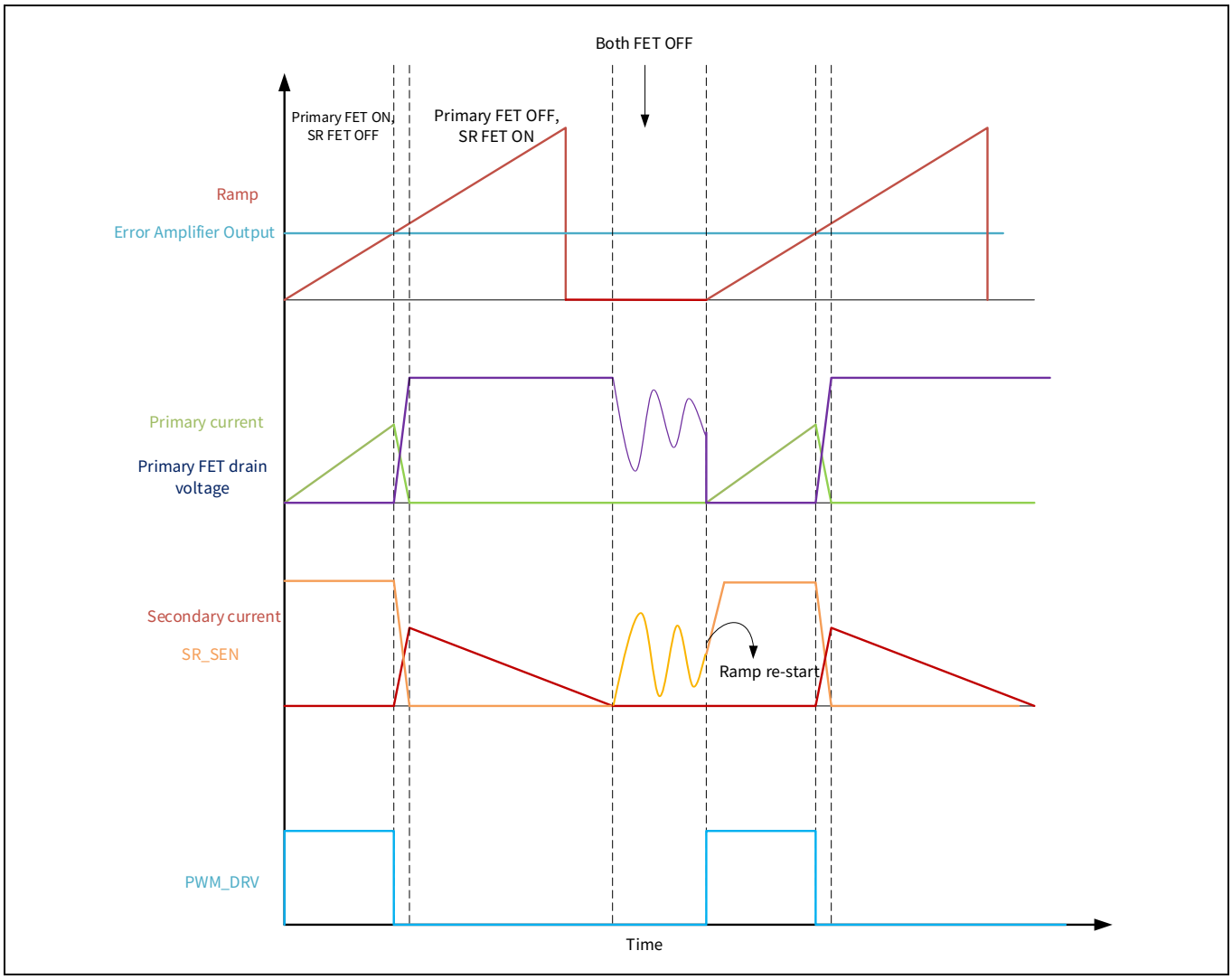


Figure 7 PWM_DRV in DCM/valley switching mode

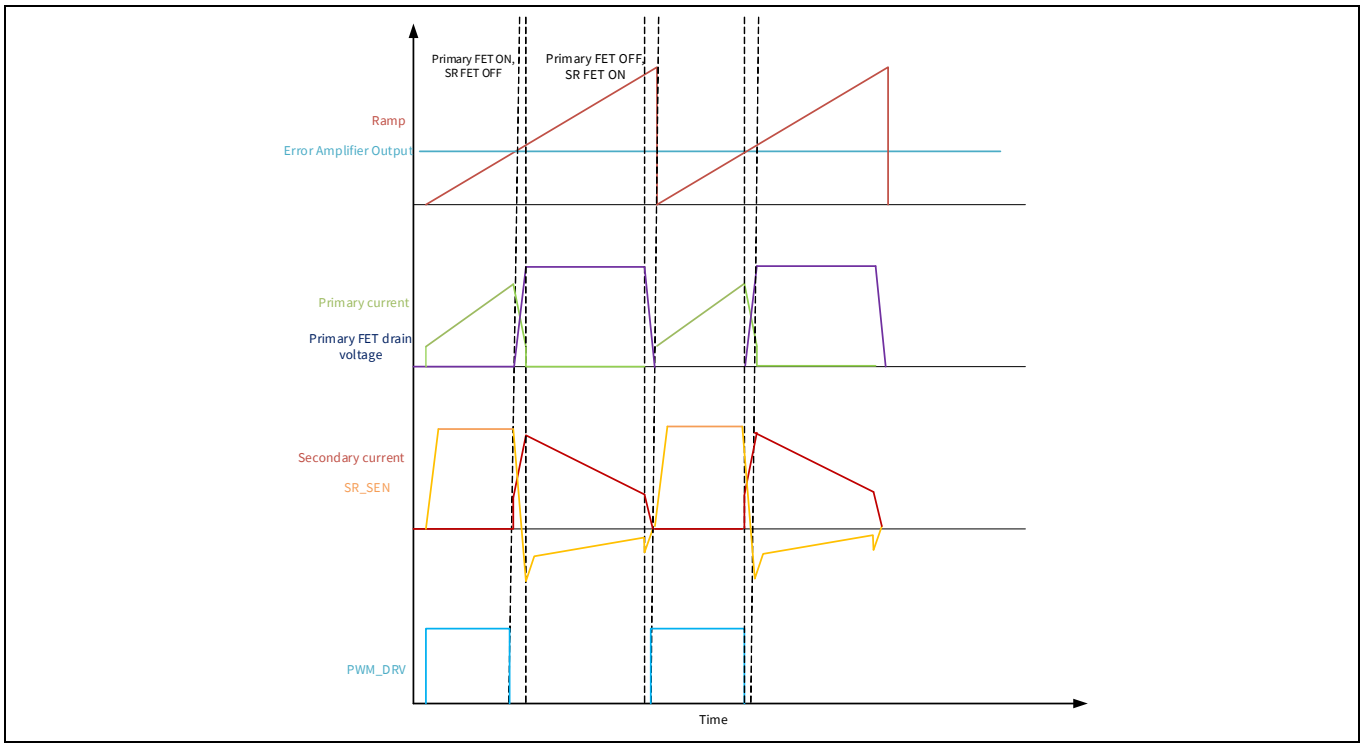


Figure 8 PWM_DRV in CCM mode

PAG2S-QZ also supports zero voltage switching where in it turns on the SR_GDRV for a short duration before driving PWM_DRV, as shown in **Figure 9**. This is meant to pull the primary drain voltage low, thereby ensuring zero voltage switching. ZVS pulse width is firmware configurable, thereby enabling optimization for each design.

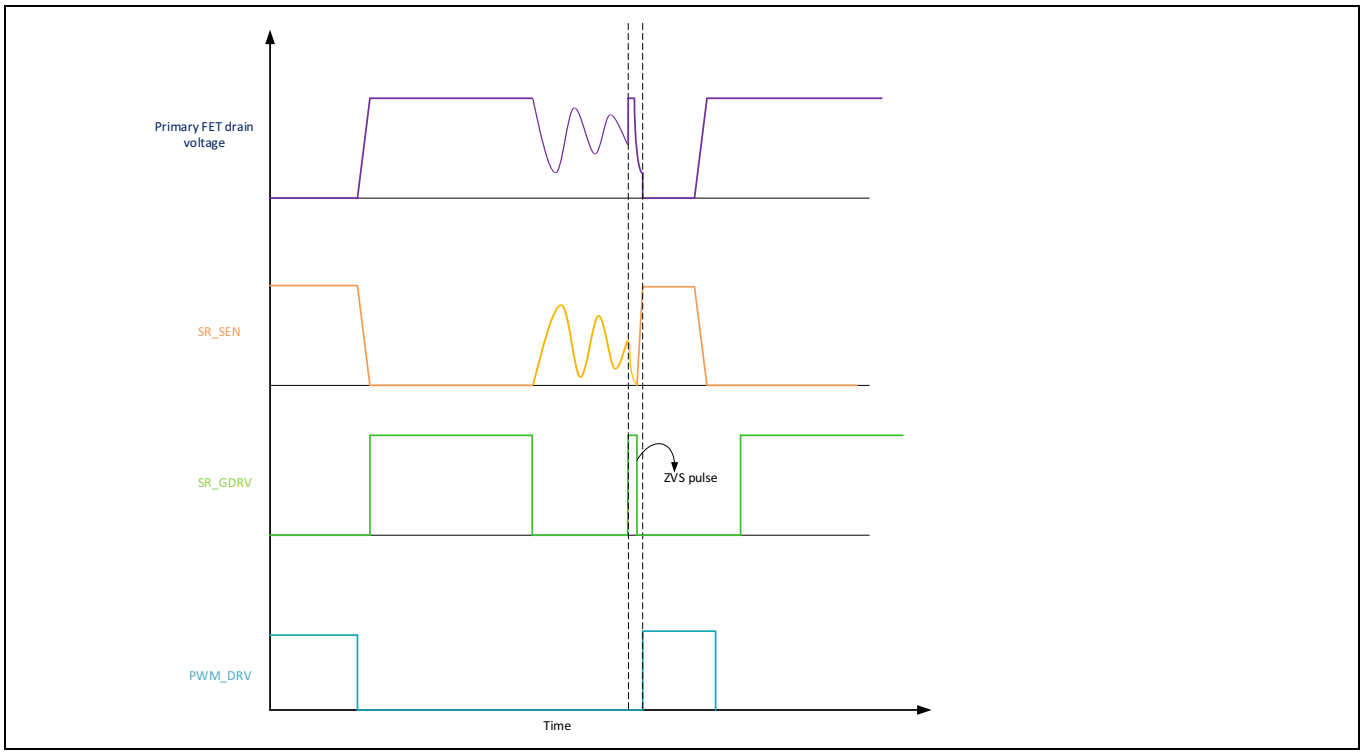


Figure 9 ZVS in DCM mode

Analog PWM smart algorithm allows the operation to automatically transition between modes based on the output power requirement. The mode of operation stays in CrCM for higher loads, moves to DCM for medium loads, and switches to skip mode or burst mode for low and ultra-low power loads (see **Figure 10**).

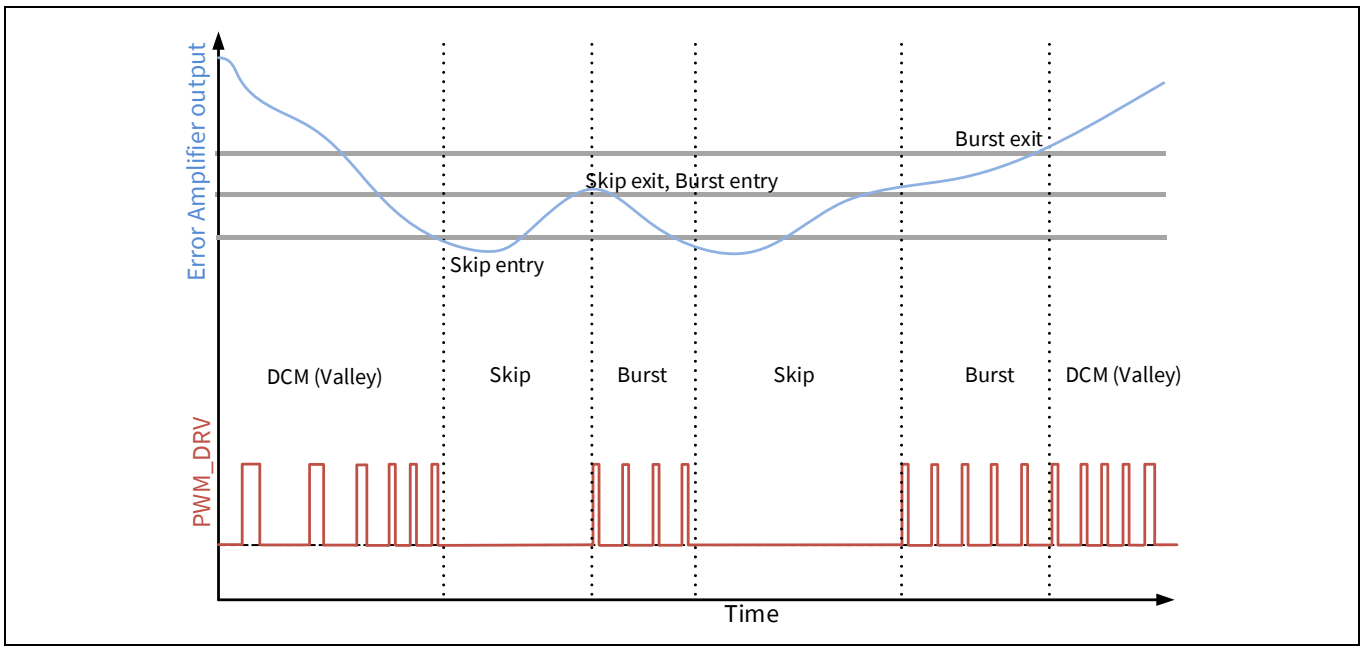


Figure 10 Error amplifier output vs modes of operation

3.4 Fault protection

3.4.1 VBUS OVP, UVP, OCP, and SCP

VBUS undervoltage and overvoltage faults are monitored using internal VBUS_IN/VBUS_C resistor dividers. VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers (CSA). The fault thresholds and response mechanisms are firmware-configurable.

3.4.2 Overtemperature protection

Over-temperature monitoring is done using an external thermistor and internal ADC. The thermistor can be connected to any free GPIO. PAG2S-QZ has an integrated 8-bit SAR ADC, which is available for general purpose analog-to-digital conversions. The fault thresholds and response mechanisms are firmware-configurable.

3.4.3 ESD, CC OVP, and DP/DM OVP

PAG2S-QZ offers ESD protection on all pins. Further, the chip integrates protection against accidental short of CC pins to the high-voltage VBUS_C rail and also protects against overvoltage on DP/DM pins.

3.5 Power modes

PAG2S-QZ supports multiple power modes - Active, Sleep, and Deep Sleep. Transitions between these modes is handled by the application firmware depending on the operating conditions.

3.6 MCU subsystem

PAG2S-QZ integrates a 32-bit Cortex®-M0+ MCU with 64-KB flash, 8-KB SRAM, and 64-KB ROM. PAG2S-QZ also supports 1x TCPWM and 2x ADC.

4 Electrical specifications

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit
$V_{BUS\_IN\_MAX}$	Maximum input supply voltage	–0.3	–	34	V
V_{DDD_MAX}	V_{DDD} supply voltage	–		6	
V_SR_DRAIN_MAX	Voltage on SR_SEN pin			34	
$V_{CC\_PIN\_ABS}$	Voltage on CC1, CC2 pins				
V_{GPIO_ABS}	GPIO voltage	–0.5		V_{DDD} + 0.5	
I_{GPIO_ABS}	Current per GPIO	–		25	mA
I_LU	Pin current for latch-up	–100		100	
ESD_HBM	Electrostatic discharge human body model	–		2000	V
ESD_CDM	ESD charged device model			500	

4.2 Device-level specifications

Table 4 Device-level specifications

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
Memory size						
FLASH_SIZE	Flash memory size	–	64	–	KB	SONOS flash amount (bytes)
SRAM_SIZE	SRAM memory size		8			SRAM amount (bytes)
SROM_SIZE	SROM memory size		64			
Silicon power						
V_{DDD_REG}	VDDD output with VBUS 5.5 V–30 V	4.6	5	5.4	V	–
V_{DDD_MIN}	VDDD output with VBUS 3.15 V–5.5 V	VBUS – 0.33	–	–		
V_{BUS_IN}	Power supply input voltage	3.15		30.0		
V_{CCD}	Output voltage for core logic	–	1.8	–		
$V_{DDWRITE}$	Supply voltage for flash write	3	–	5.5		
C_{EFC}	External regulator voltage bypass for V_{CCD}	80	100	120	nF	X5R ceramic or better
C_{EXC}	Power supply capacitor for V_{DDD}	4	4.7	–	µF	
C_{EXV}	Power supply decoupling capacitor for V_{BUS_IN}	–	1			
C_{EXCPP}	Capacitor between SR_CPP and SR_CPN pins	0.1	–			
I_{GPIO_ABS}	Current per GPIO	–		25	mA	Absolute maximum

Table 4 Device-level specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
T_{SLEEP}	Wakeup from Sleep mode		0		µs	–
$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode		35			
I_{DD_A}	Active current from V_{BUS_IN} (Type-C attached)		25.0		mA	V_{BUS_IN} = 11 V, T_A = 25°C, CC1/CC2 in Tx or Rx, CPU at 24 MHz, SR/PWM at 100 kHz EA/ADC/CSA/UVOV blocks ON
I_{DD_A1}	Current from V_{BUS_IN} (Type-C attached) in PWM mode	–	13.0	–		V_{BUS_IN} = 28 V, T_A = 25°C, Clock at 24 MHz, SR/PWM at 100 kHz, SR cap = 3 nF, No toggling on CC
I_{DD_A3}	Current from V_{BUS_IN} (Type-C attached) in low-power PWM mode		4			V_{BUS_IN} = 28 V, T_A = 25°C, Clock at 3 MHz, PWM mode, No toggling on CC
$I_{DD\_DS1\_UA}$	Deep Sleep current from V_{BUS_IN} (Type-C unattached) in PWM mode		350		µA	V_{BUS_IN} = 5 V, T_A = 25°C, Type-C unattached, PWM mode, downstream facing port (DFP) mode
L_SEC	Secondary-side inductor	3	–		µH	Secondary-side inductor

4.3 Functional block specifications

Table 5 Functional block specifications

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
Synchronous rectifier						
VCPP1	Voltage doubler output voltage with V_{BUS} = 3.3 V–5.5 V	5	–	–	V	–
VCPP2	Voltage doubler output voltage with V_{BUS} = 5.5 V–30 V	9		11		
TR_SR	Rise time (1 V to V_{OH} – 1 V) of sync-rectifier gate driver output with C_L = 3 nF, including (with and without double bypass mode)	–		75	ns	
TF_SR1	Fall time (V_{OH} – 1 V to 1 V) of sync-rectifier gate driver output with C_L = 3 nF (with doubler mode)		25	50		
TF_SR2	Fall time (V_{OH} – 1 V to 1 V) of sync-rectifier gate driver output with C_L = 3 nF (with doubler bypass mode)		15	30		
VTRIP_NSN_100	Negative sense trip voltage to turn ON secondary switch	50	100	150	mV	
VTRIP_ZCD	Negative sense trip voltage to turn OFF secondary switch	–8	–5	–3		
VTRIP_ZCDF	Trip voltage to turn OFF secondary switch through fast ZCD	0	7	10		
TD_ON	Turn on propagation delay from SR_DRAIN at 100 mV to SR_GDRV reaching 1 V	–	40	80	ns	
IO_SRC_SNK	Output peak current (source and sink)	–	1	–	A	
TR_SR1	Rise time (1 V to V_{OH} – 1 V) of sync-rectifier gate driver output with CL = 3 nF, including (with doubler mode)	–	–	75	ns	
TR_SR2	Rise time (1 V to V_{OH} – 1 V) of sync-rectifier gate driver output with CL = 3 nF, including (with doubler bypass mode)	–	–	30		
PWM						
FSW	Switching frequency	20	–	300	kHz	–
PWM_ON	Minimum controllable ON time	100		–	ns	
V_{OL_PTDR}	Output LOW voltage at the output of pulse-edge transformer driver (I_{Sink} = 8 mA)	–	–	0.5	V	V_{DDD} = 3 V, Iol = 8 mA
GPIO						
I_LU	Latch up current limits	-100	–	100	mA	–
RPU	Pull-up resistor value	3.5	5.6	8.5	kΩ	
RPD	Pull-down resistor value					

Table 5 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3 V V_{DDD}
C_{PIN_A}	Maximum pin capacitance			22	pF	Capacitance on DP, DM pins
C_{PIN}			3	7		All V_{DDD}, all other GPIOs
V_{OH}	Output voltage HIGH level	V_{DDD} – 0.6	–	–	V	Ioh = –4 mA
V_{OL}	Output voltage LOW level	–		0.6		Iol = 10 mA
V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}		–		–
V_{IL_CMOS}	Input voltage LOW threshold	–		0.3 × V_{DDD}		
V_{IH_TTL}	LVTTL input	2		–		
V_{IL_TTL}	LVTTL input	–		0.8		
V_{HYSTTL}	Input hysteresis LVTTL	80	–	–	mV	
$V_{HYSCMOS}$	Input hysteresis CMOS	0.1 × V_{DDD}				
IDIODE	Current through protection diode to V_{DDD}/V_{SS}	–		100.0	µA	
T_{RISEF}	Rise time in Fast Strong mode	1		15	ns	C_{LOAD} = 25 pF
T_{FALLF}	Fall time in Fast Strong mode			15.0		–
T_{RISES}	Rise time in Slow Strong mode	10		70		
T_{FALLS}	Fall time in Slow Strong mode					
F_{GPIO_OUT1}	GPIO F_{OUT}; 2.85 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode.	–	–	28	MHz	–
F_{GPIO_OUT2}	GPIO F_{OUT}; 2.85 V ≤ V_{DDD} ≤ 5.5 V. Slow Strong mode.			6		
F_{GPIO_IN}	GPIO input operating frequency; 2.85 V ≤ V_{DDD} ≤ 5.5 V.			28		
Flash macro						
FLASH_ERASE	Row erase time	–	–	15.5	ms	–
FLASH_WRITE	Row (block) write time (erase and program)			20		
FLASH_DR	Flash data retention	15		–	Years	25°C to 55°C, all V_{DDD}
FLASH_ENPB	Flash write endurance	100K			Cycles	25°C to 85°C, all V_{DDD}
FLASH_ENPB1	Flash write endurance	10K				25°C to 125°C, all V_{DDD}
FLASH_ROW_PGM	Row program time after erase	–		7	ms	–
$T_{BULKERASE}$	Bulk erase time (32 KB)			35		
$T_{DEVPROG}$	Total device program time			7.5	secs	
F_{RET1}	Flash retention, T_A ≤ 55°C, 100k P/E cycles	15		–	Years	–
F_{RET2}	Flash retention, T_A ≤ 85°C, 10k P/E cycles	10				
F_{RET3}	Flash retention, T_A ≤ 105°C, 10k P/E cycles	3				

Table 5 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
SWD						
F_SWDCLK1	All V_{DDD}	–	–	14	MHz	–
T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T		–	ns	
T_SWDI_HOLD						
T_SWDO_VALID		–		0.50 × T		
T_SWDO_HOLD		1		–		
ILO / IMO / POR						
F_{IMO}	IMO frequency	24	36	48	MHz	–
IMO_STL	IMO settling time when the trim register is changed	–	–	200	ns	25°C T_A, all V_{DDD}, 48 MHz ≥ F_{IMO} ≥ 24 MHz
F_{CPU}	CPU input frequency			48	MHz	–
F_{ILO}	ILO frequency	15	40	80	kHz	
SR_POWER_UP	Power supply slew rate during power up	–	–	67	V/ms	
F_{IMOTOL}	Frequency variation at 24 MHz and 48 MHz (trimmed)	–2		2	%	
$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	–
$T_{STARTILO1}$	ILO start-up time			2	ms	
EXTCLKFREQ	External clock input frequency			16	MHz	
EXTCLKDUTY	Duty cycle; measured at V_{DD}/2	45		55	%	
TCLKSWITCH	System clock source switching time	3		4	Periods	
$V_{RISEIPOR}$	Power-on-reset (POR) rising trip voltage	0.72		1.5	V	
$V_{FALLIPOR}$	POR falling trip voltage	0.62		1.4		
VDDD_BOD	Brown-out detect (BOD) trip voltage active/ sleep modes	2.34		3		
VCCD_BOD		1.64		2		
VCCD_BOD_DPSLP		1.1		2		
Timer						
SYS_TIM_RES	Sys timer resolution	–	16	–	bits	–
WDT_RES	WDT resolution		16			
TCPWM						
$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS
T_{PWMEXT}	Output trigger pulse widths	2/Fc		–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
T_{CRES}	Resolution of counter	1/Fc				Minimum time between successive counts
PWM_{RES}	PWM resolution					Minimum pulse width of PWM output

Table 5 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
PD transceiver						
vSwing	Transmitter output HIGH voltage	1.05		1.2	V	
vSwing_low	Transmitter output LOW voltage			0.075		
zDriver	Transmitter output impedance	33		75	Ω	
Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
Idac_1p5a	Source current for 1.5 A @ 5-V advertisement	166		194		
Idac_3a	Source current for 3 A @ 5-V advertisement	304		356		
zOPEN	CC impedance to ground when disabled	108		–	kΩ	
DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15		0.25	V	
DFP_1.5A_0p4	CC voltages on DFP side – 1.5 A	0.35	–	0.5		–
DFP_3A_0p8	CC voltages on DFP side – 3 A	0.75		0.85		
DFP_3A_2p6	CC voltages on DFP side – 3 A	2		2.75		
Vattach_ds	Deep Sleep attach threshold	0.30		0.6	–	
Rattach_ds	Deep Sleep pull-up resistor	10		50	kΩ	
LSCSA DC specifications						
Csa_Acc1	CSA accuracy with 5 mV < Vsense < 10 mV	–0.75	–	0.75	mV	–
Csa_Acc2	CSA accuracy with 10 mV < Vsense < 15 mV					
Csa_Acc3	CSA accuracy with 15 mV < Vsense < 25 mV					
Csa_Acc4	CSA accuracy with Vsense = 50 mV					
SCP_6A	Short circuit current detect @ 6 A	5.4	6	6.6	A	–
SCP_10A	Short circuit current detect @10 A	9	10	11		
SCP_20A	Short circuit current detect @ 20 A	18	20	22		
OCP threshold	OCP trip with 5 mΩ and current > 4 A	117	130	143	%	
Av	Nominal gain values supported: 40, 60	30	–	60	V/V	
LSCSA AC specifications						
T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	2.5	–	µs	1 nF NFET gate capacitance, VBUS_IN = 28 V
$T_{SCP\_GATE\_1}$			7.5			3 nF NFET gate capacitance, V_{BUS_IN} = 28 V

Table 5 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details / conditions
UVOV						
VTHOV	Overvoltage threshold accuracy, 4 V–30 V	–3	–	3	%	–
VTHUV1	Undervoltage threshold accuracy, 3 V–4 V	–4		4		
VTHUV2	Undervoltage threshold accuracy, 4 V–30 V	–3		3		
VBUS gate driver DC specifications						
GD_VGS	Gate to source overdrive during ON condition	5	–	10	V	NFET driver is ON
GD_Rpd	Resistance when pull-down enabled	–		2	KΩ	Applicable on VBUS_CTRL to turn-off external NFET
GD_drv	Programmable typical gate current	0.3		9.75	µA	Gate driver output current
VBUS gate driver AC specifications						
T_{ON}	VBUS_ctrl LOW to HIGH (1 V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	V_{BUS_IN} = 5 V
T_{OFF}	VBUS_ctrl HIGH to LOW (90% to 10%) with 3 nF external capacitance	–	7.5	–	µs	V_{BUS_IN} = 28 V
VBUS discharge						
R1	NMOS ON resistance for DS = 1 on V_{BUS_IN}	1000	–	4000	Ω	Measured at 0.5 V
R2	NMOS ON resistance for DS = 2 on V_{BUS_IN}	500		2000		
R4	NMOS ON resistance for DS = 4 on V_{BUS_IN}	250		1000		
R8	NMOS ON resistance for DS = 8 on V_{BUS_IN}	125		500		
R16	NMOS ON resistance for DS = 16 on V_{BUS_IN}	62.5		250		
R32	NMOS ON resistance for DS = 32 on V_{BUS_IN}	31.25	–	150	–	Measured at 0.5 V
Vbus_stop_error	Error percentage of final VBUS value from setting	–		10	%	When VBUS is discharged to 5 V
R1A	NMOS ON resistance for DS = 1 on V_{BUS_C}	1000		2000	Ω	Measured at 0.5 V
R127A	NMOS ON resistance for DS = 127 on V_{BUS_C}	6.5		38		
Voltage regulation DC specifications						
V_{OUT}	Typical V_{BUS_IN} output voltage range	3.3	–	28	V	–
VR	VBUS voltage regulation accuracy	–	±3	±5	%	
Ika_off	Off-state cathode current		2.2	10	µA	

Table 5 Functional block specifications *(continued)*

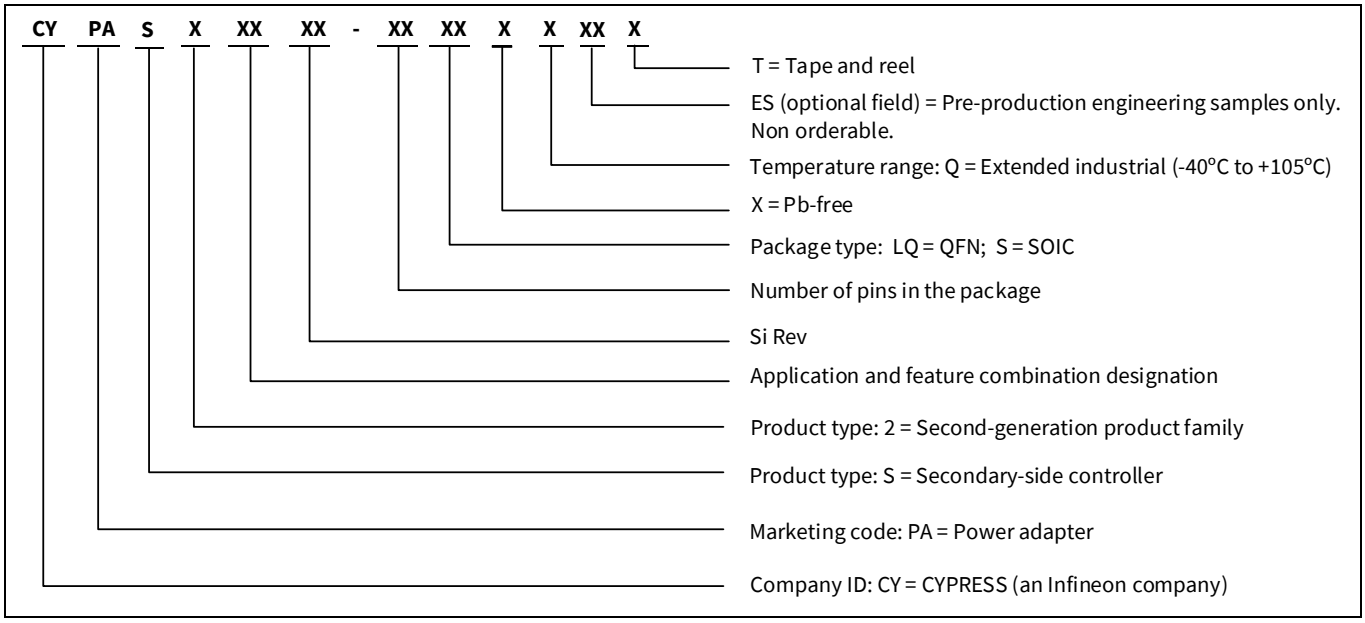
Parameter	Description	Min	Typ	Max	Unit	Details / conditions
VBUS regulator specifications						
VOLTAGE_DETECT	Voltage detect threshold voltage on V_{BUS_IN}	1.65	2.1	2.4	V	–
T_{START}	Total startup time for the regulator supply outputs with 4.7-µF load capacitance	–	50	200	µs	
ADC DC specifications						
Resolution	ADC resolution	–	8	–	bits	–
INL	Integral non linearity	–2.5	–	2.5	LSB	Reference voltage generated from V_{DDD}
INL	Integral non linearity	–1.5	–	1.5		Reference voltage generated from bandgap
VREF_ADC1	Reference voltage of ADC	V_{DDDmin}		V_{DDDmax}	V	Reference voltage generated from V_{DDD}
VREF_ADC2		1.96	2	2.04		Reference voltage generated from bandgap
VCONN switch specifications						
VCONN_OUT	VCONN minimum output voltage with 20 mA load current with Vbus = 5 V–30 V	4.5	–	–	V	–
I_{LEAK}	Connector side pin leakage current	–		10	µA	
VCONN switch AC specifications						
T_{ON}	Switch turn-on time	–	–	600	µs	–
T_{OFF}	Switch turn-off time			10		

5 Ordering information

Table 6 PAG2S-QZ ordering information

MPN	Application	Package type	Si ID	Si Rev
CYPAS211A1-32LQXQ	USB PD adapter – Secondary-side flyback control with ZVS	32-pin QFN	3B10	A1
CYPAS211A1-32LQXQT				

5.1 Ordering code definitions



6 Packaging

Table 7 Package characteristics

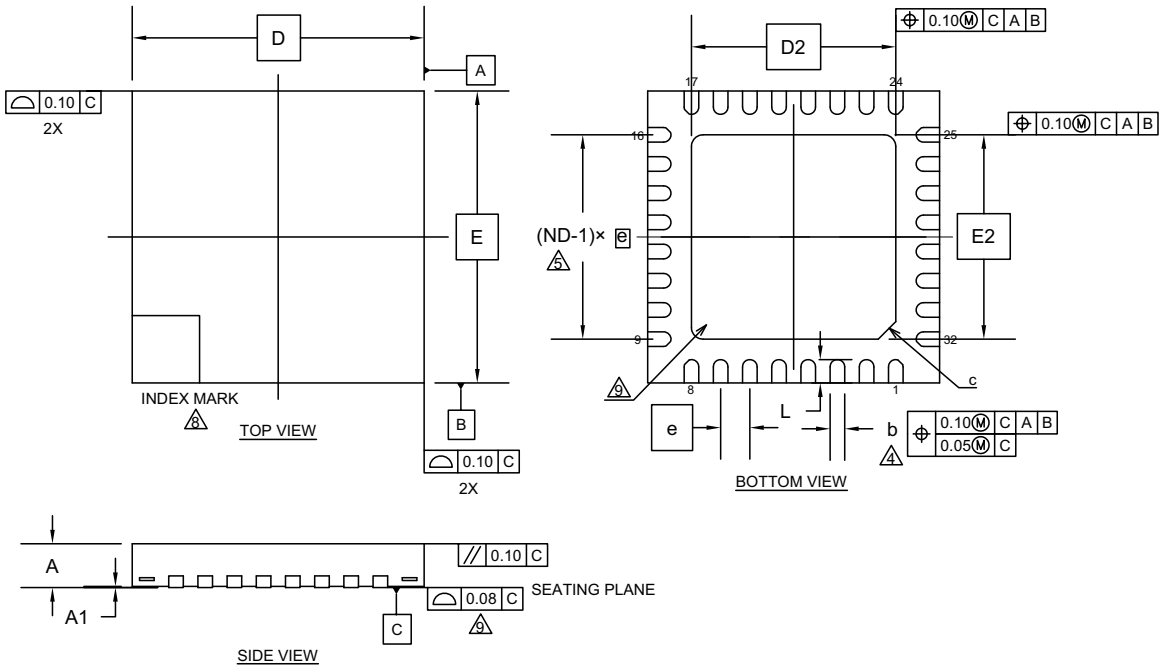
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Extended industrial	–40	–	105	°C
T_J	Operating junction temperature				150	
T_{JA}	Package θ_{JA} for 32-pin QFN	–	–	23.4	–	°C/W
T_{JB}	Package θ_{JB} for 32-pin QFN			4.85		
T_{JC}	Package θ_{JC} for 32-pin QFN			27.2		

Table 8 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
32-pin QFN	260°C	30 seconds

Table 9 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
32-pin QFN	MSL3



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.80
A_1	0.00	——	0.05
D	5.00 BSC		
E	5.00 BSC		
b	0.18	0.25	0.30
D_2	3.50 BSC		
E_2	3.50 BSC		
e	0.50 BSC		
c	0.30 REF		
L	0.35	0.40	0.45

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF : N/A

002-15160 Rev. **

Figure 11 32-lead QFN ((5.0 × 5.0 × 0.8 mm) WNP032 3.5 × 3.5 mm E-Pad (Sawn)) package outline (PG-VQFN-32), 002-15160

7 Acronyms

Table 10 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
Arm®	advanced RISC machine, a CPU architecture
BOD	brown-out detect
BMC	biphase mark code
CC	constant current
CCM	continuous conduction mode
CPU	central processing unit
CrCM	critical conduction mode
CS	current sense
CSA	current sense amplifier
CSN	current sense negative
CSP	current sense positive
DCM	discontinuous conduction mode
DFP	downstream facing port
DM	data minus
DP	data plus
DS	drive strength
EA	error amplifier
EMI	electromagnetic interference
EPR	extended power range
ESD	electrostatic discharge
ESD-HBM	electro static discharge human body model
FB	feedback
FS	full-speed
GPIO	general-purpose input/output
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LSCSA	low-side current sense amplifier
LVTTL	low-voltage transistor-transistor logic
NFET	N-channel field effect transistor
NMOS	N-type metal-oxide-semiconductor
OCP	overcurrent protection
OVP	overvoltage protection
OTP	over-temperature protection
PD	power delivery

Table 10 Acronyms used in this document *(continued)*

Acronym	Description
PHY	physical layer
POR	power-on reset
PPS	programmable power supply
PSM	pulse-skipping mode
PWM	pulse-width modulator
QR	quasi-resonant
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SCP	short-circuit protection
SDA	I^2C serial data
SPI	Serial Peripheral Interface, a communications protocol
SR	synchronous rectifier
SRAM	static random access memory
SWD	Serial Wire Debug, a test protocol
SWDCLK	serial wire debug clock
TCPWM	timer/counter/PWM
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
USB	Universal Serial Bus
USB PD	USB Power Delivery
WDT	watchdog timer
XRES	external reset I/O pin
ZCD	zero crossing defect
ZVS	zero voltage switching

8 Document conventions

8.1 Units of measure

Table 11 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*B	2023-10-10	Post to external web.
*C	2023-12-20	Updated TR_SR from 60 ns to 75 ns in **Table 5** Functional block specifications.

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