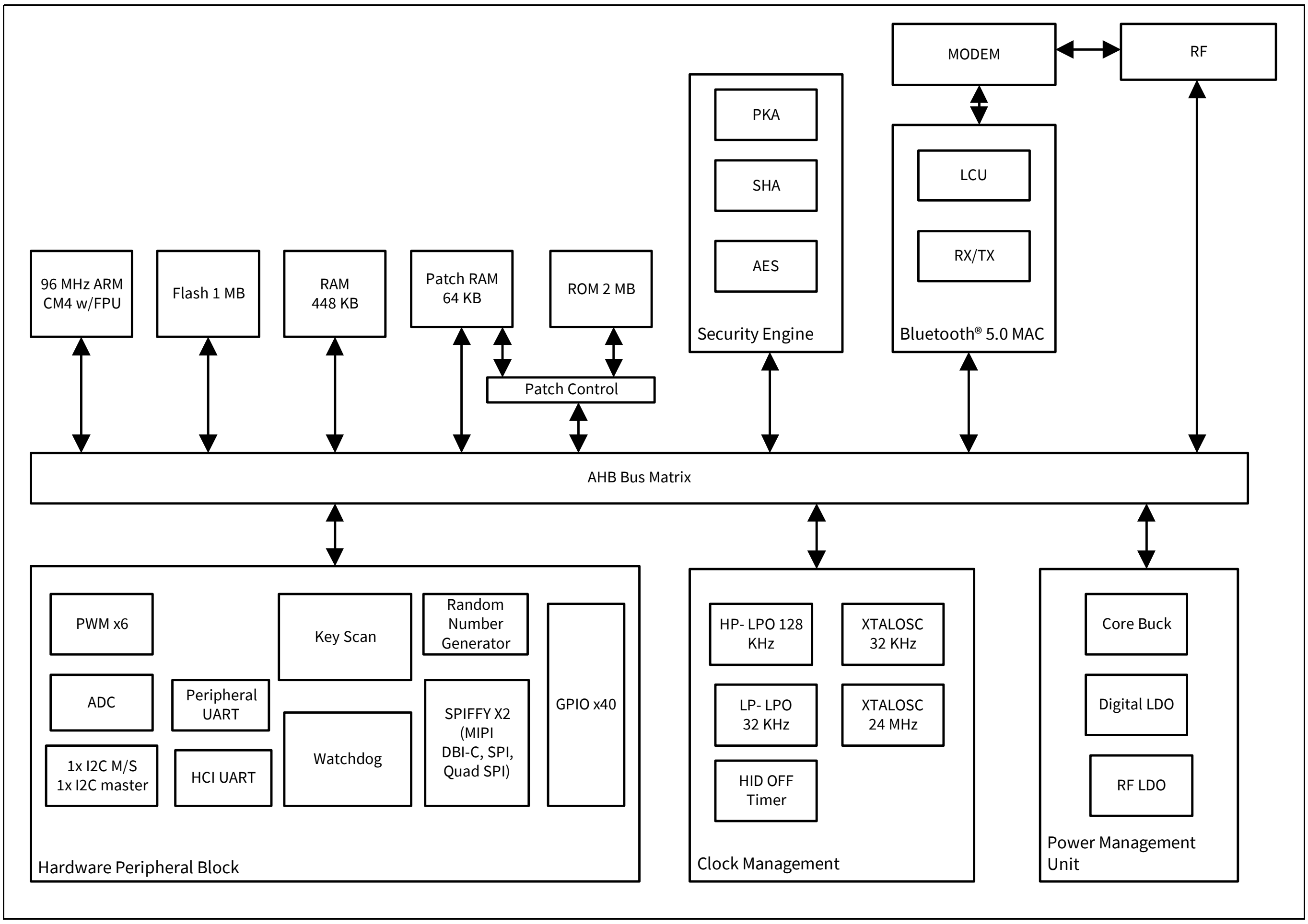
AIROC™ Bluetooth® & Bluetooth® LE system on chip

Enhanced low power

The CYW20719 is a Bluetooth® 5.1-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver with Bluetooth® LE, EDR and BR. The device is intended for use in audio, IoT, sensors (medical, home, security, and so forth) and human interface device (HID) applications. Manufactured using an advanced 40nm CMOS low-power fabrication process, the CYW20719 employs high level of integration to reduce external components, thereby minimizing application footprint and costs.

This datasheet provides details of the functional, operational, and electrical characteristics of the CYW20719 device. It is intended for hardware, design, application, and OEM engineers.

Functional block diagram



Features

- Bluetooth® subsystem
  - Complies with Bluetooth® Core Specification v5.1 with LE 2 Mbps
  - Supports Basic Rate (BR), Enhanced Data Rate (EDR) 2&3 Mbps, Bluetooth® Low Energy
  - Supports Adaptive Frequency Hopping (AFH)
  - TX power 5 dBm
  - RX sensitivity -95.5 dBm (Bluetooth® LE)
- Ultra-low-power radio
  - RX current 5.9 mA (Bluetooth® LE)
  - TX current 5.6 mA at0 dBm (Bluetooth® LE)
- Coexistence support
  - Support for Global Coexistence Interface for easy coexistence implementation with select AIROC™ Infineon Wi-Fi devices
- MCU subsystem
  - 96-MHz Arm® Cortex®-M4 microcontroller unit MCU with floating point unit (FPU)
  - Supports serial wire debug (SWD)
  - Runs Bluetooth® stack and application
  - Option to execute from on-chip flash or RAM
- Memory subsystem
  - 1 MB flash
  - 512 KB RAM
  - 2 MB ROM that stores Bluetooth® stack and driver and offloads flash for user applications
- Audio features and interfaces
  - 1x I^2S with master and slave modes
  - 1x PCM
  - PDM [2]
  - Analog front end for analog microphone [1]
- Clocks
  - On-chip 32-kHz oscillator (LP-LPO)
  - On-chip 128-kHz oscillator (HP-LPO)
  - 32-kHz crystal oscillator (Optional if low power modes not required)
  - 24-MHz crystal oscillator
  - 48-bit real time clock (RTC)
- Peripherals and communication
  - 6x 16-bit PWMs
  - Programmable key-scan matrix interface, up to 8x20 key-scanning matrix [1, 2]
  - Watchdog timer (WDT)
  - 1x peripheral UART, 1x UART for programming and HCI
  - 2x SPI (master or slave mode) Blocks (SPI, Quad SPI, and MIPI DBI-C)
  - 1x I^2C master
  - 1x 28-channel ADC (10-ENoB for DC measurement and 12-ENOB for audio measurement)
  - Hardware security engine

Notes
1. Available only in WLCSP package.
2. Subjected to driver support in Bluetooth SDK.

- General purpose input output (GPIO)
  - 16 GPIOs on QFN package
  - 40 GPIOs on WLCSP package
  - Support up to 3.63 V operation
  - Four GPIOs support 16 mA and 8 mA sink at 3.3 V and 1.8 V respectively
- Operating voltage and low-power support
  - Wide operating voltage range: 1.76 V to 3.63 V
  - 5 power modes to implement ultra-low power application – managed by real time operating system
  - 0.4 µA current in HID-OFF[2] mode (wake from GPIO).
- Packages
  - 5 mm × 5 mm 40-pin quad flat no-lead (QFN)
  - 3.2 mm × 3.1 mm 134-ball wafer level chip scale package (WLCSP)
- Software support
  - ModusToolbox™ software. Features are subject to support in the Bluetooth® SDK.
  - Check the latest version of the Bluetooth® SDK Technical brief for supported features.
- Applications
  - Wearables and fitness bands
  - Home automation
  - Blood pressure monitors and other medical applications
  - Proximity sensors
  - Key Fobs
  - Thermostats and thermometers
  - Toys

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1 Bluetooth® Baseband Core

The Bluetooth® Baseband Core (BBC) implements all time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening.

Table 1 Bluetooth® features

Bluetooth® 1.0	Bluetooth® 1.2	Bluetooth® 2.0
Basic rate	Interlaced scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive frequency hopping	–
Paging and inquiry	eSCO	–
Page and inquiry scan	–	–
Sniff	–	–
Bluetooth® 2.1	**Bluetooth® 3.0**	**Bluetooth® 4.0**
Secure simple pairing	Unicast connectionless data	Bluetooth® Low Energy
Enhanced inquiry response	Enhanced power control	–
Sniff subrating	eSCO	–
Bluetooth® 4.1	**Bluetooth® 4.2**	**Bluetooth® 5.0**
Low duty cycle advertising	Data packet length extension	LE 2 Mbps
Dual mode	LE secure connection	Slot availability mask
LE link layer topology	Link layer privacy	High duty cycle advertising

1.1 BQB and regulatory testing support

The CYW20719 fully supports Bluetooth® Test mode as described in Part 1:1 of the Specification of the Bluetooth® System v3.0. This includes the transmitter tests, normal and delayed loop back tests, and reduced hopping sequence.

In addition to the standard Bluetooth® Test Mode, the CYW20719 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

2 MCU

The CYW20719 includes a Cortex® M4 processor with 2 MB of ROM, 448 KB of data RAM, 64 KB of patch RAM, and 1 MB of on-chip flash. The CM4 has a maximum speed of 96 MHz. CYW20719 supports execution from on-chip flash (OCF).

The CM4 also includes a single precision IEEE 754 compliant floating point unit (FPU).

The CM4 runs all the Bluetooth® layers as well as application code. The ROM includes LM, HCI, L2CAP, GATT, as well as other stack layers freeing up the flash for application usage. A standard SWD Interface provides debugging support.

3 External reset

An external active-low reset signal, RESET_N, can be used to put the CYW20719 in the reset state. The RESET_N should be released only after the VDDO supply voltage level has been stabilized for at least 35 ms.

4 Power Management Unit (PMU)

Figure 1 shows the CYW20719 PMU block diagram. The CYW20719 includes an integrated buck regulator, a bypass LDO, a capless LDO for digital circuits and a separate LDO for RF. The bypass LDO automatically takes over from the buck once V_{bat} supply falls below 2.1 V.

The voltage levels shown in this figure are the default settings; the firmware may change voltage levels based on operating conditions.

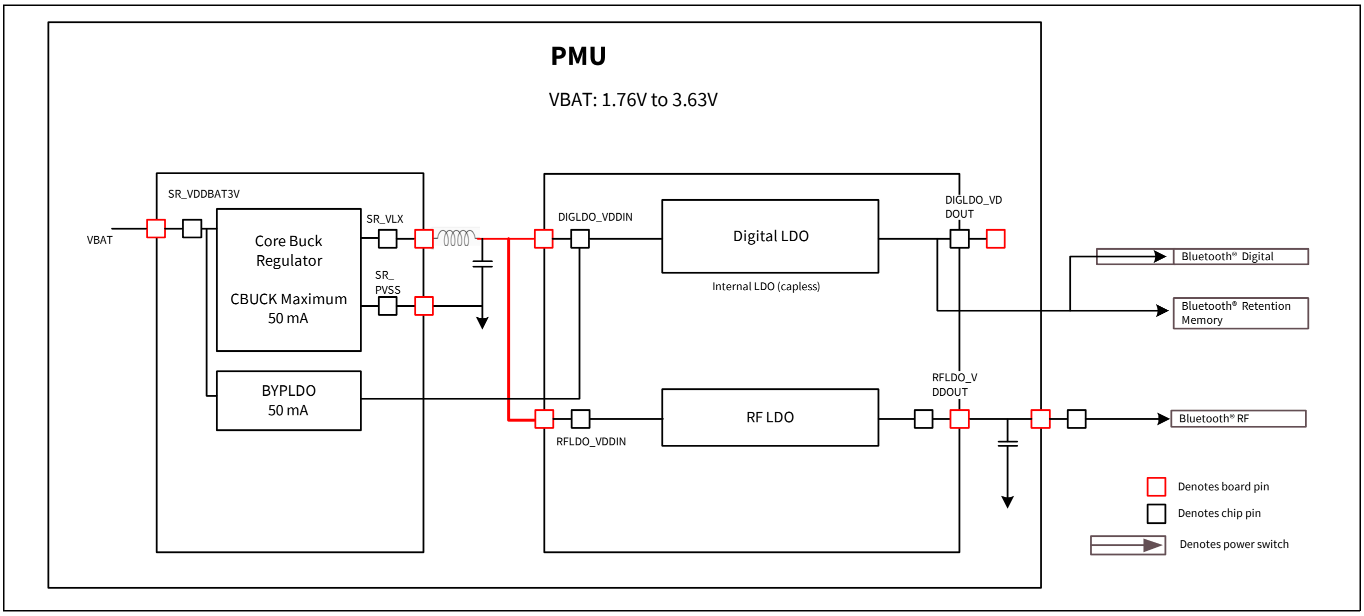


Figure 1 **Default usage mode**

5 Integrated radio transceiver

The CYW20719 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth® Radio Specification and exceeds the requirements to provide the highest communication link quality of service.

5.1 Transmitter path

The CYW20719 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

5.1.1 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

5.1.2 Power amplifier

The CYW20719 has an integrated power amplifier (PA) that can transmit up to +5 dBm.

5.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYW20719 to be used in most applications without off-chip filtering.

5.2.1 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

5.2.2 Receiver signal strength indicator

The radio portion of the CYW20719 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

5.3 Local oscillator (LO)

LO provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels for BR/EDR functionality. The CYW20719 uses an internal loop filter.

6 Peripheral and communication interfaces

6.1 I²C compatible master

The CYW20719 provides a 2-pin I^{2}C compatible Master interface to communicate with I^{2}C compatible peripherals. The I^{2}C compatible master supports the following clock speeds:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I^{2}C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^{2}C-compatible devices is not guaranteed.)

SCL and SDA lines can be routed to any of the P0-P39 GPIOs allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. I^{2}C block does not support multi master capability by either master/slave devices.

6.2 HCI UART interface

The CYW20719 includes a UART interface for factory programming as well as when operating as a Bluetooth® HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 1.5 Mbps. Typical rates are 115200, 921600, 1500000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYW20719 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%. The UART interface has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

During HCI mode the DEV_WAKE signal can be programmed to wake up the CYW20719 or allow the CYW20719 to sleep when radio activities permit. The CYW20719 can also wake up the host as needed or allow the host to sleep via the HOST_WAKE signal. The combined two signals allow the host and the CYW20719 to optimize system power consumption by allowing independent control of low power modes. DEV_WAKE and HOST_WAKE signals can be enabled via a vendor specific command.

6.3 Peripheral UART interface

The CYW20719 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYW20719 can map the peripheral UART to any GPIO (P0-P39). The Peripheral UART is functionally the same as HCI UART but with a 256 byte transmit and receive FIFO.

6.4 Crystal oscillators

6.4.1 24-MHz crystal oscillator

The CYW20719 uses a 24 MHz crystal oscillator (XTAL). The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see **Figure 2**).

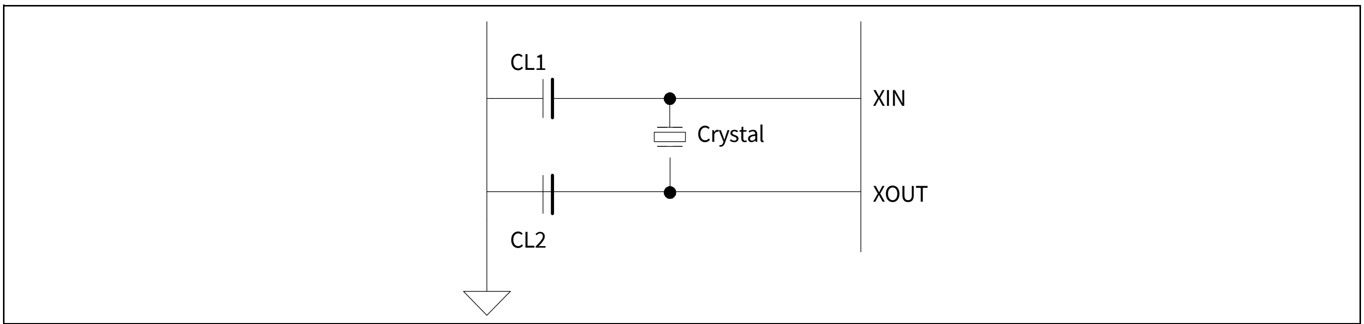


Figure 2 Recommended 24 MHz oscillator configuration

Table 2 Reference crystal electrical specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Nominal frequency	–	–	24.000	–	MHz
Oscillation mode	–	Fundamental			–
Frequency accuracy	Includes operating temperature range and aging	–	–	± 20	ppm
Equivalent series resistance	–	–	–	60	Ω
Load capacitance	–	–	8	–	pF
Drive level	–	–	–	200	µW
Shunt capacitance	–	–	–	2	pF

6.4.2 32 kHz crystal oscillator

The CYW20719 includes a 32 kHz oscillator to provide accurate timing during low power operations. **Figure 3** shows the 32 kHz XTAL oscillator with external components and **Table 3** lists the oscillator's characteristics. This oscillator can be operated with 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~6 pF. The values of C1 and C2 are used to fine-tune the oscillator.

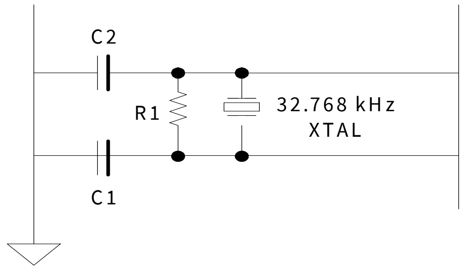


Figure 3 Recommended 32 kHz oscillator electrical specification

Table 3 Reference 32 kHz oscillator electrical specification

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	500	–	ms
XTAL drive level	P_{drv}	For crystal selection	–	–	0.5	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	2.2	pF
External AC input amplitude	V_{IN} (AC)	C_{couple} = 100 pF; R_{bias}= 10 MΩ	400	–	–	mVpp

6.5 Low-frequency clock sources

The 32-kHz low-frequency clock (lhl_lpo_32-kHz on the following figure) can be obtained from multiple sources. There are two internal low-power oscillators (LPOs) called the LP-LPO and HP-LPO and external crystal (OSC32K). The firmware determines the clock source to use among the available LPOs depending on the accuracy and power requirements. The preferred source is the external LPO (OSC32K) because it has good accuracy with the lowest current consumption. Internal LP-LPO has low current consumption and low accuracy whereas HP-LPO has higher accuracy and higher current consumption. The firmware assumes the external LPO has less than 250 PPM error with little or no jitter.

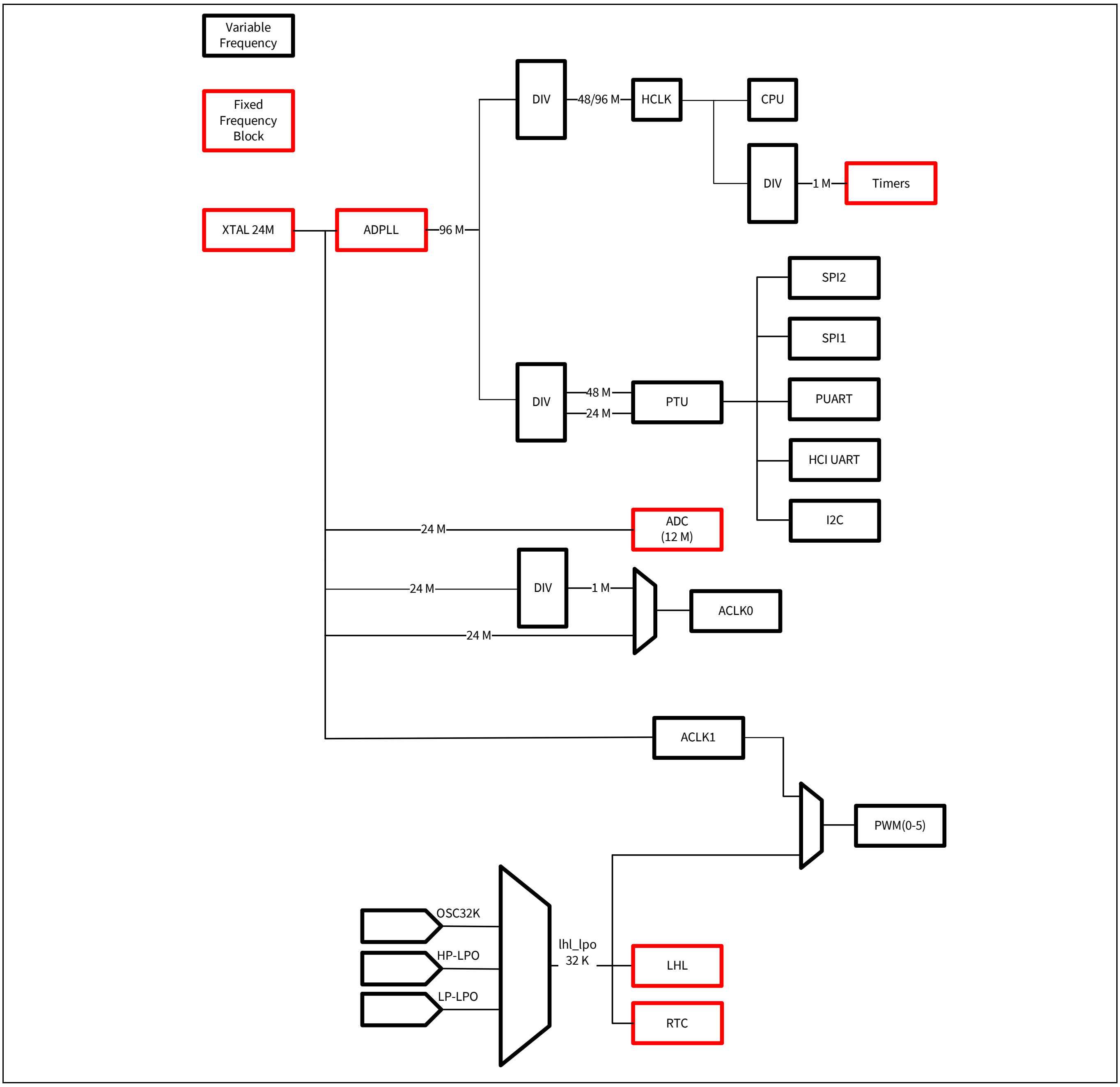


Figure 4 **Simplified clock source**

6.6 GPIO ports

The CYW20719 has 40 GPIOs labeled P0-P39 on WLCSP package and 16 GPIOs on QFN package.
All GPIOs support the following:

- programmable pull-up/down of approx 45 kΩ.
- input disable, allowing pins to be left floating or analog signals connected without risk of leakage.
- source/sink 8 mA at 3.3 V and 4 mA at 1.8 V.
- P15 is Bonded to the same pin as XTALI_32K on the QFN package (Pin 32). If External 32.768kHz crystal is not used, then this pin can be used as GPIO P15.
- P26/P27/P28/P29 (some of these pins are not available on QFN package) sink/source 16 mA at 3.3 V and 8 mA at 1.8 V.
- Most peripheral functions can be assigned to any GPIO. For details, see **Table 4** and **Table 5**.

6.7 Keyboard scanner (available only on WLCSP package)

The CYW20719 includes a HW keyscanner that supports a maximum matrix size of 20x8. The scanner has 8 inputs (also referred to as rows) and 20 outputs (also referred to as columns). Keys are detected by driving the columns down sequentially and sampling the rows. The HW scanner includes support for ghost key detection and debouncing. The scanner can also operate in sleep and PDS mode allowing low power operation while continuing to detect/store all key strokes, up or down. In other low power modes, the scanner can continue to monitor the matrix and initiate exit to active mode upon detecting a change of state.

Note Subject to the driver support in Bluetooth® SDK.

6.8 ADC

CYW20719 includes is a Σ-Δ ADC designed for audio (13 bits) and DC (10 bits) measurements. The ADC can measure the voltage on 28 GPIO. When used for analog inputs, the GPIOs must be placed in digital input disable mode to disconnect the digital circuit from the pin and avoid leakage. The internal band gap reference has ±5% accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

- P0, P1, P8-P18, P21-23, P28-P38 can be used as ADC inputs.

6.9 PWM

The CYW20719 has six internal PWMs, labeled PWM0-5

- Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register is shared among PWM0–5 (read/write). This 6-bit register is used:
  - To enable/disable each PWM channel
  - To select the clock of each PWM channel
  - To invert the output phase of each PWM channel

The application can access the PWM module through the FW driver.

Figure 5 shows the structure of one PWM channel.

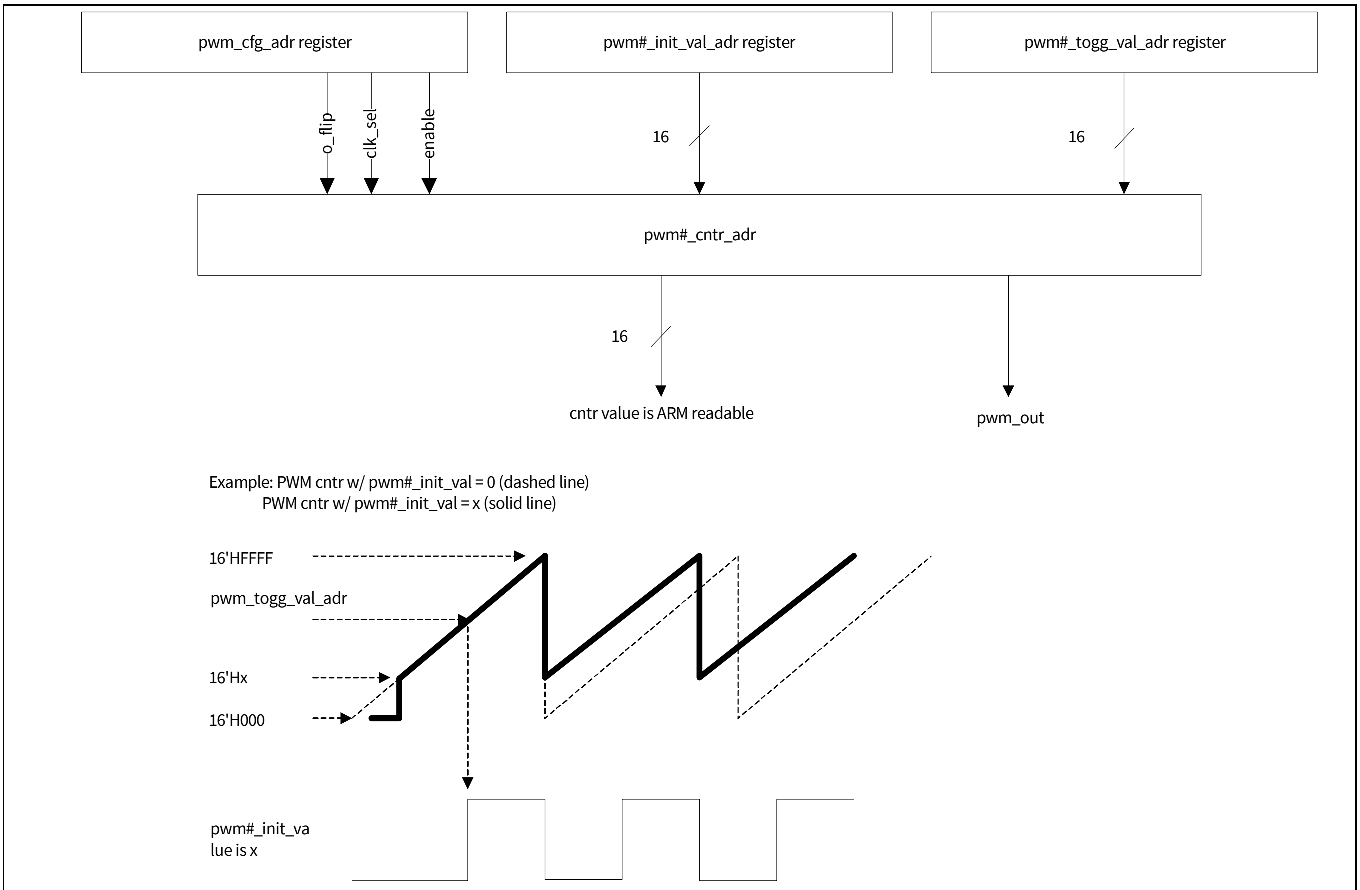


Figure 5 PWM block diagram

6.10 Serial peripheral interface block

The CYW20719 has two independent SPI interfaces. Both interfaces support Single, Dual, and Quad mode SPI operations as well as MIPI DBI-C Interface. Either of the interface can be a master/slave. SPI2 can support only one slave. SPI1 has a 1024 byte transmit and receive buffers which is shared with the host UART interface. SPI2 has a dedicated 256 byte transmit and receive buffers. To support more flexibility for user applications, the CYW20719 has optional I/O ports that can be configured individually and separately for each functional pin. SPI I/O voltage depends on VDDO.

6.10.1 MIPI interface

There are three options in DBI type-C corresponding to 9-bit, 16-bit, and 8-bit modes. The CYW20719 plays the role of host, and only the 9-bit and 8-bit modes (option 1 and option 3 in DBI-C spec) are supported. In the 9-bit mode, the SCL, CS, MOSI, and MISO pins are used. In the 8-bit mode, an additional pin DCX, indicating whether the current outgoing bit stream is a command or data byte is required.

6.11 Pulse Density Modulation (PDM) microphone

The CYW20719 accepts a ΣΔ-based one-bit PDM input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM input shares the filter path with the aux ADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4 MHz clock generated by the CYW20719 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

Note Subject to the driver support in Bluetooth® SDK.

6.12 I^{2}S interface

The CYW20719 supports a single I^{2}S digital audio port in both master and slave modes. The I^{2}S signals are:

- I^{2}S clock: I^{2}S SCK
- I^{2}S word select: I^{2}S WS
- I^{2}S data out: I^{2}S DO
- I^{2}S data in: I^{2}S DI

I^{2}S SCK and I^{2}S WS become outputs in master mode and inputs in slave mode, while I^{2}S DO always stays as an output and I^{2}S DI stays as input. The channel word length is fixed to 16 bits (frame length of 32 bits) and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I^{2}S bus, as per I^{2}S Specifications. The MSB of each data word is transmitted one bit clock cycle after the I^{2}S WS transition, synchronous with the falling edge of bit clock. Left Channel data is transmitted when I^{2}S WS is low, and right-channel data is transmitted when I2S WS is high. Data bits sent by the CYW20719 are synchronized with the falling edge of I^{2}S SCK and should be sampled by the receiver on the rising edge of the I^{2}S SCK.

The I^{2}S port is primarily used to transfer audio samples while using the A2DP profile[3]. The A2DP controller is half duplex and the direction of the audio samples depend on the A2DP role (sink/source). The I2S clock in the master mode can either be:

- 44.1 kHz x 32 bits per frame = 1411.2 kHz
- 48 kHz x 32 bits per frame = 1536 kHz

In the slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

Note
3. The I^{2}S port cannot be used at the application level for purposes other than routing A2DP audio samples.

Note PCM interface shares HW with the I^2S interface which means that both voice and audio cannot be routed at the same time.

6.13 PCM interface

The CYW20719 includes a PCM interface that can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW20719 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another device on the PCM interface and are inputs to the CYW20719. Some of the parameters of the PCM interface may be configured by the host.

The PCM interface is used for full-duplex bi-directional transfer of 8K or 16K voice samples from and to a SCO or eSCO connection[4]. By default, the PCM interface runs in an I^2S compatible mode, which allows the CYW20719 to transfer voice samples to I^2S devices.

Note PCM interface shares HW with the I^2S interface which means that both voice and audio cannot be routed simultaneously.

6.13.1 Slot mapping

The CYW20719 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM Interface, when operating in HCI mode. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz voice sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 256kHz, 512 kHz, 1024 kHz or 2048 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

6.13.2 Frame synchronization

The CYW20719 supports both short and long-frame synchronization in both master and slave modes and can be configured from the host. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

6.13.3 Data formatting

The CYW20719 may be configured to generate or accept several different data formats. For conventional narrow band speech mode, the CYW20719 always uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, filled with 0's and clocked MSB first.

6.13.4 Burst PCM mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

Note

4. The PCM interface cannot be used as a generic serial interface at the application level. It can only be used for routing SCO or eSCO voice samples.

6.14 Security engine

The CYW20719 includes a hardware security accelerator which greatly decreases the time required to perform typical security operations.This security engine includes:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)

Note Security engine is used only by Bluetooth® stack to reduce CPU overhead. It is not available for application use

6.14.1 Random number generator

This hardware block is used for key generation for Bluetooth®.

Note Availability for use by the application is subject to the support in Bluetooth® SDK.

6.15 Power modes

The CYW20719 supports the following HW power modes:

- Active mode - Normal operating mode in which all peripherals are available and the CPU is active.
- Idle mode- In this mode, the CPU is in “Wait for Interrupt” (WFI) and the HCLK, which is the high frequency clock derived from the main crystal oscillator is running at a lower clock speed. Other clocks are active and the state of the entire chip is retained.
- Sleep mode - In this mode, CPU is in WFI and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. State of the entire chip is retained, the internal LDOs run at a lower voltage (voltage is managed by the PMU), and SRAM is retained.
- Power Down Sleep (PDS) mode -This mode is an extension of the PMU Sleep wherein most of the peripherals such as UART and SPI are turned off. The entire memory is retained, and on wakeup the execution resumes from where it paused.
- Shut Down Sleep (SDS) mode -Everything is turned off except I/O Power Domain, RTC, and LPO. The device can come out of this mode either due to Bluetooth® activity or by an external interrupt. Before going into this mode, the application can store some bytes of data into “Always On RAM” (AON). When the device comes out of this mode, the data from AON is restored. After waking from SDS, the application will start from the beginning (warmboot) and has to restore its state based on information stored in AON. In the SDS mode, a single Bluetooth® task with no data activity, such as an ACL connection, Bluetooth® LE connection, or Bluetooth® LE advertisement can be performed.
- HID-OFF[5] (Timed-Wake) mode -The device can enter this mode asynchronously, that is, the application can force the device into this mode at any time. I/O Power Domain, RTC, and LPO are the only active blocks. A timer that runs off the LPO is used to wake the device up after a predetermined fixed time.
- HID-OFF[5] (External Interrupt-Waked) mode - This mode is similar to Timed-Wake, but in HID-OFF mode even the LPO and RTC are turned off. Therefore, the only wakeup source is an external interrupt.

Transition between power modes is handled by the on-chip firmware with host/application involvement. See **Firmware** Section for details.

Note

5. Subject to driver support in Bluetooth® SDK.

7 Firmware

The CYW20719 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the Bluetooth® LE baseband, Link Manager (LM), HCI, Generic Attribute Profile (GATT), Attribute Protocol (ATT), Logical Link Control and Adaptation Protocol (L2CAP) and Service Discovery Protocol (SDP) layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes.

The CYW20719 is fully supported by the ModusToolbox™ software platform. Bluetooth® SDK releases provide latest ROM patches, drivers, and sample applications allowing customized applications using the CYW20719 to be built quickly and efficiently.

Refer to CYW20719 Product Guide for details on the firmware architecture, driver documentation, power modes and how to write applications/profiles using the CYW20719.

8 Pin assignments and GPIOs

This section addresses both QFN and WLCSP pin assignments and GPIOs for the CYW20719 device.

8.1 40-pin QFN and WLCSP pin assignments

Table 4 40-pin QFN and WLCSP pin assignments

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
Microphone					
ADC_avddBAT	–	5	I	VDDIO	VDDIO
ADC_AVDDC	–	3	I	–	No Connect
Mic_avdd	–	19	I	MIC_AVDD	Microphone supply
Micbias	–	32	I	MIC_AVDD	Microphone Bias Supply
Micn	–	4	I	MIC_AVDD	Microphone negative input
Micp	–	18	I	MIC_AVDD	Microphone positive input
ADC_AVSS	–	34	I	AVSS	Analog ground
ADC_AVSSC	–	17	I	AVSS	Analog ground
ADC_REFGND	–	33	I	AVSS	Analog reference ground
Mic_avss	–	47	I	AVSS	Microphone analog ground
Baseband supply					
BT_VDDO	25	1,8,9,11,14,26,29,42,56,66,91	I	VDDO	I/O Pad Power supply
BT_VDDC	–	2,43,58,74, 99	I/O	VDDC	Baseband core power supply
VDDO	39	-	I	VDDO	LHL PAD power supply. Can be tied to BT_VDDO.
RF power supply					
BT_PAVDD	17	116	I	PAVDD	PA supply
BT_PLLVDD1p2	21	106	I	PLLVDD1P2	RFPLL and crystal oscillator supply
BT_VCOVDD1p2	20	125	I	VCOVDD1P2	VCO supply
BT_IFVDD1P2	19	110	I	IFVDD1P2	IFPLL Power Supply
Onboard LDO’s					
DIGLDO_VDDIN	16	127	I	–	Internal Digital LDO input
DIGLDO_VDDOUT	–	126	O	–	Internal Digital LDO output
RFLDO_VDDIN	15	111	I	–	RF LDO Input
RFLDO_VDDOUT	14	128	O	–	RF LDO Output
SR_VDDBAT3V	13	129	I	–	Core Buck Input
VDDBAT3V	–	120	I	–	Core Buck Input
SR_VLX	12	121	O	–	Core Buck Output
Ground pins					
BT_PAVSS	–	123	I	VSS	Ground
BT_PLLVSS	–	107	I	VSS	Ground

Table 4 40-pin QFN and WLCSP pin assignments *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
BT_VCOVSS	–	119	I	VSS	Ground
BT_IFVSS	–	115	I	VSS	Ground
BT_VSSC	–	30, 57, 75, 87, 117, 118, 124, 133, 134	I	VSS	Ground
VSSC	–	112	I	VSS	Ground
VSSO_0	–	10,1325, 28,72, 96,101	I	VSS	Ground
SR_PVSS	–	130	I	VSS	Ground
xtal_avss	–	35	I	XTAL_AVSS	Crystal ground
PMU_AVSS	–	113,114	I	PMU_AVSS	PMU ground
VSS	H	–	I	VSS	Exposed center pad, connect to ground.
UART					
BT_UART_CTS_N	30	15	I, PU	VDDO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
BT_UART_RTS_N	29	31	O, PU	VDDO	Request to send (RTS) for HCI UART interface. Leave uncon-nected if not used.
BT_UART_RXD	27	45	I	VDDO	UART serial input. Serial data input for the HCI UART interface.
BT_UART_TXD	28	46	O, PU	VDDO	UART serial output. Serial data output for the HCI UART interface.
Crystal					
BT_XTALI	22	105	I	PLLVDD1P2	Crystal oscillator input. See “The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see **Figure 2**)” for options.
BT_XTALO	23	104	O	PLLVDD1P2	Crystal oscillator output.
XTALI_32K	32	6	I	VDDO	Low-power oscillator input.
XTALO_32K	31	20	O	VDDO	Low-power oscillator output.
BT_RF	18	132	–	–	RF Antenna Port
BT_CLK_REQ	–	68	O	N/A	Used for shared-clock appli-cation.
JTAG_SEL	11	102	–	–	Reserved Arm® JTAG debug mode control. Connect to GND for all applications.

Table 4 40-pin QFN and WLCSP pin assignments *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
RST_N	10	103	I	VDDO	Active-low system reset with internal pull-up resistor.
Reserved pins					
Reserved	26	21, 36, 49, 61, 77, 84, 85, 108	N/A	N/A	Reserved. Leave unconnected.
Reserved, Connect to GND	–	16, 92	N/A	N/A	Reserved, connect to GND

8.2 40-pin QFN and WLCSP GPIOs

Table 5 40-pin QFN and WLCSP GPIOs

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
BT_DEV_WAKE	–	86	I	VDDO	A signal from the host to the CYW20719 indicating that the host requires attention.
BT_HOST_WAKE	24	76	O	VDDO	A signal from the CYW20719 device to the host indicating that the Bluetooth® device requires attention.
BT_GPIO_2	–	44	I/O	VDDO	GPIO: Can also be configured as a GCI Pin
BT_GPIO_3	–	59	I/O	VDDO	GPIO: Can also be configured as a GCI Pin
BT_GPIO_4	–	79	I/O	VDDO	GPIO: Can also be configured as a GCI Pin
BT_GPIO_5	–	78	I/O	VDDO	GPIO: Can also be configured as a GCI Pin
P0	3	93	I/O	VDDO	• GPIO: P0 • Keyboard scan input (row): KSI0 • A/D converter input 29 • Supermux I/O functions as defined in **Table 6**.
P1	4	54	I/O	VDDO	• GPIO: P1 • Keyboard scan input (row): KSI1 • A/D converter input 28 • Supermux I/O functions as defined in **Table 6**
P2	34	60	I/O	VDDO	• GPIO: P2 • Keyboard scan input (row): KSI2 • Supermux I/O functions as defined in **Table 6**
P3	–	22	I/O	VDDO	• GPIO: P3 • Keyboard scan input (row): KSI3 • Supermux I/O functions as defined in **Table 6**
P4	35	23	I/O	VDDO	• GPIO: P4 • Keyboard scan input (row): KSI4 • Supermux I/O functions as defined in **Table 6**

Notes

6. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in **Table 6** and **Table 7**.
7. During power-on reset, all inputs are disabled.
8. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

Table 5 40-pin QFN and WLCSP GPIOs *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
P5	–	37	I/O	VDDO	• GPIO: P5 • Keyboard scan input (row): KSI5 • Supermux I/O functions as defined in **Table 6**
P6	36	50	I/O	VDDO	• GPIO: P6 • Keyboard scan input (row): KSI6 • Supermux I/O functions as defined in **Table 6**
P7	37	62	I/O	VDDO	• GPIO: P7 • Keyboard scan input (row): KSI7 • Supermux I/O functions as defined in **Table 6**
P8	–	69	I/O	VDDO	• GPIO: P8 • A/D converter input 27 • Supermux I/O functions as defined in **Table 6**
P9	–	52	I/O	VDDO	• GPIO: P9 • A/D converter input 26 • External T/R switch control: tx_pd • Supermux I/O functions as defined in **Table 6**
P10	40	63	I/O	VDDO	• GPIO: P10 • Keyboard scan output (column): KSO2 • A/D converter input 25 • Supermux I/O functions as defined in **Table 6**
P11	–	70	I/O	VDDO	• GPIO: P11 • A/D converter input 24 • Supermux I/O functions as defined in **Table 6**
P12	–	40	I/O	VDDO	• GPIO: P12 • A/D converter input 23 • Supermux I/O functions as defined in **Table 6**

Notes

6. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in **Table 6** and **Table 7**.
7. During power-on reset, all inputs are disabled.
8. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

Table 5 **40-pin QFN and WLCSP GPIOs** *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
P13	–	71	I/O	VDDO	• GPIO: P13 • A/D converter input 22 • Supermux I/O functions as defined in **Table 6**
P14	–	24	I/O	VDDO	• GPIO: P14 • A/D converter input 21 • Supermux I/O functions as defined in **Table 6**
P15	32	7	I/O	VDDO	• GPIO: P15 • A/D converter input 20 • Supermux I/O functions as defined in **Table 6**
P16	33	48	I/O	VDDO	• GPIO: P16 • A/D converter input 19 • Supermux I/O functions as defined in **Table 6**
P17	38	38	I/O	VDDO	• GPIO: P17 • A/D converter input 18 • Supermux I/O functions as defined in **Table 6**
P18	–	51	I/O	VDDO	• GPIO: P18 • A/D converter input 17 • Supermux I/O functions as defined in **Table 6**
P19	–	39	I/O	VDDO	Reserved for system use. Leave unconnected.
P20	–	12	I/O	VDDO	Reserved for system use. Leave unconnected.
P21	–	53	I/O	VDDO	• GPIO: P21 • A/D converter input 14 • Supermux I/O functions as defined in **Table 6**

Notes
6. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in **Table 6** and **Table 7**.
7. During power-on reset, all inputs are disabled.
8. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

Table 5 40-pin QFN and WLCSP GPIOs *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
P22	–	27	I/O	VDDO	• GPIO: P22 • A/D converter input 13 • Supermux I/O functions as defined in **Table 6**
P23	–	64	I/O	VDDO	• GPIO: P23 • A/D converter input 12 • Supermux I/O functions as defined in **Table 6**
P24	–	90	I/O	VDDO	• GPIO: P24 • Supermux I/O functions as defined in **Table 6**
P25	8	97	I/O	VDDO	• GPIO: P25 • Supermux I/O functions as defined in **Table 6**
P26	7	83	I/O	VDDO	• GPIO: P26 • Current: 16 mA sink • Supermux I/O functions as defined in Table 6
P27	–	94	I/O	VDDO	• GPIO: P27 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6**
P28	1	41	I/O	VDDO	• GPIO: P28 • A/D converter input 11 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6**
P29	2	80	I/O	VDDO	• GPIO: P29 • A/D converter input 10 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6**

Notes

6. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in **Table 6** and **Table 7**.
7. During power-on reset, all inputs are disabled.
8. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

Table 5 40-pin QFN and WLCSP GPIOs *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
P30	–	95	I/O	VDDO	• GPIO: P30 • A/D converter input 9 • Supermux I/O functions as defined in **Table 6**
P31	–	73	I/O	VDDO	• GPIO: P31 • A/D converter input 8 • Supermux I/O functions as defined in **Table 6**
P32	–	98	I/O	VDDO	• GPIO: P32 • A/D converter input 7 • Supermux I/O functions as defined in **Table 6**
P33	9	100	I/O	VDDO	• GPIO: P33 • A/D converter input 6 • Supermux I/O functions as defined in **Table 6**
P34	5	81	I/O	VDDO	• GPIO: P34 • A/D converter input 5 • Supermux I/O functions as defined in **Table 6**
P35	–	65	I/O	VDDO	• GPIO: P35 • A/D converter input 4 • Supermux I/O functions as defined in **Table 6**
P36	–	55	I/O	VDDO	• GPIO: P36 • A/D converter input 3 • Supermux I/O functions as defined in **Table 6**
P37[8]	–	88	I/O	VDDO	• GPIO: P37 • A/D converter input 2 • Supermux I/O functions as defined in **Table 6**

Notes
6. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in **Table 6** and **Table 7**.
7. During power-on reset, all inputs are disabled.
8. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

Table 5 **40-pin QFN and WLCSP GPIOs** *(continued)*

Pin name	Pin number		I/O	Power domain	Description
	QFN-40	WLCSP			
P38	6	89	I/O	VDDO	• GPIO: P38 • A/D converter input 1 • Supermux I/O functions as defined in **Table 6**
P39	–	82	I/O	VDDO	Reserved for system use. Leave unconnected.
Strapping pins					
BT_TM1	–	67	I	–	Device test mode control. Connect to GND for all applications.
PMU_DISABLE	–	109	I	VDDO	PMU Enable/Disable. Connected to ground.

Notes

6. All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in **Table 6** and **Table 7**.
7. During power-on reset, all inputs are disabled.
8. P15 and P37 should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow through these pins until the part comes out of reset.

Table 6 GPIO supermux input functions

Input	Description
SWDCK	Serial Wire Debugger Clock
SWDIO	Serial Wire Debugger I/O
spiffy1_clk[s]	SPIFFY 1 Clock (Slave)
spiffy1_cs[s]	SPIFFY 1 Chip Select (Slave)
spiffy1_mosi[s]	SPIFFY 1 MOSI (Slave)
spiffy1_miso[m]	SPIFFY 1 MISO (Master)
spiffy1_io2	SPIFFY 1 I/O 2 (Quad SPI)
spiffy1_io3	SPIFFY 1 I/O 3 (Quad SPI)
spiffy1_int[s]	SPIFFY 1 Interrupt (Slave)
spiffy2_clk[s]	SPIFFY 2 Clock (Slave)
spiffy2_cs[s]	SPIFFY 2 Chip Select (Slave)
spiffy2_mosi[s]	SPIFFY 2 MOSI (Slave)
spiffy2_miso[m]	SPIFFY 2 MISO (Master)
spiffy2_io2	SPIFFY 2 I/O 2
spiffy2_io3	SPIFFY 2 I/O 3
spiffy2_int[s]	SPIFFY 2 Interrupt (Slave)
puart_rx	Peripheral UART RX
puart_cts_n	Peripheral UART CTS
SCL	I2C Clock
SDA	I2C Data
PCM_IN	PCM Input
PCM_CLK	PCM Clock
PCM_SYNC	PCM Sync
I2S_DI	I2S Data Input
I2S_WS	I2S Word Select
I2S_CLK	I2S Clock
PDM_IN_Ch_1	PDM Input Channel 1
PDM_IN_Ch 2	PDM Input Channel 2

Table 7 GPIO supermux output functions

Output	Description
do_P# (data out of GPIO. For example: 0)	
kso0	Key Scan output 0
kso1	Key Scan output 1
kso2	Key Scan output 2
kso3	Key Scan output 3
kso4	Key Scan output 4
kso5	Key Scan output 5
kso6	Key Scan output 6
kso7	Key Scan output 7
kso8	Key Scan output 8
kso9	Key Scan output 9
kso10	Key Scan output 10
kso11	Key Scan output 11
kso12	Key Scan output 12
kso13	Key Scan output 13
kso14	Key Scan output 14
kso15	Key Scan output 15
kso16	Key Scan output 16
kso17	Key Scan output 17
kso18	Key Scan output 18
kso19	Key Scan output 19
do_P# ^ pwm0	PWM Channel 0
do_P# ^ pwm1	PWM Channel 1
do_P# ^ pwm2	PWM Channel 2
do_P# ^ pwm3	PWM Channel 3
do_P# ^ pwm4	PWM Channel 4
do_P# ^ pwm5	PWM Channel 5
aclk0	Auxiliary clock Output 0
aclk1	Auxiliary clock Output 1
HID_OFF	HID-OFF Indicator
pa_ramp	External PA ramp
tx_pu	External PA Control Signal
rx_pu	External PA Control Signal
SWDIO	Serial Wire Debugger Input/Output
puart_tx (uart2_tx)	Peripheral UART TX
puart_rts_n (uart2_rts_n)	Peripheral UART RTS
spiffy1_CLK	SPIFFY 1 Clock
spiffy1_CS	SPIFFY 1 Chip Select
spiffy1_MOSI	SPIFFY 1 MOSI

Table 7 GPIO supermux output functions *(continued)*

Output	Description
spiffy1_MISO	SPIFFY 1 MISO
spiffy1_IO2	SPIFFY I/O 2
spiffy1_IO3	SPIFFY I/O 3
spiffy1_INT	SPIFFY Interrupt
spiffy1_DCX	MIPI-DBI Data/Command Indicator
spiffy2_CLK	SPIFFY 2 Clock
spiffy2_CS	SPIFFY 2 Chip Select
spiffy2_MOSI	SPIFFY 2 MOSI
spiffy2_MISO	SPIFFY 2 MISO
spiffy2_IO2	SPIFFY 2 I/O 2
spiffy2_IO3	SPIFFY 2 I/O 3
spiffy2_INT	SPIFFY 2 Interrupt
spiffy2_DCX	MIPI-DBI Data/Command Indicator
pcm_in_o	PCM IN
pcm_out_o	PCM Out
pcm_bclk_o	PCM Bit Clock
pcm_sync_o	PCM Sync Output
i2s_ssd	I2S Slave Serial Data
i2s_sws	I2S Slave Word Select
i2s_sck	I2S Slave Clock
i2s_msd	I2S Master Serial Data
i2s_mws	I2S Master Word Select
i2s_mck	I2S Master Clock

9 Pin/ball maps

9.1 40-pin QFN pin map

The CYW20719 40-pin QFN package is shown in **Figure 6**.

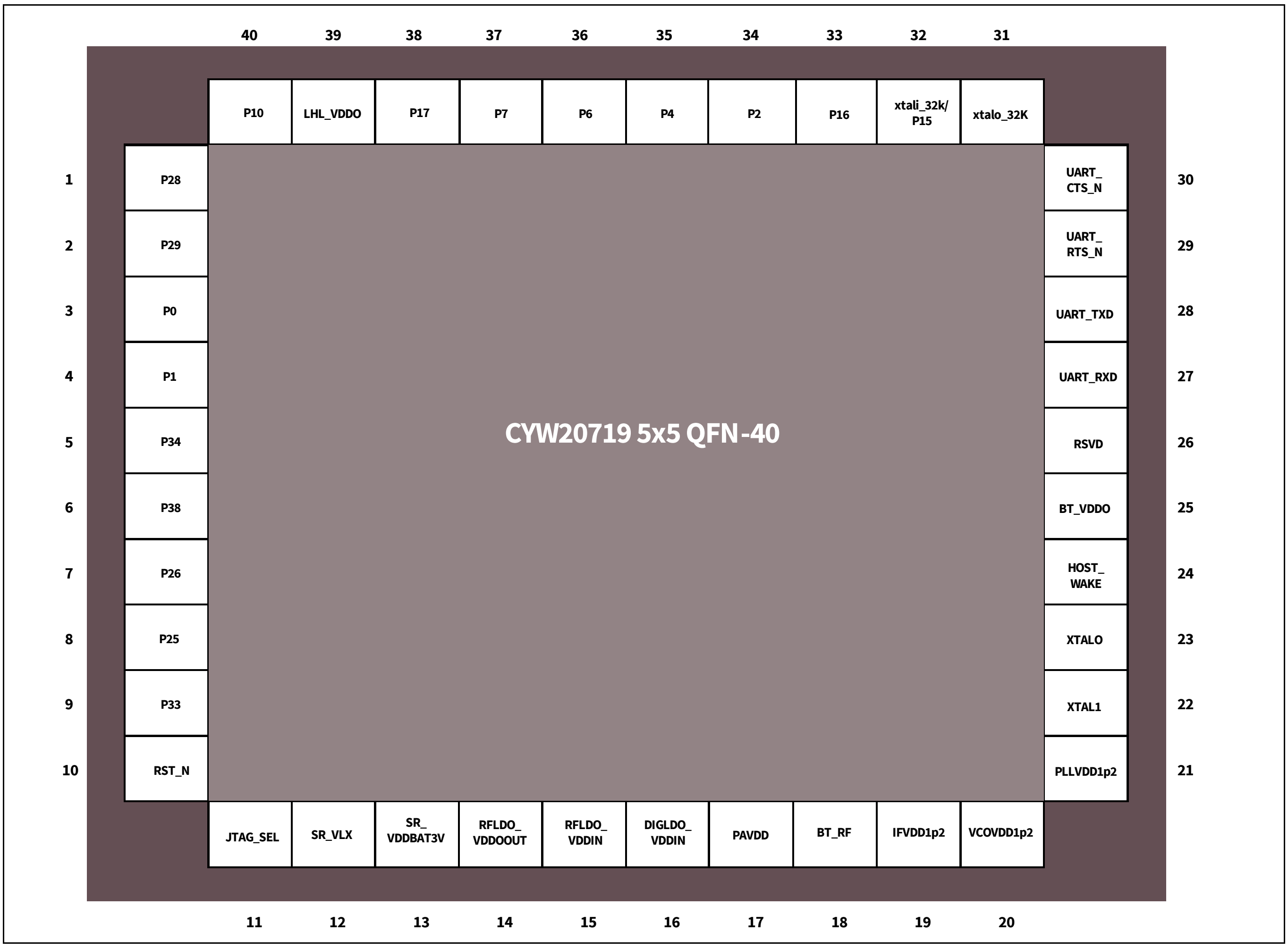


Figure 6 40-pin QFN pin map

9.2 WLCSP ball map

The CYW20719 WLCSP package is shown in **Figure 7**.

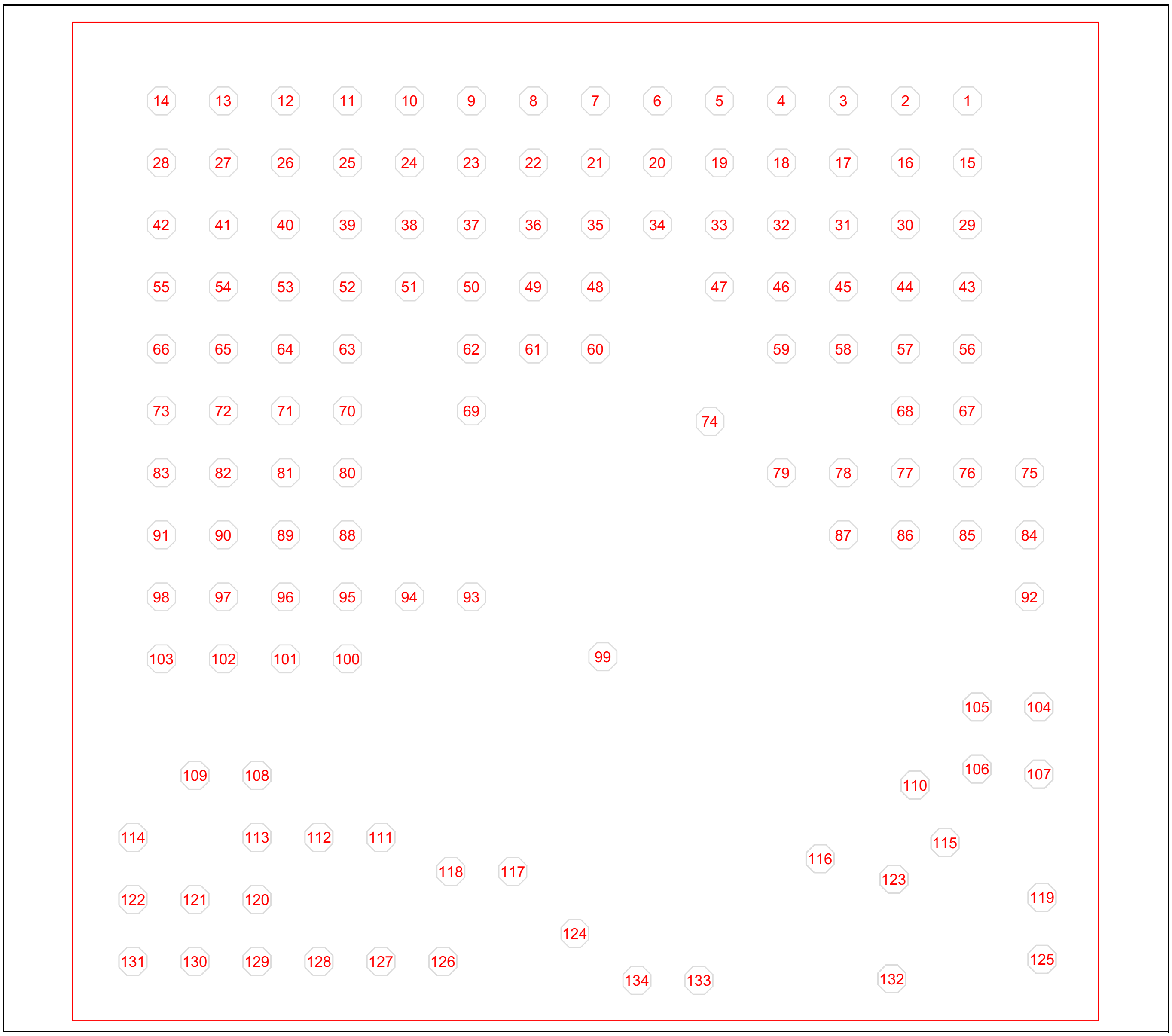


Figure 7 **WLCSP ball map**

Notes

9. **Figure 7** shows the bottom view of the WLCSP package (Bumps facing up).
10. See **Table 4** and **Table 8** and for additional WLCSP information.
11. Table 8 shows the package view from the bottom (bumps facing up).
12. Coordinate origin (0, 0) is at the center of the WLCSP package with the bumps facing up.

Table 8 CYW20719 WLCSP bump coordinates

Bump#	NET_NAME	X-COORD (µm)	Y-COORD (µm)
1	BT_VDDO	1232.28	1356.88
2	BT_VDDC	1032.28	1356.88
3	Reserved - Do not connect	832.28	1356.88
4	Micn	632.28	1356.88
5	ADC_avddBAT	432.28	1356.88
6	xtali_32K	232.29	1356.88
7	P15	32.29	1356.88
8	VDDO_0	-167.7	1356.88
9	VDDO_0	-367.7	1356.88
10	VSSO_0	-567.7	1356.88
11	VDDO_0	-767.7	1356.88
12	P20	-967.69	1356.88
13	VSSO_0	-1167.69	1356.88
14	VDDO_0	-1367.69	1356.88
15	BT_UART_CTS_N	1232.28	1156.88
16	Reserved, Connect to GND	1032.28	1156.88
17	ADC_AVSSC	832.28	1156.88
18	Micp	632.28	1156.88
19	Mic_avdd	432.28	1156.88
20	xtalo_32K	232.29	1156.88
21	Reserved	32.29	1156.88
22	P3	-167.7	1156.88
23	P4	-367.7	1156.88
24	P14	-567.7	1156.88
25	VSSO_0	-767.7	1156.88
26	VDDO_0	-967.69	1156.88
27	P22	-1167.69	1156.88
28	VSSO_0	-1367.69	1156.88
29	BT_VDDO	1232.28	956.88
30	BT_VSSC	1032.28	956.88
31	BT_UART_RTS_N	832.28	956.88
32	Micbias	632.28	956.88
33	ADC_REFGND	432.28	956.88
34	ADC_AVSS	232.29	956.88
35	xtal_avss	32.29	956.88
36	Reserved	-167.7	956.88
37	P5	-367.7	956.88
38	P17	-567.7	956.88
39	P19	-767.7	956.88

Table 8 CYW20719 WLCSP bump coordinates *(continued)*

Bump#	NET_NAME	X-COORD (µm)	Y-COORD (µm)
40	P12	-967.69	956.88
41	P28	-1167.69	956.88
42	VDDO_0	-1367.69	956.88
43	BT_VDDC	1232.28	756.89
44	BT_GPIO_2	1032.28	756.89
45	BT_UART_RXD	832.28	756.89
46	BT_UART_TXD	632.28	756.89
47	Mic_avss	432.28	756.89
48	P16	32.29	756.89
49	Reserved	-167.7	756.89
50	P6	-367.7	756.89
51	P18	-567.7	756.89
52	P9	-767.7	756.89
53	P21	-967.69	756.89
54	P1	-1167.69	756.89
55	P36	-1367.69	756.89
56	BT_VDDO	1232.28	556.89
57	BT_VSSC	1032.28	556.89
58	BT_VDDC	832.28	556.89
59	BT_GPIO_3	632.28	556.89
60	P2	32.29	556.89
61	Reserved	-167.7	556.89
62	P7	-367.7	556.89
63	P10	-767.7	556.89
64	P23	-967.69	556.89
65	P35	-1167.69	556.89
66	VDDO_0	-1367.69	556.89
67	BT_TM1	1232.28	356.89
68	BT_CLK_REQ	1032.28	356.89
69	P8	-367.7	356.89
70	P11	-767.7	356.89
71	P13	-967.69	356.89
72	VSSO_0	-1167.69	356.89
73	P31	-1367.69	356.89
74	BT_VDDC	401.88	322.94
75	BT_VSSC	1432.27	156.89
76	BT_HOST_WAKE	1232.28	156.89
77	Reserved	1032.28	156.89
78	BT_GPIO_5	832.28	156.89
79	BT_GPIO_4	632.28	156.89

Table 8 **CYW20719 WLCSP bump coordinates** *(continued)*

Bump#	NET_NAME	X-COORD (µm)	Y-COORD (µm)
80	P29	-767.7	156.89
81	P34	-967.69	156.89
82	P39	-1167.69	156.89
83	P26	-1367.69	156.89
84	Reserved	1432.27	-43.1
85	Reserved	1232.28	-43.1
86	BT_DEV_WAKE	1032.28	-43.1
87	BT_VSSC	832.28	-43.1
88	P37	-767.7	-43.1
89	P38	-967.69	-43.1
90	P24	-1167.69	-43.1
91	VDDO_0	-1367.69	-43.1
92	Reserved, Connect to GND	1432.27	-243.09
93	P0	-367.7	-243.09
94	P27	-567.7	-243.09
95	P30	-767.7	-243.09
96	VSSO_0	-967.69	-243.09
97	P25	-1167.69	-243.09
98	P32	-1367.69	-243.09
99	BT_VDDC	56.23	-435.87
100	P33	-767.7	-443.09
101	VSSO_0	-967.69	-443.09
102	JTAG_SEL	-1167.69	-443.09
103	RST_N	-1367.69	-443.09
104	BT_XTALO	1462.79	-597.97
105	BT_XTALI	1262.79	-597.97
106	BT_PLLVDD1p2	1262.79	-797.97
107	BT_PLLVSS	1462.79	-814.63
108	Reserved	-1059.5	-819
109	PMU_DISABLE	-1259.5	-819
110	BT_IFVDD1p2	1062.79	-849.66
111	RFLDO_VDDIN1P5	-659.5	-1018.99
112	VSSC	-859.5	-1018.99
113	PMU_AVSS	-1059.5	-1018.99
114	PMU_AVSS	-1459.49	-1018.99
115	BT_IFVSS	1159.51	-1035.5
116	BT_PAVDD	756.99	-1087.29
117	BT_VSSC	-234	-1128.6
118	BT_VSSC	-433.99	-1128.6
119	BT_VCOVSS	1472.59	-1212.28

Table 8 **CYW20719 WLCSP bump coordinates** *(continued)*

Bump#	NET_NAME	X-COORD (µm)	Y-COORD (µm)
120	VDDBAT3V	-1059.5	-1218.99
121	SR_VLX	-1259.5	-1218.99
122	Reserved	-1459.49	-1218.99
123	BT_PAVSS	994.94	-1153.5
124	BT_VSSC	-34	-1328.59
125	BT_VCOVDD1p2	1472.59	-1412.28
126	DIGLDO_VDDOUT	-459.5	-1418.99
127	DIGLDO_VDDIN1P5	-659.5	-1418.99
128	RFLDO_VDDOUT	-859.5	-1418.99
129	SR_VDDBAT3V	-1059.5	-1418.99
130	SR_PVSS	-1259.5	-1418.99
131	Reserved	-1459.49	-1418.99
132	BT_RF	988.31	-1475
133	BT_VSSC	365.99	-1479.96
134	BT_VSSC	165.99	-1479.96

10 Specifications

10.1 Electrical characteristics

Caution: The absolute maximum ratings in the following table indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 9 Absolute maximum ratings

Requirement Parameter	Specifications			Unit
	Min	Nom	Max	
Maximum junction temperature	–	–	125	°C
VDD IO (BT_VDDO, VDDO_0)	–0.5	–	3.795	V
VDD RF (BT_IFVDD1p2, BT_PLLVDD1p2, BT_VCOVDD1p2, BT_PAVDD)	–0.5	–	1.38	V
VDDBAT3V/SR_VDDBAT3V	–0.5	–	3.795	V
DIGLDO_VDDIN1P5	–0.5	–	1.65	V
RFLDO_VDDIN1P5	–0.5	–	1.50	V
MIC_AVDD	–0.5	–	3.795	V

Table 10 ESD/latch up

Requirement parameter	Specifications			Unit
	Min	Nom	Max	
ESD tolerance HBM	–2000	–	2000	V
ESD tolerance CDM	–500	–	500	V
Latch up	–	200	–	mA

Table 11 Environmental ratings

Characteristics	Value	Unit
Operating temperature	–30 to +85	°C
Storage temperature	–40 to +150	°C

Note

13.Lowest operating temperature for the 32 kHz xtal is -10°C.

Table 12 Recommended operating conditions

Parameter	Specifications			Unit
	Min	Typ	Max	
VDDIO (BT_VDDO, VDDO_0)	1.76	3.0	3.63	V
VDDBAT3V/SR_VDDBAT3V	1.76	3.0	3.63	V
MIC_AVDD	1.76	3.0	3.63	V

10.1.1 Core buck regulator

Table 13 Core buck regulator

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage DC, VBAT	DC voltage range inclusive of disturbances	1.76	3.0	3.63	V
CBUCK output current	Low Power Operation Mode (LPOM) only	–	–	65	mA
Output voltage range	Programmable, 30mV/step default = 1.2 V (bits = 0000)	1.2	1.26	1.5	V
Output voltage DC accuracy	Includes load and line regulation	–4	–	+4	%
LPOM efficiency (high load)	–	–	85	–	%
LPOM efficiency (low load)	–	–	80	–	%
Input supply voltage ramp-up time	0 to 3.3 V	40	–	–	µs

- Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.
- Maximum capacitor value refers to the total capacitance seen at a node where the capacitor is connected. This also includes any decoupling capacitors connected at the load side, if any.

10.1.2 Recommended external component for core buck regulator

Table 14 Recommended external component for core buck regulator

Parameter	Conditions	Min	Typ	Max	Unit
External output inductor L	2.2 µH ±25%, DCR=114 mΩ ±20%, ACR<1Ω (for frequency<1 MHz)	–	2.2	–	µH
External output capacitor, Cout	4.7 µF ±10%, 6.3V, 0402, X5R, MLCC capacitor +board total-ESR < 20 mΩ	–	4.7	–	µF
External input capacitor, Cin	For SR_VDDBAT pin Ceramic, X5R, 0402, ESR<30 mΩ at 4 MHz, +/-20%, 6.3V, 10 µF	–	10	–	µF

10.1.3 Recommended external components for RFLDO

Table 15 Recommended external components for RFLDO

Parameter	Conditions	Min	Typ	Max	Unit
External output capacitor, Co	Total ESR (trace/cap): 5 m–240 mΩ	0.5	2.2	4.7	µF

10.1.4 Digital I/O characteristics

Table 16 Digital I/O characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage (VDDO = 3 V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3 V)	V_{IH}	2.4	–	–	V
Input low voltage (VDDO = 1.8 V)	V_{IL}	–	–	0.4	V
Input high voltage (VDDO = 1.8 V)	V_{IH}	1.4	–	–	V
Output low voltage	V_{OL}	–	–	0.45	V
Output high voltage	V_{OH}	VDDO – 0.45 V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Input capacitance	C_{IN}	–	–	0.4	pF
Output low current (VDDO = 3 V, V_{OL} = 0.5 V)	I_{OL}	–	–	8.0	mA
Output low current (VDDO = 1.8 V, V_{OL} = 0.5 V)	I_{OL}	–	–	4.0	mA
Output high current (VDDO = 3 V, V_{OH} = 2.55 V)	I_{OH}	–	–	8.0	mA
Output high current (VDDO = 1.8 V, V_{OH} = 1.35 V)	I_{OH}	–	–	4.0	mA

10.1.5 ADC electrical characteristics

Table 17 Electrical characteristics

Parameter	Symbol	Conditions/comments	Min	Typ	Max	Unit
Current consumption	I_{TOT}	–	–	2	3	mA
Power down current	–	At room temperature	–	1	–	µA
ADC core specification						
ADC reference voltage	VREF	From BG with ±3% accuracy	–	0.85	–	V
ADC sampling clock	–	–	–	12	–	MHz
Absolute error	–	Includes gain error, offset and distortion. Without factory calibration.	–	–	5	%
		Includes gain error, offset and distortion. After factory calibration.	–	–	2	%
ENOB	–	For audio application	12	13	–	Bit
		For static measurement	10	–	–	
ADC input full scale	FS	For audio application	–	1.6	–	
		For static measurement	1.8	–	3.6	
Conversion rate	–	For audio application	8	16	–	kHz

Note

14.Conditional requirement for the measurement time of 10 µs. Relaxed with longer measurement time for each GPIO input channel.

Table 17 Electrical characteristics *(continued)*

Parameter	Symbol	Conditions/comments	Min	Typ	Max	Unit
Signal bandwidth	–	For audio application	20	–	8K	Hz
		For static measurement	–	DC	–	
Input impedance	R_{IN}	For audio application	10	–	–	KΩ
		For static measurement	500	–	–	
Startup time	–	For audio application	–	10	–	ms
		For static measurement	–	20	–	µs
MIC PGA specifications						
MIC PGA gain range	–	–	0	–	42	dB
MIC PGA gain step	–	–	–	1	–	dB
PGA input referred noise	–	At 42 dB PGA gain A-weighted	–	–	4	µV
MIC Bias Specifications						
MIC bias output voltage	–	At 3 V supply, 25°C, default settings	–	2.4	–	V
MIC bias loading current	–	–	–	–	3	mA
MIC bias noise	–	Refers to PGA input 20 Hz to 8 kHz, A-weighted	–	–	3	µV
MIC bias PSRR	–	at 1 kHz	40	–	–	dB
ADC SNR	–	A-weighted 0 dB PGA gain, Temperature= 25°C	–	78	–	dB
ADC THD + N	–	−3 dBFS input 0 dB PGA gain, Temperature= 25°C	–	70	–	dB
GPIO input voltage		Always lower than avddBAT	–	–	3.6	V
GPIO source impedance[14]	–	Resistance	–	–	1	kΩ
		Capacitance	–	–	10	pF

Note

14.Conditional requirement for the measurement time of 10 µs. Relaxed with longer measurement time for each GPIO input channel.

10.1.6 Current consumption

In **Table 18**, current consumption measurements are taken at input of VBAT and VDDIO combined (LDOIN = VDDIO = 3.0V).

Table 18 Current consumption Bluetooth®/LE

Operational mode	Conditions	Typ	Unit
HCI	48 MHz with Pause	1.1	mA
	48 MHz Without Pause	2.2	mA
RX	Continuous RX	5.9	mA
TX	Continuous TX - 0 dBm	5.6	mA
PDS		61	µA
HID-Off	32 kHz XTAL and 16 KB Retention RAM on	1.6	µA
Advertising	Unconnectable - 1 sec	14	µA
	Connectable undirected - 1 sec	17	µA
LE connection - SDS	Master - 1 sec	16	µA
	Slave - 1 sec	17	µA
Page scan - PDS	Interlaced - R1	122	µA
Sniff - PDS	500 ms Sniff, 1 attempt, 0 timeout - Master	132	µA
	500 ms Sniff, 1 attempt, 0 timeout - Slave	138	µA
Bi-directional data exchange	Continuous DM5 or DH5 packets - Master/Slave	6.9	mA

10.2 RF specifications

Note Table 19 and **Table 20** apply to single-ended industrial temperatures. Unused inputs are left open.

Table 19 Receiver RF specifications

Parameter	Mode and conditions	Min.	Typ.	Max.	Unit
Frequency range	–	2402	–	2480	MHz
RX sensitivity (QFN)[15]	GFSK, 0.1% BER, 1 Mbps	–	–92.0[15]	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–94.0[16]	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–88.0[16]	–	dBm
RX sensitivity (WLCSP)[15]	GFSK, 0.1% BER, 1 Mbps	–	–91.5[16]	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–93.5[16]	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–87.5[16]	–	dBm

Notes
15. Dirty TX is off.
16. Up to 1dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
17. The receiver sensitivity is measured at BER of 0.1% on the device interface.
18. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
19. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).
20. Desired signal is -64 dBm Bluetooth®-modulated signal, interferer 1 is –39 dBm sine wave at frequency f1, interferer 2 is –39 dBm Bluetooth® modulated signal at frequency f2, f0 = 2*f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.

Table 19 Receiver RF specifications *(continued)*

Parameter	Mode and conditions	Min.	Typ.	Max.	Unit
Maximum input	All data rates	–	–	–20	dBm
GFSK modulation					
C/I cochannel	GFSK, 0.1% BER[15]	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER[16]	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER[17]	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER[15]	–	–	–40.0	dB
C/I image channel	GFSK, 0.1% BER[17]	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER[17]	–	–	–20.0	dB
QPSK modulation					
C/I cochannel	p/4-DQPSK, 0.1% BER[17]	–	–	13.0	dB
C/I 1 MHz adjacent channel	p/4-DQPSK, 0.1% BER[18]	–	–	0	dB
C/I 2 MHz adjacent channel	p/4-DQPSK, 0.1% BER[17]	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	p/4-DQPSK, 0.1% BER[19]	–	–	–40.0	dB
C/I image channel	p/4-DQPSK, 0.1% BER[17]	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	p/4-DQPSK, 0.1% BER[17]	–	–	–20.0	dB
8PSK modulation					
C/I cochannel	8-DPSK, 0.1% BER[17]	–	–	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER[17]	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER[17]	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER[19]	–	–	–33.0	dB
C/I image channel	8-DPSK, 0.1% BER[17]	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER[17]	–	–	13	dB
Out-of-band blocking performance (CW)[18]					
30 MHz to 2000 MHz	BDR GFSK 0.1% BER	–	–10.0	–	dBm
2000 MHz to 2399 MHz	BDR GFSK 0.1% BER	–	–27.0	–	dBm
2498 MHz to 3000 MHz	BDR GFSK 0.1% BER	–	–27.0	–	dBm
3000 MHz to 12.75 GHz	BDR GFSK 0.1% BER	–	–10.0	–	dBm
Inter-modulation performance[15]					
Bluetooth®, interferer signal level	BDR GFSK 0.1% BER	–	–	–39.0	dBm

Notes

15.Dirty TX is off.

16.Up to 1dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.

17.The receiver sensitivity is measured at BER of 0.1% on the device interface.

18.Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).

19.Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).

20.Desired signal is -64 dBm Bluetooth®-modulated signal, interferer 1 is –39 dBm sine wave at frequency f1, interferer 2 is –39 dBm Bluetooth® modulated signal at frequency f2, f0 = 2*f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.

Table 19 Receiver RF specifications *(continued)*

Parameter	Mode and conditions	Min.	Typ.	Max.	Unit
Spurious emissions					
30 MHz to 1 GHz	–	–	–	–57.0	dBm
1 GHz to 12.75 GHz	–	–	–	–55.0	dBm

Notes

15. Dirty TX is off.
16. Up to 1dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
17. The receiver sensitivity is measured at BER of 0.1% on the device interface.
18. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
19. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).
20. Desired signal is -64 dBm Bluetooth®-modulated signal, interferer 1 is –39 dBm sine wave at frequency f1, interferer 2 is –39 dBm Bluetooth® modulated signal at frequency f2, f0 = 2*f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.

Table 20 Transmitter RF specifications

Parameter	Min	Typ	Max	Unit
Transmitter section				
Frequency range	2402	–	2480	MHz
GFSK TX power	–	5	–	dBm
EDR TX power	–	0	–	dBm
20 dB bandwidth	–	930	1000	kHz
Adjacent channel power				
|M – N| = 2	–	–	–20	dBm
|M – N| ≥ 3	–	–	–40	dBm
Out-of-band spurious emission				
30 MHz to 1 GHz	–	–	–36.0	dBm
1 GHz to 12.75 GHz	–	–	–30.0	dBm
1.8 GHz to 1.9 GHz	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–47.0	dBm
LO performance				
Initial carrier frequency tolerance	–75	–	+75	kHz
Frequency drift				
DH1 packet	–25	–	+25	kHz
DH3 packet	–40	–	+40	kHz
DH5 packet	–40	–	+40	kHz
Drift rate	–20		20	kHz/50 µs
Frequency deviation				
Average deviation in payload (sequence used is 00001111)	140	–	175	kHz
Maximum deviation in payload (sequence used is 10101010)	115	–	–	kHz
Channel spacing	–	1	–	MHz
Modulation accuracy				
p/4-DQPSK frequency stability	–10	–	10	kHz

Table 20 Transmitter RF specifications *(continued)*

<table>
<tr><th>Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>p/4-DQPSK RMS DEVM</td><td>–</td><td>–</td><td>20</td><td>%</td></tr>
<tr><td>p/4-QPSK Peak DEVM</td><td>–</td><td>–</td><td>35</td><td>%</td></tr>
<tr><td>p/4-DQPSK 99% DEVM</td><td>–</td><td>–</td><td>30</td><td>%</td></tr>
<tr><td>8-DPSK frequency stability</td><td>–10</td><td>–</td><td>10</td><td>kHz</td></tr>
<tr><td>8-DPSK RMS DEVM</td><td>–</td><td>–</td><td>13</td><td>%</td></tr>
<tr><td>8-DPSK Peak DEVM</td><td>–</td><td>–</td><td>25</td><td>%</td></tr>
<tr><td>8-DPSK 99% DEVM</td><td>–</td><td>–</td><td>20</td><td>%</td></tr>
<tr><td colspan="5">In-band spurious emissions</td></tr>
<tr><td>1.0 MHz < |M – N| < 1.5 MHz</td><td>–</td><td>–</td><td>–26</td><td>dBc</td></tr>
<tr><td>1.5 MHz < |M – N| < 2.5 MHz</td><td>–</td><td>–</td><td>–20</td><td>dBm</td></tr>
<tr><td>|M – N| > 2.5 MHz</td><td>–</td><td>–</td><td>–40</td><td>dBm</td></tr>
</table>

Table 21 Bluetooth® LE RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sensitivity (QFN)[21]	LE GFSK, 0.1% BER, 1 Mbps	–	–95.5[22]	–	dBm
RX sensitivity (WLCSP)[21]	LE GFSK, 0.1% BER, 1 Mbps	–	–94.5[22]	–	dBm
TX power	N/A	–	5.5	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[22]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

Notes

21. Dirty Tx is Off.
22. Up to 1dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
23. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Table 22 BLE2M RF specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sensitivity[24]	255 Packets	–	–90.5	–	dBm
TX power	N/A	–	5.5	–	dBm
Mod char: Delta F1 average	N/A	450	500	550	kHz
Mod char: Delta F2 max	N/A	370	–	–	kHz
Mod char: Ratio	N/A	0.8	–	–	%
Frequency drift	N/A	–50	–	50	kHz
Drift rate	N/A	–20	–	20	kHz/50µs

Note
24.Dirty Tx is Off.

Table 23 CYW20719 GPS and GLONASS band spurious emission

Parameter	Conditions	Min	Typ	Max	Unit
1570-1580 MHz	GPS	–	–160	–	dBm/Hz
1592-1610 MHz	GLONASS	–	–159	–	dBm/Hz

10.3 Timing and AC characteristics

In this section, use the numbers listed in the Reference column of each table to interpret the following timing diagrams.

10.3.1 UART timing

Table 24 UART timing specifications

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.67	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N HIGH	–	–	1.33	Bit periods

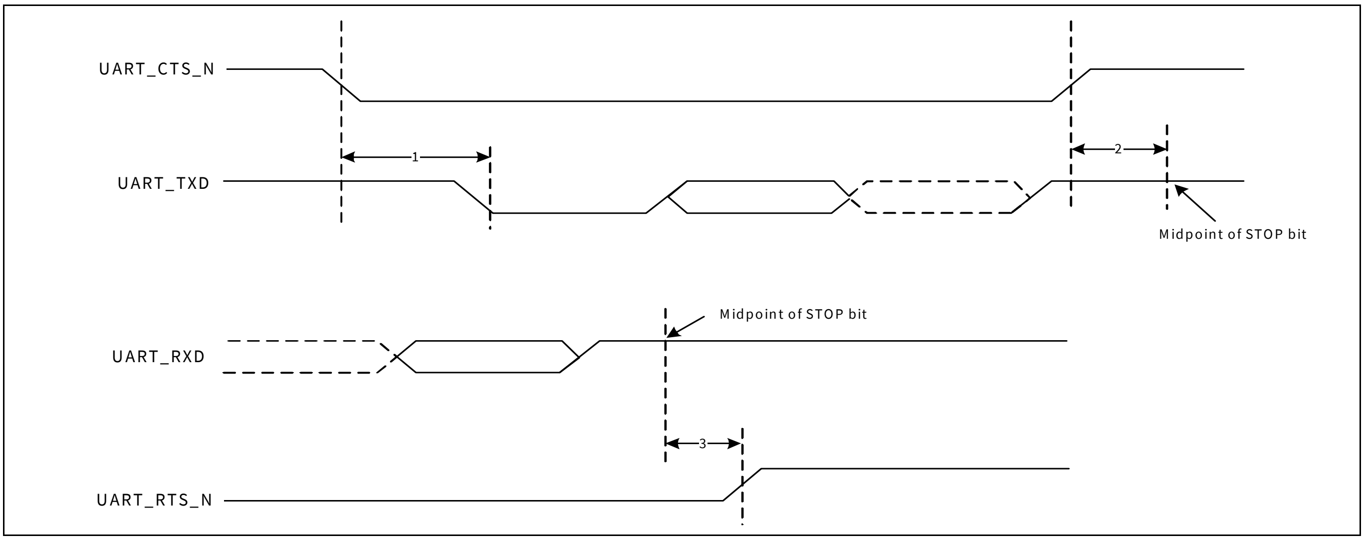


Figure 8 UART timing

10.3.2 SPI timing

The SPI interface can be clocked from 1 to 12 MHz and 24 MHz.

Table 25 and **Figure 9** show the timing requirements when operating in SPI Mode 0 and 2.

Table 25 SPI Mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

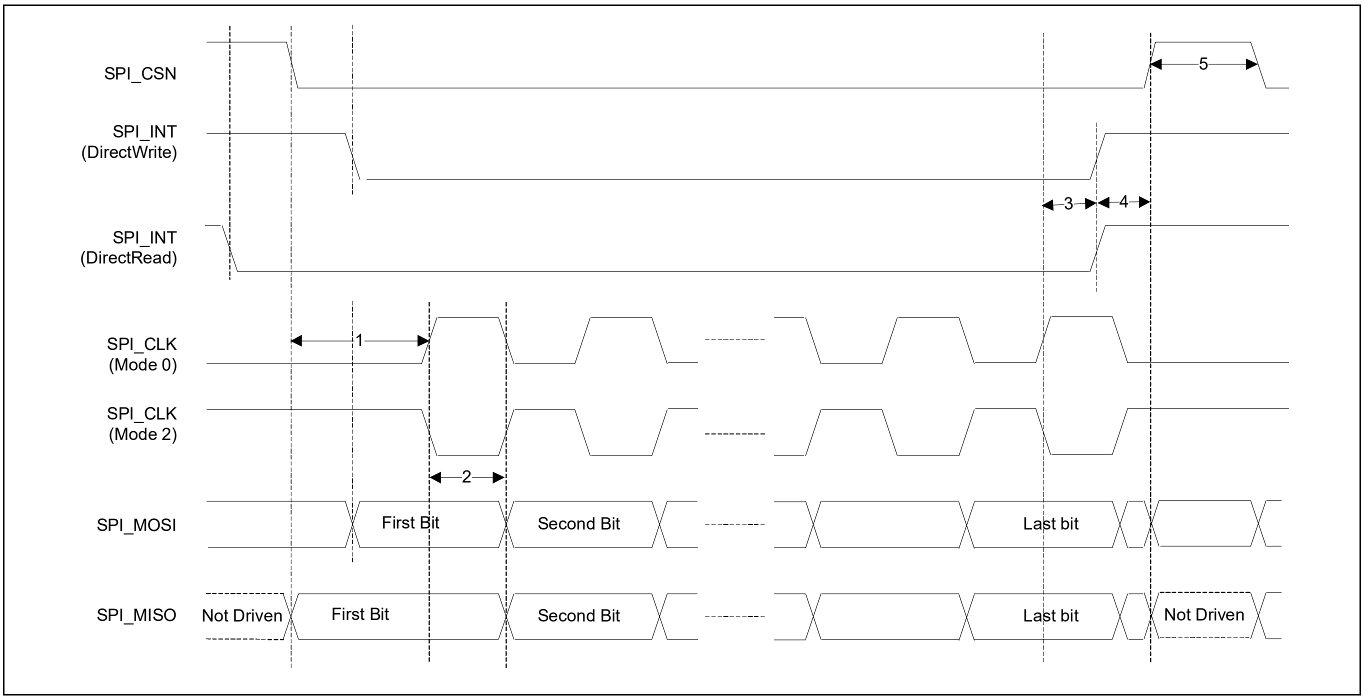


Figure 9 SPI timing, Mode 0 and 2

Table 26 and **Figure 10** show the timing requirements when operating in SPI Mode 0 and 2.

Table 26 SPI Mode 1 and 3

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

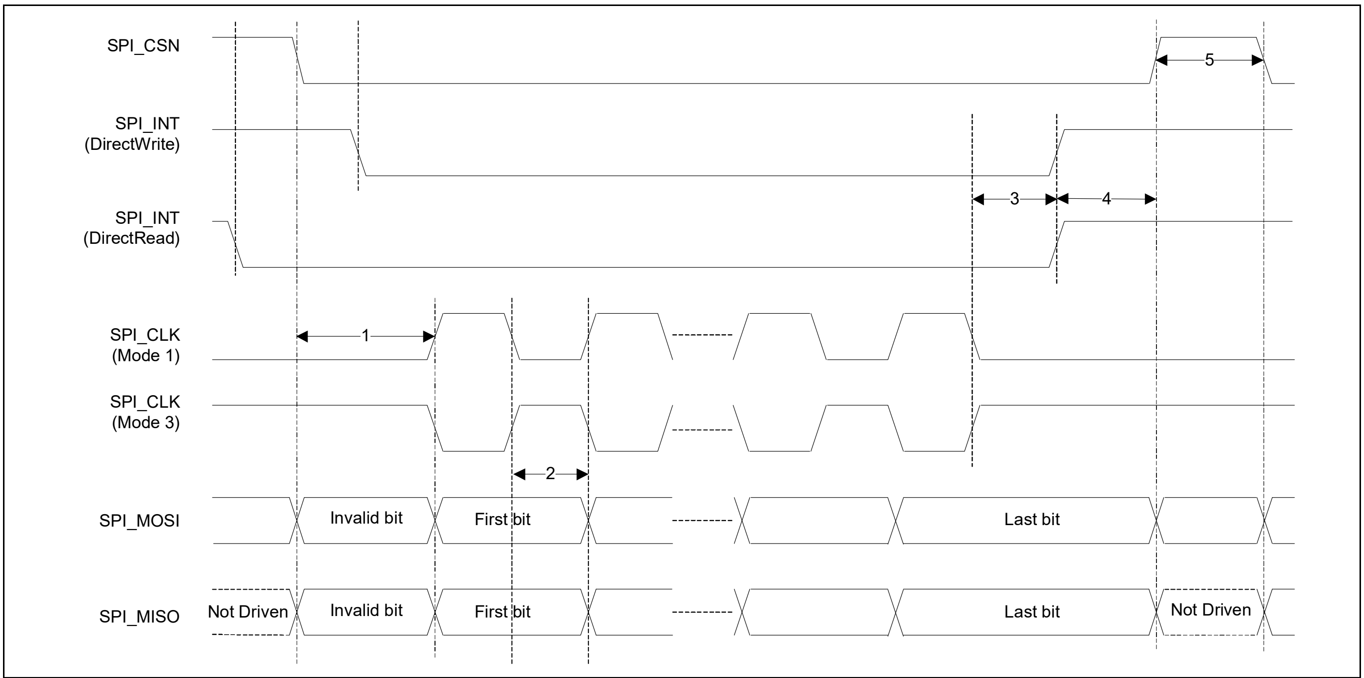


Figure 10 SPI timing, Mode 1 and 3

10.3.3 I²C compatible interface timing

The specifications in **Table 27** references **Figure 11**.

Table 27 I²C Compatible Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Min.	Max.	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	
4	Clock low time	650	–	
5	Clock high time	280	–	
6	Data input hold time[25]	0	–	
7	Data input setup time	100	–	
8	STOP condition setup time	280	–	
9	Output valid from clock	–	400	
10	Bus free time[26]	650	–	

Notes

25. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
26. Time that the CBUS must be free before a new transaction can start.

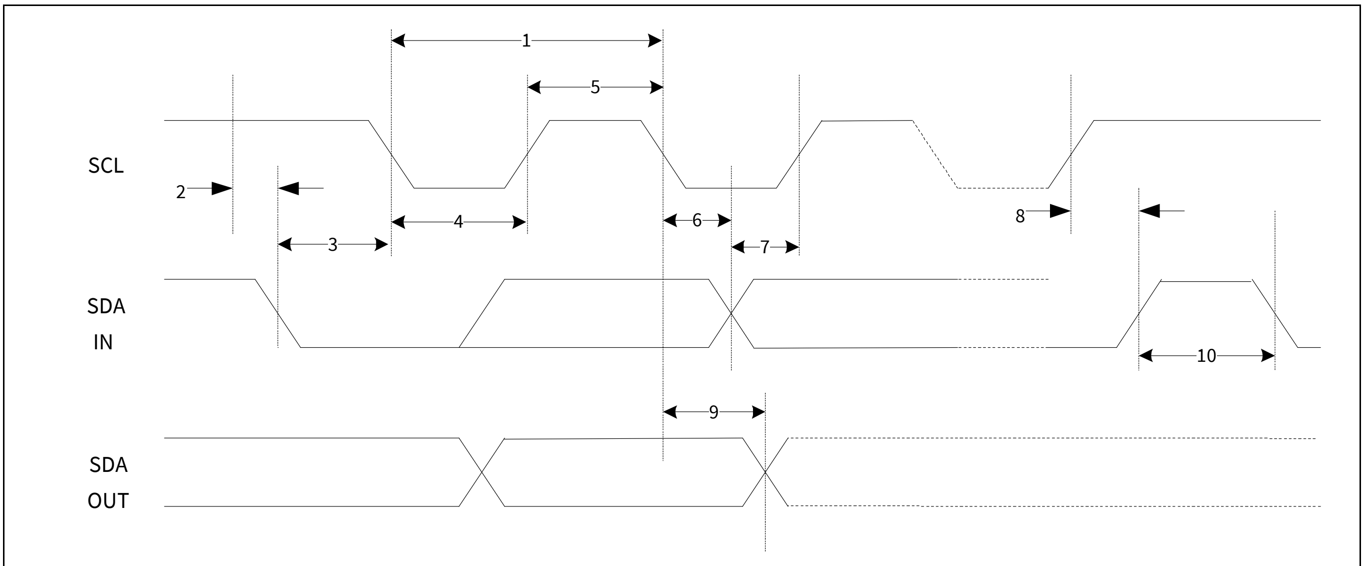


Figure 11 I²C interface timing diagram

Table 28 Timing for I²S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max.	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	[27]
Master mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[28]
LOW t_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[28]
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[29]
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[29]
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	[30]
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	[31]
Hold time t_{htr}	0	–	–	–	–	–	–	–	[30]
Receiver									
Setup time t_{sr}	–	–	–	–	$0.2T_{tr}$	–	–	–	[32]
Hold time t_{hr}	–	–	–	–	$0.2T_{tr}$	–	–	–	[32]

Notes

27. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
28. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
29. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
30. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that $t_{htr} \geq$ zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
31. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
32. The data setup and hold time must not be less than the specified receiver setup and hold time.

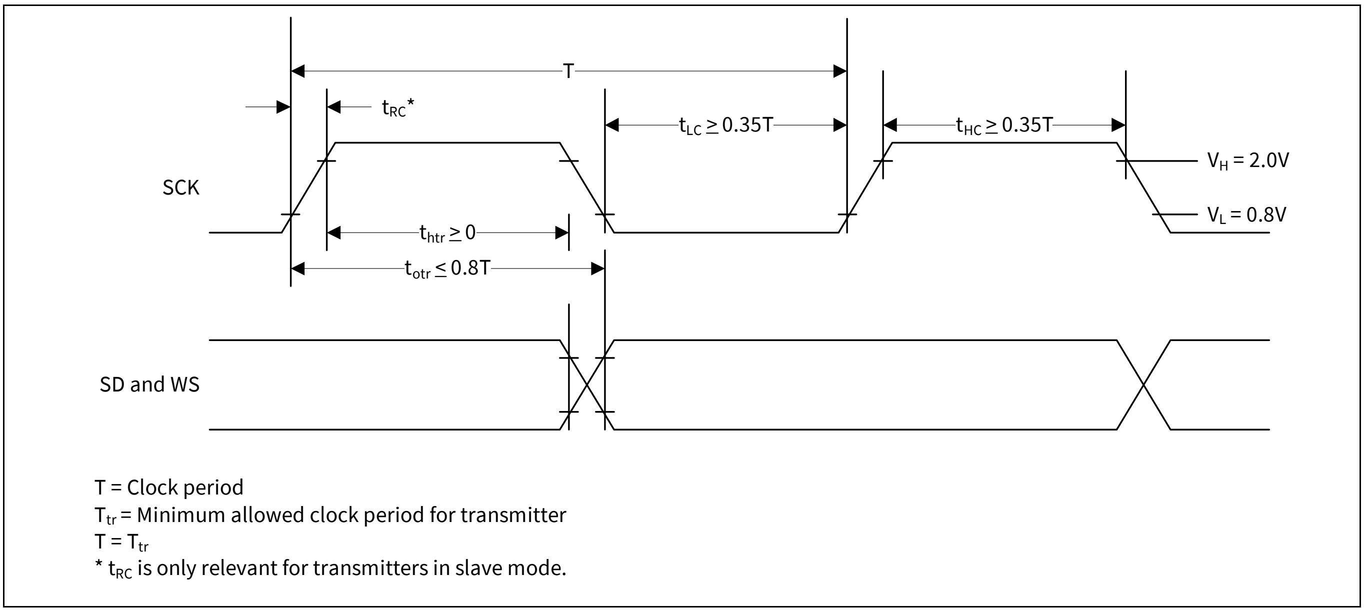


Figure 12 **I²S transmitter timing**

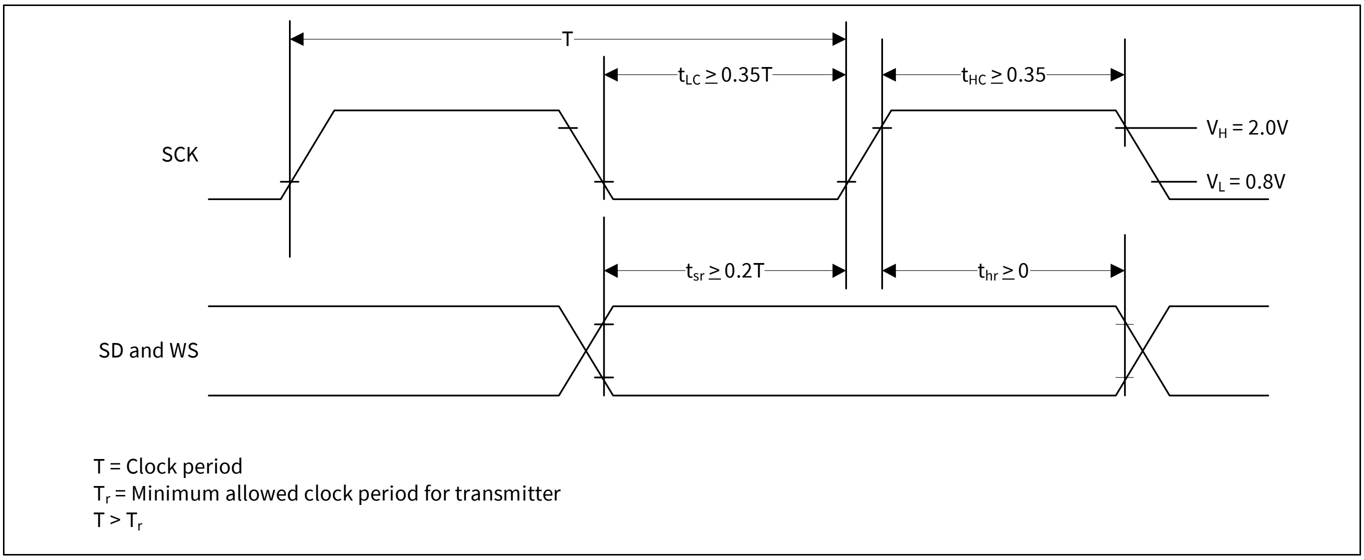
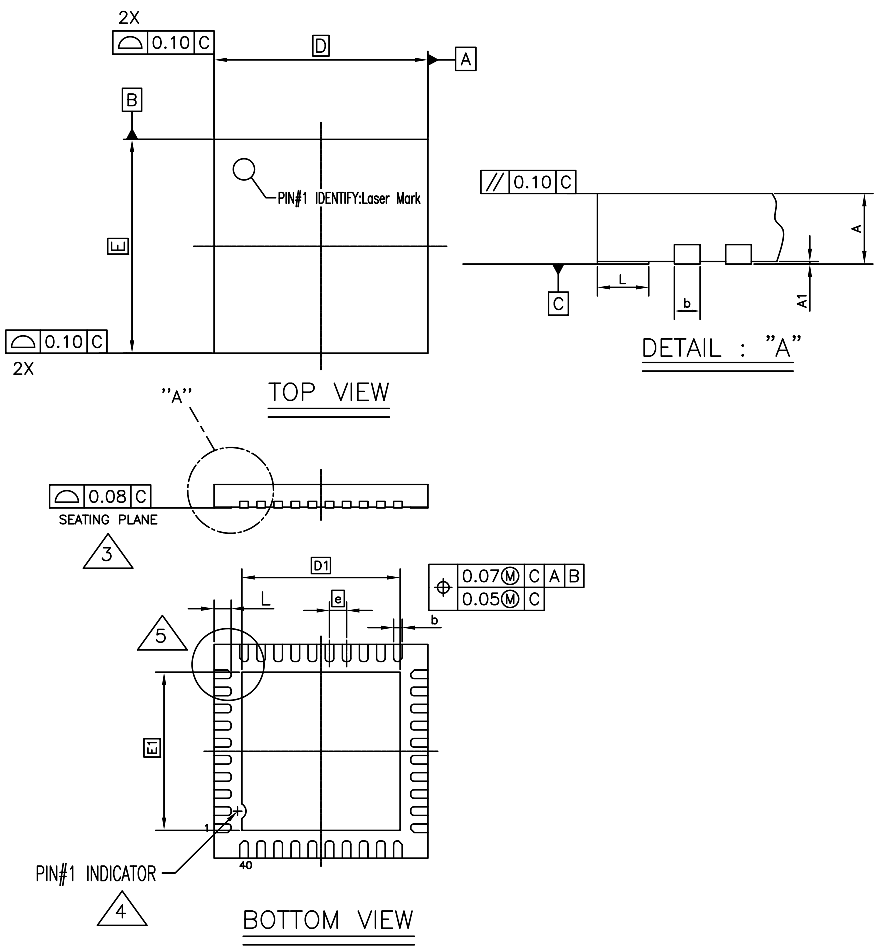


Figure 13 **I²S receiver timing**

11 Mechanical information

11.1 40-pin QFN package



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	-	-	0.05
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
D1	3.70 BSC		
E1	3.70 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
N	40		

NOTE:

1. ALL DIMENSIONS ARE IN MM.
2. MAX COPLANARITY IS 0.08mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.

3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

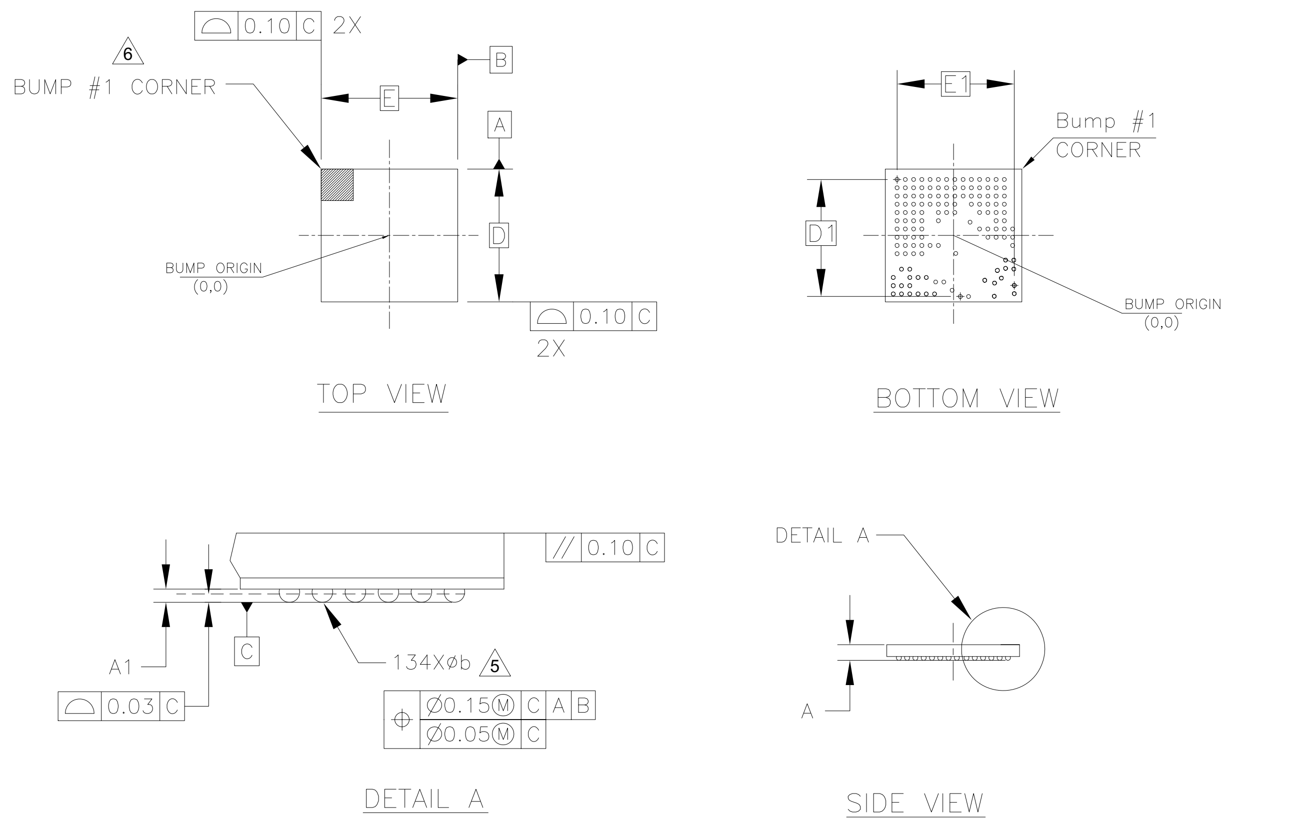
4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY.

5. EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

002-13583 *A

Figure 14 CYW20719 5.0 mm × 5.0 mm 40-pin QFN package

11.2 WLCSP package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.33
A1	0.075	-	-
D	3.22 BSC		
E	3.31 BSC		
D1	2.84 BSC		
E1	2.84 BSC		
N	134		
Ø b	0.100	0.115	0.130

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. BUMP #1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-16658 *A

Figure 15 CYW20719 3.3 × 3.2 × 0.33 mm 134-balls WLCSP package

11.3 WLCSP package keep-out

Figure 16 shows the top view of the WLCSP package (Bumps facing down).

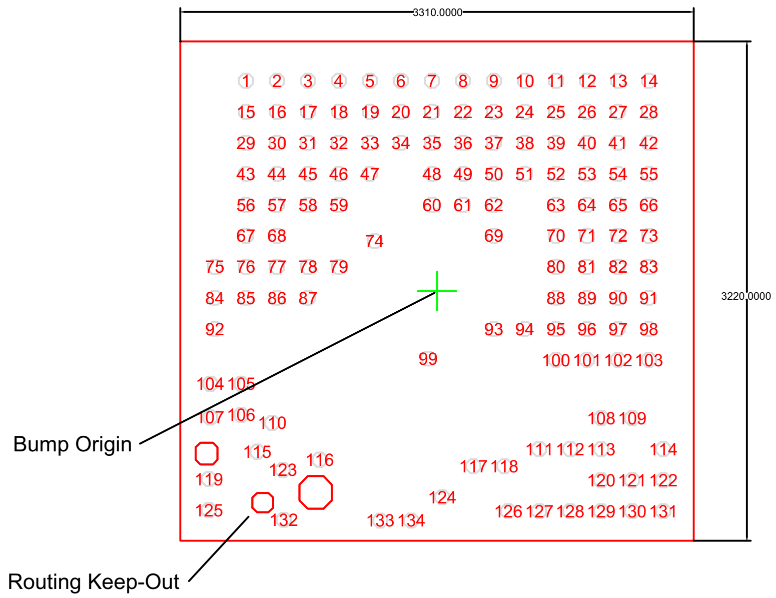


Figure 16 CYW20719YB2 WLCSP keep-out model

11.4 Tape reel and packaging specifications

Table 29 CYW20719 tape reel specifications

Parameter	Value
Quantity per reel	5000
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	12 mm
Tape pitch	8 mm

The top-left corner of the CYW20719 package is situated near the sprocket holes, as shown in **Figure 17**.

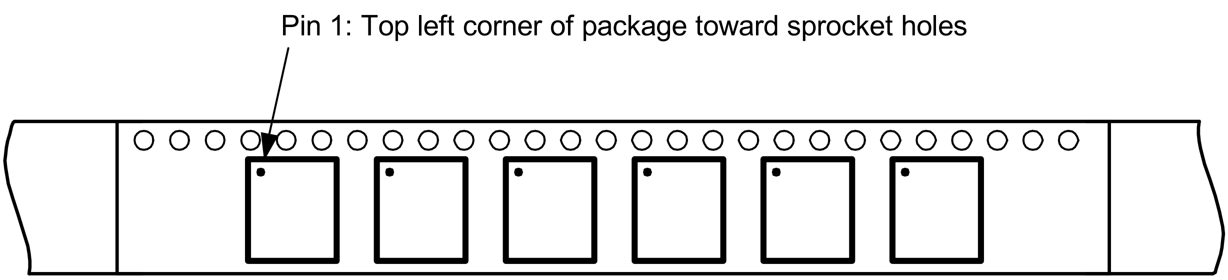


Figure 17 Pin 1 orientation

12 Ordering information

Table 30 Ordering information

Part number	Package	Ambient operating temperature
CYW20719B2KWB9G	3.2 × 3.1 134-Ball WLCSP	–30°C to 85°C
CYW20719B2KUMLG	5 × 5 40-pin QFN	–30°C to 85°C

13 Acronyms

Table 31 Acronyms used in this document

Term	Description
AFH	adaptive frequency hopping
ATT	Attribute Protocol
BBC	Bluetooth® Baseband Core
BDR	basic data rate
BR	basic data rate
BQS	Bluetooth® Qualification Body
CRC	cyclic redundancy check
ED	erroneous data
EIR	extended inquiry response
EPR	encryption pause resume
FEC	forward error correction
FPU	floating point unit
GATT	Generic Attribute Profile
GAP	generic access profile
GFSK	Gaussian Frequency Shift Keying
GPIO	general-purpose I/O
HCI	host control interface
IF	intermediate frequency
JTAG	Joint Test Action Group
L2CAP	Logical Link Control and Adaptation Protocol
LCU	link control unit
LDO	low drop-out
LE	low energy
LM	Link Manager
LO	local oscillator
LPO	low power oscillator
LSTO	link supervision time out
PA	power amplifier
PBF	packet boundary flag
PDM	pulse density modulation
PDS	Power down sleep
PLL	phase locked loop
PMU	power management unit
POR	power-on reset
PRBS	Pseudo Random Binary Sequence
PWM	pulse width modulation
QFN	quad flat no-lead
QoS	quality of service

Table 31 Acronyms used in this document *(continued)*

Term	Description
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read-only memory
RX/TX	receive/transmit
SCO	synchronous connection-oriented
SDP	Service Discovery Protocol
SDS	Shut Down Sleep
SPI	serial peripheral interface
SPIFFY	serial peripheral interface fully functional
SSP	secure simple pairing
SSR	sniff subrating
SWD	serial wire debug
TSSI	transmit signal strength indicator
UART	universal asynchronous receiver/transmitter
WLCSP	wafer level chip scale package

14 Document conventions

14.1 Units of measure

Table 32 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
dBi	decibels relative to isotropic
dBm	decibel-milliwatts
GHz	gigahertz
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
kV	kilovolt
mA	milliamperes
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
mm	millimeters
Msps	megasamples per second
mV	millivolt
µA	microampere
µF	microfarad
µm	micrometers
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*G	2022-02-14	Removed "Preliminary" status. Updated **Table 4**.
*H	2023-01-17	Migrated to the Infineon template.

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