

# EZ-PD™ CCG7SC single-port USB Type-C with PD and buck-boost controller

## General description

EZ-PD™ CCG7SC is a highly integrated single-port USB Type-C Power delivery (PD) solution with an integrated buck-boost controller. It complies to the latest USB Type-C and PD specifications, and is targeted for single-port consumer charging applications. Integration offered by EZ-PD™ CCG7SC not only reduces the BOM but also provides a footprint optimized solution for Single-port consumer charging needs. It also includes hardware-controlled protection features on the VBUS. EZ-PD™ CCG7SC supports a wide input voltage range (4 to 24 V with 40 V tolerance) and programmable switching frequency (150 to 600 kHz) in an integrated PD solution.

EZ-PD™ CCG7SC is a highly programmable USBPD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128-KB flash, 16-KB RAM and 32-KB ROM that leaves most flash available for user application use. It also includes various analog and digital peripherals such as ADC, PWMs and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging.

## Applications

- Single-port consumer charging applications
- Power source charger
- Cigarette lighter adapter (CLA)

## Features

### USBPD

- Supports one USBPD port
- Supports latest USBPD 3.1 including programmable power supply (PPS) mode
- Extended data messaging

### Type-C

- Configurable resistors  $R_p$  and  $R_d$
- VBUS provider NFET gate driver
- Integrated 100-mW VCONN power supply and control

### 1x buck-boost controller

- 150 to 600 kHz switching frequency
- 4.5 to 24 V input, 40 V tolerant
- 3.3 to 21.5 V output
- 20-mV voltage and 50-mA current steps for PPS
- Supports selectable pulse skipping mode (PSM) and forced continuous current/conduction mode (FCCM)
- Supports soft start
- Programmable spread spectrum frequency modulation for low EMI

### 1x legacy/proprietary charging block

- Supports Qualcomm QC 2.0/3.0/4.0/5.0, Apple charging 2.4 A, Samsung adaptive fast charging (AFC), USB BC 1.2

## Features

### System-level fault protection

- On-chip VBUS overvoltage protection (OVP), overcurrent protection (OCP), undervoltage protection (UVP)
- VBUS to CC short protection
- Under-voltage lockout (UVLO)
- Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
- Supports connector and board temperature measurement using external thermistors

### 32-bit MCU subsystem

- 48-MHz Arm® Cortex®-M0 CPU
- 128-KB flash
- 16-KB SRAM
- 32-KB ROM

### Peripherals and GPIOs

- Up to 13 GPIOs including two overvoltage GPIOs
- 2x 8-bit ADC
- 8x 16-bit timer/counter/PWMs (TCPWM)

### Communication interfaces

- 3x SCBs (I<sup>2</sup>C/SPI/UART/LIN)

### Clocks and oscillators

- Integrated oscillator eliminating the need for an external clock

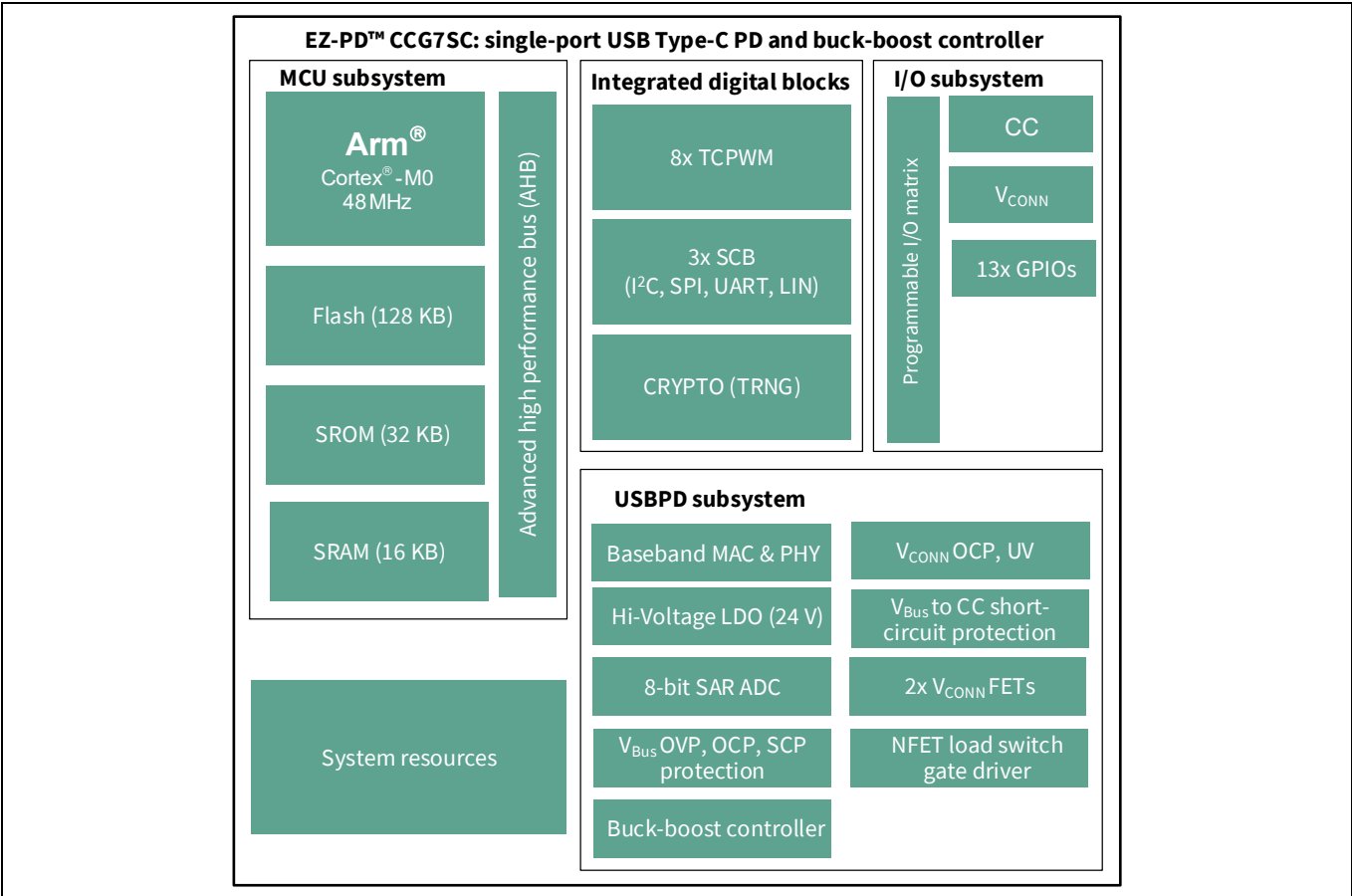
### Power supply

- 4 to 24 V input (40 V tolerant)
- 3.3 to 21.5 V output
- Integrated LDO capable of 5 V @ 75 mA

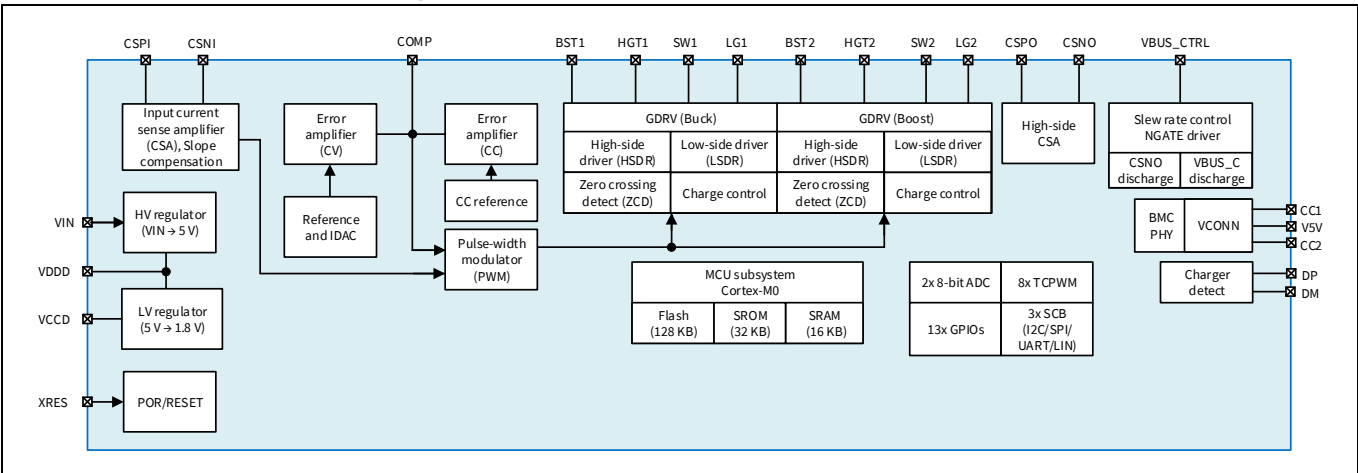
### Package

- 40-pin QFN (6 mm × 6 mm) package with -40°C to +105°C extended industrial temperature range

## Logic block diagram



## Functional block diagram



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## 1 Functional overview

### 1.1 MCU subsystem

#### 1.1.1 CPU

The Cortex-M0 in EZ-PD™ CCG7SC devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an Interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from deep sleep mode.

#### 1.1.2 Flash ROM and SRAM

EZ-PD™ CCG7SC devices have 128-KB flash and 32-KB ROM for non-volatile storage. ROM stores libraries for authentication and device drivers such as I<sup>2</sup>C, SPI, and so on. That spares flash for user application. Flash provides the flexibility to store code for any customer feature and allows firmware upgrades to meet the latest **USB power delivery specification** and application needs.

The 16-KB RAM is used under software control to store the temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

### 1.2 USB PD subsystem

This subsystem provides the interface to the Type-C USB port. This subsystem comprises:

- USB PD physical layer
- VCONN switches and 100mW VCONN source
- Undervoltage protection (UVP), overvoltage protection (OVP) on VBUS
- Output high-side current sense amplifier (HS CSA) for VBUS
- VBUS discharge control
- Gate driver for VBUS provider NFET
- Charger detection block for legacy charging (for example: BC1.2, Apple charging, and so on)
- VBUS to CC short-circuit protection

#### 1.2.1 USBPD physical layer

The USBPD subsystem contains the USBPD physical layer block and supporting circuits. The USBPD physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the PD 3.1 standard. All communication is half-duplex. The physical layer or PHY implements collision avoidance to minimize communication errors on the channel. The USBPD block includes all termination resistors ( $R_p$  and  $R_d$ ) and their switches as required by the USB Type-C spec.  $R_p$  and  $R_d$  resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. The  $R_p$  resistor is implemented as a current source.

The CCG7SC device family along with the accompanying firmware is fully compliant with revision 3.1 of the **USB power delivery specification**. The device supports programmable power supply (PPS) operation at all valid voltages from 3.3 V to 21 V.

EZ-PD™ CCG7SC devices support  $R_p$  under HW control in unconnected (standby) state to minimize standby power.

EZ-PD™ CCG7SC devices support USBPD extended messages containing data of up to 260 bytes. The extended messages are larger than expected by USBPD 2.0 hardware. As per the USBPD protocol specification, USBPD 3.1 compliant devices implement a chunking mechanism; messages are limited to revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

### 1.2.2 VCONN switches

EZ-PD™ CCG7SC internal LDO voltage regulator is capable of powering a 100mW VCONN supply for electronically marked cable assemblies (EMCA), VCONN-powered devices (VPD), and VCONN-powered accessories (VPA) as defined in the USB Type-C specification. All circuitry including VCONN switches and overcurrent protection is integrated in the device. In the event the VCONN current exceeds the VCONN OCP limit, CCG7SC can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

### 1.2.3 VBUS UVP and OVP

VBUS under-voltage and overvoltage faults are monitored using internal resistor dividers. The fault thresholds and response times are user configurable. Refer to the [EZ-PD™ configuration utility](#) for more details. In the event of a UVP or OVP, EZ-PD™ CCG7SC can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

### 1.2.4 VBUS OCP and SCP

VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. Similar to OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. Refer to the [EZ-PD™ configuration utility](#) for more details. In the event of OCP or SCP, CCG7SC can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

### 1.2.5 HS-CSA for VBUS

EZ-PD™ CCG7SC device family supports VBUS current measurement and control using an external resistor (5mΩ) in series with the VBUS path. The voltage drop across this resistor is used to measure the average output current. The same resistor is also used to sense and precisely control the output current in the PPS current foldback mode of operation.

### 1.2.6 VBUS discharge control

The chip supports high-voltage (21.5 V) VBUS discharge circuitry. Upon the detection of device disconnection, faults, or hard resets, the chip will discharge the output VBUS terminals to vSafe5V and/or vSafe0V within the time limits specified in the [USB power delivery specification](#).

### 1.2.7 Gate driver for VBUS provider NFET

EZ-PD™ CCG7SC devices have an integrated high-voltage gate driver to drive the gate of an external high-side NFET on the VBUS provider path. The gate driver drives the load switch that controls the connection between CSNO and VBUS\_C. VBUS\_CTRL is the output of this integrated high-voltage gate driver. To turn off the external NFET, the gate driver drives CSNO low to 0 V. To turn on the external NFET, it drives the gate to CSNO + 8 V. There is an optional slow turn-on feature which reduces the high-current spikes on the output. For a typical gate capacitance of 3 nF, a slow turn-on time of 2 ms to 10 ms is configurable using firmware.

### 1.2.8 Legacy charge detection and support

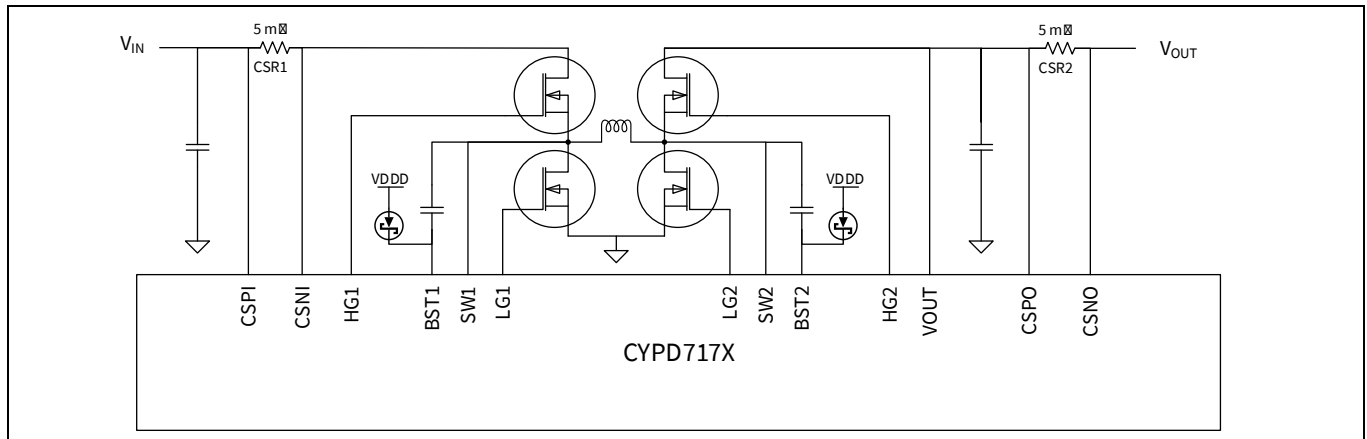
EZ-PD™ CCG7SC implements battery charger emulation and detection (source and sink) for USB BC.1.2, legacy Apple charging, Qualcomm quick charge 2.0/3.0/4.0/5.0, and Samsung AFC protocols.

### 1.2.9 VBUS to CC short protection

CC pins have integrated protection from accidental shorts to high-voltage VBUS and VBAT. EZ-PD™ CCG7SC devices can handle up to 24 V external voltage on its CC pins without damage. In the event, an overvoltage is detected on the CC pin, it can be configured to shut down the Type-C port completely. The port will resume normal operation once the CC voltage detected is within normal range.

### 1.3 Buck-boost subsystem

The buck-boost subsystem in EZ-PD™ CCG7SC devices can be configured to operate in buck-boost mode, buck-only mode or boost-only mode. While buck-boost mode requires four external switching FETs, buck-only and boost-only modes require only two FETs. **Figure 1** shows the buck-boost subsystem's main external components and connections.



**Figure 1 Buck-boost schematic showing external components**

Buck-boost subsystem in EZ-PD™ CCG7SC devices have the following key functional blocks:

- High side (cycle-by-cycle) current sense amplifier
- High side and low side gate driver
- Pulse width modulator
- Error amplifier

#### 1.3.1 High side (cycle-by-cycle) current sense amplifier (CSA)

EZ-PD™ CCG7SC device's buck-boost controller implements peak current control in both boost and buck modes. A high side current sense amplifier (CSA) is used for peak current sensing through an external resistor (5mΩ; see CSR1 in **Figure 1**) placed in series with the buck control FET. This current sense amplifier has a high bandwidth and a very wide common mode range. This current sense resistor is connected to the CSA block through pins CSPI and CSNI as shown in **Figure 1**. This block implements slope compensation to avoid sub-harmonic oscillation for the internal current loop. In addition to peak current sensing, it provides a current limit comparator for shutting off the buck-boost converter if the current hits an upper threshold which is programmable.

#### 1.3.2 High-side gate driver and low-side gate driver (HG/LG)

EZ-PD™ CCG7SC' buck-boost controller provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pin. The high side gate drivers drive the high side external FET with a nominal VGS of 5V. The High-side gate driver has a programmable drive strength to drive external FET. An external capacitor and Schottky diode form a bootstrap network to collect and store the high voltage source ( $V_{IN} + \sim 5V$  for HG1 and  $V_{BUS} + \sim 5V$  for HG2) needed to drive the high-side FET. The low side gate driver drives the low side external FET with a nominal VGS of 5V using energy sourced from EZ-PD™ CCG7SC' internal LDO regulator and stored in the capacitor between PVDD and PGND. Low-side gate driver has programmable drive strength to drive external FET. In addition to drive strength, the high-side gate driver and the low-side gate driver have programmable options for deadtime control and zero-crossing levels. High-side gate driver and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The gate drivers for the switching FETs function at their nominal drive voltage levels (5V) provided the VIN voltage is between 4.5V and 24V.



### 1.3.3 Error amplifier (EA)

EZ-PD™ CCG7SC' buck-boost controller contains two error amplifiers for output voltage and current regulation. The error amplifier is a trans-conductance type amplifier with single compensation pin (COMP) to ground for both the voltage and current loops. In voltage regulation, the output voltage is compared with the internal reference voltage and the output of EA is fed to the PWM block. In current regulation, the average current is sensed by VBUS high side current sense amplifier through the external resistor. The output of the VBUS CSA is compared with an internal reference in error amplifier block and EA output is fed to the PWM block. EZ-PD™ CCG7SC firmware configures and controls the integrated programmable error amplifier circuit for achieving the required VBUS voltage output from the power section.

### 1.3.4 Pulse width modulator (PWM)

EZ-PD™ CCG7SC device family's PWM block generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design.

EZ-PD™ CCG7SC devices have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: pulse skipping mode (PSM) and forced continuous conduction mode (FCCM).

### 1.3.5 Pulse skipping mode (PSM)

In pulse skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, EZ-PD™ CCG7SC devices monitor the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the EZ-PD™ CCG7SC devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

### 1.3.6 Forced continuous conduction mode (FCCM)

In Forced continuous conduction mode (FCCM), the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. "backwards" or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

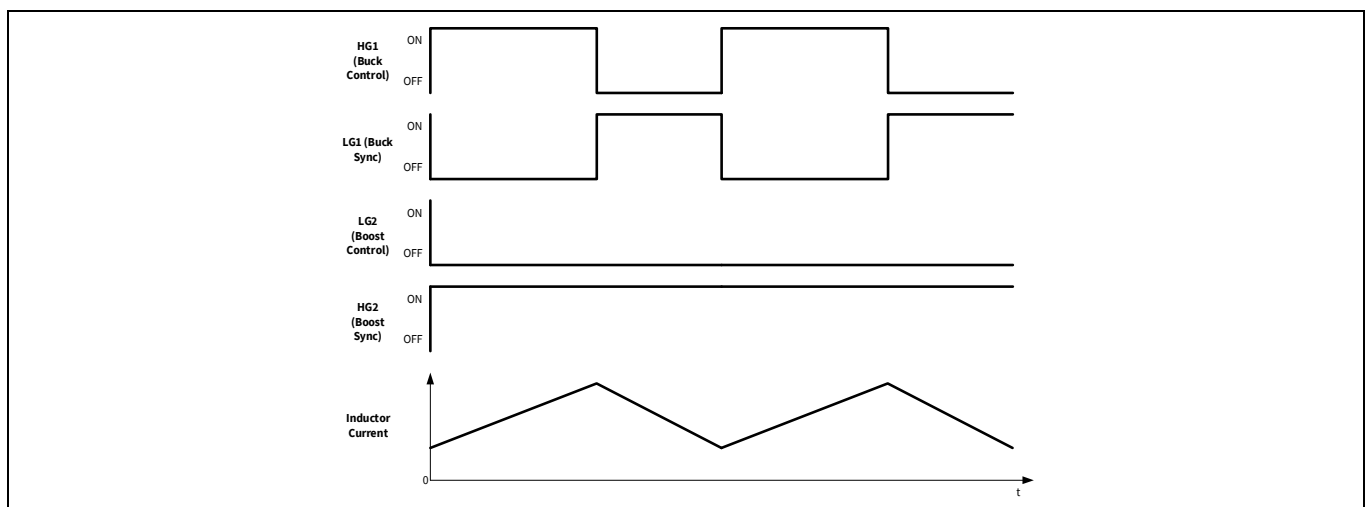


### 1.4 Buck-boost controller operation regions

The input-side CSA's output is compared with the output of the error amplifier to determine the pulse width of the PWM. PWM block compares the input voltage and output voltage to determine the buck, boost, and buck-boost regions. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact VIN vs VOUT thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

#### 1.4.1 Buck region operation (VIN >> VBUS)

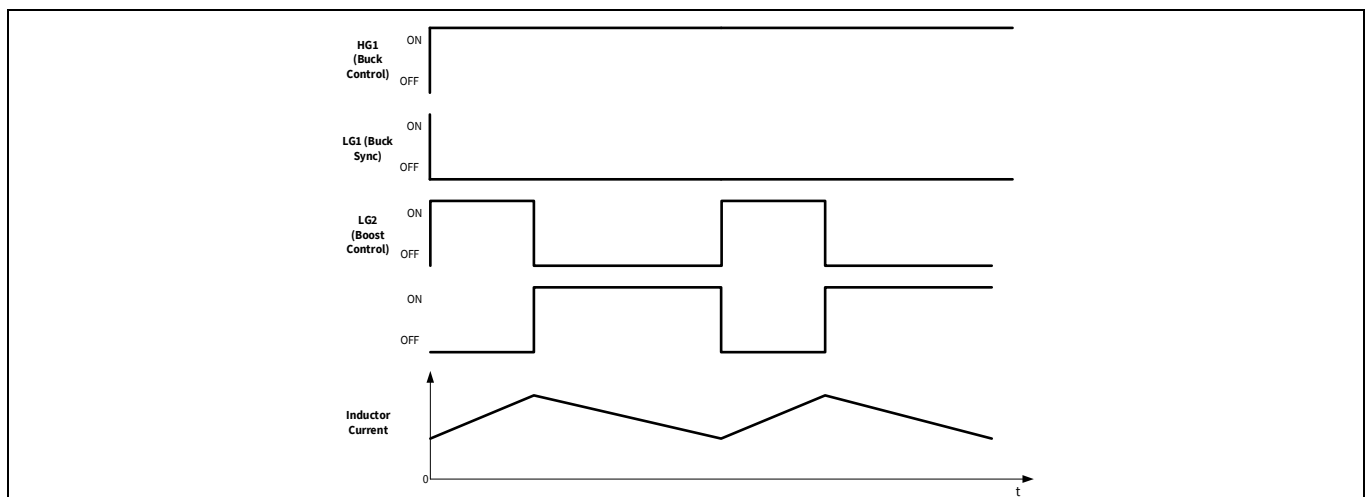
When the VIN voltage is significantly higher than the required VBUS voltage, EZ-PD™ CCG7SC devices operate in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in [Figure 2](#).



**Figure 2** Buck operation waveforms

#### 1.4.2 Boost region operation (VIN << VBUS)

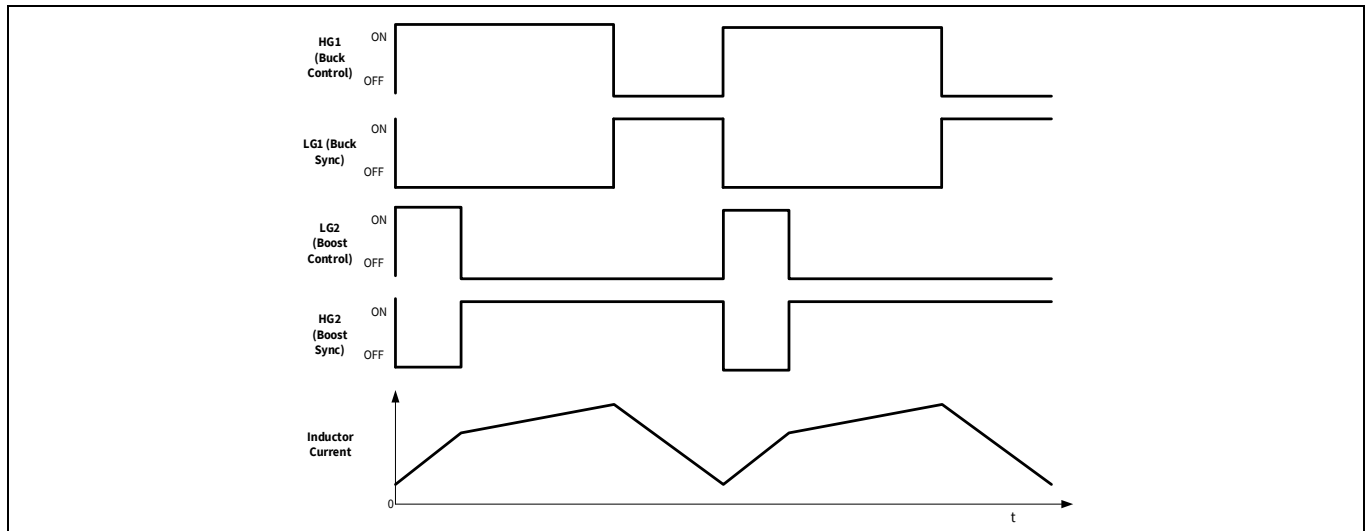
When the VIN voltage is significantly lower than the required VBUS voltage, EZ-PD™ CCG7SC devices operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned off and the buck control FET turned on. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in [Figure 3](#).



**Figure 3** Boost operation waveforms

### 1.4.3 Buck-boost region 1 operation ( $V_{IN} \sim V_{BUS}$ )

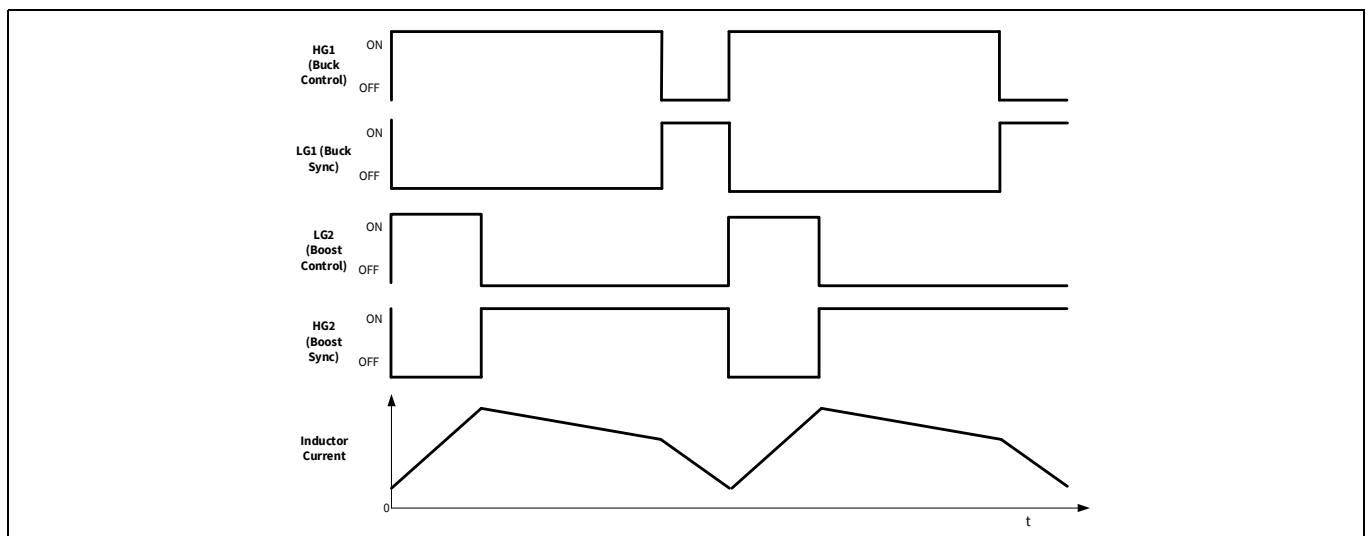
When the  $V_{IN}$  voltage is slightly higher than the required  $V_{BUS}$  voltage, EZ-PD™ CCG7SC devices operate in the buck-boost region 1. In this region, the boost side works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in [Figure 4](#).



**Figure 4** Buck-boost region 1 ( $V_{IN} \sim V_{BUS}$ ) operation waveforms

### 1.4.4 Buck-boost region 2 operation ( $V_{IN} \sim V_{BUS}$ )

When the  $V_{IN}$  voltage is slightly lower than the required  $V_{BUS}$  voltage, EZ-PD™ CCG7SC devices operate in the buck-boost region 2. In this region, the buck side works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in [Figure 5](#).



**Figure 5** Buck-boost region 2 ( $V_{IN} \sim V_{BUS}$ ) operation waveforms

## 1.4.5 Switching frequency and spread spectrum

EZ-PD™ CCG7SC devices offer programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

## 1.5 Analog blocks

### 1.5.1 ADC

EZ-PD™ CCG7SC devices have two 8-bit SAR ADCs for general purpose A-D conversion applications in the chip. The ADCs can be accessed from the GPIOs through an on-chip analog mux. See [Table 25](#) for detailed specs on the ADCs.

## 1.6 Integrated digital blocks

### 1.6.1 Serial communication block (SCB)

EZ-PD™ CCG7SC devices have three SCB blocks that can be configured for I<sup>2</sup>C, SPI, UART or LIN. These blocks implement full multi-master and slave I<sup>2</sup>C interfaces capable of multi-master arbitration. This I<sup>2</sup>C implementation is compliant with the standard Philips I<sup>2</sup>C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I<sup>2</sup>C port I/Os for SCB0 are overvoltage tolerant (OVT). The I<sup>2</sup>C ports for SCB1-2 are not OVT tolerant.

### 1.6.2 Timer, counter, pulse-width modulator (TCPWM)

The TCPWM block of EZ-PD™ CCG7SC devices support eight timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

### 1.7 I/O subsystem

The EZ-PD™ CCG7SC devices have 13 GPIOs including the I<sup>2</sup>C and SWD pins which can also be used as GPIOs. The GPIO block implements the following:

- Eight output drive modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Disabled
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in deep sleep mode)
- Selectable slew rates for dV/dt related noise control.
- Overvoltage tolerance (OVT) on one pair of GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB Type-C port are also fixed in order to reduce internal multiplexing complexity. Data output registers and pin state register store, respectively, the values to be driven on the pins and the states of the pins themselves.

The configuration of the pins can be done by the programming of registers through software for each digital I/O port. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during deep sleep mode or remain ON. If the operation is restored using reset, then the pins shall go the high-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The IOs (on data bus) do not draw current on power down.

### 1.8 System resources

#### 1.8.1 Watchdog timer

EZ-PD™ CCG7SC devices have a watchdog timer running from the internal low-speed oscillator (ILO). This allows Watchdog operation during Deep sleep and generate a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the reset cause register.

#### 1.8.2 Reset

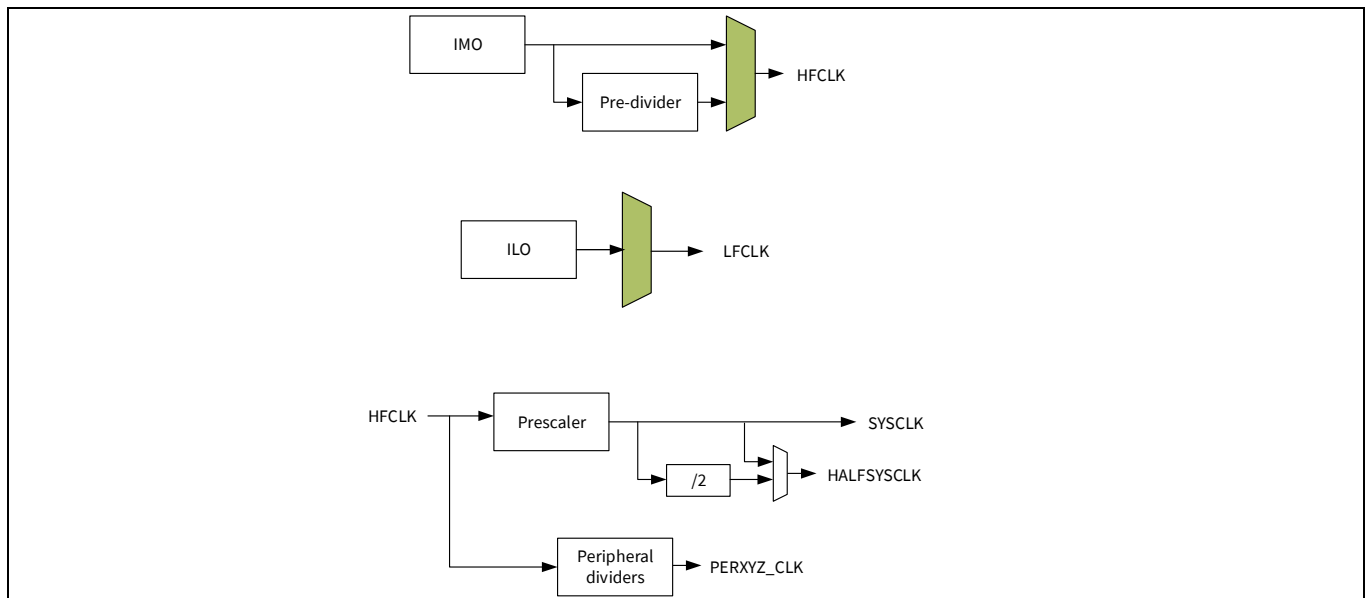
EZ-PD™ CCG7SC devices can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is preserved through reset and allows application firmware to determine the cause of the reset. XRES pin is the dedicated pin for asserting an external hardware reset.

#### 1.8.3 Clock system

EZ-PD™ CCG7SC devices have a fully integrated clock with no external crystal required. EZ-PD™ CCG7SC device's clock system is responsible for providing clocks to all sub-systems that require clocks (SCB and PD) and for switching between different clock sources.

The HFCLK signal can be divided down as shown to generate synchronous clocks for the digital peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The clock dividers generate either enabled clocks (that is, 1 in N clocking where N is the divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors).

In [Figure 6](#), PERXYZ\_CLK represents the clocks for different peripherals.



**Figure 6** Clocking architecture of EZ-PD™ CCG7SC devices

#### 1.8.4 IMO clock source

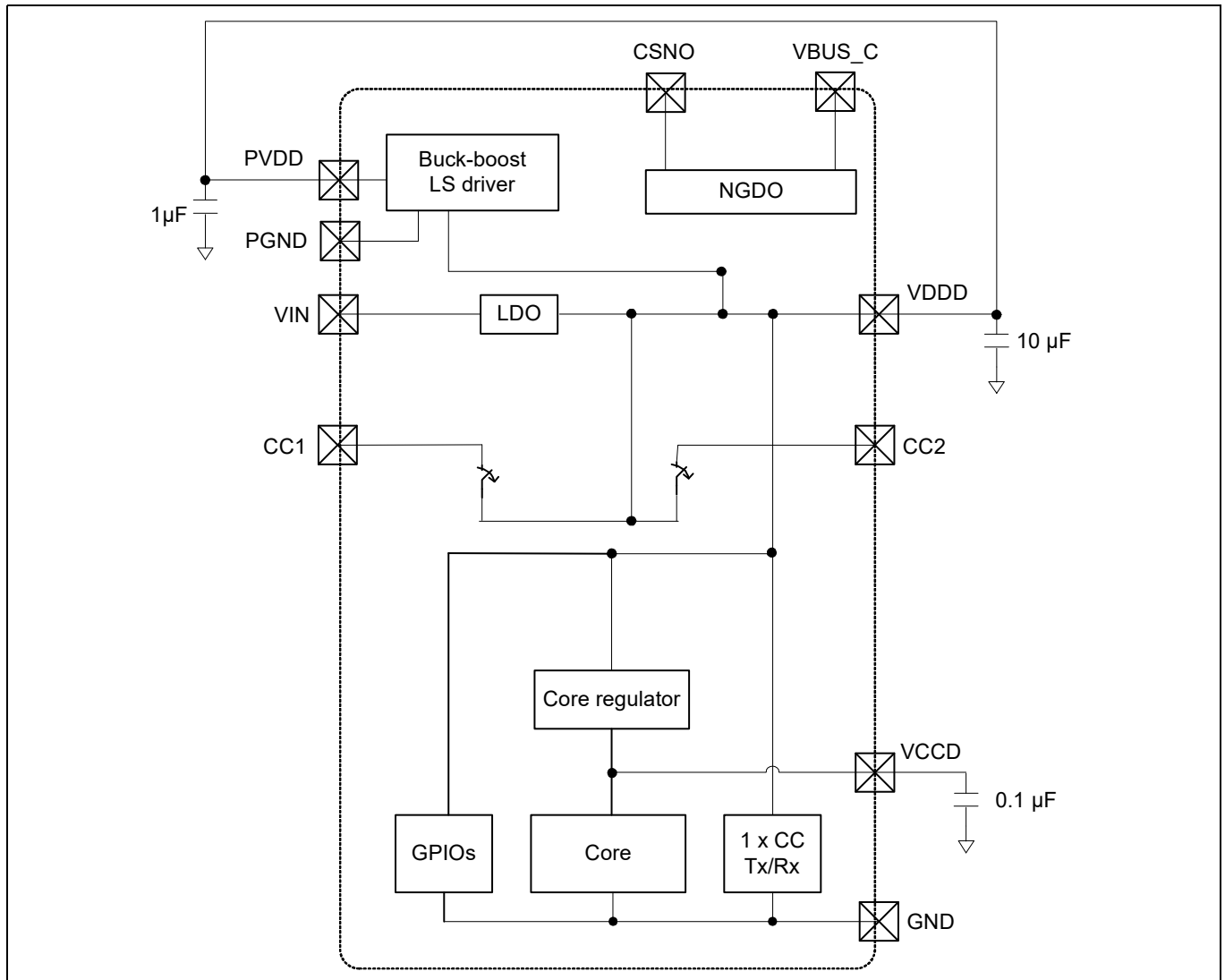
The internal main oscillator is the primary source of internal clocking in EZ-PD™ CCG7SC devices. IMO default frequency for EZ-PD™ CCG7SC devices is 48 MHz $\pm$ 2%.

#### 1.8.5 ILO clock source

The internal low-power oscillator is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB suspend (deep sleep) mode.

## 2 Power subsystem

**Figure 7** shows an overview of the power subsystem architecture for EZ-PD™ CCG7SC devices. The power subsystem of EZ-PD™ CCG7SC devices operate from VIN supply which can vary from 4 V to 24 V. The VDDD pin, the output of an internal 5V LDO, gets input from VIN supply. The current capability of the VDDD pin is up to 75mA including internal as well as external loads. EZ-PD™ CCG7SC devices have two different power modes: Active and Deep sleep, transitions between which are managed by the power system. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1-μF capacitor for the regulator stability only. This pin is not supported as a power supply for external load.



**Figure 7** Power system requirement block diagram

## 2.1 VIN under-voltage lockout (UVLO)

EZ-PD™ CCG7SC supports UVLO to allow the device to shut down when the input voltage is below the reliable level. It guarantees predictable behavior when the device is up and running.

## 2.2 Using external VDDD supply

By default, external VDDD is not supported for EZ-PD™ CCG7SC devices. However, usage of external VDDD supply can be enabled using firmware. The prerequisite for enabling external forcing of VDDD is to always maintain VIN higher than VDDD.

## 2.3 Power modes

The Power modes of the device accessible and observable by the user are listed in [Table 1](#).

**Table 1** Power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep controller is sequencing the system out of reset
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep sleep regulator powers logic, but only low-frequency clock is available.
XRES	Power is valid and XRES is asserted. Core is powered down.



## 3 Pin list

**Table 2 40-QFN package pinout**

S#	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
1	HG1	-0.5	PVDD+0.5 <sup>[1, 2, 3]</sup>	Buck high side gate driver output. Connect to the buck (input) side control (high side) FET gate. Use a wide trace to minimize inductance of this connection. Absolute min and max are with respect to SW1 pin.
2	SW1	-0.7	35	Negative power rail of the buck high side gate driver. This is also connected to one input terminal of zero current detection of buck low side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
3	LG1	-0.5	PVDD+0.5 <sup>[1]</sup>	Buck low side gate driver output. Connect to the buck (input) side sync (low side) FET gate. Use a wide trace to minimize inductance of this connection.
4	PGND	-0.3	0.3	Ground of low side gate driver. This is also connected to one input terminal of zero current detection of buck low side gate driver. Connect directly to the port's board ground plane.
5	PVDD	–	VDDD	Supply of low side gate driver. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ CCG7SC IC as possible.
6	LG2	-0.5	PVDD+0.5 <sup>[1]</sup>	Boost low side gate driver output. Connect to the boost (output) side control (low side) FET gate. Use a wide trace to minimize inductance of this connection.
7	VOUT	-0.3	24	Output of the Buck-boost converter. This is also connected to one input terminal of reverse current protection of Boost high side gate driver. Connect to the boost sync (high side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
8	SW2	-0.3	24	Negative power rail of the boost high side gate driver. This is also connected to one input terminal of reverse current protection of boost high side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
9	HG2	-0.5	PVDD+0.5 <sup>[1, 4]</sup>	Boost high side gate driver output. Connect to the boost (output) side sync (high side) FET gate. Use a wide trace to minimize inductance of this connection.
10	BST2	–	PVDD+0.5 <sup>[1, 4]</sup>	Boosted power supply of the boost high side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST2. Also, connect a bootstrap capacitor from this pin to SW2.
11	VBUS_CTRL	-0.5	32	VBUS NFET gate driver output. Connect to the provider NFET's gate.
12	COMP	-0.5	PVDD+0.5 <sup>[1]</sup>	Error amplifier output pin. Connect a compensation network to GND. Contact Infineon® for assistance in designing the compensation network.
13	VBUS_C	-0.3	24	Type-C connector VBUS voltage. Connect to the Type-C connector's VBUS pin.
14	CSNO	-0.3	24	Negative input of output current sensing amplifier. Connect to negative terminal of the output current sense resistor.

### Notes

1. Maximum voltage must not exceed 6 V.
2. Maximum absolute voltage w.r.t GND must not exceed 40 V.
3. The absolute maximum value is with respect to SW1.
4. The absolute maximum value is with respect to SW2.

**Table 2** 40-QFN package pinout (continued)

S#	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
15	CSPO	-0.3	24	Positive input of output current sensing amplifier. Connect to positive terminal of the output current sense resistor.
16	CC2	-0.5	24	Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
17	CC1	-0.5	24	Type-C connector configuration channel 1. Connect directly to the CC1 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
18	DP_GPIO0/ P0.0	-0.5	PVDD+0.5 <sup>[1]</sup>	USB D+/GPIO: D+ for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7SC does not support USB data transmission on this pin.
19	DM_GPIO1/ P0.1	-0.5	PVDD+0.5 <sup>[1]</sup>	USB D-/GPIO: D- for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7SC does not support USB data transmission on this pin.
20	VDDD	–	6	5-V LDO output. Connect a 1-μF ceramic bypass capacitor to this pin.
21	GPIO2/ P0.2	-0.5	PVDD+0.5 <sup>[1]</sup>	General purpose IO, available for system level function.
22	GPIO3/ P0.3	-0.5	PVDD+0.5 <sup>[1]</sup>	
23	GPIO4/ P0.5	-0.5	PVDD+0.5 <sup>[1]</sup>	
24	CGND	-0.3	0.5	CC block ground. Connect to the exposed pad (EPAD).
25	GPIO5/ P1.4	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO
26	GPIO6/ P1.3	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO
27	GPIO7/ P1.2	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO
28	GPIO8/ P1.1	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO/SWD programming and debug data signal
29	GPIO9/ P1.0	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO/SWD programming and debug clock signal
30	GPIO10/ P2.2	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO
31	XRES	-0.5	PVDD+0.5 <sup>[1]</sup>	External reset – active low. Contains a 3.5-KΩ to 8.5-KΩ internal pull-up.
32	GPIO11	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO
33	GPIO12	-0.5	PVDD+0.5 <sup>[1]</sup>	GPIO
34	GND	–	–	Chip ground. Connect to the exposed pad (EPAD).
35	VDDD	–	6	5-V LDO output. Connect a 10-μF bypass capacitor to this pin.
36	VCCD	–	–	1.8-V core LDO output. Connect a 0.1-μF bypass capacitor to ground. Do not connect anything else to this pin.
37	VIN	-0.3	40	4V–24V input supply. Connect a ceramic bypass capacitor to GND close to this pin.
38	CSPI	-0.3	40	Positive input of input current sense amplifier. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
39	CSNI	-0.3	40	Negative input of Input current sense amplifier. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.

## Notes

1. Maximum voltage must not exceed 6 V.
2. Maximum absolute voltage w.r.t GND must not exceed 40 V.
3. The absolute maximum value is with respect to SW1.
4. The absolute maximum value is with respect to SW2.

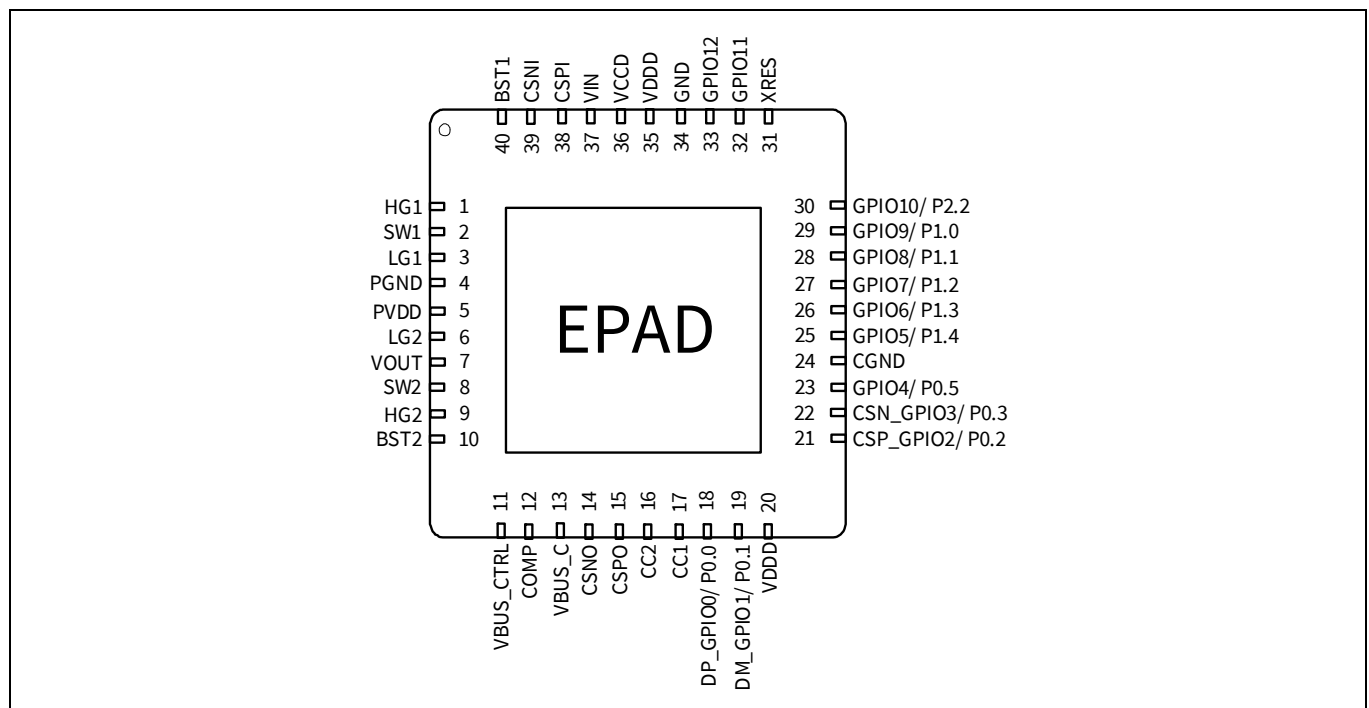
## Pin list

**Table 2** 40-QFN package pinout (continued)

S#	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
40	BST1	–	PVDD+0.5 <sup>[1, 2, 3]</sup>	Boosted power supply of the buck high side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST1. Also, connect a bootstrap capacitor from this pin to SW1.
–	EPAD	–	–	Exposed ground pad. Connect directly to pin 36 and pin 22.

### Notes

1. Maximum voltage must not exceed 6 V.
2. Maximum absolute voltage w.r.t GND must not exceed 40 V.
3. The absolute maximum value is with respect to SW1.
4. The absolute maximum value is with respect to SW2.



**Figure 8** EZ-PD™ CCG7SC 40-QFN pinout

## 4 EZ-PD™ CCG7SC programming and bootloading

There are two ways to program application firmware into a EZ-PD™ CCG7SC device:

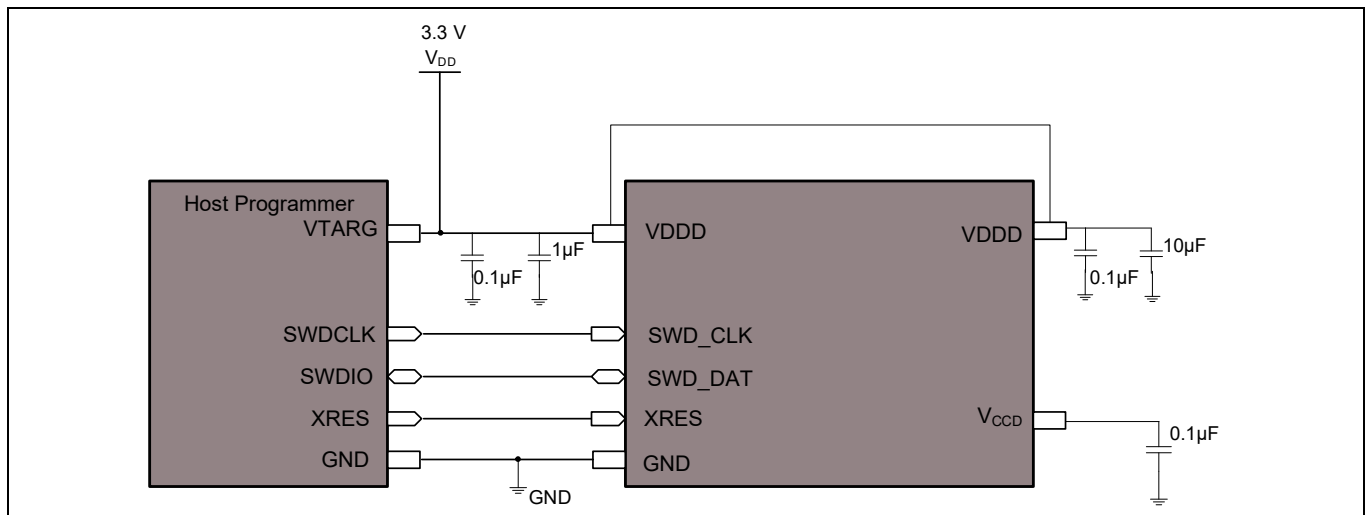
1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, I2C)

Generally, the EZ-PD™ CCG7SC devices are programmed over SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the EZ-PD™ CCG7SC device's application firmware can be updated via the appropriate bootloader interface. By default, the EZ-PD™ CCG7SC devices ship with a combined I2C/CC bootloader. Infineon® strongly recommends customers to use the [EZ-PD™ configuration utility](#) to turn off the application FW update over CC or I2C interface in the firmware that is updated into EZ-PD™ CCG7SC's flash before mass production. This prevents unauthorized firmware from being updated over CC interface in the field. If you desire to retain the application firmware update over CC/ I2C interfaces feature post-production for on-field firmware updates, contact [Infineon Sales](#) for further guidelines.

### 4.1 Programming the device flash over SWD interface

The EZ-PD™ CCG7SC family of devices can be programmed using the SWD interface. Infineon® provides programming hardware called [CY8CKIT-005 MiniProg4 kit](#), which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file.

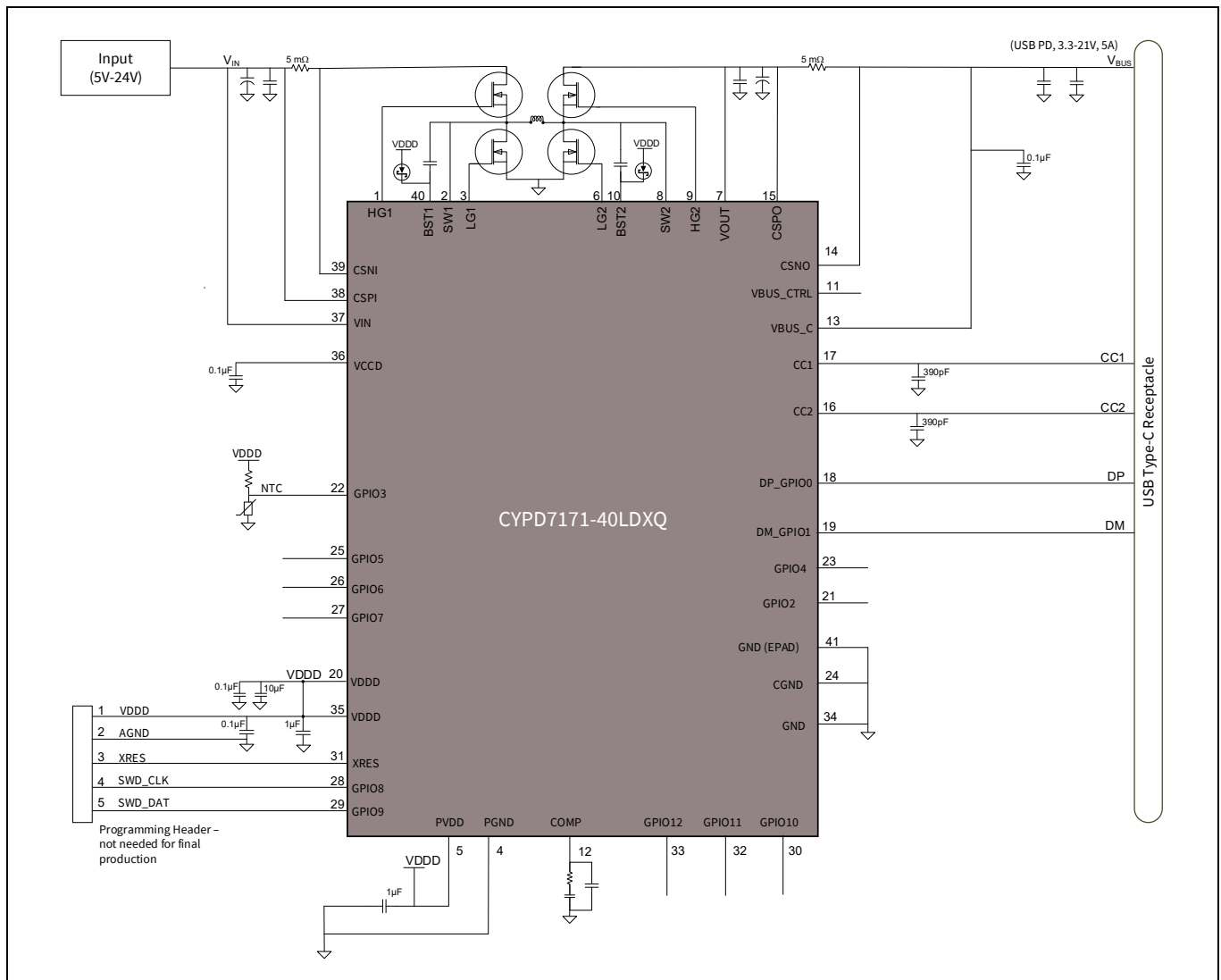
As shown in the block diagram (see [Figure 9](#)), the SWD\_DAT and SWD\_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pins of EZ-PD™ CCG7SC device. If the EZ-PD™ CCG7SC device is powered using an on-board power supply, it can be programmed using the "reset programming" option. For more details, refer the [CCGx \(CYPDxxxx\) programming specifications](#).



**Figure 9** Connecting the programmer to CYPD7XXX device

## 5 Applications

**Figure 10** illustrates a single-port cigarette lighter adapter (CLA) application block diagram using EZ-PD™ CCG7SC. CLA is powered by the car battery and is used for charging the mobile/tablet/notebook. In this application, CCG7SC will always be in DFP role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck-boost controller to supply the required voltage and current. The DP/DM lines of the Type-C receptacles are connected to CCG7SC to support legacy charging protocols such as QC3.0, Samsung AFC, Apple 2.4A charging, BC v1.2, and so on. When no load is connected to the USB Type-C port, CCG7SC remains in Standby mode without switching on the buck-boost controller.



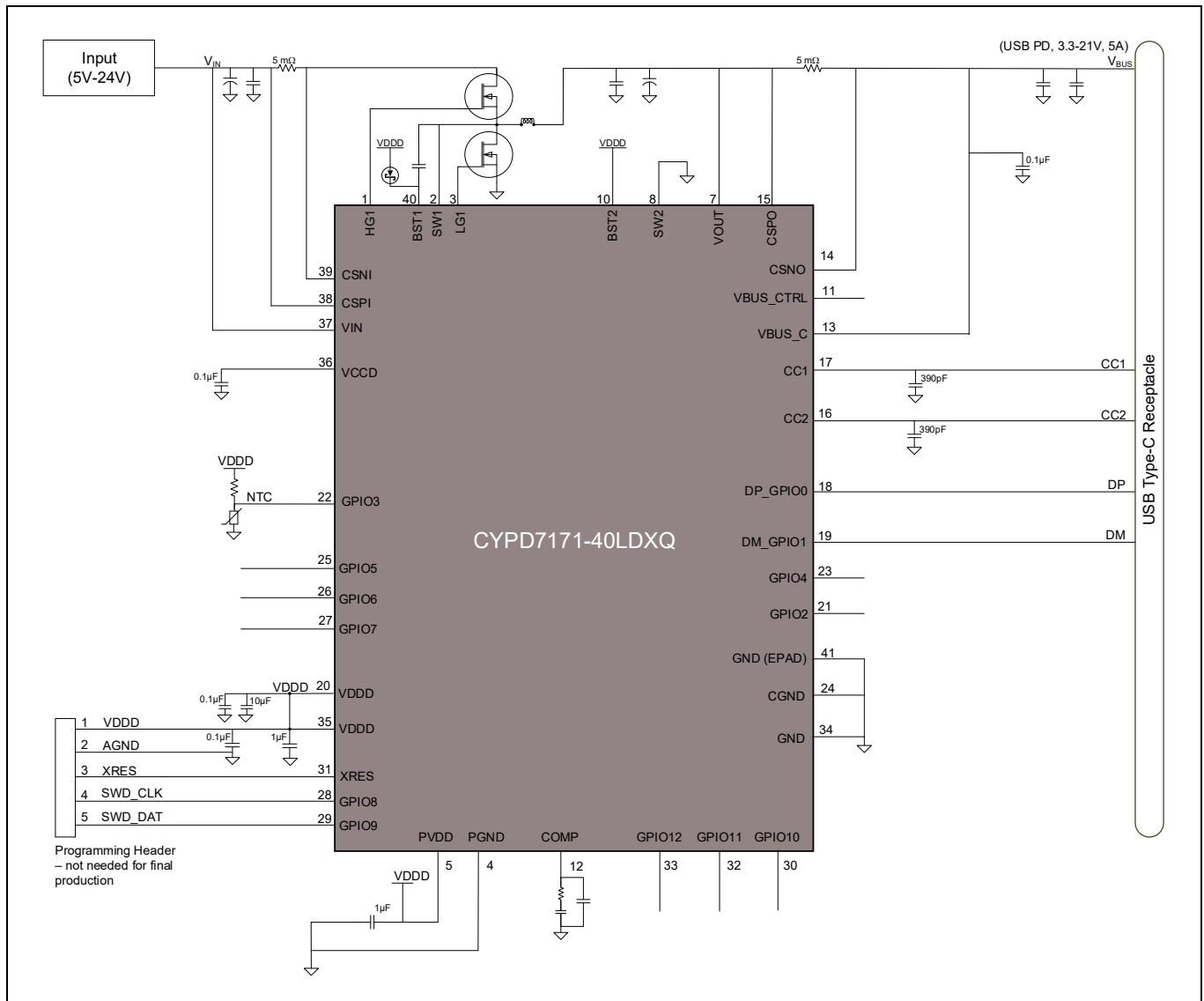
**Figure 10** EZ-PD™ CCG7SC CLA applications diagram

**Figure 11** shows a buck only mode application block diagram using CCG7SC. This application uses the integrated buck controller to supply the required voltage and current to the connected device. This application is identical to the CLA application, except that this application uses only buck topology when compared to the buck-boost

## Applications

topology in the CLA application. In a buck application, the negotiated voltage should always be lower than the input voltage.

If the input voltage drops lower than the output voltage, then the output voltage will not be maintained and the port will shut down. This application can also be configured to support the legacy charging protocols – BC1.2 DCP, Qualcomm QC2.0/3.0, Apple charging, and Samsung AFC.



**Figure 11** EZ-PD™ CCG7SC charger and adapter application diagram - Step-down (buck) DCDC converter only

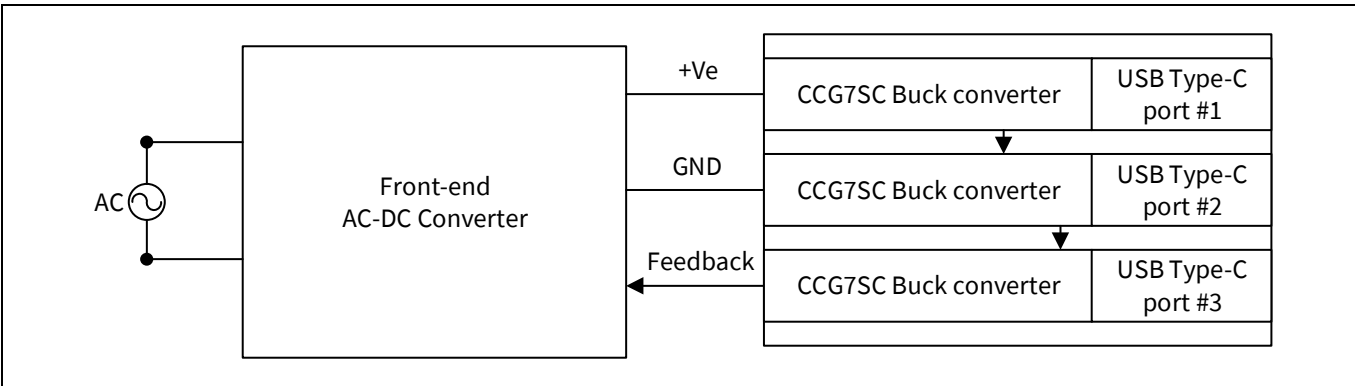
## Applications

The USB-PD multi (3)-port charger and adapter solution for AC-DC power application can be achieved with a combination of one **CCG7DC** and one CCG7SC controller, or with three individual CCG7SC controllers. **Figure 12** illustrates USB-PD multi (3)-port charger and adapter solution for AC-DC power application block diagram using EZ-PD™ CCG7DC and CCG7SC. Here CCG7DC will be supporting to provide required voltage current for two ports and CCG7SC will be supporting to provide required voltage current for third (single) port. **Figure 13** illustrates USB-PD multi (3)-port charger and adapter solution for AC-DC power application block diagram using EZ-PD™ CCG7SC. Here three CCG7SC controllers will support to provide required voltage current for three ports.

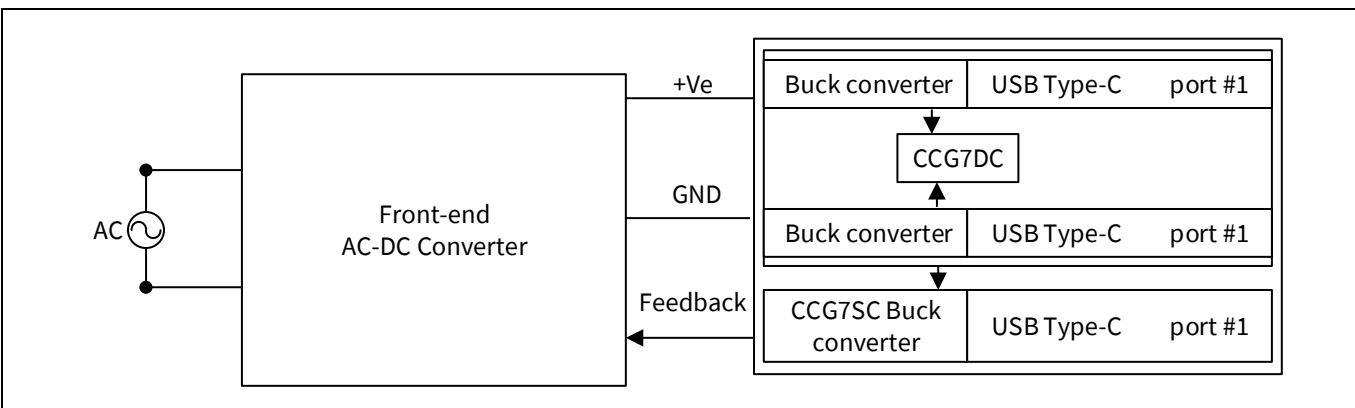
The front-end AC-DC converter has the capability to produce the requested output voltage and the buck converter ensures that the defined **USB power delivery specification** and performance are met for multiport adapter applications.

In this application, CCG7DC / CCG7SC will always be in DFP role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck controller to supply the required voltage and current.

The DP/DM lines of the Type-C receptacles are connected to CCG7DC / CCG7SC to support legacy charging protocols such as QC3.0, Samsung AFC, Apple 2.4A charging, BC v1.2, and so on. When no load is connected to the USB Type-C port, CCG7DC remains in Standby mode without switching the buck converter.



**Figure 12** CCG7SC-based 3 port charger and adapter solution



**Figure 13** CCG7DC+CCG7SC-based 3 port charger and adapter solution



**Table 3** provides the consumer charging applications GPIO pin mapping for the application diagram in **Figure 10**.

**Table 3 Consumer charging applications GPIO pin mapping for application diagram in Figure 10**

Pin #	Pin name	Function	GPIO	Consumer charging applications
18	DP_GPIO0	USB DP of Type-C port. Supports BC 1.2, QC, Apple charging and AFC.	P0.0	DP
19	DM_GPIO1	USB DM of Type-C port. Supports BC 1.2, QC, Apple charging and AFC.	P0.1	DM
22	GPIO3	Thermistor	P0.3	NTC
28	GPIO8	Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7SC device.	P1.1	GPIO
29	GPIO9	Connect to the host programmer's SWDDAT (data) for programming the EZ-PD™ CCG7SC device.	P1.0	

## 6 Electrical specifications

### 6.1 Absolute maximum ratings

**Table 4** Absolute maximum ratings<sup>[5]</sup>

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
$V_{IN\_MAX}$	Maximum input supply voltage	–	–	40	V	–
$V_{DDD\_MAX}$	Maximum supply voltage relative to $V_{SS}$	–	–	6		–
$V_{5V\_MAX}$	Maximum supply voltage relative to $V_{SS}$	–	–	6		–
$V_{BUS\_C\_MAX}$	Max $V_{BUS\_C}$ (P0/P1) voltage relative to $V_{SS}$	–	–	24		–
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins	–	–	24		–
$V_{GPIO\_ABS}$	Inputs to GPIO	–0.5	–	$V_{DDD} + 0.5$		–
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6		–
$I_{GPIO\_ABS}$	Maximum current per GPIO	–25	–	25	mA	–
$I_{GPIO\_INJECTION}$	GPIO injection current, max for $V_{IH} > V_{DDD}$ , and min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	–	–	2000	V	All pins.
ESD_CDM	Electrostatic discharge charged device model	–	–	500		Charged device model ESD
LU	Pin current for latch-up	–100	–	100	mA	–
$T_J$	Junction temperature	–40	–	125	°C	–

#### Note

- Usage above the absolute maximum conditions listed in **Table 4** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

### 6.2 Device-level specifications

All specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$  and  $T_J \leq 125^{\circ}\text{C}$ , except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

#### 6.2.1 DC specifications

**Table 5 DC specifications (operating conditions)**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V <sub>IN</sub>	Input supply voltage	4.0	–	24	V	–
SID.PWR#1A	V <sub>IN_BB</sub>	Buck-boost operating input supply voltage	4.5	–	24		–
SID.PWR#2	V <sub>DDD_REG</sub>	VDDD output with VIN 5.5 V to 24 V, max load = 75 mA	4.6	–	5.5		–
SID.PWR#2A	V <sub>DDD_BYPASS</sub>	VDDD output with VIN 4.5 V to 5.5 V, max load = 75 mA	V <sub>IN</sub> -0.7		5.5		–
SID.PWR#3	V <sub>DDD_MIN</sub>	VDDD output with VIN 4 V to 4.5 V, max load = 20mA	V <sub>IN</sub> - 0.2	–	–		–
SID.PWR#20	VBUS	VBUS_C valid range	3.3	–	21.5		–
SID.PWR#5	V <sub>CCD</sub>	Regulated output voltage (for core Logic)	–	1.8	–		–
SID.PWR#16	C <sub>EFC_VCCD</sub>	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic
SID.PWR#17	C <sub>EXC_VDDD</sub>	Power supply decoupling capacitor for V <sub>DDD</sub>	–	10	–	μF	
SID.PWR#18	C <sub>EXV</sub>	Bootstrap supply capacitor (BST1, BST2)	–	0.1	–		
SID.PWR#24	I <sub>DD_ACT</sub>	Supply current at 0.4 MHz switching frequency	–	50	–	mA	T <sub>A</sub> = 25°C, VIN = 12 V. CC IO IN transmit or receive, no I/O sourcing current, No VCONN load current, CPU at 24 MHz, PD port active. Buck-boost converter on, 3-nF gate driver capacitance.

#### Deep Sleep mode

SID_DS1	$I_{DD\_DS1}$	$V_{IN} = 12\text{ V}$ . CC wakeup on, Type-C not connected, Source mode	–	80	–	$\mu\text{A}$	Type-C not attached, CC enabled for wakeup. $R_p$ connection should be enabled for the PD port. $T_A = 25^{\circ}\text{C}$ . All faults disabled.
SID_DS2	$I_{DD\_DS2}$	$V_{IN} = 12\text{ V}$ , GPIO wake-up	–	50	–		USBPD disabled. Wake-up from GPIO. $T_A = 25^{\circ}\text{C}$ . All faults disabled.
SID_DS3	$I_{DD\_DS3}$	$V_{IN} = 12\text{ V}$ . CC wakeup on, Type-C not connected, Source mode	–	300	–		Type-C not attached, CC enabled for wakeup. $R_p$ connection should be enabled for the PD port. $T_A = 25^{\circ}\text{C}$ . All faults disabled.

### 6.2.2 CPU

**Table 6 CPU specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	$F_{CPU}$	CPU input frequency	–	–	48	MHz	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , all $V_{DD}$
SID.PWR#19	$T_{DEEPSLEEP}$	Wake-up from Deep Sleep mode	–	35	–	$\mu\text{s}$	–
SYS.XRES#5	$T_{XRES}$	External reset pulse width	5	–	–		

### 6.2.3 GPIO

**Table 7 GPIO DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#9	$V_{IH\_CMOS}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS input
SID.GIO#10	$V_{IL\_CMOS}$	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		
SID.GIO#11	$V_{IH\_TTL}$	LVTTL input	2.0	–	–		$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#12	$V_{IL\_TTL}$	LVTTL input	–	–	0.8		$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#7	$V_{OH\_3V}$	Output voltage high level	$V_{DD} - 0.6$	–	–		$I_{OH} = -4 \text{ mA}$ , $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#8	$V_{OL\_3V}$	Output voltage low level	–	–	0.6		$I_{OL} = 10 \text{ mA}$ , $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#2	$R_{pu}$	Pull-up resistor when enabled	3.5	5.6	8.5	$k\Omega$	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#3	$R_{pd}$	Pull-down resistor when enabled	3.5	5.6	8.5		
SID.GIO#4	$I_{IL}$	Input leakage current (absolute value)	–	–	2	nA	$+25^{\circ}\text{C } T_A$ , 3-V $V_{DD}$
SID.GIO#5	$C_{PIN\_A}$	Max pin capacitance	–	–	22	pF	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , capacitance on DP, DM pins
SID.GIO#6	$C_{PIN}$	Max pin capacitance	–	3	7		$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , all $V_{DD}$ , all other I/Os
SID.GIO#13	$V_{HYSTTL}$	Input hysteresis, LVTTL, $V_{DD} > 2.7 \text{ V}$	100	–	–	mV	$V_{DD} > 2.7 \text{ V}$
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.1 \times V_{DD}$	–	–		–

**Table 8 GPIO AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#16	$T_{RISEF}$	Rise time in fast strong mode	2	–	12	ns	$C_{load} = 25 \text{ pF}$ , $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#17	$T_{FALLF}$	Fall time in fast strong mode	2	–	12		
SID.GIO#18	$T_{RISES}$	Rise time in slow strong mode	10	–	60		
SID.GIO#19	$T_{FALLS}$	Fall time in slow strong mode	10	–	60		
SID.GIO#20	$F_{GPIO\_OUT1}$	GPIO $F_{OUT}$ ; $3.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ . Fast strong mode.	–	–	16	MHz	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
SID.GIO#21	$F_{GPIO\_OUT2}$	GPIO $F_{OUT}$ ; $3.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ . Slow strong mode.	–	–	7		
SID.GIO#22	$F_{GPIO\_IN}$	GPIO input operating frequency; $3.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ .	–	–	16		

**Table 9 GPIO OVT DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	-140	-	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT_GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5	-	8.5	kΩ	-40°C ≤ T <sub>A</sub> ≤ +105°C, all V <sub>DDD</sub>
SID.GPIO_20VT_GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value	3.5	-	8.5		-40°C ≤ T <sub>A</sub> ≤ +105°C, all V <sub>DDD</sub>
SID.GPIO_20VT_GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	-	-	2	nA	+25°C T <sub>A</sub> , 3-V V <sub>DDD</sub>
SID.GPIO_20VT_GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	-	-	10	pF	-40°C ≤ T <sub>A</sub> ≤ +105°C, all V <sub>DDD</sub>
SID.GPIO_20VT_GIO#33	GPIO_20VT_Voh	GPIO_20VT output voltage high level	V <sub>DDD</sub> -0.6	-	-	V	I <sub>OH</sub> = -4 mA
SID.GPIO_20VT_GIO#36	GPIO_20VT_Vol	GPIO_20VT output voltage low level	-	-	0.6		I <sub>OL</sub> = 8 mA
SID.GPIO_20VT_GIO#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input	2	-	-		-40°C ≤ T <sub>A</sub> ≤ +105°C, all V <sub>DDD</sub>
SID.GPIO_20VT_GIO#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input	-	-	0.8		-40°C ≤ T <sub>A</sub> ≤ +105°C, all V <sub>DDD</sub>
SID.GPIO_20VT_GIO#43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100	-	-	mV	-40°C ≤ T <sub>A</sub> ≤ +105°C, all V <sub>DDD</sub>
SID.GPIO_20VT_GIO#45	GPIO_20VT_ITOT_GPIO	GPIO_20VT maximum total sink pin current to ground	-	-	95	mA	V (GPIO_20VT pin) > V <sub>DDD</sub>

**Table 10 GPIO OVT AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT rise time in fast strong mode	1	-	15	ns	All V <sub>DDD</sub> , C <sub>load</sub> = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT fall time in fast strong mode	1	-	15		
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT rise time in slow strong mode	10	-	70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT Fall time in slow strong mode	10	-	70		
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3 V ≤ V <sub>DDD</sub> ≤ 5.5 V. Fast strong mode.	-	-	33	MHz	All V <sub>DDD</sub>
SID.GPIO_20VT_GIO#50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3 V ≤ V <sub>DDD</sub> ≤ 5.5 V. Slow strong mode.	-	-	7		
SID.GPIO_20VT_GIO#52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ V <sub>DDD</sub> ≤ 5.5 V	-	-	8		

### 6.2.4 XRES

**Table 11 XRES DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	$V_{IH\_XRES}$	Input voltage high threshold on XRES pin	$0.7 \times V_{DDD}$	–	–	V	CMOS input
SID.XRES#2	$V_{IL\_XRES}$	Input voltage low threshold on XRES pin	–	–	$0.3 \times V_{DDD}$		
SID.XRES#3	$C_{IN\_XRES}$	Input capacitance on XRES pin	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	$0.05 \times V_{DDD}$	–	mV	–

### 6.3 Digital peripherals

The following specifications apply to the timer/counter/PWM peripherals in the timer mode.

#### 6.3.1 Pulse width modulation (PWM) for GPIO pins

**Table 12 PWM AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	$TCPWM_{FREQ}$	Operating frequency	–	–	$F_c$	MHz	$F_c \text{ max} = CLK\_SYS$
SID.TCPWM.3	$T_{PWMEXT}$	Output trigger pulse width	$2/F_c$	–	–	ns	Minimum possible width of overflow, underflow, and CC (Counter equals compare value) outputs
SID.TCPWM.4	$T_{CRES}$	Resolution of counter	$1/F_c$	–	–		Minimum time between successive counts
SID.TCPWM.5	$PWM_{RES}$	PWM resolution	$1/F_c$	–	–		Minimum pulse width of PWM output

#### 6.3.2 I<sup>2</sup>C

**Table 13 Fixed I<sup>2</sup>C AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	$F_{I2C1}$	Bit rate	–	–	1	Mbps	–

#### 6.3.3 UART

**Table 14 Fixed UART AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	$F_{UART}$	Bit rate	–	–	1	Mbps	–

### 6.3.4 SPI

**Table 15 Fixed SPI AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	$F_{SPI}$	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

**Table 16 Fixed SPI master mode AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	$T_{DMO}$	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	$T_{DSI}$	MISO valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	$T_{HMO}$	Previous MOSI data hold time	0	–	–		Referred to slave capturing edge

**Table 17 Fixed SPI Slave Mode AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	$T_{DMI}$	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	$T_{DSO}$	MISO valid after Sclock driving edge	–	–	$48 + (3 \times T_{CPU})$		$T_{CPU} = 1/F_{CPU}$
SID171A	$T_{DSO\_EXT}$	MISO valid after Sclock driving edge in ext clk mode	–	–	48		–
SID172	$T_{HSO}$	Previous MISO data hold time	0	–	–		–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–		–

### 6.3.5 Memory

**Table 18 Flash AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#2	FLASH_WRITE	Row (block) write time (Erase and program)	–	–	20	ms	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , all $V_{DDD}$
SID.MEM#1	FLASH_ERASE	Row erase time	–	–	15.5		
SID.MEM#5	FLASH_ROW_PGM	Row program time after erase	–	–	7		
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35	s	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7.5		
SID.MEM#6	FLASH_ENPB	Flash write endurance	100k	–	–	cycles	$25^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$ , all $V_{DDD}$
SID182	$F_{RET1}$	Flash retention, $T_A \leq 55^{\circ}\text{C}$ , 100K P/E cycles	20	–	–	years	–
SID182A	$F_{RET2}$	Flash retention, $T_A \leq 85^{\circ}\text{C}$ , 10K P/E cycles	10	–	–		



### 6.4 System resources

#### 6.4.1 Power-on-reset (POR) with brown out

**Table 19 Imprecise power-on reset (IPOR)**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , all $V_{DD}$
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4		

**Table 20 Precise POR**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , all $V_{DD}$
SID192	$V_{FALLDPSLP}$	BOD trip voltage in deep sleep mode	1.1	–	1.5		

#### 6.4.2 SWD interface

**Table 21 SWD interface specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	$3.0\text{ V} \leq V_{DDIO} \leq 5.5\text{ V}$	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	$0.25 \times T$	–	–	ns	
SID.SWD#3	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	$0.25 \times T$	–	–		
SID.SWD#4	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	$0.50 \times T$		
SID.SWD#5	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–		

#### 6.4.3 Internal main oscillator

**Table 22 IMO AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	$F_{IMOTOL}$	Frequency variation at 48 MHz (trimmed)	–	–	$\pm 2$	%	$3.0\text{ V} \leq V_{DD} < 5.5\text{ V}$ , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	$\mu\text{s}$	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , all $V_{DD}$
SID.CLK#1	$F_{IMO}$	IMO frequency	24	–	48	MHz	

#### 6.4.4 Internal low-speed oscillator

**Table 23 ILO AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO start-up time	–	–	2	ms	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , all $V_{DD}$
SID238	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID.CLK#5	$F_{ILO}$	ILO frequency	20	40	80	kHz	–

### 6.4.5 PD

**Table 24 PD DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05	-	1.2	V	-
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage			0.075		
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33		75	Ω	
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10			MΩ	
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64		96	μA	
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5V advertisement	166		194		
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5V advertisement	304		356		
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59		5.61	kΩ	
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108				
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-standard USB	0.15		0.25	V	
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35		0.45		
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75		0.85		
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45		2.75		
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-standard USB	0.61		0.7		
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16		1.31		
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3		0.6	%	
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10		50	kΩ	
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80		120	mV	

### 6.4.6 Analog-to-digital converter

**Table 25 ADC DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	-	8	-	Bits	-
SID.ADC.2	INL	Integral non-linearity	-1.5	-	1.5	LSB	Reference voltage generated from bandgap.
SID.ADC.3	DNL	Differential non-linearity	-2.5		2.5		Reference voltage generated from V <sub>DD</sub> .
SID.ADC.4	Gain Error	Gain error	-1.5		1.5		Reference voltage generated from bandgap.
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V <sub>DD</sub> min		V <sub>DD</sub> max	V	Reference voltage generated from V <sub>DD</sub> .
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04		Reference voltage generated from Deep sleep reference.

### 6.4.7 HS CSA

**Table 26 HS CSA DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.1	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	-15	-	15	%	Active mode
SID.HSCSA.2	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	-10		10		
SID.HSCSA.3	Csa_Acc3	CSA accuracy 15 mV < Vsense < 25 mV	-5		5		
SID.HSCSA.4	Csa_Acc4	CSA accuracy 25 mV < Vsense	-3		3		
SID.HSCSA.7	Csa_SCP_Acc1	CSA SCP at 6A with 5-mΩ sense resistor	-10		10		
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10A with 5-mΩ sense resistor	-10		10		
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1A with 5-mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5A with 5-mΩ sense resistor	123	130	137		

**Table 27 HS CSA AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.AC.1	T <sub>SCP_GATE</sub>	Delay from SCP threshold trip to external NFET power gate turn off	-	3.5	-	μs	1nF NFET gate
SID.HSCSA.AC.2	T <sub>SCP_GATE_1</sub>	Delay from SCP threshold trip to external NFET power gate turn off		8			3nF NFET gate

### 6.4.8 UV/OV

**Table 28 UV/OV specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold Accuracy, 4 V to 11 V	-3	-	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold Accuracy, 11 V to 21.5 V	-3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold Accuracy, 3 V to 3.3 V	-4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold Accuracy, 3.3 V to 4.0 V	-3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold Accuracy, 4.0 V to 21.5 V	-3		3		

### 6.4.9 VCONN switch

**Table 29 VCONN switch DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.VCONN.1	VCONN_OUT	VCONN output voltage with 20 mA load current	4.5	–	5.5	V	–
DC.VCONN.2	I <sub>LEAK</sub>	Connector side pin leakage current	–	–	10	μA	
DC.VCONN.3	I <sub>OCP</sub>	VCONN overcurrent protection threshold	22.5	30	42.5	mA	

**Table 30 VCONN switch AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.VCONN.1	T <sub>ON</sub>	VCONN switch turn-on time	–	–	600	μs	–
AC.VCONN.2	T <sub>OFF</sub>	VCONN switch turn-off time			10		

### 6.4.10 V<sub>BUS</sub>

**Table 31 V<sub>BUS</sub> discharge specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.1	R1	20-V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5 V.
SID.VBUS.DISC.2	R2	20-V NMOS ON resistance for DS = 2	250		1000		
SID.VBUS.DISC.3	R4	20-V NMOS ON resistance for DS = 4	125		500		
SID.VBUS.DISC.4	R8	20-V NMOS ON resistance for DS = 8	62.5		250		
SID.VBUS.DISC.5	R16	20-V NMOS ON resistance for DS = 16	31.25		125		
SID.VBUS.DISC.6	Vbus_stop_error	Error percentage of final VBUS value from setting	–		10	%	When VBUS is discharged to 5 V.

### 6.4.11 Voltage regulation

**Table 32 Voltage regulation DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	VOUT	CSNO output voltage range	3.3	–	21.5	V	–
SID.DC.VR.2	VR	CSNO voltage regulation accuracy	–	±3	±5	%	
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0	V	

**Table 33 Voltage regulator specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.1	T <sub>START</sub>	Total startup time for the regulator supply outputs	–	–	200	μs	–

### 6.4.12 VBUS gate driver

**Table 34 VBUS gate driver DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON.
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on VBUS_CTRL to turn off external NFET.
SID.GD.5	GD_drv	Programmable typical gate current	0.3		9.75	μA	–

**Table 35 VBUS gate Driver AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.3	T <sub>ON</sub>	VBUS_CTRL low to high (1V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	CSNO = 5 V
SID.GD.4	T <sub>OFF</sub>	VBUS_CTRL high to low (90% to 10%) with 3 nF external capacitance	–	7	–	μs	CSNO = 21.5 V

### 6.4.13 PWM controller

**Table 36 Buck-boost PWM controller specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PWM.1	F <sub>SW</sub>	Switching frequency	150	–	600	kHz	–
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	
PWM.3	Ratio_buck_BB	Buck to buck boost ratio		1.16		V/V	
PWM.4	Ratio_boost_BB	Boost to buck boost ratio		0.84			

### 6.4.14 NFET gate driver

**Table 37 Buck-boost NFET gate driver specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DR.1	R_HS_PU	Top-side gate driver on-resistance-gate pull-up	-	2	-	Ω	-
DR.2	R_HS_PD	Top-side gate driver on-resistance-gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance-gate pull-up		2			
DR.4	R_LS_PD	Bottom-side gate driver on-resistance-gate pull-down		1.5			
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
DR.9	Tr_LS	Bottom-side gate driver rise time		25			
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

### 6.4.15 LS-SCP

**Table 38 LS-SCP DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSSCP.DC.1	SCP_6A	Short circuit current detect @ 6A	5.4	6	6.6	A	Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.1A	SCP_6A_SE	Short circuit current detect @ 6A	4.5	6	7.5		Using single ended inputs (CSP_GPIO2) and internal ground
SID.LSSCP.DC.2	SCP_10A	Short circuit current detect @10A	9	10	11		Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.2A	SCP_10A_SE	Short circuit current detect @10A	7.5	10	12.5		Using single ended inputs (CSP_GPIO2) and internal ground

### 6.4.16 Thermal

**Table 39 Thermal specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

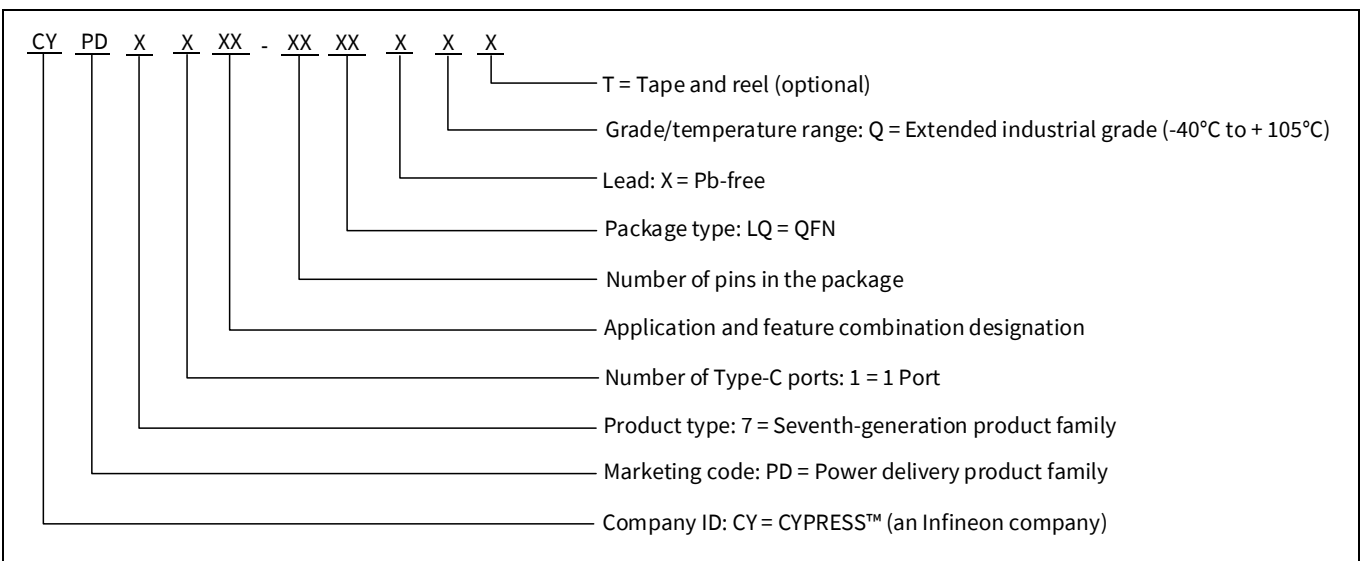
## 7 Ordering information

**Table 40** lists the EZ-PD™ CCG7SC part numbers and features.

**Table 40 EZ-PD™ CCG7SC ordering information**

MPN	Application	Termination resistor	Role	Switching frequency	Package type
CYPD7171-40LQXQ	Single-port USB-C PD AC-DC Power adapter, power source only	R <sub>P</sub>	DFP (Power source only)	150 kHz - 600 kHz	40-pin QFN
CYPD7171-40LQXQT					

### 7.1 Ordering code definitions



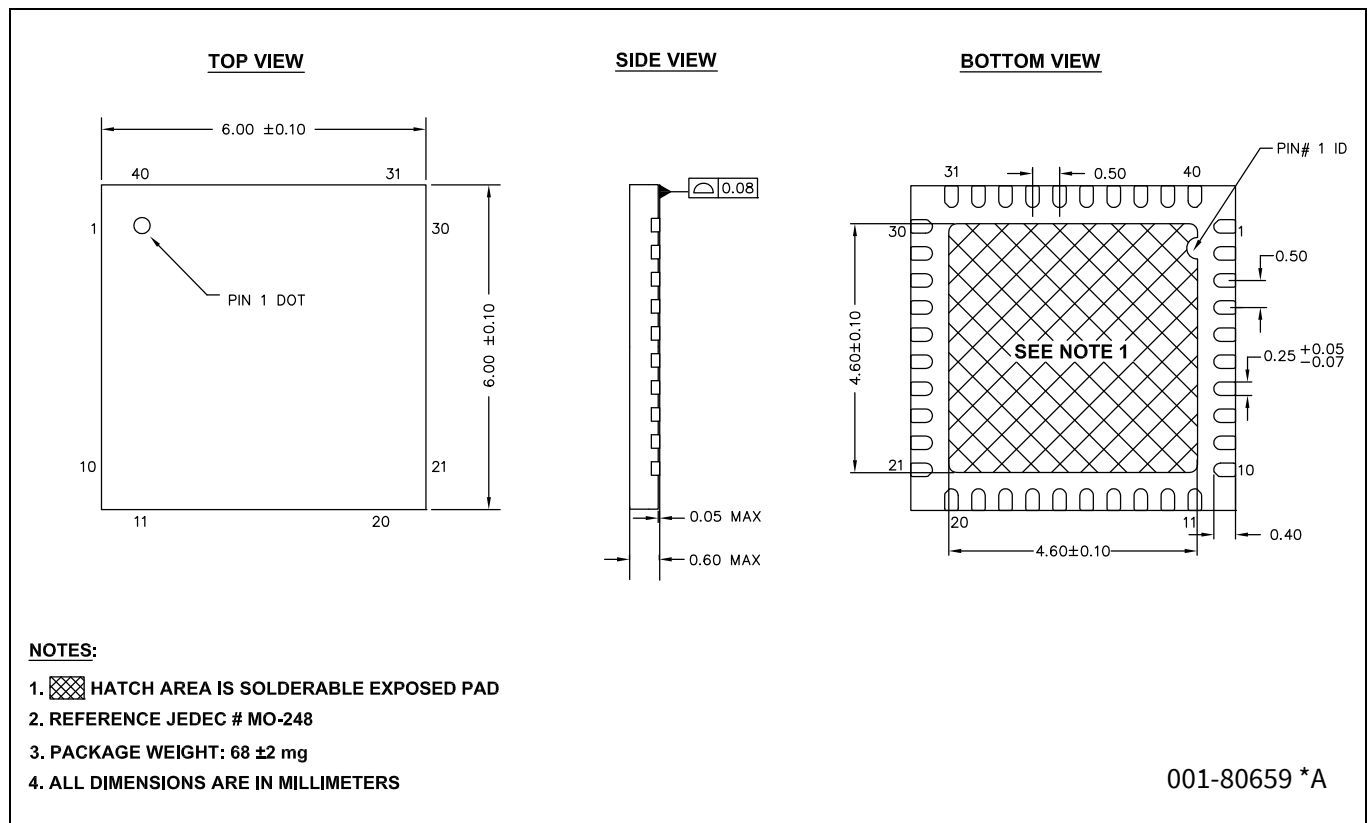


## 8 Packaging

**Table 41** Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$T_J$	Operating junction temperature	-	-40	25	125	°C
$T_{JA}$	Package $\theta_{JA}$		-	-	15.45	°C/W
$T_{JC}$	Package $\theta_{JC}$		-	-	4.4	

### 8.1 Package diagram



**Figure 14** 40L-QFN package outline

## 9 Acronyms

**Table 42** Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	Samsung adaptive fast charging
Arm®	advanced RISC machine, a CPU architecture
CPU	central processing unit
CSA	current sense amplifier
DAC	digital-to-analog converter
FCCM	forced continuous current/conduction mode
GPIO	general-purpose input/output
HSDR	high-side driver
I <sup>2</sup> C, or IIC	inter-integrated circuit, a communications protocol
IDAC	current DAC
I/O	input/output, see also GPIO
LSDR	low-side driver
MCU	microcontroller unit
OCP	overcurrent protection
OVP	overvoltage protection
PD	power delivery
POR	power-on reset
PSoC™	programmable system-on-chip
PSM	pulse skipping mode
PWM	pulse-width modulator
RAM	random-access memory
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
TCPWM	timer/counter/PWM
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	universal asynchronous transmitter receiver, a communications protocol
UFP	upstream facing port
UVP	undervoltage protection
USB	universal serial bus
UVLO	under-voltage lockout
VPA	VCONN powered accessories
ZCD	zero crossing detector

## 10 Document conventions

### 10.1 Units of measure

**Table 43** Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msp	megasamples per second
μA	microampere
μF	microfarad
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second

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