USB Type-C port controller for power sinks

General description

EZ-PD™ BCR-PLUS is Infineon's highly-integrated pre-programmed USB Type-C sink port controller and a part of the Barrel Connector Replacement (BCR) family. It has the ability to support ports with or without USB data capability. It mainly targets electronic devices that have legacy barrel connectors (up to 100W) or USB micro-B connectors for power such as drones, smart speakers, power tools, and other rechargeable devices.

EZ-PD™ BCR-PLUS complies with the latest USB Type-C and USB Power Delivery (PD) standards and enables users to quickly convert their devices from being powered through a barrel connector to being powered via the USB-C connector with few external components and no additional firmware development. The EZ-PD™ BCR-PLUS device ships with pre-programmed firmware with functionality as documented in this datasheet. Additional configuration changes are possible over the EZ-PD™ Configuration Utility. EZ-PD™ BCR-PLUS integrates a complete USB Type-C transceiver, USB PD policy manager, a load switch controller with a soft start, all termination resistors required for a USB Type-C port, and system-level ESD protection. It is available in a 24-pin QFN package.

Features

- USB Type-C and USB-PD support
  - Supports USB PD 3.1 Version 1.6 Spec including programmable power supply mode
  - Supports one USB Type-C port
- Legacy charging
  - Support for legacy charging or Type-C 5V operation when connected to USB Type-A ports
  - Support for legacy charging protocols like BC1.2, Apple, AFC, QC 2.0[1]
- System-level fault protection
  - VBUS to CC short protection
  - On-chip overvoltage protection (OVP), overcurrent protection (OCP), over temperature protection (OTP)
- Power
  - 3.0 V to 24.5 V operation (30 V tolerant)
  - Integrated VBUS load switch gate drivers with in-rush current control
- Firmware
  - Firmware update available through I^2C bootloader as well as over SWD interface
  - CCG UFP Host Processor Interface (HPI) based Sink PPS support
  - I2C/HPI supports 1.8 V as well as 3.3 V IO operation.
- System-Level ESD Protection
  - On CC, VBUS_IN_DIS, DC_OUT_DIS, D+, D–, HPI_SDA and HPI_SCL pins
  - ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C
- Packages
  - 24-pin QFN package
  - Supports extended industrial temperature range (–40°C to +105°C)

Note
1. Customers need to acquire their own licensing for AFC and QC2.0.

Logic block diagram

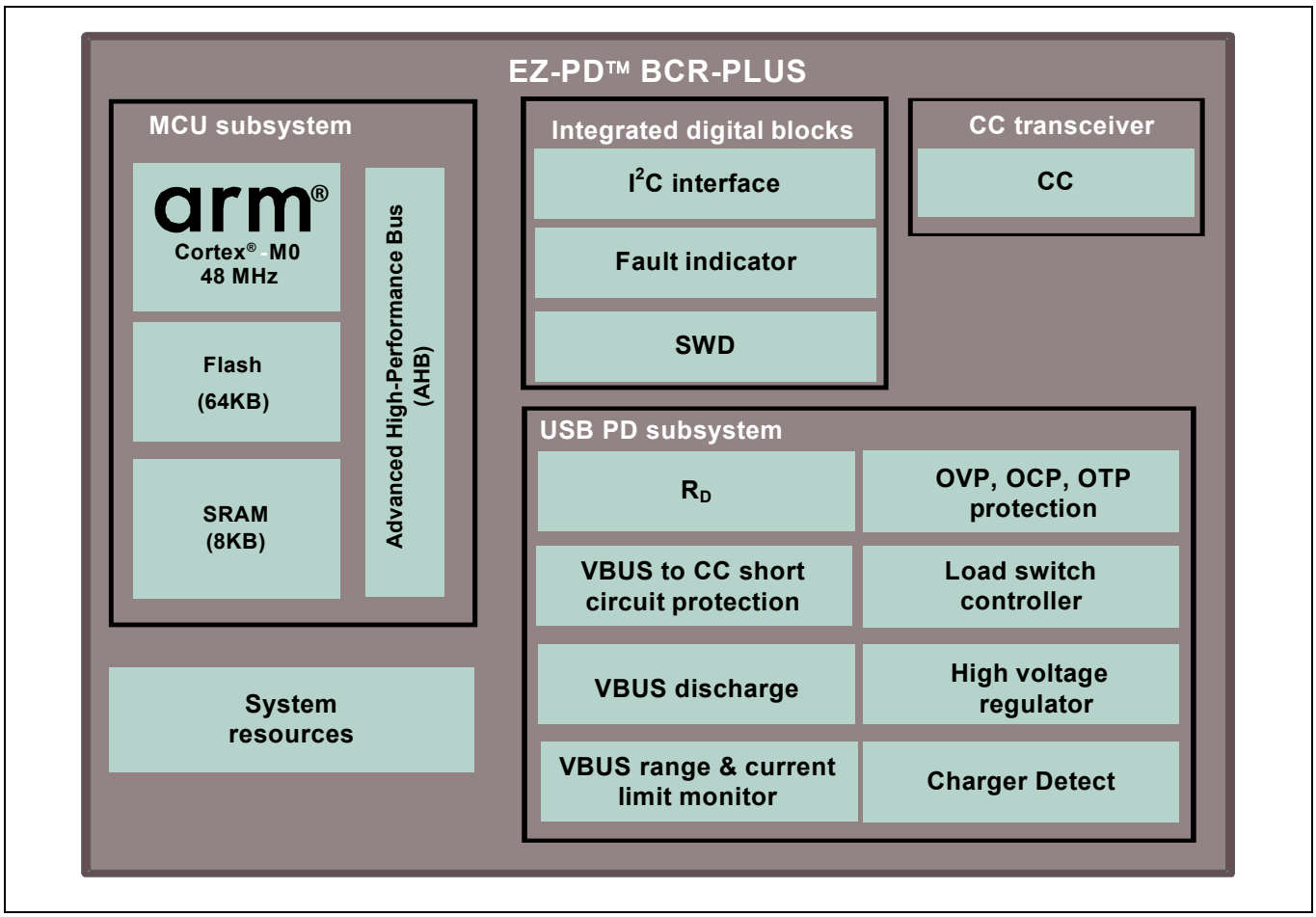


Table of contents

1 Functional overview

1.1 USB-PD subsystem

The USB-PD subsystem provides the interface to the USB Type-C USB port. This subsystem comprises a high-voltage regulator, OVP, and supply switch blocks. This subsystem also includes all ESD protection required and supported on the USB Type-C port.

1.1.1 USB-PD physical layer

The USB-PD physical layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the USB PD 3.1 version 1.6 standard. All communication is half-duplex. The physical layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USB-PD block includes the termination resistor R_D and its switch as required by the USB-PD spec. R_D resistor is required to implement connection detection, plug orientation detection, and for establishing USB UFP role.

According to the USB Type-C spec, a USB Type-C controller such as the EZ-PD™ BCR device must present certain termination resistors depending on its role in its unpowered state. The Sink role requires R_D resistor to be present on the CC pins even in an unpowered state. To implement this function, EZ-PD™ BCR has a dead battery R_D resistor bonded to both the CC pins.

1.1.2 VBUS overvoltage, overcurrent, overtemperature protection

The EZ-PD™ BCR-PLUS device has an integrated hardware block for VBUS OVP, OCP and OTP with configurable thresholds and response times on the USB Type-C port.

In an event of OCP and OTP, the BCR-PLUS device reports the event to the external I^2C master over HPI (if the protection is enabled). The device turns off the consumer FET path and enables the FAULT signal. Once the OCP/OTP condition no longer exists, the external master sends the HPI command for enabling the consumer FET. If OCP is detected again, the firmware repeats all the actions described above.

In an event of OVP, the BCR-PLUS device follows the PD protocol by informing the external master about the event, enables the hard-reset of the device and also sends an alert message to the port partner.

OTP is not implemented in the default pre-programmed firmware that ships with the EZ-PD™ BCR-PLUS device. It needs to be enabled using the EZ-PD™ Configuration Utility and the FLIP pin needs to be re-purposed as a thermistor input.

1.1.3 VBUS short protection

The EZ-PD™ BCR device provides VBUS short protection on CC1 an CC2 pins. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A USB-PD controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, the EZ-PD™ BCR device can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the CC1 and CC2 pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without the EZ-PD™ BCR device connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when the EZ-PD™ BCR device is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

1.1.4 Sink load switch controller on VBUS path

The EZ-PD™ BCR device has an integrated load switch controller to drive external PFETs on the VBUS sink path. This load switch controller has a soft start feature that limits the in-rush current flowing through the sink power path when the system is connected to an external load and powered on.

1.1.5 SAFE_PWR_EN gate driver

The EZ-PD™ BCR device has a SAFE_PWR_EN gate driver that can be used to drive an alternate load switch/FET. It is enabled whenever the EZ-PD™ BCR device is unable to negotiate the requested power contract. In such a scenario, the EZ-PD™ BCR device negotiates a 5-V/900-mA contract which can be delivered through the SAFE_PWR_EN FET to an alternate power rail in the system. This allows the system to operate in a limited mode when the requested power is unavailable through the USB Type-C port.

1.1.6 VBUS discharge FETs

The EZ-PD™ BCR device also has an integrated VBUS discharge FET used to discharge VBUS to meet the USB-PD specification timing on a detach condition.

1.2 Integrated digital blocks

1.2.1 Serial communication block (SCB)

The integrated SCB is configured to act as an I^2C block for the Part Numbers device. The Part Numbers device has an I^2C slave interface that can be connected to an I^2C host. The slave address is 0x08. Contact Cypress Technical Support for further details related with CCG UFP HPI specification.

The I^2C interface is capable of operating at speeds of up to 1 Mbps (Fast-mode Plus). The I^2C interface is also compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (**UM10204**). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C interface is not completely compliant with the I^2C spec in the following aspects:

- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

2 Programming and nonvolatile configuration of BCR-PLUS devices

2.1 Making nonvolatile configuration changes

The BCR-PLUS device ships with pre-programmed application firmware. Customers can make configuration changes using the EZ-PD™ Configuration Utility. Once the changes are made using the EZ-PD™ Configuration Utility, the configuration changes can be saved as a binary file and updated over the I^{2}C interface by the embedded controller/application processor. Refer to **Figure 1** for more details. The configuration table related changes that are made are nonvolatile.

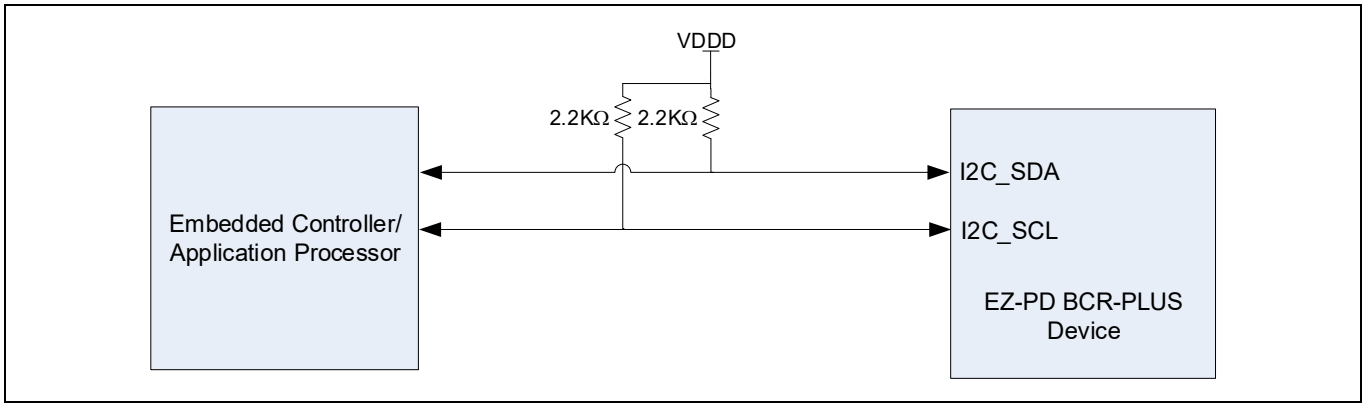


Figure 1 Configuration table and firmware update over I^{2}C interface

2.2 Firmware update

Infineon may make periodic firmware updates to the BCR-PLUS device. For customers that have in-field firmware update mechanism in place, they could update the firmware of the BCR-PLUS device over the I^{2}C interface.

3 Power systems overview

The EZ-PD™ BCR-PLUS device can operate from two possible external supply sources: VBUS_IN_DIS (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS_IN_DIS, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. Refer to the application diagram (see **Figure 4**) for capacitor connections.

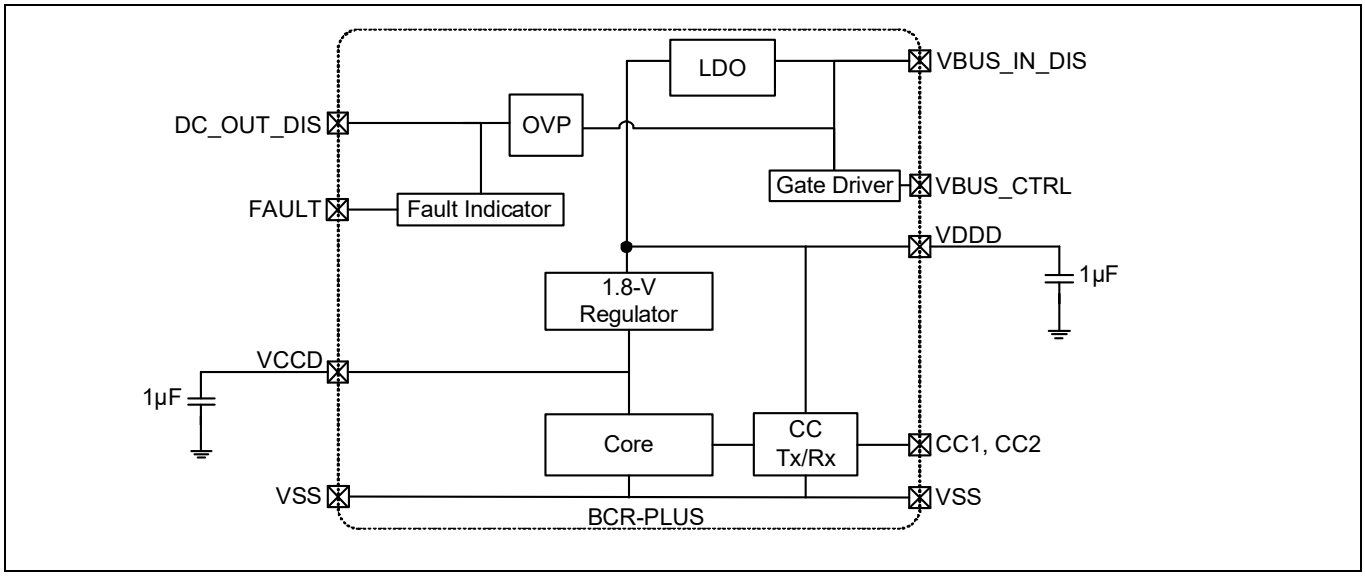


Figure 2 Power system requirement block diagram

4 Pinouts

Table 1 EZ-PD™ BCR-PLUS pin descriptions

24-pin QFN	Pin name	Pin function for CYPD3176 default firmware	Description
1	P1.0	VBUS_MIN	Connect a resistor divider to this pin that is connected to 3.3 V (from the VDDD pin) to indicate the minimum voltage needed by the system from the attached power adapter. See **Table 2** in **Application overview** section for details.
2	P1.1	VBUS_MAX	Connect a resistor divider to this pin that is connected to 3.3 V (from the VDDD pin) to indicate the maximum voltage needed by the system from the attached power adapter. See **Table 2** in **Application overview** section for details.
3	VBUS_CTRL		Connect this pin to the gate of a FET through a series resistor. This pin is the output of a PMOS FET gate driver that is slew-rate controlled. This signal is enabled when the EZ-PD™ BCR-PLUS device successfully negotiates a power contract within the requested range set by VBUS_MIN and VBUS_MAX voltage settings.
4	SAFE_PWR_EN		Connect this signal to the gate of a FET through a series resistor. This pin is the output of a PMOS FET gate driver. This signal is enabled when the EZ-PD™ BCR-PLUS device fails to negotiate for higher power and defaults to 5 V.
5	P1.2	D+	USB D+. Connect this pin to the D+ line of the Type-C connector for support for legacy and proprietary charging.
6	P1.3	D-	USB D–. Connect this pin to the D– line of the Type-C connector for support for legacy and proprietary charging.
7	P0.0	HPI_INT	Active Low HPI Interrupt pin. This pin is configured as “open drain low” mode in firmware. Therefore, it is required to have an external pull-up resistor connected to either 1.8 V or 3.3 V (recommended value = 10 kΩ).
8	P0.1	FAULT	The EZ-PD™ BCR-PLUS device pulls this pin high if the power adapter cannot supply the required voltage or current or if an OVP/OCP/OTP event is detected. The pin is low otherwise. OTP event will affect the functionality of this signal only if OTP is enabled using the EZ-PD™ Configuration Utility. The default firmware pre-programmed on CYPD3176 devices does not support OTP. The driving mode of the FAULT pin changes depending on the type of the resistor connected. When there is a pull-up resistor to 1.8V (recommended value = 10 kΩ), the FAULT pin operates as an open-drain drive low IO. When there is a weak pull-down resistor connected to GND (recommended value = 100 kΩ), the pin operates as a strong drive IO mode at 3.3 V level.

Table 1 EZ-PD™ BCR-PLUS pin descriptions *(continued)*

24-pin QFN	Pin name	Pin function for CYPD3176 default firmware	Description
9	CHARGING_MODE		This pin can be configured in 2 different ways to support the legacy charging protocols: • Option 1: BC1.2 support only. Connect pin to a 5-kΩ resistor pulled up to VDDD • Option 2: All Legacy charging protocols supported: Leave this pin floating.
10	P2.1	DATAMODE/FLIP	Connect this pin to a 1-kΩ pull-up resistor for applications that do not require data communication. Leave this pin unconnected for applications that need to sink power as well as support USB communication. Once the EZ-PD™ BCR-PLUS device is powered up, this pin will be sampled to determine the data mode of the device. When this pin is left unconnected, it will also be reconfigured to indicate the orientation of the type-C cable connection after sampling this pin. In the output mode (FLIP functionality), the EZ-PD™ BCR-PLUS device drives this line low if no device is attached or if CC polarity is unflipped (CC1 connected). If a device is attached on CC2 (polarity is flipped), the EZ-PD™ BCR-PLUS device drives this line high. While reporting FLIP status, this is a strong drive output pin.
11	DC_OUT_DIS		Connect this pin to the output of the PFETs controlled by the VBUS_FET_EN pin. This is used for monitoring the VBUS output. This is the power output of the system.
12	P2.2	HPI_SDA	This is the I2C slave interface provided for a host processor to control and monitor the EZ-PD™ BCR-PLUS device. For more details, refer to the CCG UFP HPI Specification. These pins are open drain drive low IOs and can operate at either 1.8 V or 3.3 V levels depending on external pull-up resistors connected to these pins.
13	P2.3	HPI_SCL	
14	CC2		Communication Channel 2 pin used to negotiate a voltage/current with the attached adapter.
15	CC1		Communication Channel 1 pin used to negotiate a voltage/current with the attached adapter.
16	P3.1	ISNK_FINE	Connect resistor divider networks to these pins that are to 3.3 V (from the VDDD pin) to set the operating current requested from the power adapter. See **Table 3** and **Table 4** in **Application overview** section for details.
17	P3.0	ISNK_COARSE	
18	VBUS_IN_DIS		Connect to VBUS of USB Type-C connector. Used to supply power to the EZ-PD™ BCR-PLUS device and monitor incoming voltage.
19	CSP	CSP	Current sense input
20	DNU1		Leave this pin unconnected
21	DNU2		Leave this pin unconnected
22	VSS		Ground pin, connect to USB Type-C connector GND.
23	VDDD		Output of internal 3.3-V regulator. Connect 1-µF and 2x 100-nF capacitors to this pin.

Table 1 EZ-PD™ BCR-PLUS pin descriptions *(continued)*

24-pin QFN	Pin name	Pin function for CYPD3176 default firmware	Description
24	VCCD		Output of internal 1.8-V regulator. Connect a 1-µF decoupling capacitor to this pin.
–	EPAD		Ground. Connect to same ground as VSS.

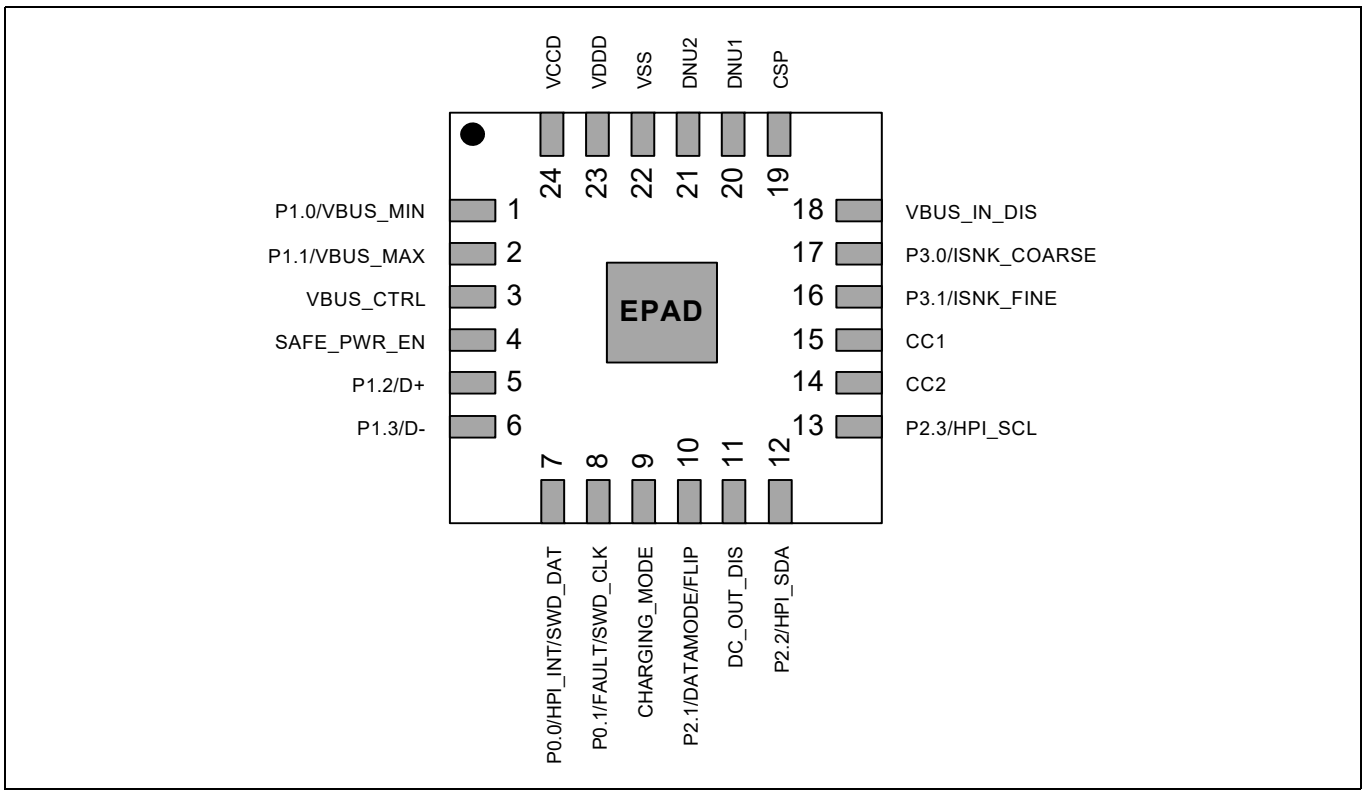
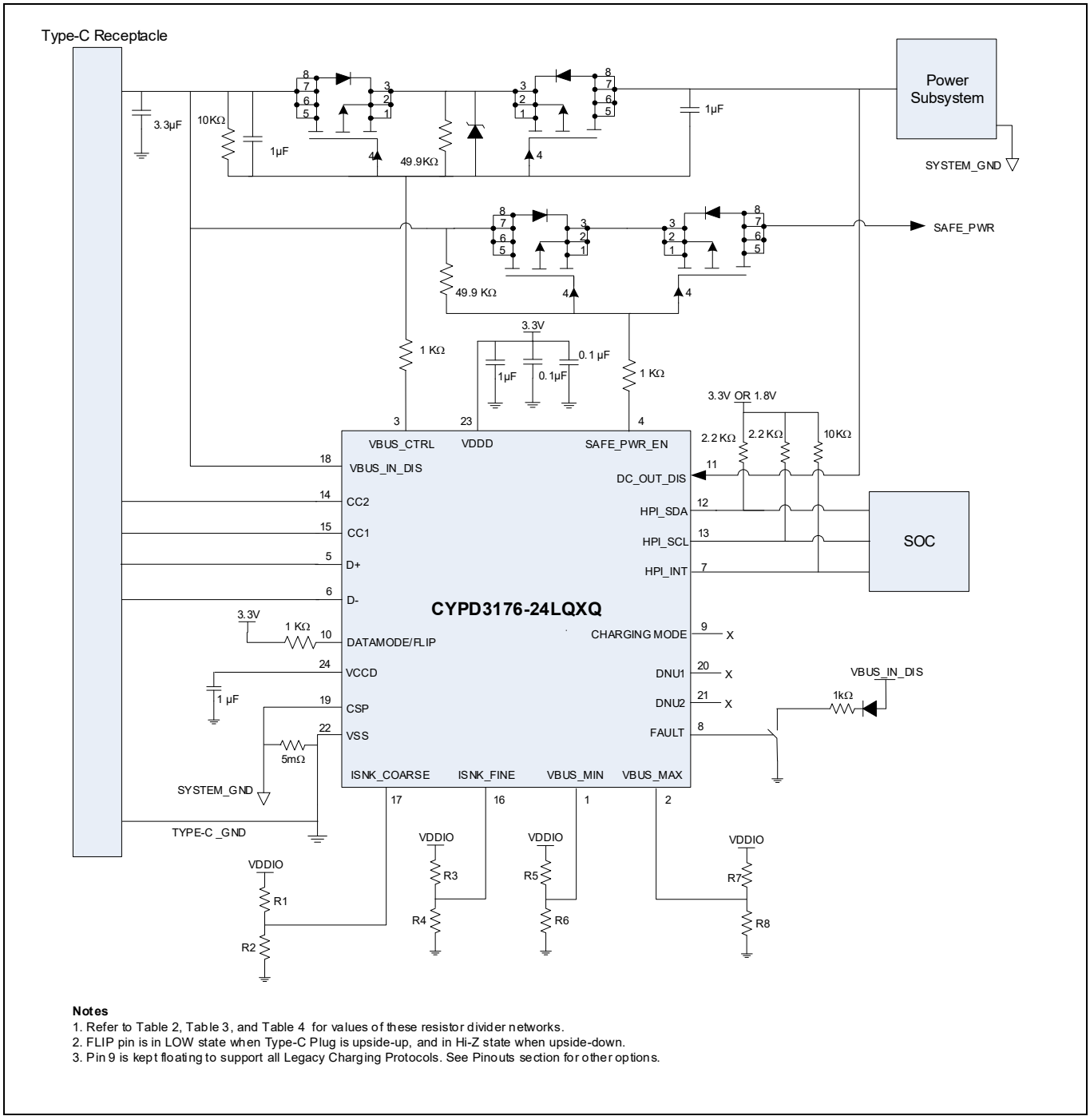


Figure 3 Pinout of 24-QFN package (top view)

5 Application overview

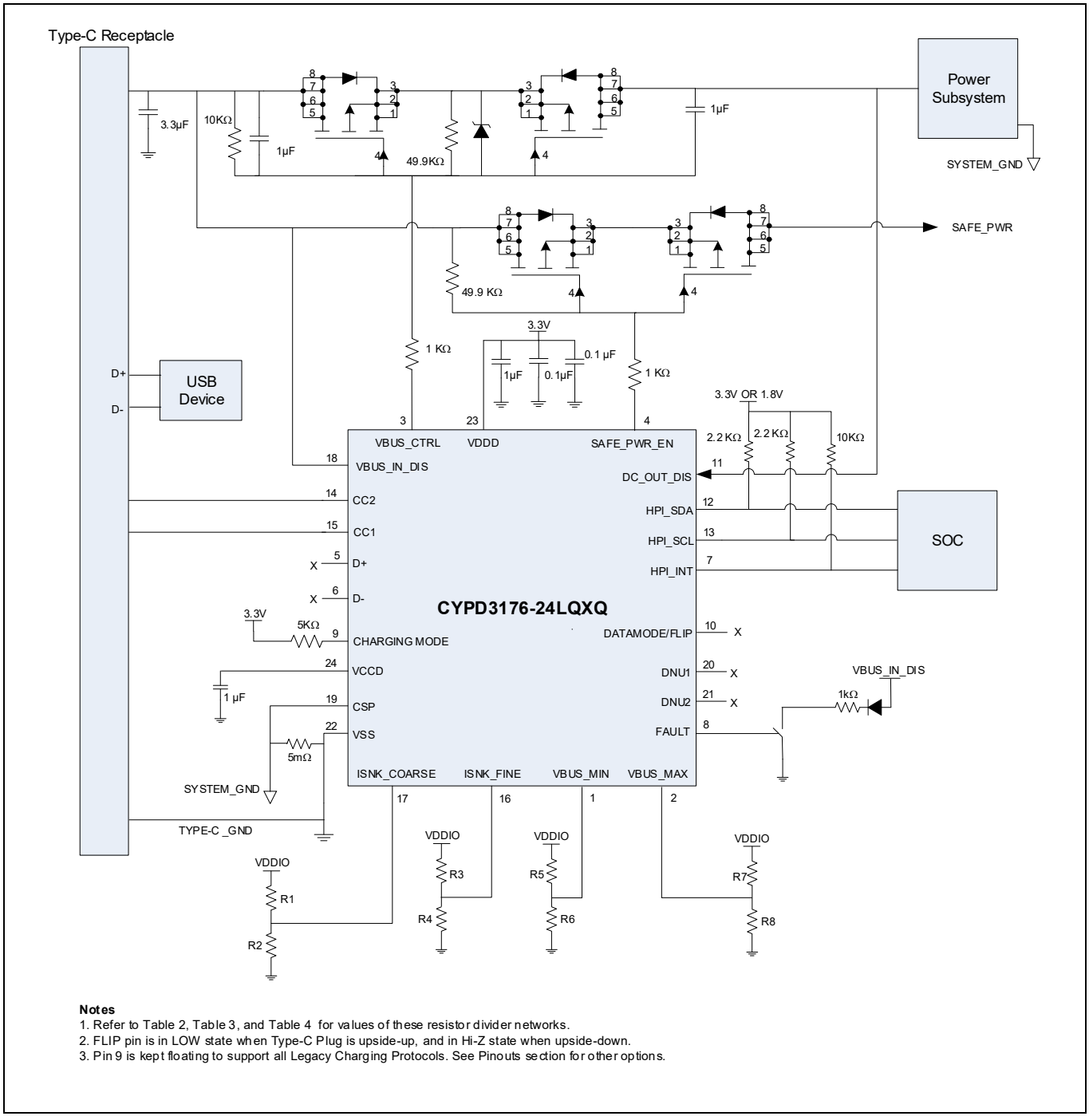
Figure 4 and **Figure 5** illustrate the EZ-PD™ BCR-PLUS based application diagram using the 24-pin QFN part. It has three main parts: USB Type-C receptacle to provide the input power to the application, the power subsystem used as the output power, and four sets of resistor divider networks to select the desired output voltage and current values.

The 'Fault' pin is used to indicate any voltage faults. When a fault condition is enabled, the output voltage of this application will go down to 0V and the EZ-PD™ BCR-PLUS device will attempt a protocol reset to recover from fault. For a detailed reference schematic, refer to the **CY4534 EZ-PD™ BCR EVK Schematic**.



Notes
1. Refer to Table 2, Table 3, and Table 4 for values of these resistor divider networks.
2. FLIP pin is in LOW state when Type-C Plug is upside-up, and in Hi-Z state when upside-down.
3. Pin 9 is kept floating to support all Legacy Charging Protocols. See Pinouts section for other options.

Figure 4 EZ-PD™ BCR-PLUS based application diagram for power sinks only (for electronic systems requiring 12 V to 15 V Input at 2 A)



Notes
1. Refer to Table 2, Table 3, and Table 4 for values of these resistor divider networks.
2. FLIP pin is in LOW state when Type-C Plug is upside-up, and in Hi-Z state when upside-down.
3. Pin 9 is kept floating to support all Legacy Charging Protocols. See Pinouts section for other options.

Figure 5 EZ-PD™ BCR-PLUS based application diagram for power sinks plus data peripherals (for electronic systems requiring 12 V to 15 V Input at 2 A)

The four sets of resistor divider networks are used to determine the voltage and current range that the EZ-PD™ BCR device will negotiate with the USB Type-C power adapter. **Table 2**, **Table 3**, and **Table 4** show the values of pull-up and pull-down resistors on each pin applicable for a desired VBUS_MIN, VBUS_MAX, ISNK_COARSE or ISNK_FINE value.

Notes

- If VBUS_MIN is more than VBUS_MAX, the setting on VBUS_MAX is used as both minimum and maximum VBUS setting for the system.
- EZ-PD™ BCR device does not monitor the current on VBUS_IN_DIS and enforce it within ISNK limits. It is the responsibility of the system to not consume more current than what the power adapter can provide.
- VBUS_MIN and VBUS_MAX can be set to the same value to select one specific voltage level from the Type-C power adapter.
- Ensure that the board layout design does not inject any noise into the VBUS_MIN, VBUS_MAX, ISNK_COARSE, ISNK_FINE pins.

Table 2 Resistor divider values for minimum or maximum voltage requested on VBUS

Voltage requested (V)	Resistor ratio relative to VDDD = 3.3 V	Suggested pull-up resistor value (kΩ)	Suggested pull-down resistor value (kΩ)	Voltage range on pin (mV)
5	0/6	Open	0	0–248
9	1/6	5.1	1	249–786
12	2/6	5.1	2.4	787–1347
15	3/6	5.1	5.1	1348–1920
19	4/6	5.1	10	1921–2778
20	≥ 5/6	0	Open	≥ 2779

Table 3 Resistor divider values for coarse setting on operating current (for VDDD = 3.3 V)

Operating current requested for coarse setting (A)	Resistor ratio relative to VDDD = 3.3 V	Suggested pull-up resistor value (kΩ)	Suggested pull-down resistor value (kΩ)	Voltage range on pin (mV)
0	0/6	Open	0	0–248
1	1/6	5.1	1	249–786
2	2/6	5.1	2.4	787–1347
3	3/6	5.1	5.1	1348–1920
4	4/6	5.1	10	1921–2778
5	≥ 5/6	0	Open	≥ 2779

Table 4 Resistor divider values for fine setting on operating current (for VDDD = 3.3 V)

Operating current requested for fine setting (A)	Resistor ratio relative to VDDD = 3.3 V	Suggested pull-up resistor value (kΩ)	Suggested pull-down resistor value (kΩ)	Voltage range on pin (mV)
+0	0/6	Open	0	0–248
+250	1/6	5.1	1	249–786
+500	2/6	5.1	2.4	787–1347
+750	3/6	5.1	5.1	1348–1920
+900	≥ 4/6	0	Open	≥ 1921

5.1 FAULT pin behavior

The FAULT pin is driven low by default, and is driven high under the following conditions:

- A USB-PD contract could not be negotiated and the VBUS_MIN voltage indicated is not 5 V.
- A USB-PD contract was negotiated but none of the voltages offered are within VBUS_MIN and VBUS_MAX ranges.
- Voltages offered by the power adapter are within VBUS_MIN, VBUS_MAX range but the current is below ILIM limit.
- VBUS voltage supplied by power adapter is outside expected limits.
- External load draws more current than the expected current threshold (Sink OCP).
- Sink device's temperature measured by an external thermistor exceeds the programmed threshold (only when OTP is enabled using the EZ-PD™ Configuration Utility).

If a PD contract is re-negotiated for any reason, the FAULT pin will hold its state until the contract is complete and the result of the contract can be determined correctly.

5.2 SAFE_PWR_EN pin behavior

This gate driver is enabled when the PD contract defaults to 5 V due to mismatching capabilities. This driver is not enabled when the device is configured so that 5 V input is accepted by the system. This driver is also not enabled when there is an overvoltage condition on the 5 V VBUS input at the USB-C connector.

The system can use this power to run any digital logic (on Embedded Controller) that notifies the user about an incompatible power adapter. For customers who do not prefer to have this feature can disable it using the EZ-PD™ Configuration Utility.

5.3 VBUS_FET_EN pin behavior

This gate driver is enabled when a power adapter with matching power capabilities is detected, as determined by the VBUS_MIN, VBUS_MAX, ISNK_COARSE and ISNK_FINE pins. When enabling the gate driver, the current sink inside the driver is used to ensure that the gate voltage rises slowly (rate of rise can be externally controlled) which in turn controls the inrush current of the system.

When VBUS is out of range (i.e in an event of OVP or UVP), the gate driver is quickly disabled. This gate driver can be turned on or off independently over HPI interface. Refer to the CCG UFP HPI Specification for more details on disabling/enabling consumer path during power contract re-negotiations for fixed/variable PDOs.

5.4 Legacy charging support

BCR-PLUS device supports BC 1.2, QC 2.0 sink (Class B), AFC and Apple charging protocols. When a non-PD charger is connected, the BCR-PLUS device is able to negotiate any of the legacy charging protocols supported by the sink device. Customers can select support for all legacy charging protocols or BC1.2 protocol based on the hardware setup for the CHARGING_MODE pin (see **Pinouts** for more details). If the connected Type-C charger supports multiple charging protocols, then the order of priority of negotiation is as follows:

Negotiation sequence: (PD → BC1.2 → AFC → QC2.0 (Class B) → Apple → Type-C Only)

USB-PD is of higher priority over any of the legacy charging protocols. PD and BC 1.2 detection start simultaneously, but if the power adapter supports PD, then PD takes preference over BC 1.2.

When negotiating legacy protocols, the BCR-PLUS device negotiates voltage and current based on the VBUS_MIN/MAX and ISNK_COARSE/ISNK_FINE settings. Note that when VBUS_MIN and VBUS_MAX are set to 5 V, the BCR-PLUS device is capable of accepting VBUS voltages between 4.75 V to 5.5 V when negotiating legacy charging protocols. If the power adapter is not able to support the voltage/current requirements, then the BCR-PLUS device negotiates a 5 V contract and turns on the SAFE_PWR path. Legacy charging support can be disabled using the EZ-PD™ Configuration Utility.

6 Electrical specifications

6.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS} on VBUS_IN_DIS and DC_OUT_DIS pins	–	–	30	V	Absolute max.
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1, CC2 pins	–	–	22[2]	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDD} + 0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	Applicable to pins HPI_INT and GPIO_1
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS_IN_DIS, HPI_SDA and HPI_SCL pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for D+, D–, CC1, CC2, VBUS_IN_DIS, HPI_SDA and HPI_SCL pins

Table 6 Pin based absolute maximum ratings

Pin No.	Pin name	Absolute minimum (volts)	Absolute maximum (volts)
1	P1.0/VBUS_MIN	-0.5	VDDD + 0.5
2	P1.1/VBUS_MAX	-0.5	VDDD + 0.5
3	VBUS_CTRL	-0.3	VBUS_MAX
4	SAFE_PWR_EN	-0.3	VBUS_MAX
5	P1.2/D+	-0.5	VDDD + 0.5
6	P1.3/D-	-0.5	VDDD + 0.5
7	P0.0/HPI_INT/SWD_DAT	-0.5	6
8	P0.1/FAULT/SWD_CLK	–0.5	6
9	CHARGING_MODE	–0.5	VDDD + 0.5
10	P2.1/DATAMODE/FLIP	–0.5	VDDD + 0.5
11	DC_OUT_DIS	–0.5	VBUS_MAX
12	P2.2/HPI_SDA	–0.5	22
13	P2.3/HPI_SCL	–0.5	22
14	CC2	–0.5	22
15	CC1	–0.5	22
16	P3.1/ISNK_FINE	–0.5	VDDD + 0.5
17	P3.0/ISNK_COARSE	–0.5	VDDD + 0.5
18	VBUS_IN_DIS	–0.5	VBUS_MAX
19	CSP	–0.5	VDDD + 0.5
20	DNU1	Leave this pin unconnected.	
21	DNU2	Leave this pin unconnected.	
22	VSS	0	0
23	VDD	–0.5	6
24	VCCD	–0.5	2.3

Note
2. As per USB PD specification, maximum allowed VBUS = 21.5 V.

6.2 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 120°C, except where noted.

Table 7 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#2	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	Sink mode, –40°C ≤ T_A ≤ 105°C
SID.PWR#3	V_{BUS_IN}	Power supply input voltage	3.0	–	24.5	V	–40 °C ≤ T_A ≤ 105°C
SID.PWR#5	V_{CCD}	Output voltage for core Logic	–	1.8	–	V	–
SID.PWR#13	C_{exc}	Power supply decoupling capacitor for V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#14	C_{exv}	Power supply decoupling capacitor for VBUS_IN_DIS	–	0.1	–	µF	X5R ceramic or better
Active mode. Typical values measured at V_{DDD} = 5.0 V or V_{BUS} = 5.0 V and T_A = 25°C.							
SID.PWR#8	I_{DD_A}	Supply current from V_{BUS} or V_{DDD}	–	10	–	mA	V_{DDD} = 5 V OR V_{BUS} = 5 V, T_A = 25°C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, EA/ADC/CSA/UVOV ON, CPU at 24 MHz.
Sleep mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25°C.							
SID25A	I_{DD_S}	CC, I^2C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	V_{DDD} = 3.3 V, T_A = 25°C, All blocks except CPU are on, CC IO on, EA/ADC/CSA/UVOV on.
Deep Sleep mode. Typical values measured at T_A = 25°C.							
SID_PB_DS_A_SNK	$I_{DD\_PB\_DS\_A\_SNK}$	V_{BUS} 4.0 to 24.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	For sink applications, V_{BUS} = 24.5 V, T_A = 25°C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV on.

Table 8 AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#17	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID.PWR#18	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{POR\_HIZ\_T}$	Power-on I/O Initialization Time	–	3	–	ms	–

6.2.1 I/O

Table 9 I/O DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDD2.7-}$	LVTTL input, VDDD < 2.7 V	0.7 × V_{DDD}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDD2.7-}$	LVTTL input, VDDD < 2.7 V	–	–	0.3 × V_{DDD}	V	–
SID.GIO#41	$V_{IH\_VDDD2.7+}$	LVTTL input, VDDD ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IH\_VDDD2.7+}$	LVTTL input, VDDD ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} – 0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA at 3-V V_{DDD}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all V_{DDD}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all V_{DDD}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GIO#17	C_{PIN_A}	Max pin capacitance	–	–	22	pF	Capacitance on D+, D– pins. Guaranteed by characterization.
SID.GIO#17A	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all other I/Os. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL V_{DDD} > 2.7 V	15	40	0	mV	Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DDD} < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by design.
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
SID.GIO#41A	V_{IH_VCCHIB}	V_{IH}, 1.8 V input mode	1.26	–	–	V	–
SID.GIO#42A	V_{IL_VCCHIB}	V_{IL}, 1.8 V input mode	–	–	0.54	V	–
SID.GIO#43A	V_{HYS_VCCHIB}	Input hysteresis, 1.8 V input mode	90	–	–	mV	–

Table 9 I/O DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 10 I/O AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF

Table 11 HPI pins DC specifications (Applicable to pins HPI_SDA and HPI_SCL only)

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT Latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT Pull-up resistor value	1	–	25	kΩ	+25°C T_A, 1.4 V to GPIO_20VT_Voh (min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT Pull-down resistor value	2.5	–	20	kΩ	+25°C T_A, 1.4-V to V_{DDD}
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	–	25	pF	–40°C to +85°C T_A, All V_{DDD}, F = 1 MHz
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT Output Voltage low level	–	–	0.4	V	I_{OL} = 2 mA
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 12 HPI pins AC specifications (Applicable to pins HPI_SDA and HPI_SCL only)

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT#70	GPIO_20VT_TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	–	45	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_TfallF	GPIO_20VT Fall time in Fast Strong Mode	2	–	15	ns	All V_{DDD}, C_{load} = 25 pF

6.3 Digital peripherals

The following specifications apply to the timer/counter/PWM peripherals in the Timer mode.

6.3.1 I^2C

Table 13 Fixed I^2C DC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	1.4	–	µA	–

Table 14 Fixed I^2C AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	400	kbps	–

6.4 System resources

6.4.1 Power-on reset (POR) with brown-out SWD interface

Table 15 Imprecise POR (PRES)

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	POR rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 16 Precise POR

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 17 USB PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0V and 1.32 V applied at CC1 or CC2
SID.PD.6	Vgndoffset	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter

Table 18 LS-CSA specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSCSA.1	Cin_inp	CSP Input capacitance	7	–	10	pF	Guaranteed by characterization

Table 18 LS-CSA specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSCSA.2	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active Mode
SID.LSCSA.3	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10	%	
SID.LSCSA.4	Csa_Acc3	CSA accuracy 15 mV < Vsense < 20 mV	–6	–	6	%	
SID.LSCSA.5	Csa_Acc4	CSA accuracy 20 mV < Vsense < 30 mV	–5	–	5	%	
SID.LSCSA.6	Csa_Acc5	CSA accuracy 30 mV < Vsense < 50 mV	–4	–	4	%	
SID.LSCSA.7	Csa_Acc6	CSA accuracy 50 mV < Vsense	–4	–	4	%	
SID.LSCSA.8	Csa_SCP_Acc1	CSA SCP 80 mV	–16.5	–	30	%	
SID.LSCSA.9	Csa_SCP_Acc2	CSA SCP 100 mV	–13.4	–	24	%	
SID.LSCSA.10	Csa_SCP_Acc3	CSA SCP 150 mV	–9.4	–	16	%	
SID.LSCSA.11	Csa_SCP_Acc4	CSA SCP 200 mV	–7.5	–	12	%	
SID.LSCSA.12	Av	Nominal Gain values supported: 5, 10, 20, 35, 50, 75, 125, 150	5	–	150	V/V	–
SID.LSCSA.24	Av1_E_Trim	Gain Error	–3	–	3	%	Guaranteed by characterization
SID.LSCSA.31	Av_E_SCP	Gain Error of SCP stage	–3.5	–	3.5	%	Guaranteed by characterization

Table 19 LS-CSA AC specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSCSA.AC.1	T_{OCP_GPIO}	Delay from OCP threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.2	T_{OCP_Gate}	Delay from OCP threshold trip to external PFET Power Gate Turn off	–	–	50	µs	–
SID.LSCSA.AC.3	T_{SCP_GPIO}	Delay from SCP threshold trip to output GPIO toggle	–	–	15	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.4	T_{SCP_Gate}	Delay from SCP threshold trip to external PFET Power Gate Turn off	–	–	50	µs	–
SID.LSCSA.AC.5	T_{SR_GPIO}	Delay from SR threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

6.4.2 Gate driver specifications

Table 20 Gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	R_{PD}	Pull-down resistance	–	–	3	kΩ	Applicable on VBUS_CTRL and SAFE_PWR_EN to turn ON external PFET.
SID.GD.2	R_{PU}	Pull-up resistance	–	–	4	kΩ	Applicable on VBUS_CTRL to turn OFF external PFET.
SID.GD.3	I_{PD0}	Pull-down current sink at drive strength of 1	25	–	75	µA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_CTRL and SAFE_PWR_EN to turn ON external PFET.
SID.GD.4	I_{PD1}	Pull-down current sink at drive strength of 2	50	–	150	µA	
SID.GD.5	I_{PD2}	Pull-down current sink at drive strength of 4	140	–	300	µA	
SID.GD.6	I_{PD3}	Pull-down current sink at drive strength of 8	280	–	580	µA	
SID.GD.7	I_{PD4}	Pull-down current sink at drive strength of 16	560	–	1200	µA	
SID.GD.8	I_{PD5}	Pull-down current sink at drive strength of 32	1120	–	2300	µA	
SID.GD.9	I_leak_p1	Pin leakage on VBUS_CTRL	–	0.003	–	µA	+25°C T_J, 5-V V_{DDD}, 20-V V_{BUS}
SID.GD.10	I_leak_c1	Pin leakage on SAFE_PWR_EN	–	0.003	–	µA	+25°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.11	I_leak_p2	Pin leakage on VBUS_CTRL	–	–	2	µA	+85°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.12	I_leak_c2	Pin leakage on SAFE_PWR_EN	–	–	2	µA	+85°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.13	I_leak_p3	Pin leakage on VBUS_CTRL	–	–	7	µA	+125°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.14	I_leak_c3	Pin leakage on SAFE_PWR_EN	–	–	7	µA	+125°C T_J, 5-V V_{DDD}, 20-V V_{BU}

Table 21 Gate driver AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.15	T_{PD1}	Pull down delay on SAFE_PWR_EN	–	–	2	µs	Cload = 2 nF, Delay to VBUS – 1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 kΩ tied between SAFE_PWR_EN and VBUS
SID.GD.16	$T_{r\_discharge}$	Discharge rate of output node on SAFE_PWR_EN	–	–	5	V/µs	80% to 20%, 50 kΩ tied between SAFE_PWR_EN and VBUS, Cload = 2 nF, Vinitial = 24 V
SID.GD.17	T_{PD2}	Pull down delay on VBUS_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS – 1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 kΩ tied between SAFE_PWR_EN and VBUS
SID.GD.18	T_{PU}	Pull up delay on VBUS_CTRL	–	–	18	µs	Cload = 2 nF, Delay to VBUS – 1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 kΩ tied between SAFE_PWR_EN and VBUS
SID.GD.19	SR_{PU}	Output slew rate on VBUS_CTRL	–	–	5	V/µs	Cload = 2 nF, 20% to 80% of VBUS_CTRL range
SID.GD.20	SR_{PD}	Output slew rate on VBUS_CTRL	–	–	5	V/µs	Cload = 2 nF, 80% to 20% of VBUS_CTRL range

Table 22 VBUS discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by characterization.

Table 23 Voltage (VBUS) regulation DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	$V_{\_IN\_3}$	V(pad_in) at 3-V target	2.85	3	3.15	V	Active mode shunt regulator at 3 V with bandgap
SID.DC.VR.2	$V_{\_IN\_5}$	V(pad_in) at 5-V target	4.75	5	5.25	V	Active mode shunt regulator at 5 V
SID.DC.VR.3	$V_{\_IN\_9}$	V(pad_in) at 9-V target	8.55	9	9.45	V	Active mode shunt regulator at 9 V
SID.DC.VR.4	$V_{\_IN\_15}$	V(pad_in) at 15-V target	14.25	15	15.75	V	Active mode shunt regulator at 15 V
SID.DC.VR.5	$V_{\_IN\_20}$	V(pad_in) at 20-V target	19	20	21	V	Active mode shunt regulator at 20 V
SID.DC.VR.6	$V_{\_IN\_3\_DS}$	V(pad_in) at 3-V target	2.7	3	3.3	V	Deep Sleep mode shunt regulator at 3 V with bandgap
SID.DC.VR.7	$V_{\_IN\_5\_DS}$	V(pad_in) at 5-V target	4.5	5	5.5	V	Deep Sleep mode shunt regulator at 5 V
SID.DC.VR.8	$V_{\_IN\_9\_DS}$	V(pad_in) at 9-V target	8.1	9	9.1	V	Deep Sleep mode shunt regulator at 9 V
SID.DC.VR.9	$V_{\_IN\_15\_DS}$	V(pad_in) at 15-V target	13.5	15	16.5	V	Deep Sleep mode shunt regulator at 15 V
SID.DC.VR.10	$V_{\_IN\_20\_DS}$	V(pad_in) at 20-V target	18	20	22	V	Deep Sleep mode shunt regulator at 20 V
SID.DC.VR.11	I_{KA_OFF}	Off-state cathode current	–	–	10	µA	–
SID.DC.VR.12	I_{KA_ON}	Current through cathode pin	–	–	10	mA	–

Table 24 VBUS short protection specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VSP.1	V_SHORT_TRIGGER	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by characterization.

Table 25 VBUS DC regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.2	VBUS_DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

Table 26 VBUS AC regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.3	T_{start}	Total startup time for the regulator supply outputs	–	–	200	µs	Guaranteed by characterization

6.4.3 Analog to digital converter (used for determining VBUS_MIN, VBUS_MAX, ISNK_COARSE, ISNK_FINE Values)

Table 27 ADC DC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V_{REF_ADC2}	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

Table 28 ADC AC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

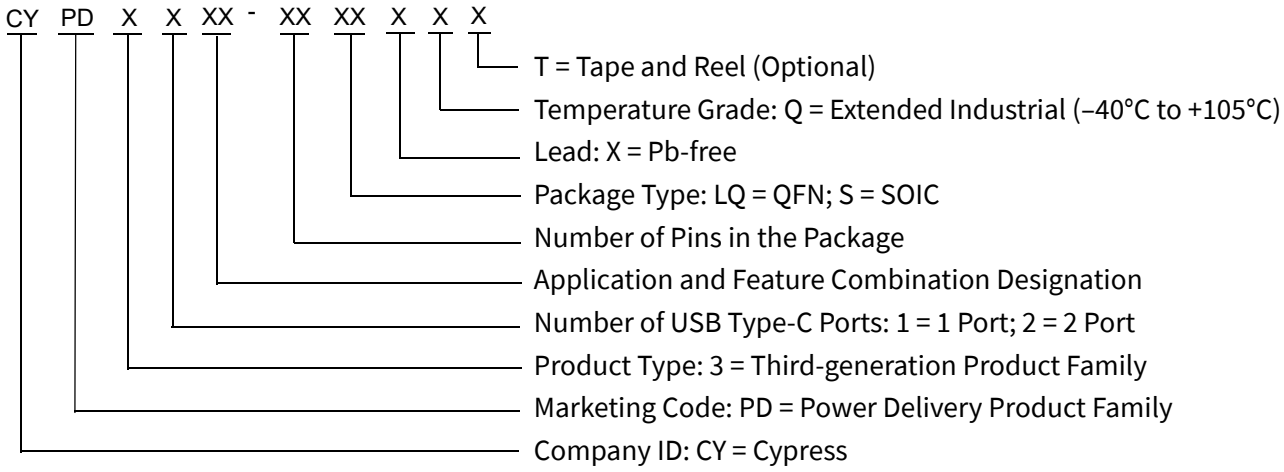
7 Ordering information

Table 29 lists the Part Numbers part numbers and features.

Table 29 EZ-PD™ BCR ordering information

MPN	Application	Termination resistor	Role	Package type	Si ID
CYPD3176-24LQXQ	Barrel Connector Replacement or Generic UFP Sink	R_D, R_{D-DB}	UFP	24-Pin QFN	2011

7.1 Ordering code definitions



8 Packaging

Table 30 Package characteristics

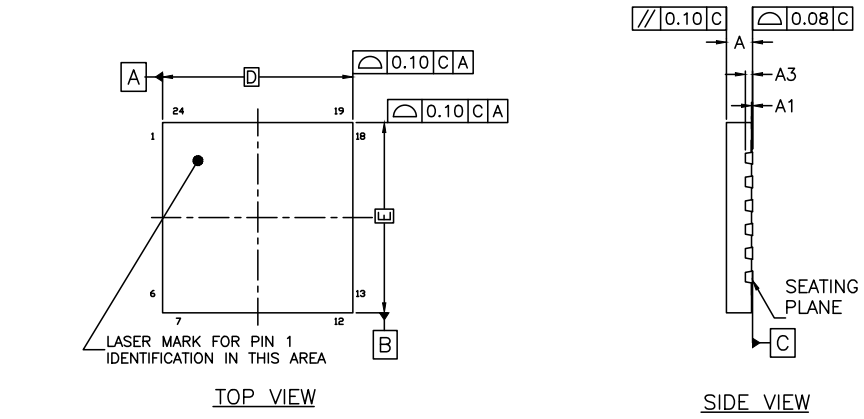
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Extended Industrial	–40	25	105	°C
T_J	Operating junction temperature	Extended Industrial	–40	25	120	°C
T_{JA}	Package θ_{JA} (24-pin QFN)	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC} (24-pin QFN)	–	–	–	4.78	°C/W

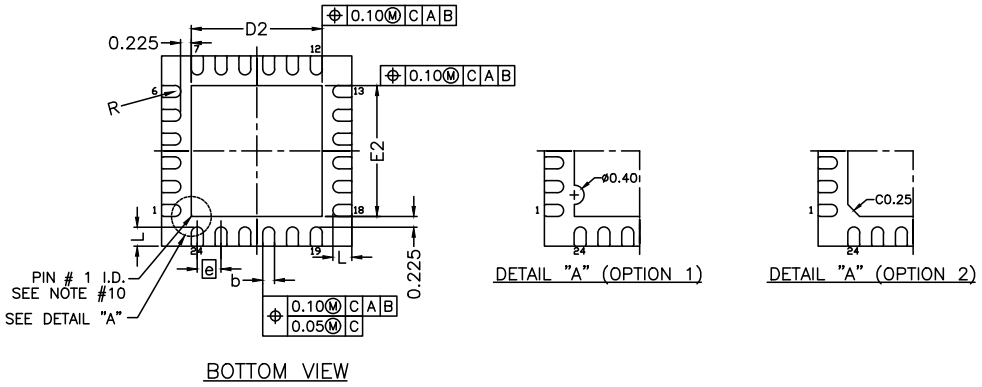
Table 31 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
24-pin QFN	260°C	30 seconds

Table 32 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A1	0.00	—	0.05
A3 (Option 1)	0.152 REF		
A3 (Option 2)	0.127 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.65	2.75	2.85
E	4.00 BSC		
E2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.
10. INDEX FEATURE CAN EITHER BE AN OPTION 1 : "MOUSE BITE" OR OPTION 2 : CHAMFER.

002-16934 *E

Figure 6 24-pin QFN ((4.0 × 4.0 × 0.6 mm), 2.75 × 2.75 mm E-Pad (Sawn)) package outline, 002-16934

9 Acronyms

Table 33 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	adaptive fast charging
Arm®	advanced RISC machine, a CPU architecture
BCR	barrel connector replacement
BOD	brown-out detect
BMC	Biphase Mark Code
CC	configuration channel
CPU	central processing unit
CS	current sense
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
ESD	electrostatic discharge
GPIO	general-purpose input/output
HPI	host processor interface
IC	integrated circuit
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I/O	input/output, see also GPIO
LDO	low-dropout regulator
MCU	microcontroller unit
NC	no connect
OCP	overcurrent protection
OTP	over-temperature protection
OVP	overvoltage protection
OVT	overvoltage tolerant
PD	power delivery
PHY	physical layer
POR	power-on reset
PMOS	P-channel MOSFET (metal oxide semiconductor field effect transistor)
PPS	programmable power supply
PRES	precise power-on reset
PSoC™	Programmable System-on-Chip™
PWM	pulse-width modulator
RISC	reduced-instruction-set computing
RX	receive
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
SDK	software development kit

Table 33 Acronyms used in this document *(continued)*

Acronym	Description
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UFP	upstream facing port
USB	Universal Serial Bus

10 Document conventions

10.1 Units of measure

Table 34 Units of measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	mega samples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
**	2021-02-17	Initial release.
*A	2021-05-18	Updated **General description**: Updated description. Updated **Functional overview**: Updated **USB-PD subsystem**: Updated **VBUS overvoltage, overcurrent, overtemperature protection**: Updated description. Updated **Programming and nonvolatile configuration of BCR-PLUS devices**. Replaced “BCR-PLUS Programming and Bootloading” with “Programming and nonvolatile configuration of BCR-PLUS devices” in heading. Removed description below heading. Removed “Application Firmware Update over I^2C Interface”. Added **Making nonvolatile configuration changes**. Removed “Programming the Device Flash over SWD Interface”. Added **Firmware update**. Updated **Pinouts**: Updated **Table 1**. Updated **Application overview**: Updated **Legacy charging support**: Replaced “CHARGING_MODE Pin Behavior and Legacy Charging Support” with “Legacy charging support” in heading. Updated description. Removed table “Implementation of Charging Mode Options Using Resistor Divider Combinations”. Updated **Electrical specifications**: Updated **System resources**: Updated **Power-on reset (POR) with brown-out SWD interface**: Added **Table 18**. Added **Table 19**.
*B	2022-05-20	Changed status from Preliminary to Final. Updated **Packaging**: spec 002-16934 – Changed revision from *C to *E.
*C	2022-06-24	Removed “Restricted” status.
*D	2023-04-28	Updated **Features** section. Updated **Table 1** in Pinouts. Updated **Figure 4**, **Figure 5**. Added **Table 6**. Updated **Table 9**.

Important notice

Notice regarding compliance with Universal Serial Bus specification. Cypress offers firmware and hardware solutions that are certified to comply with the Universal Serial Bus specification, USB Type-C™ Cable and Connector Specification, and other specifications of USB Implementers Forum, Inc (USB-IF). You may use Cypress or third party software tools, including sample code, to modify the firmware for Cypress USB products. Modification of such firmware could cause the firmware/hardware combination to no longer comply with the relevant USB-IF specification. You are solely responsible ensuring the compliance of any modifications you make, and you must follow the compliance requirements of USB-IF before using any USB-IF trademarks or logos in connection with any modifications you make. In addition, if Cypress modifies firmware based on your specifications, then you are responsible for ensuring compliance with any desired standard or specifications as if you had made the modification. CYPRESS IS NOT RESPONSIBLE IN THE EVENT THAT YOU MODIFY OR HAVE MODIFIED A CERTIFIED CYPRESS PRODUCT AND SUCH MODIFIED PRODUCT NO LONGER COMPLIES WITH THE RELEVANT USB-IF SPECIFICATIONS.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-04-28
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-32090 Rev. *D

IMPORTANT NOTICE
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:

CYPD3176-24LQXQ CYPD3176-24LQXQT