EZ-PD™ PAG2P primary-side startup controller

General description

EZ-PD™ PAG2P (**P**ower **A**dapter **G**eneration **2** **P**rimary) is Infineon's second generation integrated primary-side startup controller for AC/DC applications targeting the mobile power adapter segment. EZ-PD™ PAG2P interface's with the AC mains rectified output on the primary side and receives the necessary PWM signal from the secondary side to provide a regulated output voltage. EZ-PD™ PAG2P is designed to operate in two configurations: half-bridge running in non-complementary state (Active Clamp Flyback) or a low-side switch configuration with a snubber circuit (QR, DCM, CCM). EZ-PD™ PAG2P is available in two versions:

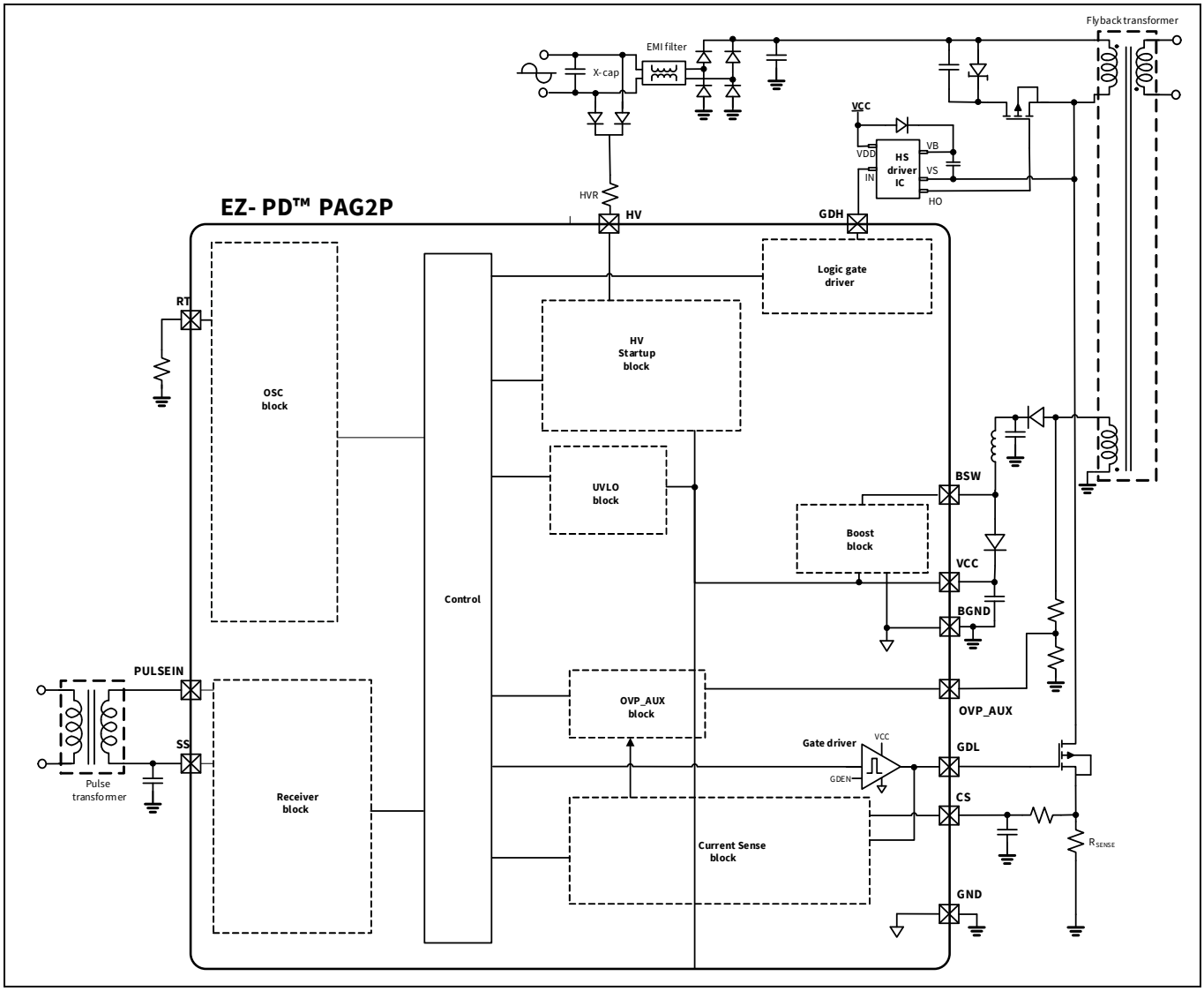
- Non X-cap applications
- X-cap applications

EZ-PD™ PAG2P is designed to complement a secondary controlled AC/DC flyback converter topology. In this topology, voltage and current regulation is performed by the secondary controller (EZ-PD™ PAG2S). EZ-PD™ PAG2P is responsible for providing the start-up function, driving the primary side FET as well as responding to fault conditions.

Features

- Works across universal AC mains input from 85 VAC to 265 VAC
- Low-side gate driver to drive primary side FET
- A logic-level gate driver to control external high-side floating gate driver IC (ACF)
- Free-running oscillator with PWM generator for start-up
- Line under voltage protection (UVP) and line overvoltage protection (OVP)
- Secondary overvoltage protection via auxiliary winding (SOVP)
- Overcurrent protection (OCP)
- Short-circuit protection (SCP)
- VCC pin short protection (VCCPSP)
- Integrated V_{CC} boost switch to support varied output voltage without the need for an external regulated LDO
- Integrated high-voltage start-up and shunt regulator
- A novel dual-output PET receiver is used to drive both high/low side switch using a single PET

Functional block diagram



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1 Pinout

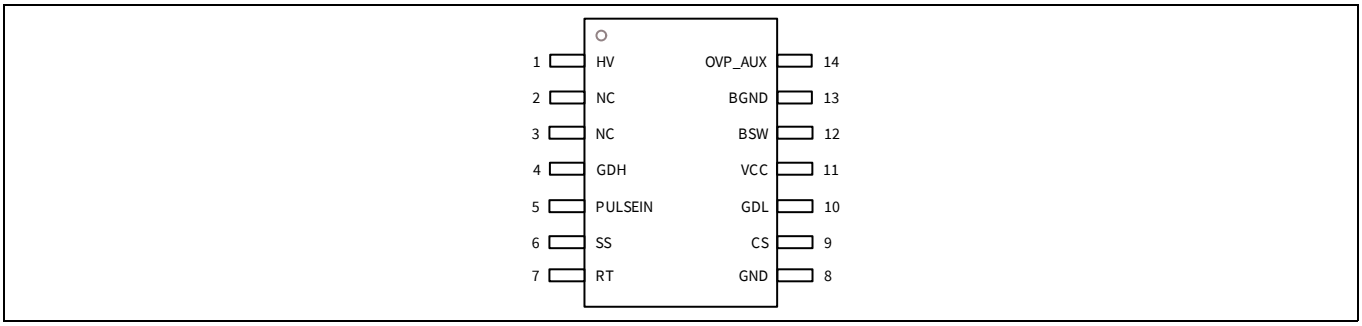


Figure 1 Pin map (SOIC-14)

Table 1 EZ-PD™ PAG2P pin description

Pin number	Pin name	Description
1	HV	High voltage start-up power supply input. HV is the power supply source during the start-up phase. This pin can be connected to either the bridge rectifier output or directly to the AC mains through the diodes. This pin has a maximum voltage rating of 500 V.
2,3	NC	No connect
4	GDH	High-side gate driver logic signal output. This pin is connected to high side FET via external high-side floating driver IC
5	PULSEIN	Pulse edge transformer (PET) input. EZ-PD™ PAG2P synchronizes to the secondary side pulses received at the PULSEIN input.
6	SS	External soft-start ramp capacitor terminal. This pin connects to the other end of the pulse transformer. The external capacitor connected to the SS pin determines the soft-start time.
7	RT	External timing resistor or bias current source. The RT pin is used to connect to an external timing resistor of 50 kΩ which determines the free running oscillator frequency. Oscillator frequency is typically 30 kHz.
8	GND	Ground
9	CS	Current sense input. Current sense input is used to provide overcurrent or short-circuit protection. Protection is provided by two current sense thresholds, CSTH1 (pulse by pulse) and CSTH2 (Short circuit) in the primary side by turning OFF the primary FET.
10	GDL	Primary FET low-side gate driver signal
11	V_{CC}	Low voltage power supply input
12	BSW	Boost converter switch node connected to drain terminal of internal HV NFET. This pin is connected to external boost inductor and diode.
13	BGND	Boost converter return pin connected to source terminal of internal HV NFET. This pin is connected to GND.
14	OVP_AUX	Auxiliary winding overvoltage detection input. EZ-PD™ PAG2P monitors this pin for overvoltage condition of secondary side, using an external resistor divider. Any voltage exceeding V_OVPAUXRISE on this pin is treated as an overvoltage fault condition. The overvoltage condition is monitored only during startup or open loop operation.

2 Application overview

EZ-PD™ PAG2P works with Infineon's secondary side controller PAG2S. **Figure 2** shows the application diagram of a USB Power Delivery adapter solution with 'EZ-PD™ PAG2P + EZ-PD™ PAG2S'. In this system, once the start-up phase is complete, the primary FET control is completely synchronized to the PWM pulses received from the secondary side. The PWM pulses are transmitted over an isolation barrier using a PET. EZ-PD™ PAG2P takes over control of the primary FET only during power-up and system fault scenarios.

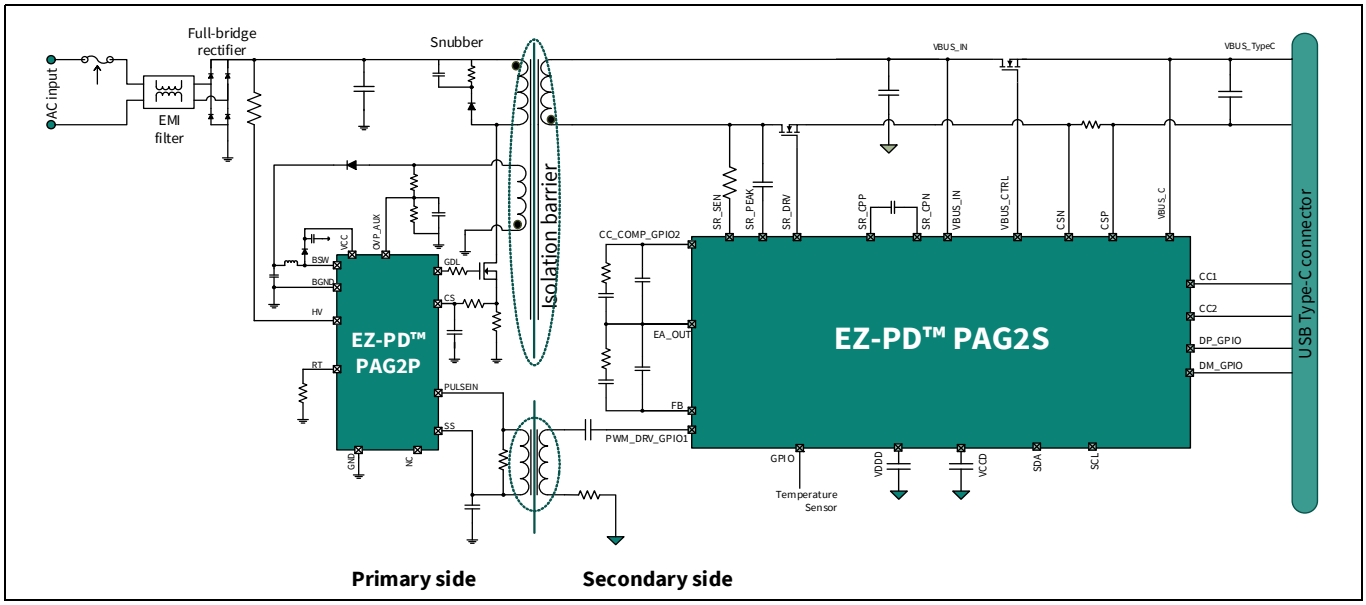


Figure 2 Type-C based mobile phone power adapter with EZ-PD™ PAG2P and EZ-PD™ PAG2S in a secondary controlled flyback topology configuration

Figure shows the application diagram for power adapter where PAG2P is powered directly from the AC mains before the full bridge rectifier. This topology enables discharging the X-cap using PAG2P instead of using a passive resistor with an added high side FET running in non-complementary half bridge mode. This is also known as ACF topology. The added high-side FET provides an advantage of recycling the leakage energy to the input thereby improving efficiency wherein traditional flyback the leakage energy would be dissipated in the snubber.

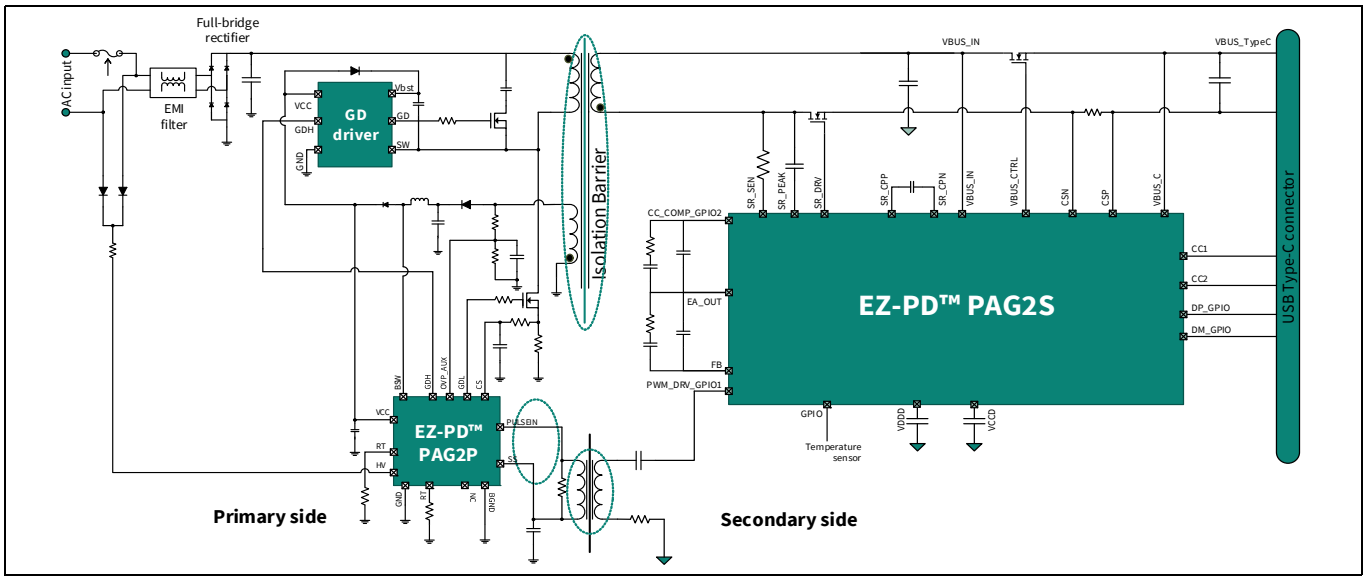


Figure 3 Type-C based power adapter with EZ-PD™ PAG2P with in X-cap discharge mode an ACF configuration

PAG2P works with not only PAG2S but also the PAG1S. **Figure 4** shows the application diagram of a USB power delivery adapter solution with 'EZ-PD™ PAG2P + EZ-PD™ PAG1S'.

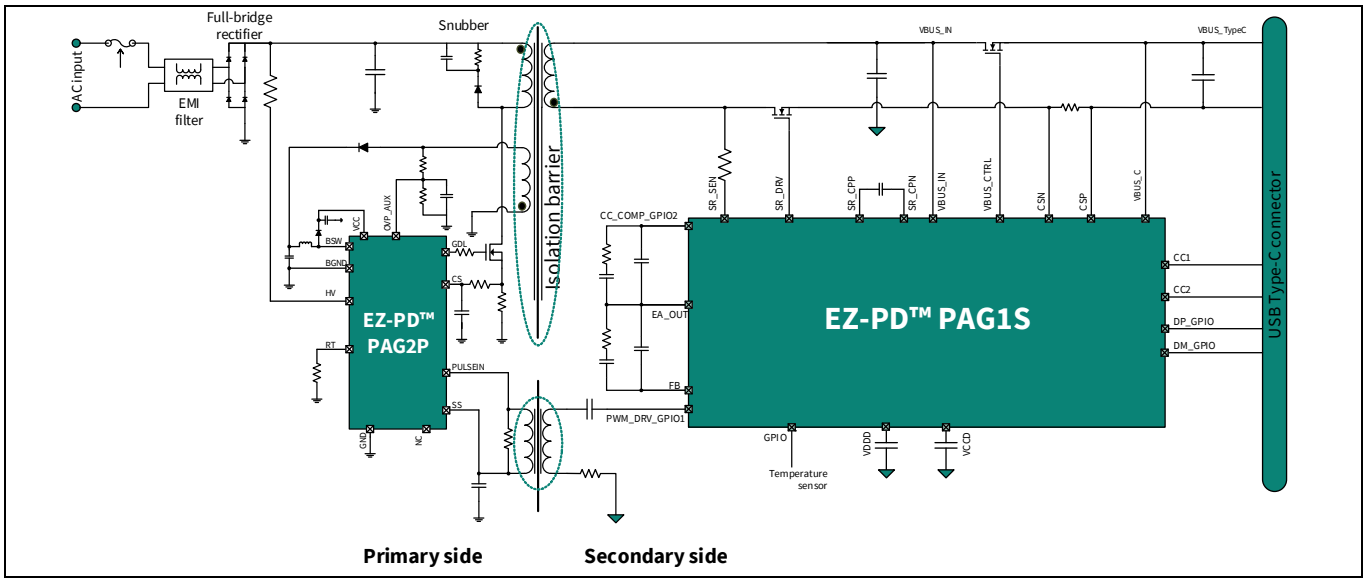


Figure 4 Type-C based power adapter with EZ-PD™ PAG2P with EZ-PD™ PAG1S in a secondary controlled flyback topology configuration

3 Functional description

3.1 High voltage start-up

The line voltage is within normal operating range, then the gate driver starts switching. An internal high-voltage JEFT take current from HV pin to charge up the VCC capacitor during start-up phase. An auxiliary winding from the flyback transformer will be used to supply EZ-PD™ PAG2P after start-up phase and no current will be sourced from the HV pin after start-up phase. Additionally, two modes are supported, namely, X-cap mode and non X-cap mode. A VCC pin short protection is introduced. In the case of VCC pin shorted to ground, EZ-PD™ PAG2P shall limit the startup current to maximum of I_HV_VCCSTG and avoid overheating of the IC.

3.1.1 X-cap mode

The HV pin of PAG2P is connected to the AC mains through diodes. A UVLO is included to prevent false startup when the line voltage is low and keeps the primary FET OFF. An OVP is implemented to shut the primary FET OFF when line voltage exceeds V_HV_OVRISE. PAG2P discharges the X-capacitor via HV pin when the X-cap mode is enabled.

3.1.2 Non X-cap mode

The HV pin is connected to the DC rectified voltage. The pin powers PAG2P during startup. Additionally, it provides under voltage and overvoltage protection via HV pin. As long as the fault is present, protection is enabled.

3.2 Soft-start

The soft-start feature allows PAG2P to gradually increase the output voltage of the flyback converter till the secondary side takes control of the regulation. Soft-start is used during initial start-up sequence and fault condition. The duration of the soft-start is controlled by an external capacitor connected to the SS pin and the frequency of soft-start is determined by an external resistor connected to the RT pin. An internal current source of I_{SSCURR} charges the external capacitor and the maximum amplitude for the soft-start ramp is 3.75 V. A 3.75 V dictates the maximum duty cycle. Duty cycle is gradually increased from 1% to maximum 70% according to the soft-start capacitor.

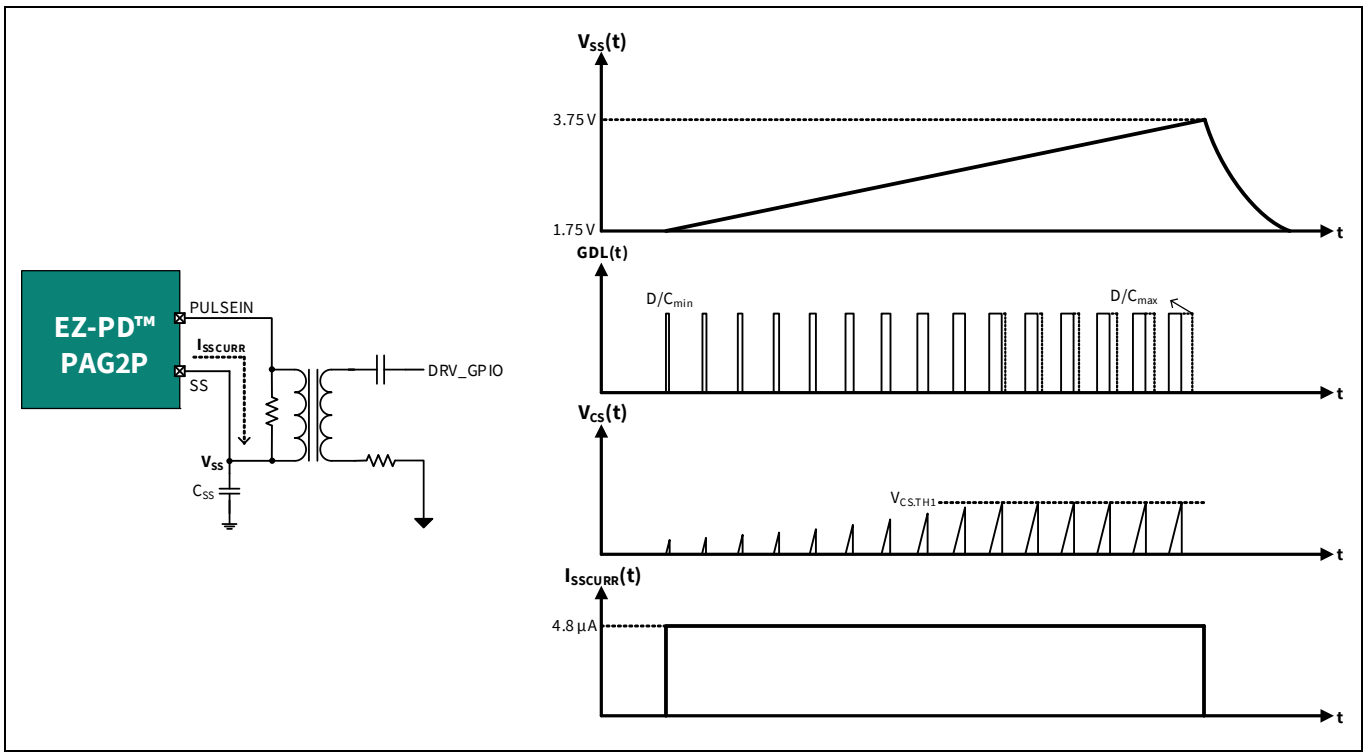


Figure 5 Soft-start operation

A Soft-start time is calculated via following equation. A bigger soft-start capacitance allows a longer soft-start time. A typical soft-start time is about 41.67 ms when the 0.1 µF soft-start capacitor is used.

$$t_{SS} = C_{SS} \times \frac{2.0V}{I_{SSCURR}}$$

3.3 X-cap mode

PAG2P monitors AC line by turning ON internal current source every 1 ms. X-cap mode is detected when line UV event occur less than 3 times within 128 ms time period. At every half-line cycle, line UV event is expected unless AC line is disconnected. Once X-cap mode is enabled, PAG2P will turn ON internal discharge path to discharge the X-capacitor.

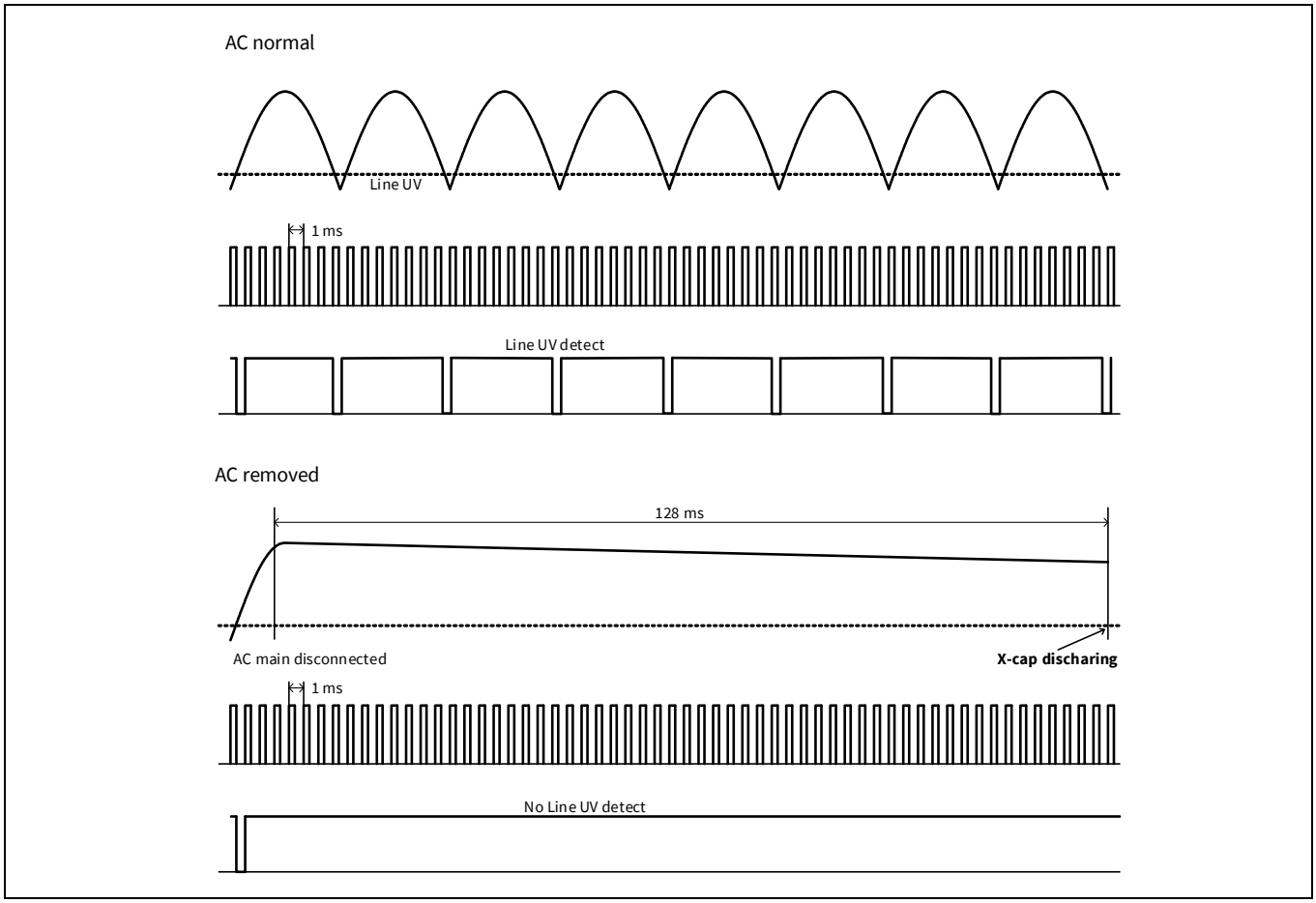


Figure 6 X-cap mode operation

3.4 Secondary synchronization

During the start-up phase, PAG2P performs synchronization with the secondary side pulses from the PULSEIN pin when the secondary side is ACTIVE. The PWM signal from the secondary side is coupled to the primary side using a pulse edge transformer (PET). Four conditions have to be met to synchronize with PWM signal from secondary side.

- Brown-in (V_{HV} > V_HV_UVRISE)
- V_{SS} > 1.75 V
- FBon/FBoff signal is coming

Once the above conditions are met, PAG2P controls primary side gate driver accordingly. The PET is an important component to ensure proper frequency response and should have an adequate Q-factor to avoid excessive overshoot. The pulse width measured on the PULSEIN pin shall be within T_PULSEINPW.

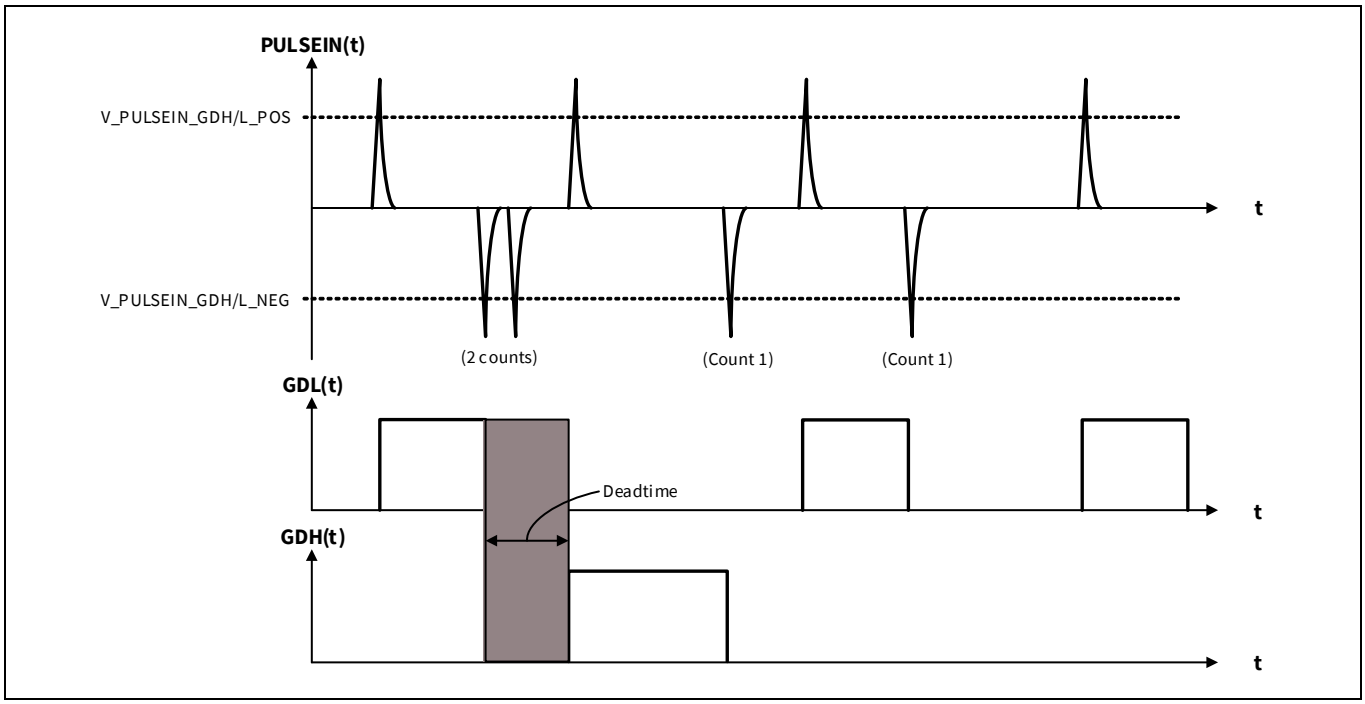


Figure 7 Pulse edge transformer

A novel dual-output PET receiver is implemented with on-the-fly decoding scheme to differentiate PWML and PWMH signals received from secondary side and primary side gate drivers accordingly. A positive pulse followed by one time negative detection indicates starts of PWML. A positive pulse followed by two consecutive negative detection means starts of PWMH. A negative detection followed by positive pulse indicates stops of PWML/PWMH.

3.5 Low-side gate driver

A gate driver is to drive an external primary side FET and it shall be capable of providing fast, high-current gate drive pulses. The propagation delay from the PULSEIN pin to the GDL pin shall be less than T_GDLPDR or T_GDLPDF. The pulse amplitude shall be greater than V_PULSEIN_GDL_POS min and V_PULSEIN_GDL_NEG max.

3.6 High-side gate driver

The HS gate driver is required to provide logic-level control to an external high-side floating driver IC to drive an external primary side FET and capable of driving a FET which at the source node will have a maximum floating voltage of 700 V. The propagation delay from the PULSEIN pin to the GDH pin shall be less than T_GDHPDR or T_GDHPDF. The pulse amplitude shall be greater than V_PULSEIN_GDH_POS min and V_PULSEIN_GDH_NEG max. The high side gate driver is meant to be used in an ACF configuration. Dead-time between the low side FET and high side FET is determined by EZ-PD™ PAG2S during initial startup. Dead-time is programmable from the secondary side with proprietary dead-time calibration routine.

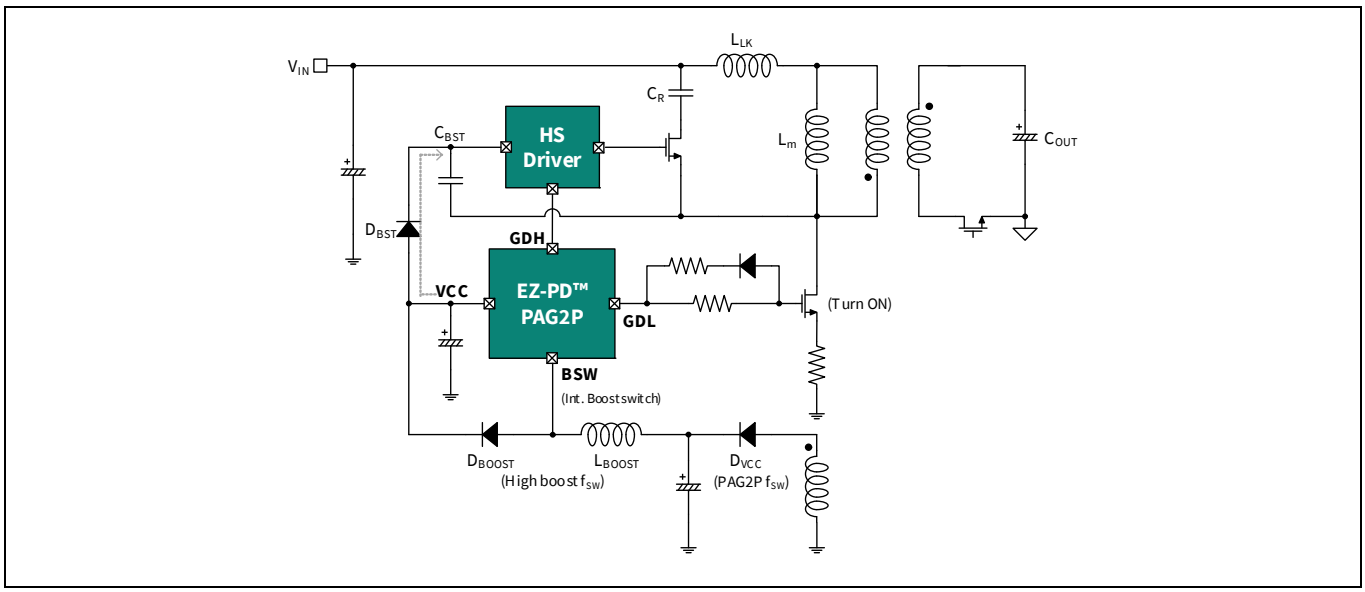


Figure 8 Active clamp flyback configuration

3.7 Current sense fault protection

Current sense fault protection is used to detect overcurrent due to larger current flowing from flyback transformer or protect against any short circuit which might be present due to the flyback transformer being shorted or the FET being shorted. Protection is provided by two current sense thresholds, CSTH1 (pulse by pulse current limit) and CSTH2 (short circuit) for 3 consecutive cycles in the primary side by turning OFF the primary FET (for CSTH1) or by shutting down (for CSTH2).

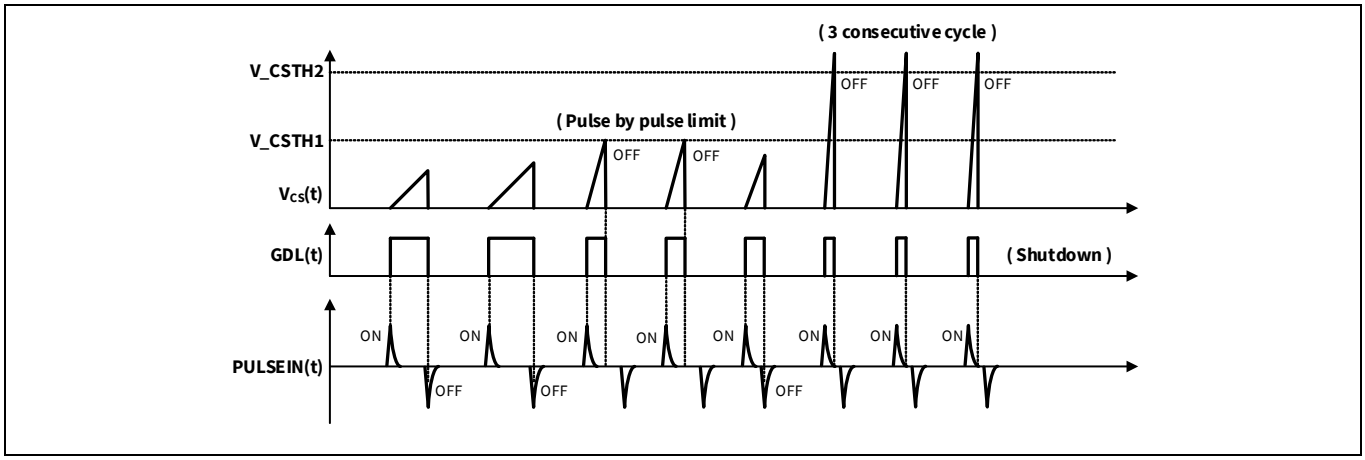


Figure 9 Current sense fault protection

3.8 Auxiliary overvoltage protection

OVP_AUX pin monitors the secondary side output voltage during soft-start. In open loop, if OVP_AUX exceeds V_OVPAUXRISE, the soft-start resumes after TAR seconds. Auxiliary overvoltage protection is not activated during closed loop.

3.9 Vcc boost converter

The BSW pin of EZ-PD™ PAG2P is connected to an external inductor which the other terminal is connected to an auxiliary winding from the flyback transformer through a diode. The BSW pin is also connected to Vcc pin through an external diode to form a boost regulator topology together with the inductor. Once EZ-PD™ PAG2S controls primary side gate driver, boost converter will take-over from high-voltage start-up circuit to supply Vcc during close loop.

A current coming from HV pin charges Vcc capacitor while start-up phase. Once Vcc is increased up to 7.5 V, internal LDO is ready. Then, EZ-PD™ PAG2P spend some time for initialization. After finishing initialization, the free running oscillator comes in and V_AUXIN is built up gradually. Vcc boost converter is enabled and Vcc is regulated to V_VCCREG unless V_AUXIN is over than V_VINOV. An auxiliary winding (V_AUXIN) take over supplying Vcc when the V_AUXIN is higher than V_VINOV. Boost converter resumes switching when V_AUXIN is below V_VINUV.

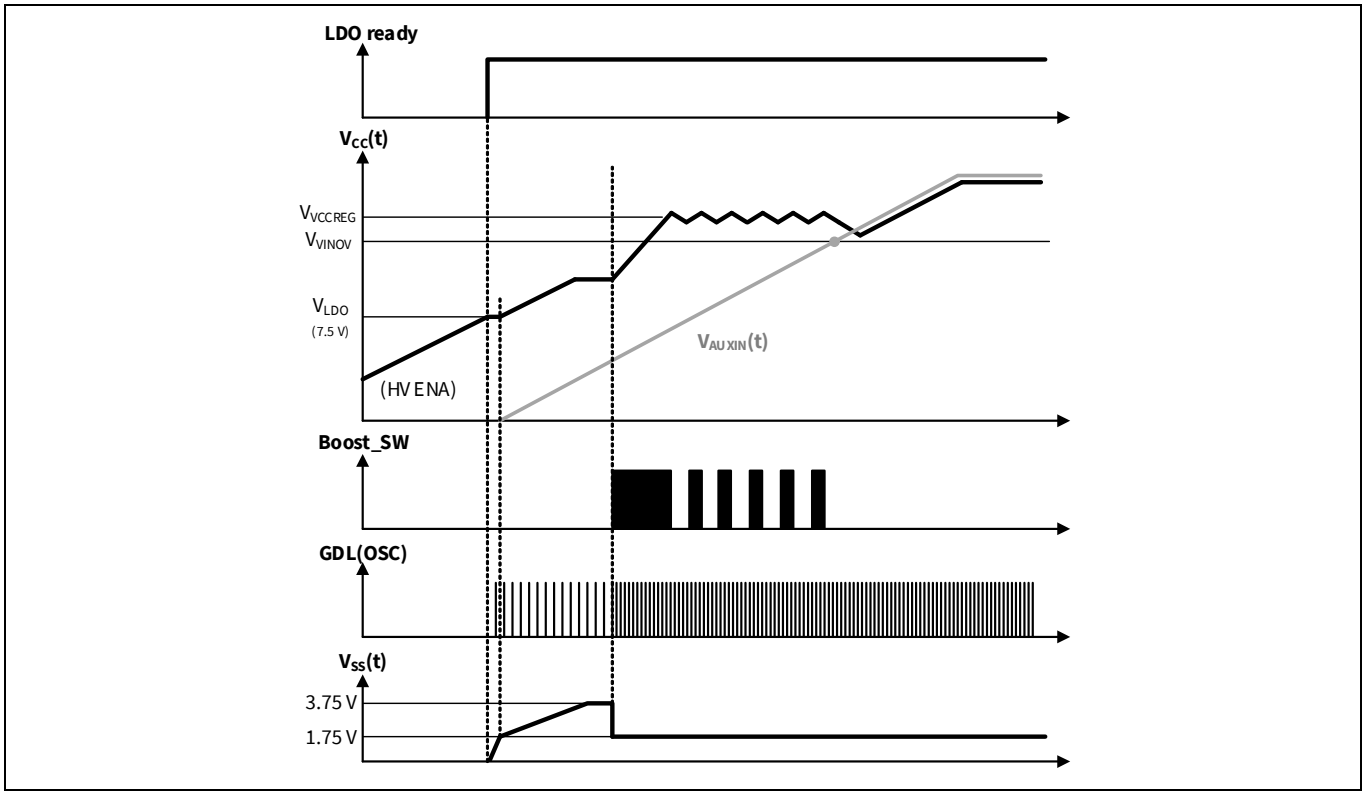


Figure 10 Power-up sequence

3.10 Auto-restart timer

A fixed timer of TAR sec is available for various fault conditions. The timer is synched to the free-running oscillator. The free-running oscillator will be running at FOSC.

3.11 Protection and fault condition

Primarily there are four type of protection actions used in various fault conditions.

- **Auto-restart:** In this mode, EZ-PD™ PAG2P will wait TAR sec before doing a soft-start. This sequence keeps repeating continuously if fault condition persists (See **Figure 11**).
- **Latch or shut-down:** No Auto restart timer or soft-start is implemented. Shuts the IC down and power to the IC needs to be removed to unlatch.
- **Gate OFF:** This only turns OFF the gate drive pulse and waits for the fault condition to pass before the IC functions normally.
- **Max duty cycle:** Gate driver will be ON for 19 µs (maximum duty) during soft-start. When secondary is in control, gate driver will be ON for 30 µs (maximum duty).

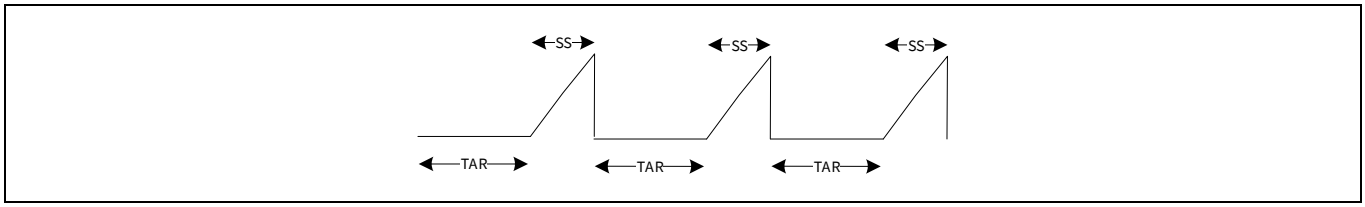


Figure 11 Auto-restart

Table 2 Fault conditions and protection action

S#	Fault	Action
1a	HV pin falls below the threshold voltage V_{HV_UVFALL} in open loop	Gate driver output is low immediately. Gate driver output resumes uncompleted soft-start switching if HV pin exceeds V_{HV_UVRISE} within T_{HV_UVDB}. Gate driver output recovers switching with new soft-start if HV pin exceeds V_{HV_UVRISE} over T_{HV_UVDB}.
1b	HV pin falls below the threshold voltage V_{HV_UVFALL} in close loop	Gate driver output is low after T_{HV_UVDB}. Gate driver output recovers switching if HV pin exceeds V_{HV_UVRISE}.
2a	HV pin exceeds threshold voltage V_{HV_OVRISE} in open loop	Gate driver output is low during fault condition followed by Auto restart if HV pin falls below V_{HV_OVFALL}.
2b	HV pin exceeds threshold voltage V_{HV_OVRISE} in close loop	Gate driver output is low during fault condition. Gate driver output recovers switching if HV pin falls below V_{HV_OVFALL}.
3	OVP_AUX pin exceeds threshold voltage	Gate driver output is low during fault condition followed by Auto restart.
4	CS pin exceeds threshold voltage V_{CSTH1}	Gate driver output is low during fault condition.
5	CS pin exceeds threshold voltage V_{CSTH2} for 3x Gate Driver output switching cycles consecutively	Shutdown
6	Receive STOP command (3 Stop pulses followed by no pulses for 200 ms) from Secondary side	Gate driver output is low followed by shutdown.
7	Receive no pulses from Secondary side for TAR sec after last Stop pulse	Auto restart
8	Receive Gate Driver Start pulse and no Stop pulse from Secondary side	Keep gate driver ON for 30 µs followed by Auto restart.
9	Receive High-side Gate Driver Start pulse and no Stop pulse from Secondary side	Keep High-side gate driver ON for 30 µs.

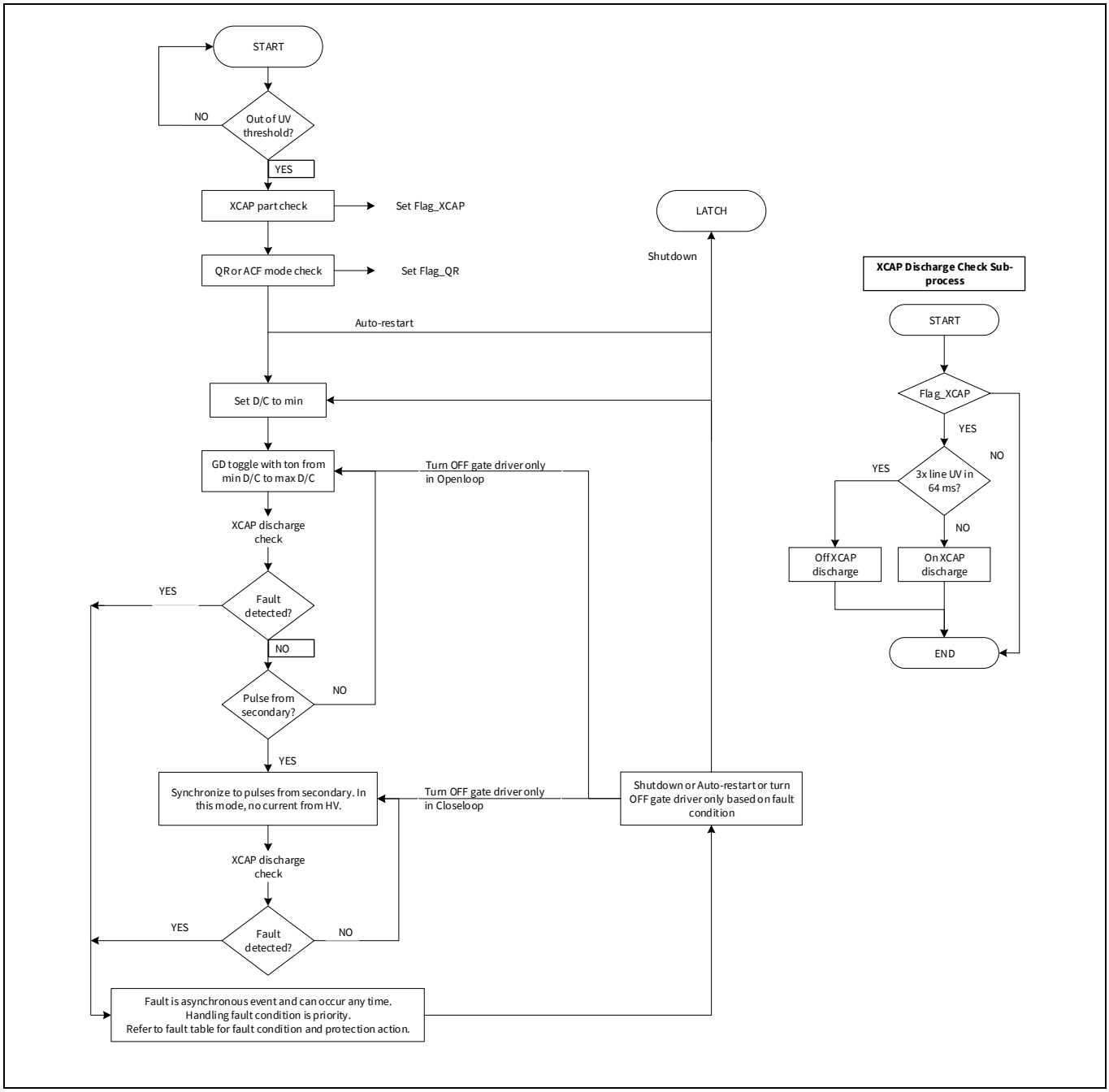


Figure 12 EZ-PD™ PAG2P operation flow chart

4 Comparison table between EZ-PD™ PAG1P and EZ-PD™ PAG2P

Table 3 Comparison table between EZ-PD™ PAG1P and EZ-PD™ PAG2P

Feature	EZ-PD™ PAG1P	EZ-PD™ PAG2P
ACF compatible	No	Yes (With secondary side controller)
Package	SOIC-10	SOIC-14
Protections	Brown-in, Brown-out, Line-OVP, OCP, OVP, UVLO	Brown-in, Brown-out, Line-OVP, OCP, CSPSP, VCCPSP, SCP, Secondary-OVP, UVLO
V_{CC}	Supplied via aux winding / External voltage regulator is required	No need external voltage regulator / Boost switch is integrated
High voltage start-up	Yes (via VDD700 pin)	Yes (via HV pin)
X-cap discharge mode	Yes	Yes
Soft-start	Programmable soft-start	Programmable soft-start
V_{CC} pin short protection	No	Yes

5 Electrical specifications

Table 4 Absolute maximum ratings

Description	Min	Typ	Max	Unit	Details/conditions
Voltage on HV	0	–	500	V	–
Output current on GDL	-1		1	A	
Voltage on BSW	0		24	V	
Voltage on Vcc	0		24		
Voltage on GDH, CS, SS, OVP_AUX	-0.3		8.25		
Voltage on PULSEIN	-5		8.25		
Voltage on RT	0		8.25		
Electrostatic discharge human body model	2000		–	V	
Electrostatic discharge charged device model	500				
Pin current for latch-up	-100		100	mA	Except for SS and OVP_AUX. For SS and OVP_AUX, use -0.5V. For OVP_AUX, max -1.5mA. For RT, negative injection is not recommended.

Table 5 Silicon power specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
HV	High voltage supply	120	–	380	V	–
V_AUXIN	Auxiliary supply	1.5	–	22		
I_HV_LATCH	Current from HV (HV = 380 V)	–	65	200	µA	EZ-PD™ PAG2P is in shutdown
I_HV_NOGD	Current from HV (HV = 380 V)		380	600		All circuits active except LS gate driver not toggling
I_HV_ACTIVE	Current from HV (HV = 325 V)		880	1100		All circuits active including LS gate driver toggling at 30 kHz; CL = 1 nF, Vcc not driven
I_Vcc_NOGD	Current from Vcc (Vcc = 12 V)		380	600		All circuits active except LS gate driver not toggling
I_Vcc_ACTIVE	Current from Vcc (Vcc = 12 V)		880	1100		All circuits active including LS gate driver toggling at 30 kHz; CL = 1 nF

Table 5 Silicon power specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I_Vcc_ACTIVE_LS	Current from Vcc (Vcc = 12 V)	–	–	7	mA	All circuits active including LS gate driver toggling at 300 kHz; CL = 1 nF
I_Vcc_ACTIVE_HS	Current from Vcc (Vcc = 12 V)			5		External HS gate driver IC toggling at 300 kHz; CL = 1 nF
I_XCAP_DISCHARGE	Current from HV while discharging X-cap	0.48		–		–
I_HV_STARTUP	Current from HV when starting up	–	10	15	mA	HV = 380V; Vcc higher than V_VCCSTG max
I_HV_VCCSTG	Current from HV when Vcc shorted to ground	0.5	–	4		HV = 380V; Vcc lower than V_VCCSTG min
V_VCCSTG	Vcc short to ground protection threshold	0.9		3.2	V	–

Table 6 Electrical characteristic of HV pin

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_HV_UVRISE	Under voltage rising threshold on HV	90	100	118	V	–
V_HV_UVFALL	Under voltage falling threshold	81	90	110		
V_HV_OVRISE	Overvoltage rising threshold	400	430	490		
V_HV_OVFALL	Overvoltage falling threshold	395	420	480		
T_HV_UVDB	Debounce time under-voltage falling	24	30	52	ms	

Table 7 Electrical characteristic of OVP_AUX pin

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_OVPAUXRISE	Overvoltage threshold ON AUXIN	1.03	1.2	1.32	V	–
V_OVPAUXFALL	Overvoltage falling threshold ON AUXIN	1.01	1.18	1.3		
T_OVPAUXBLK	Blanking time on OVP_AUX when GDL output goes HIGH to LOW	130	200	275	ns	

Table 8 Electrical characteristic of LS gate driver GDL pin

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_GDLVOL	GDL low level output voltage	–	–	2	V	Vcc = 12 V and sinking 200 mA
V_GDLVOH	GDL high level output voltage	9		–		
T_GDLTR	Rise time (20~80%)	–	25	45	ns	CL = 1 nF, Vcc = 12 V
T_GDLTF	Fall time (80~20%)		15	35		
T_GDLPDR	PULSEIN to GDL rising delay (50~20%)		–	100		
T_GDLPDF	PULSEIN to GDL falling delay (50~80%)			100		
T_GDLPDR_QR	PULSEIN to GDL rising delay (50~20%) in QR mode			80		–
T_GDLPDF_QR	PULSEIN to GDL falling delay (50~80%) in QR mode			80		

Table 9 Electrical characteristic of HS gate driver GDH pin

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_GDHVOL	GDH Low level output voltage	–	–	0.5	V	Vcc = 12 V and sinking 1 mA
V_GDHVOH	GDH High level output voltage	4		–		
T_GDHTR	Rise time (20~80%)	–	20	40	ns	CL = 25 pF
T_GDHTF	Fall time (80~20%)		5	15		
T_GDHPDR	PULSEIN to GDH rising delay (50~20%)		–	100		
T_GDHPDF	PULSEIN to GDH falling delay (50~80%)			100		

Table 10 Electrical characteristic of CS pin

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_CSTH1	Threshold voltage pulse-by-pulse	250	300	350	mV	–
V_CSTH2	Shutdown threshold voltage	500	600	700		
T_CSPD	Delay time CS to GDH/GDL	–	–	120	ns	CL = 1 nF
T_CSLEB	Leading edge blanking time	75	125	150		–

Table 11 Electrical characteristic of PULSEIN pin

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_PULSEIN_G-DL_POS	Positive pulse amplitude for GDL sensing	1.6	–	5	V	Reference to SS pin
V_PULSEIN_G-DL_NEG	Negative pulse amplitude for GDL sensing	-5		-1.4		
V_PULSEIN_G-DH_POS	Positive pulse amplitude for GDH sensing	1.6		5		
V_PULSEIN_G-DH_NEG	Negative pulse amplitude for GDH sensing	-5		-1.4		
T_PULSEINPW	Minimum pulse width	10		200	ns	–

Table 12 Electrical characteristic of free running oscillator

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FOSC	Frequency	24	30	36	kHz	FOSC = (I_RTCURR/40)*(1/5pF) * (1/4) = 30 kHz
DCMIN	Minimum duty cycle	1	–	–	%	–
DCMAX	Maximum duty cycle	–		70	%	

Table 13 Electrical characteristic of RT pin

Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
RT	Timing resistor	–	50± 1%	–	kΩ	± 1%
I_RTCURR	Current through RT		24 + 10% / - 12%		µA	–

Table 14 Electrical characteristic of SS pin/auto restart time

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I_SSCURR	Current for charging soft-start capacitor	4.2	4.8	6	µA	Soft start time = Css*Δ V/I_SSCURR; Maximum soft start voltage is 3.75 V and start of soft start is 1.75 V.
TAR	Auto-restart time	1.6	2	2.8	s	–

Table 15 Electrical characteristic of BSW pin

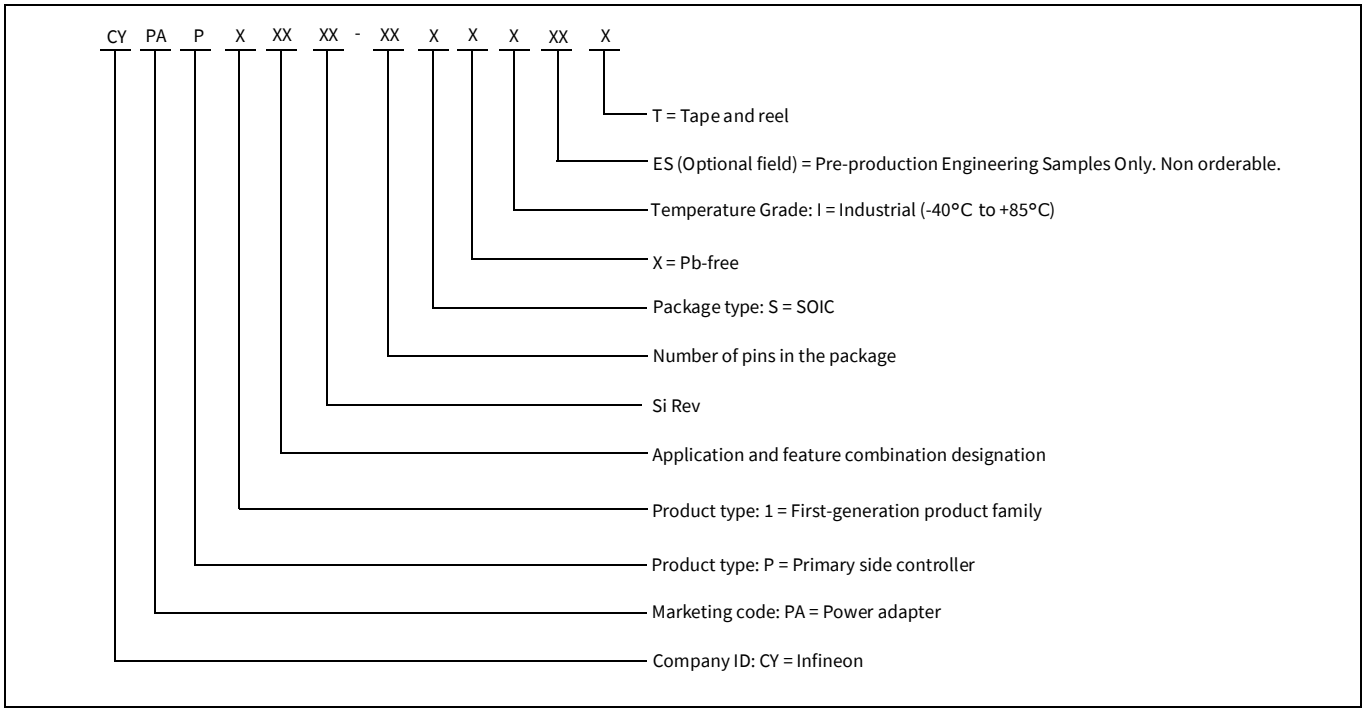
Parameter	Description	Min	Typ	Max	Unit	Details/conditions
R_BSW	RDSON of internal NFET	–	–	2	Ω	–
I_BSW	Peak current threshold		350	500	mA	V_AUXIN = 12 V; L = 10 µH 200 mΩ
V_VCCREG	Vcc average regulation setpoint	13.5	14.5	16.5	V	Load= 10 mA, V_AUXIN = 1.5 V, L = 10 µH 200 mΩ, PMEG120G10ELR
V_VCCREG2	Vcc average regulation setpoint	13.5	14.5	16.5		Load= 5 mA, V_AUXIN = 1.0 V, L = 10 µH 200 mΩ, PMEG120G10ELR
V_VINOV	Highest VIN to disable boost switching	12.3	14	15.5		–
V_VINUV	Hysteresis below V_VINOV to enable boost switching	12.2	13.8	15.3		
V_VCCVINDIFF	V_VINOV(max) – V_VCCREG(min)	–	–	0		

6 Ordering Information

Table 16 Ordering part numbers

MPN	Mode	Package type	Silicon revision	Packaging
CYPAP211A1-14SXI	Non X-cap	14-pin SOIC	A1	Tube
CYPAP211A1-14SXIT	Non X-cap			Tape and reel
CYPAP212A1-14SXI	X-cap			Tube
CYPAP212A1-14SXIT	X-cap			Tape and reel

6.1 Ordering code definitions



7 Packaging

Table 17 Package characteristics

Spec ID#	Parameter	Description	Min	Typ	Max	Unit
BID#17	TA	Operating Ambient temperature	-40	–	85	°C
BID#20	TJ	Operating Junction temperature			125	
BID#26	PKG_1	Package 1: Type	–		SOIC	–
BID#32	PKG_1TJA	Package 1: Theta-JA		108	–	°C/W

Table 18 Package list

Package	Description	Package drawing #
14-pin SOIC	14-pin 8.65 × 6 × 1.75 mm with 1.27 mm pitch	See **Figure 13**

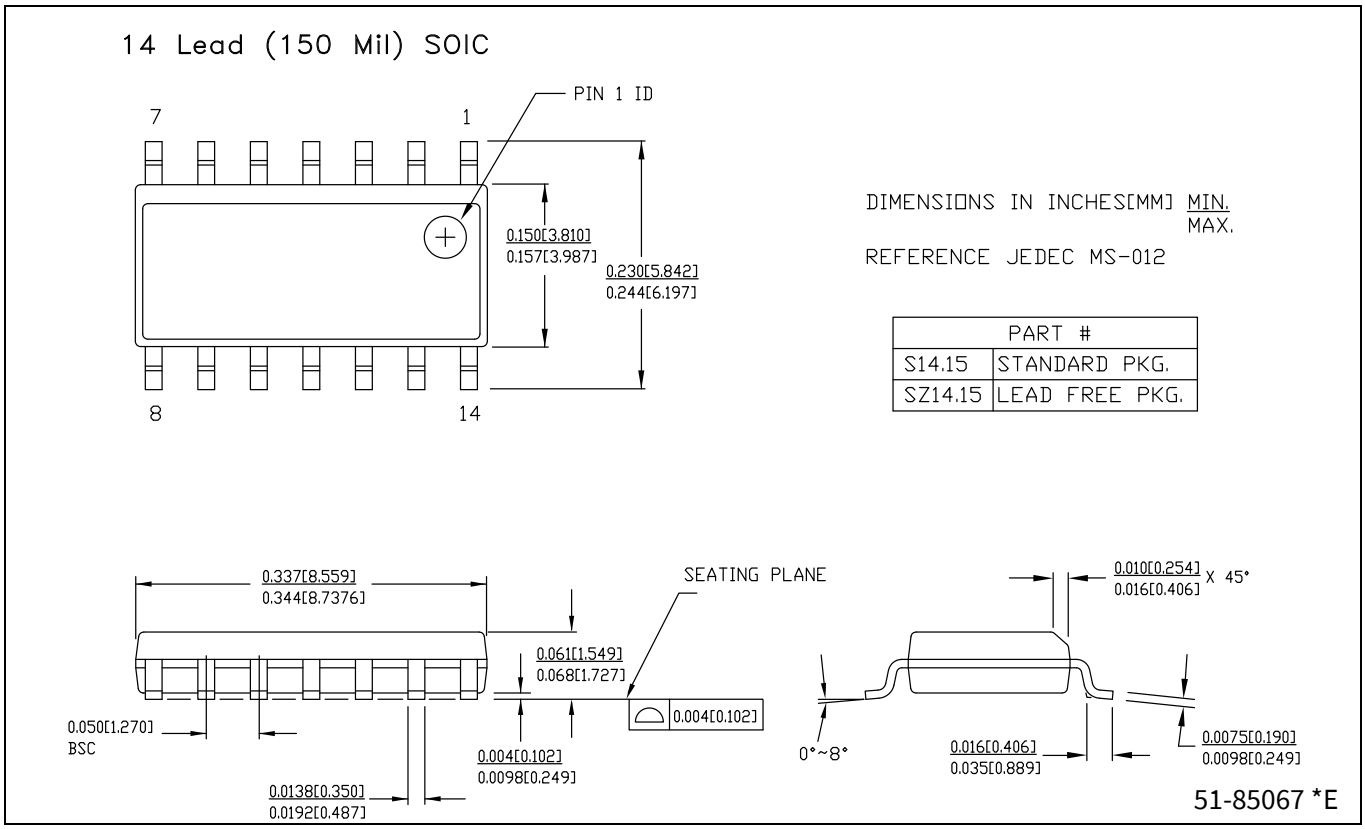


Figure 13 14-pin SOIC package mechanical drawing (PG_DSO-14-800)

8 Acronyms

Table 19 Acronyms used in this document

Acronym	Description
BSW	boost converter switch
CDM	charged device model
ESD	electrostatic discharge
HBM	Human body model
HV	high voltage
LDO	low dropout
OCP	Overcurrent protection
OVP	Overvoltage protection
PET	Pulse edge transformer
RT	timing resistor
SCP	Short-circuit protection
SOVP	Secondary overvoltage protection
SS	soft-start
UVP	Under voltage protection
VAC	input AC voltage

9 Document conventions

9.1 Units of measure

Table 20 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilo ohm
MHz	megahertz
MΩ	mega-ohm
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
ns	nanosecond
pF	picofarad
s	second

Revision history

Document revision	Date	Description of changes
*F	2023-06-13	Release to web.

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Email:
erratum@infineon.com

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