Automotive PSoC™ 4: PSoC™ 4100S family

Based on Arm® Cortex®-M0+ CPU

Functional description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU, while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4100S product family is a member of the PSoC™ 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CAPSENSE™) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC™ 4100S products will be upward compatible with members of the PSoC™ 4 platform for new applications and design needs.

Features

- Automotive Electronics Council (AEC) AEC-Q100 Qualified
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64 KB of flash with read accelerator
  - Up to 8 KB of SRAM
- Programmable analog
  - Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and Comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low-power mode.
  - 12-bit 1-Msps SAR ADC with differential and single-ended modes, and channel sequencer with signal averaging
  - Single-slope 10-bit ADC function provided by a capacitance sensing block
  - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in Deep Sleep low-power mode
- Programmable digital
  - Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs
- Low-power 1.71-V to 5.5-V operation
  - Deep Sleep mode with operational analog and 2.5-µA digital system current
- Capacitive sensing
  - Capacitive sigma-delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (> 5:1) and water tolerance
  - Infineon-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- LCD drive capability
  - LCD segment drive capability on GPIOs
- Serial communication
  - Three independent run-time reconfigurable serial communication blocks (SCBs) with re-configurable I^2C, SPI, UART, or LIN slave functionality
- Timing and pulse-width modulation
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, edge, and pseudo-random modes
  - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications
- Programmable GPIO pins
  - 40-pin QFN, and 28-pin SSOP packages
  - Any GPIO pin can be CAPSENSE™, analog, or digital
  - Drive modes, strengths, and slew rates are programmable

Features

- PSoC™ Creator design environment
  - Integrated development environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
  - Applications programming interface (API) component for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
  - After schematic entry, development can be done with Arm®-based industry-standard development tools
- Temperature ranges
  - A-grade: –40°C to +85°C
  - S-grade: –40°C to +105°C
  - E-grade: –40°C to +125°C[1]

Note
1. This device can also operate at temperatures exceeding 125°C (the high temperature of the AEC-Q100 Grade 1 operating range) for a limited amount of time depending on the mission profile of the application. Infineon provides a retention calculator to help estimate the retention lifetime based on the customers' individual temperature profiles for operation throughout the –40°C to +150°C ambient temperature range. Go to the **Infineon community page** for more details.

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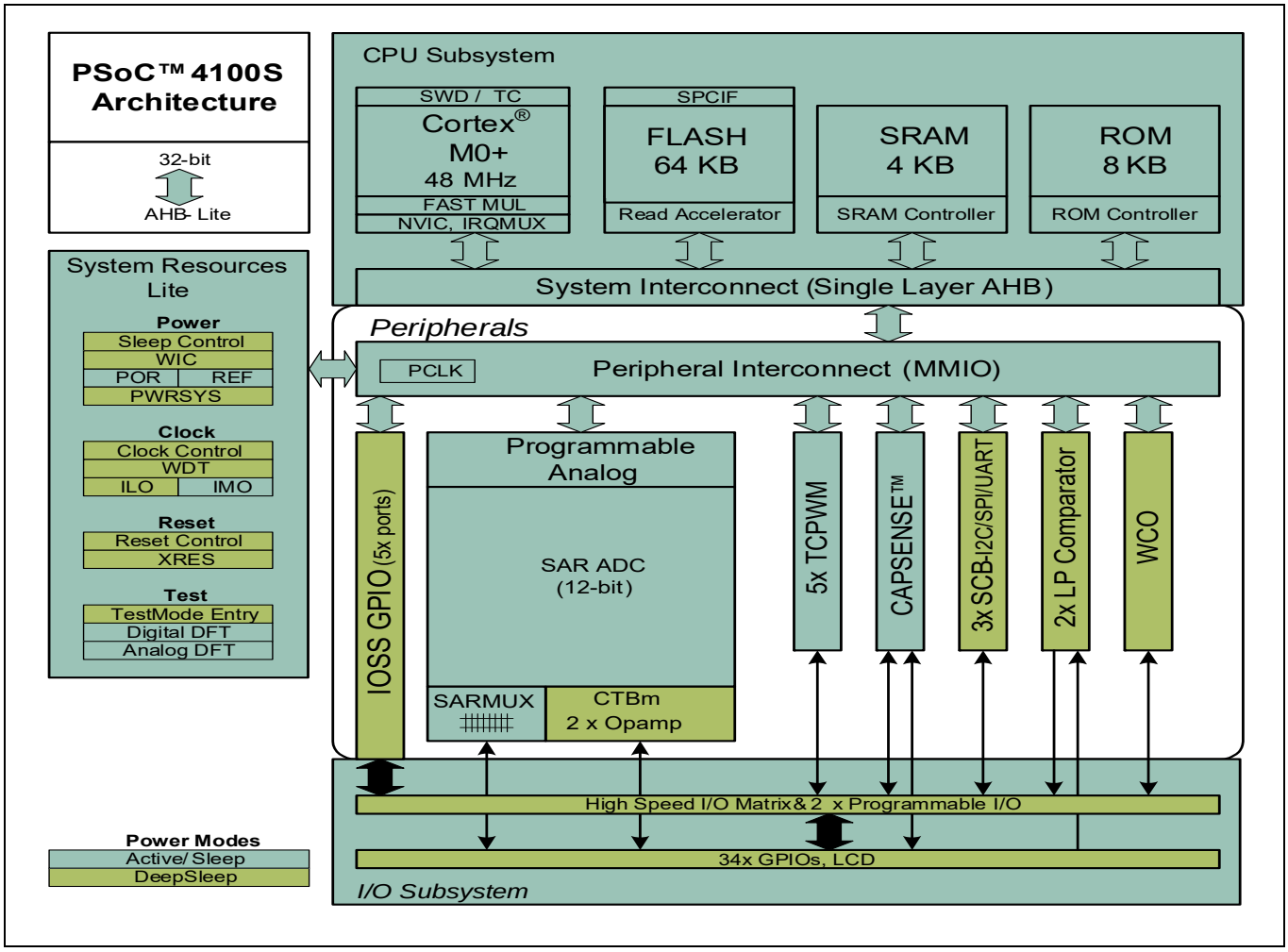


Figure 1 Logic block diagram

1 Functional overview

PSoC™ 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® SWD interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully integrated programming and debug support for the PSoC™ 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC™ 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC™ 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC™ 4100S allows the customer to make.

1.1 CPU and memory subsystem

1.1.1 CPU

The Cortex®-M0+ CPU in the PSoC™ 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the SWD interface, which is a two-wire form of JTAG. The debug configuration used for PSoC™ 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

1.1.2 Flash

The PSoC™ 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

1.1.3 SRAM

8 KB of SRAM are provided with zero wait state access at 48 MHz.

1.1.4 SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

1.2 System resources

1.2.1 Power system

The power system is described in detail in the section **"Power"** on page 17. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC™ 4100S operates with a single external supply over the range of either 1.8 V ± 5% (externally regulated) or 1.8 V to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC™ 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

1.2.2 Clock system

The PSoC™ 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4100S consists of the internal main oscillator (IMO), internal low-speed oscillator (ILO), a 32 kHz watch crystal oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

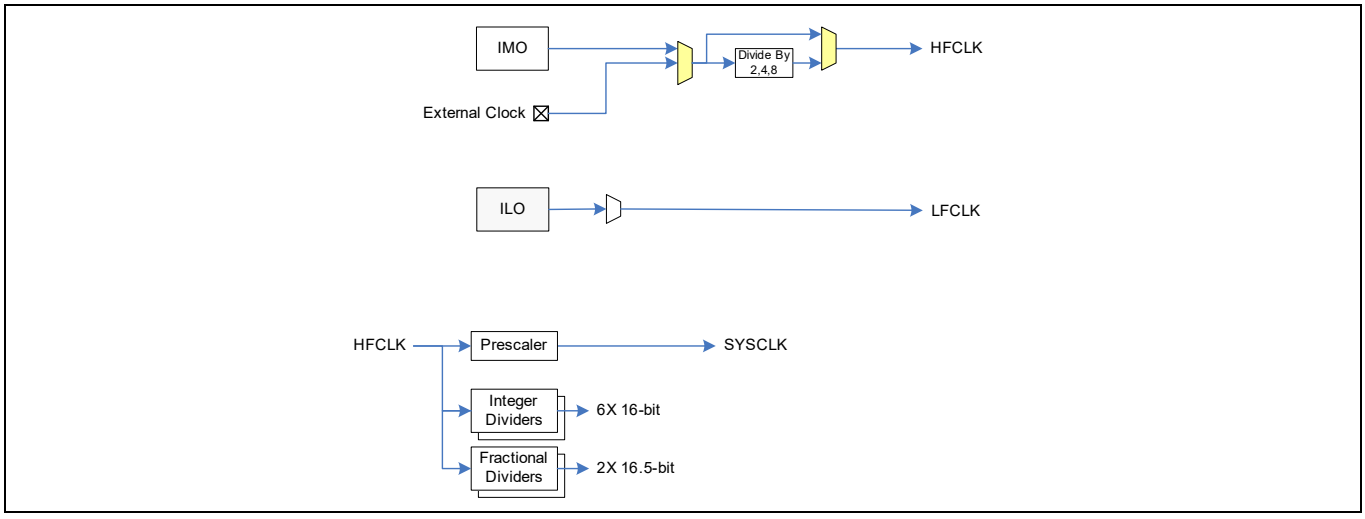


Figure 2 Clocking architecture

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC™ 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC™ Creator.

1.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4100S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon-provided calibration settings is ±2%.

1.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

1.2.5 Watch crystal oscillator (WCO)

The PSoC™ 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

1.2.6 Watchdog timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

1.2.7 Reset

The PSoC™ 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

1.3 Analog blocks

1.3.1 12-bit successive approximation register (SAR) ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

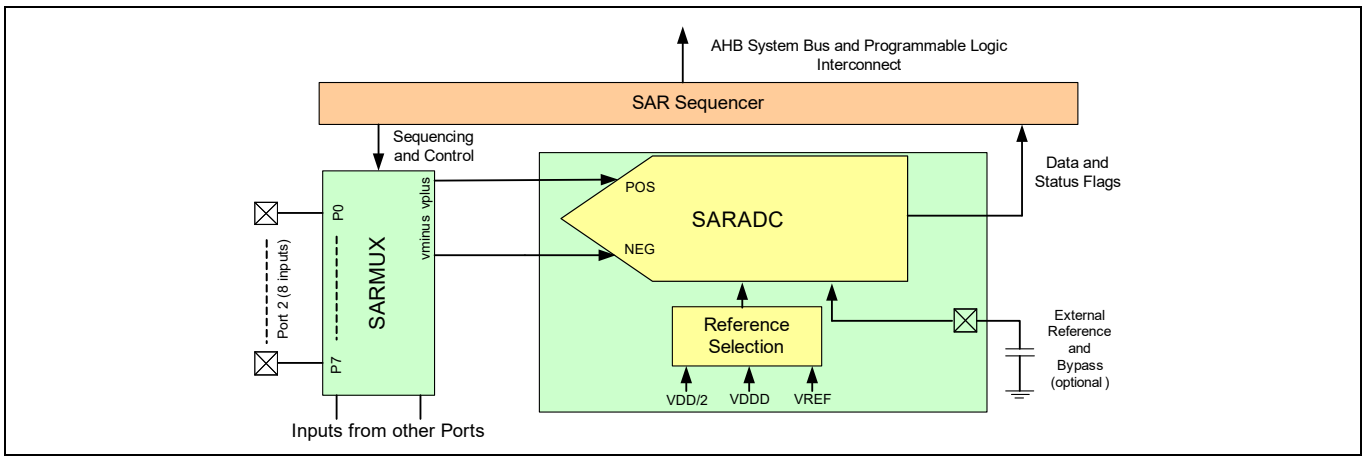


Figure 3 SAR ADC

1.3.2 Two opamps (Continuous-time block; CTB)

The PSoC™ 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

1.3.3 Low-power comparators (LPC)

The PSoC™ 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

1.3.4 Current DACs

The PSoC™ 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

1.3.5 Analog multiplexed buses

The PSoC™ 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

1.3.6 Programmable digital blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

1.4 Fixed function digital

1.4.1 Timer/counter/PWM (TCPWM) block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC™ 4100S.

1.4.2 Serial communication block (SCB)

The PSoC™ 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, UART or LIN Slave functionality.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC™ 4100S and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The PSoC™ 4100S is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

1.5 LIN slave mode

The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN Slave is compliant with LIN v1.3, v2.1/2.2, ISO 17987-6, and SAE J2602-2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length. PSoC™ Creator software supports up to two LIN slave interfaces in the PSoC™ 4 device, providing built-in application programming interfaces (APIs) based on the LIN specification standard.

1.6 GPIO

The PSoC™ 4100S has up to 38 GPIOs.

The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disabled state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC™ 4100S).

1.7 Special function peripherals

1.7.1 CAPSENSE™

CAPSENSE™ is supported in the PSoC™ 4100S through a CSD block that can be connected to any pins through an analog multiplex bus via analog switches. CAPSENSE™ function can thus be provided on any available pin or group of pins in a system under software control. A PSoC™ Creator component is provided for the CAPSENSE™ block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CAPSENSE™ block has two IDACs, which can be used for general purposes if CAPSENSE™ is not being used (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available).

The CAPSENSE™ block also provides a 10-bit Slope ADC function which can be used in conjunction with the CAPSENSE™ function.

The CAPSENSE™ block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

1.7.2 LCD segment drive

The PSoC™ 4100S has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

2 Pinouts

Table 1 provides the pin list for PSoC™ 4100S for the for the 40-pin QFN, and 28-pin SSOP packages. All port pins support GPIO.

Table 1 Pin list

40-pin QFN-Auto		28-pin SSOP-Auto	
Pin	**Name**	**Pin**	**Name**
22	P0.0	19	P0.0
23	P0.1	20	P0.1
24	P0.2	21	P0.2
25	P0.3	22	P0.3
26	P0.4		
27	P0.5		
28	P0.6	23	P0.6
29	P0.7	24	P0.7
30	XRES	25	XRES
31	VCCD	26	VCCD
32	VSSD	27	VSS
33	VDD	28	VDD
33	VDD		
34	VSSA		
35	P1.0	1	P1.0
36	P1.1	2	P1.1
37	P1.2	3	P1.2
38	P1.3	4	P1.3
39	P1.4	5	P1.4
40	P1.7/VREF	6	P1.7/VREF
1	P2.0		
2	P2.1		
3	P2.2		
4	P2.3		
5	P2.4	7	P2.4
6	P2.5	8	P2.5
7	P2.6	9	P2.6
8	P2.7	10	P2.7
9	VSSD		
10	P3.0	11	P3.0
11	P3.1	12	P3.1
12	P3.2	13	P3.2

Table 1 Pin list *(continued)*

40-pin QFN-Auto		28-pin SSOP-Auto	
Pin	**Name**	**Pin**	**Name**
13	P3.3	14	P3.3
14	P3.4		
15	P3.5		
16	P3.6		
17	P3.7		
18	P4.0	15	P4.0
19	P4.1	16	P4.1
20	P4.2	17	P4.2
21	P4.3	18	P4.3

The power pins description is as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ± 5%)

VDD: On some packages, VDDA and VDDD are shorted inside and brought out as a single power supply.

NC: No connection

2.1 Alternate pin functions

Each port pin has can be assigned to one of multiple functions. For example, it can be an analog I/O, a digital peripheral function, an LCD pin, or a CAPSENSE™ pin.

Table 2 provides the pin assignments.

Table 2 Alternate pin functions

Name	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2	Deep Sleep 3	Deelp Sleep 4
P0.0	lpcomp.in_p[0]			scb[2].uart_cts:0	tcpwm.tr_in[0]	lcd.com[0]	lcd.seg[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]			scb[2].uart_rts:0	tcpwm.tr_in[1]	lcd.com[1]	lcd.seg[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]					lcd.com[2]	lcd.seg[2]		scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]					lcd.com[3]	lcd.seg[3]		scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	lcd.com[4]	lcd.seg[4]	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	lcd.com[5]	lcd.seg[5]	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6	srss.adft_por_pad_hv		srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1	lcd.com[6]	lcd.seg[6]		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0		lcd.com[7]	lcd.seg[7]		scb[1].spi_select0:1
P1.0	pass.ctb0_pads[0]		tcpwm.line[2]:1	scb[0].uart_rx:1		lcd.com[8]	lcd.seg[8]	scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	pass.ctb0_pads[1]		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		lcd.com[9]	lcd.seg[9]	scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	pass.ctb0_pads[2] pass.ctb0_oa0_out_10x		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	lcd.com[10]	lcd.seg[10]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	pass.ctb0_pads[3] pass.ctb0_oa1_out_10x		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	lcd.com[11]	lcd.seg[11]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	pass.ctb0_pads[4]					lcd.com[12]	lcd.seg[12]		scb[0].spi_select1:1
P1.5	pass.ctb0_pads[5]					lcd.com[13]	lcd.seg[13]		scb[0].spi_select2:1
P1.6	pass.ctb0_pads[6]					lcd.com[14]	lcd.seg[14]		scb[0].spi_select3:1
P1.7	pass.ctb0_pads[7] pass.sar_ext_vref0 pass.sar_ext_vref1					lcd.com[15]	lcd.seg[15]		scb[2].spi_clk
P2.0	pass.sarmux_pads[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	lcd.com[16]	lcd.seg[16]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	pass.sarmux_pads[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	lcd.com[17]	lcd.seg[17]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	pass.sarmux_pads[2]	prgio[0].io[2]				lcd.com[18]	lcd.seg[18]		scb[1].spi_clk:2

Table 2 Alternate pin functions *(continued)*

Name	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2	Deep Sleep 3	Deelp Sleep 4
P2.3	pass.sarmux_pads[3]	prgio[0].io[3]				lcd.com[19]	lcd.seg[19]		scb[1].spi_select0:2
P2.4	pass.sarmux_pads[4]	prgio[0].io[4]	tcpwm.line[0]:1			lcd.com[20]	lcd.seg[20]		scb[1].spi_select1:1
P2.5	pass.sarmux_pads[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1			lcd.com[21]	lcd.seg[21]		scb[1].spi_select2:1
P2.6	pass.sarmux_pads[6]	prgio[0].io[6]	tcpwm.line[1]:1			lcd.com[22]	lcd.seg[22]		scb[1].spi_select3:1
P2.7	pass.sarmux_pads[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lcd.com[23]	lcd.seg[23]	lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		lcd.com[24]	lcd.seg[24]	scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		lcd.com[25]	lcd.seg[25]	scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		lcd.com[26]	lcd.seg[26]	cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		lcd.com[27]	lcd.seg[27]	cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]	lcd.com[28]	lcd.seg[28]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0			lcd.com[29]	lcd.seg[29]		scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0			lcd.com[30]	lcd.seg[30]		scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lcd.com[31]	lcd.seg[31]	lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		lcd.com[32]	lcd.seg[32]	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		lcd.com[33]	lcd.seg[33]	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpads csd.cmodpadd			scb[0].uart_cts:0		lcd.com[34]	lcd.seg[34]	lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tankpads csd.csh_tankpadd			scb[0].uart_rts:0		lcd.com[35]	lcd.seg[35]	lpcomp.comp[1]:0	scb[0].spi_select0:0

3 Power

Figure 4 illustrates the set of power supply pins as implemented for the PSoC™ 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input.

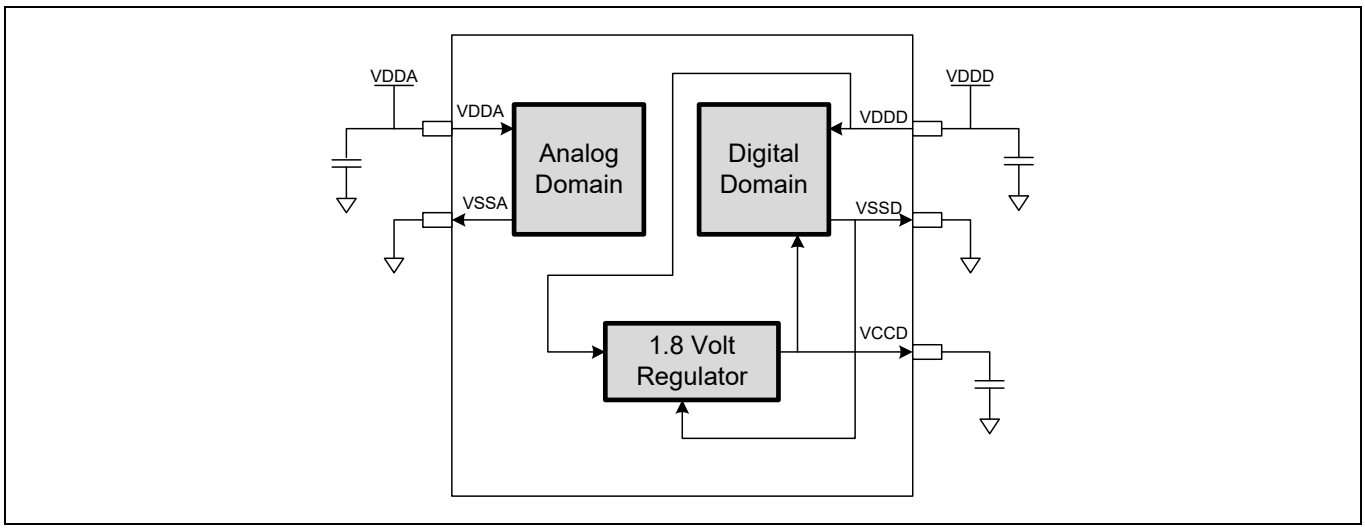


Figure 4 Power supply connections

There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is 1.8 V ± 5% (externally regulated; 1.71 V to 1.89 V, internal regulator bypassed).

3.1 Mode 1: 1.8 V to 5.5 V external supply

In this mode, the PSoC™ 4100S is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC™ 4100S supplies the internal logic and its output is connected to the VCCD pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

3.2 Mode 2: 1.8 V ± 5% external supply

In this mode, the PSoC™ 4100S is powered by an external power supply that must be within the range of 1.71 V to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

On some packages, V_{DDD} and V_{DDA} pins are shorted inside the package and brought out as a generic V_{DD} pin. In that case, only 0.1 µF and 1 µF decoupling capacitors are required on the V_{DD} pin. **Figure 5** illustrates an example of a bypass scheme.

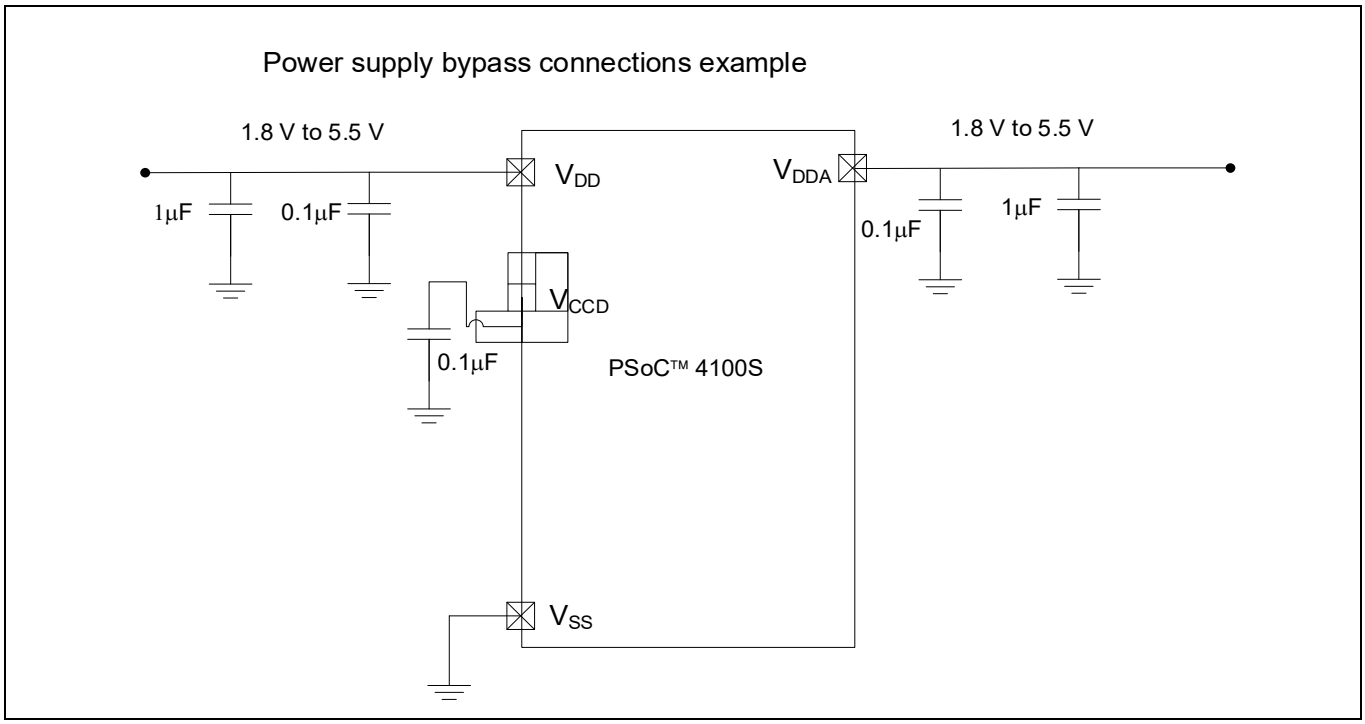


Figure 5 External supply range from 1.8 V to 5.5 V with internal regulator active

4 Development support

The PSoC™ 4100S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **www.infineon.com/psoc4** to find out more.

4.1 Documentation

A suite of documentation supports the PSoC™ 4100S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC™ Creator. The software user guide shows you how the PSoC™ Creator build process works in detail, how to use source control with PSoC™ Creator, and much more.

Component Datasheets: The flexibility of PSoC™ allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC™ application notes discuss a particular application of PSoC™ in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC™ device, including a complete description of all PSoC™ registers. The TRM is available in the Documentation section at **www.infineon.com/psoc4**.

4.2 Online

In addition to print documentation, the PSoC™ forums connect you with fellow PSoC™ users and experts in PSoC™ from around the world, 24 hours a day, 7 days a week.

4.3 Tools

With industry standard cores, programming, and debugging interfaces, the PSoC™ 4100S family is part of a development tool ecosystem. Visit us at **www.infineon.com/psoccreator** for the latest information on the revolutionary, easy to use PSoC™ Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

5 Electrical specifications

5.1 Absolute maximum ratings

Table 3 Absolute maximum ratings[2]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95		–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} + 0.5		–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Note
2. Usage above the absolute maximum conditions listed in **Table 3** may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

5.2 Device-level specifications

All specifications are valid for –40°C ≤ TA ≤ 85°C for Grade-A devices, –40°C ≤ T_A ≤ 105°C for Grade-S devices, and –40°C ≤ T_A ≤ 125°C for Grade-E devices. Specifications are valid for 1.71 V to 5.5 V, except where noted.[3]

5.2.1 DC specifications

Table 4 DC specifications

Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DDD} = V_{DDA})	1.71	–	1.89		Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		X5R ceramic or better
Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25°C.							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Max is at 125°C and 5.5 V.
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	4.75		Max is at 125°C and 5.5 V.
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	6.85		Max is at 125°C and 5.5 V.
Sleep Mode, V_{DDD} = 1.8 V to 5.5 V (Regulator on)							
SID22	I_{DD17}	I^2C wakeup WDT, and Comparators on	–	1.7	2.2	mA	6 MHz. Max is at 125°C and 5.5 V.
SID25	I_{DD20}	I^2C wakeup, WDT, and Comparators on.	–	2.2	2.5		12 MHz. Max is at 125°C and 5.5 V.
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	I_{DD23}	I^2C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHz. Max is at 125°C and 5.5 V.
SID28A	I_{DD23A}	I^2C wakeup, WDT, and Comparators on	–	1.0	1.2	mA	12 MHz. Max is at 125°C and 5.5 V.
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	150	µA	Max is at 3.6 V and 125°C.
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	150	µA	Max is at 5.5 V and 125°C.
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	160	µA	Max is at 1.89 V and 125°C.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Note

3. This device is not AEC-Q100 Grade 0 qualified, so Infineon does not guarantee performance at +150°C. The specifications for 125°C < T_A ≤ 150°C are best estimates of the performance.

5.2.2 AC specifications

Table 5 AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID49[4]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID50[4]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		–

Note
4. Guaranteed by characterization.

5.2.3 GPIO

Table 6 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}[5]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		CMOS Input
SID241	V_{IH}[5]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID243	V_{IH}[5]	LVTTL input, $V_{DDD} \geq$ 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq$ 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} – 0.6	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} – 0.5	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–40°C ≤ T_A ≤ 125°C
SID63A	R_{PULLUP}	Pull-up resistor	3	–	–		125°C < T_A ≤ 150°C
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–40°C ≤ T_A ≤ 125°C
SID64A	$R_{PULLDOWN}$	Pull-down resistor	3	–	–		125°C < T_A ≤ 150°C
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67[6]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq$ 2.7 V, –40°C ≤ T_A ≤ 125°C
SID67A[6]	V_{HYSTTL}	Input hysteresis LVTTL	7.5	–	–		125°C < T_A ≤ 150°C
SID68[6]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[6]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[6]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A[6]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Notes
5. V_{IH} must not exceed V_{DDD} + 0.2 V.
6. Guaranteed by characterization.

Table 7 GPIO AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF, –40°C ≤ T_A ≤ 125°C
SID70A	T_{RISEF}	Rise time in fast strong mode	–	–	25		3.3 V V_{DDD}, Cload = 25 pF, 125°C < T_A ≤ 150°C
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF, –40°C ≤ T_A ≤ 125°C
SID71A	T_{FALLF}	Fall time in fast strong mode	–	–	25		3.3 V V_{DDD}, Cload = 25 pF, 125°C < T_A ≤ 150°C
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF, –4°C ≤ T_A ≤ 125°C
SID72A	T_{RISES}	Rise time in slow strong mode	–	–	130	ns	3.3 V V_{DDD}, Cload = 25 pF, 125°C < T_A ≤ 150°C
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF, –40°C ≤ T_A ≤ 125°C
SID73A	T_{FALLS}	Fall time in slow strong mode	–	–	130	ns	3.3 V V_{DDD}, Cload = 25 pF, 125°C < T_A ≤ 150°C
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V≤ V_{DDD} ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48		90/10% V_{IO}

5.2.4 XRES

Table 8 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81[7]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5 V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 9 XRES AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83[7]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[7]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

Note
7. Guaranteed by characterization.

5.3 Analog peripherals

5.3.1 CTBm opamp

Table 10 CTBm opamp specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	I_{DD}	Opamp block current, External load					
SID269	I_{DD_HI}	power = hi	–	1100	1850	µA	–
SID270	I_{DD_MED}	power = med	–	550	950		$-40°C \le T_A \le 125°C$
SID270A	I_{DD_MED}	power = med	–	–	1075		$125°C < T_A \le 150°C$
SID271	I_{DD_LOW}	power = lo	–	150	350		$-40°C \le T_A \le 125°C$
SID271A	I_{DD_LOW}	power = lo	–	–	500		$125°C < T_A \le 15$ °C
	G_{BW}	Load = 20 pF, 0.1 mA, V_{DDA} = 2.7 V					
SID272	G_{BW_HI}	power = hi	6	–	–	MHz	Input and output are 0.2 V to V_{DDA} – 0.2 V, $-40°C \le T_A \le 125°C$
SID272A	G_{BW_HI}	power = hi	4.5	–	–		$125°C < T_A \le 150°C$
SID273	G_{BW_MED}	power = med	3	–	–		Input and output are 0.2 V to V_{DDA} – 0.2 V, $-40°C \le T_A \le 125°C$
SID273A	G_{BW_MED}	power = med	–	3	–		$125°C < T_A \le 150°C$
SID274	G_{BW_LO}	power = lo	–	1	–		Input and output are 0.2 V to V_{DDA} – 0.2 V
	I_{OUT_MAX}	V_{DDA} = 2.7 V, 500 mV from rail					
SID275	$I_{OUT\_MAX\_HI}$	power = hi	10	–	–	mA	Output is 0.5 V, V_{DDA} – 0.5 V
SID276	$I_{OUT\_MAX\_MID}$	power = mid	10	–	–		Output is 0.5 V, V_{DDA} – 0.5 V
SID277	$I_{OUT\_MAX\_LO}$	power = lo	–	5	–		Output is 0.5 V, V_{DDA} – 0.5 V
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail					
SID278	$I_{OUT\_MAX\_HI}$	power = hi	4	–	–	mA	Output is 0.5 V, V_{DDA} – 0.5 V
SID279	$I_{OUT\_MAX\_MID}$	power = mid	4	–	–		Output is 0.5 V, V_{DDA} – 0.5 V
SID280	$I_{OUT\_MAX\_LO}$	power = lo	–	2	–		Output is 0.5 V, V_{DDA} – 0.5 V

Table 10 CTBm opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	I_{DD_Int}	Opamp block current Internal Load					
SID269_I	$I_{DD\_HI\_Int}$	power = hi	–	1500	1700	µA	–
SID270_I	$I_{DD\_MED\_Int}$	power = med	–	700	900		–
SID271_I	$I_{DD\_LOW\_Int}$	power = lo	–	–	–		–
	G_{BW}	V_{DDA} = 2.7 V					
SID272_I	$G_{BW\_HI\_Int}$	power = hi	8	–	–	MHz	Output is 0.25 V to V_{DDA} – 0.25 V
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA} – 0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	power = hi, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	power = hi, Iload = 1 mA	0.2	–	V_{DDA} – 0.2		–
SID285	V_{OUT_3}	power = med, Iload = 1 mA	0.2	–	V_{DDA} – 0.2		–
SID286	V_{OUT_4}	power = lo, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2		–

Table 10 CTBm opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA} – 0.2 V, –40°C ≤ T_A ≤ 125°C
SID288C	V_{OS_TR}	Offset voltage, trimmed	–1.3	–	1.3		High mode, input 0 V to V_{DDA} – 0.2 V, 125°C < T_A ≤ 150°C
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA} – 0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA} – 0.2 V
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode, –40°C ≤ T_A ≤ 125°C
SID290C	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–15	–	15		High mode, 125°C < T_A ≤ 150°C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Medium mode, –40°C ≤ T_A ≤ 125°C
SID290D	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±15	–		Medium mode, 125°C < T_A ≤ 150°C
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode, –40°C ≤ T_A ≤ 125°C
SID290E	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±15	–		Low mode, 125°C < T_A ≤ 150°C
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA} – 0.2 V, Output is 0.2 V to V_{DDA} – 0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA} – 0.2 V

Table 10 CTBm opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
		Noise					
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	72	–	nV/rtHz	Input and output are at 0.2 V to V_{DDA} – 0.2 V
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	28	–		Input and output are at 0.2 V to V_{DDA} – 0.2 V
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	15	–		Input and output are at 0.2 V to V_{DDA} – 0.2 V
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	–
	COMP_MODE	Comparator mode; 50 mV drive, T_{rise} = T_{fall} (approx.)					
SID300	TPD1	Response time; power = hi	–	150	–	ns	Input is 0.2 V to V_{DDA} – 0.2 V
SID301	TPD2	Response time; power = med	–	500	–		Input is 0.2 V to V_{DDA} – 0.2 V
SID302	TPD3	Response time; power = lo	–	2500	–		Input is 0.2 V to V_{DDA} – 0.2 V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					

Table 10 CTBm opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1400	–	µA	25°C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	700	–		25°C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	200	–		25°C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–		25°C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–		25°C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–		25°C
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V
SID_DS_9	$G_{BW\_LOW\_M1}$	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V
SID_DS_12	$G_{BW\_Low\_M2}$	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to V_{DDA} – 0.2 V

Table 10 CTBm opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–		With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_15	$V_{OS\_LOW\_M2}$	Mode 1, Low current	–	5	–		With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–		With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–		With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–		With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		–
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		–
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		–

5.3.2 Comparator

Table 11 Comparator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	Normal mode, $-40°C \le T_A \le 125°C$
SID84A	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	±15	–		$125°C < T_A \le 150°C$, normal mode
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		Low power mode, $-40°C \le T_A \le 125°C$
SID85A	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	±4	–		$125°C < T_A \le 150°C$, low power mode
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		$-40°C \le T_A \le 125°C$
SID86A	V_{HYST}	Hysteresis when enabled	–	–	40		$125°C < T_A \le 150°C$
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		–
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15		$V_{DDD} \ge 2.2$ V at –40°C
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \ge 2.7$ V, $-40°C \le T_A \le 125°C$
SID88B	CMRR	Common mode rejection ratio	–	50	–		$V_{DDD} \ge 2.7$ V; $125°C < T_A \le 150°C$
SID88A	CMRR	Common mode rejection ratio	42	–	–		$V_{DDD} \le 2.7$ V, $-40°C \le T_A \le 125°C$
SID88C	CMRR	Common mode rejection ratio	–	42	–		$V_{DDD} \le 2.7$ V; $125°C < T_A \le 150°C$
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	–
SID248	I_{CMP2}	Block current, low power mode	–	–	100		–
SID259	I_{CMP3}	Block current in ultra low-power mode	–	–	6		$V_{DDD} \ge 2.2$ V at –40°C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	–

Table 12 Comparator AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID91	T_{RESP1}	Response time, normal mode, 50 mV overdrive	–	38	110	ns	–
SID258	T_{RESP2}	Response time, low power mode, 50 mV overdrive	–	70	200		–
SID92	T_{RESP3}	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	$V_{DDD} \ge 2.2$ V at –40°C

5.3.3 Temperature sensor

Table 13 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40°C to +85°C
SID93A	$T_{SENSACC}$	Temperature sensor accuracy	–15	–	+15	°C	–85°C to +150°C

5.3.4 SAR ADC

Table 14 SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	8		8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference, $-40°C \le T_A \le 125°C$
SID99A	A_OFFSET	Input offset voltage	–	–	2.7	mV	$125°C < T_A \le 150°C$
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	–

Table 15 SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V, $-40°C \le T_A \le 125°C$
SID107A	A_CMRR	Common mode rejection ratio	–	66	–	dB	$125°C < T_A \le 150°C$
SID108	A_SAMP	Sample rate	–	–	1	Msps	$-40°C \le T_A \le 125°C$
SID108A	A_SAMP	Sample rate	–	–	0.375	Msps	$125°C < T_A \le 150°C$
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz, $-40°C \le T_A \le 125°C$
SID109A	A_SNR	Signal-to-noise and distortion ratio (SINAD)	–	65	–	dB	$125°C \le T_A \le 150°C$
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	–
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}, $-40°C \le T_A \le 125°C$
SID111A	A_INL	Integral non linearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V to V_{DD}, $-40°C \le T_A \le 125°C$
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}, $-40°C \le T_A \le 125°C$
SID111C	A_INL	Integral non linearity. V_{DD} = 4.5 V to 5.5 V, 375 ksps	–4.5	–	3.3	LSB	V_{REF} = 1 V to V_{DD}, $125°C < T_A \le 150°C$
SID111D	A_INL	Integral non linearity. V_{DD} = 3 V to 4.5 V, 300 ksps	–4.5	–	3.3	LSB	V_{REF} = 1 V to V_{DD}, $125°C < T_A \le 150°C$
SID111E	A_INL	Integral non linearity. V_{DD} = 1.71 V to 3 V, 150 ksps	–4.5	–	3.4	LSB	V_{REF} = 1 V to V_{DD}, $125°C < T_A \le 150°C$
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}, $-40°C \le T_A \le 125°C$
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 V to V_{DD}, $-40°C \le T_A \le 125°C$
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}, $-40°C \le T_A \le 125°C$
SID112C	A_DNL	Differential non linearity. V_{DD} = 4.5 V to 5.5 V, 375 ksps	–1	–	3.2	LSB	V_{REF} = 1 V to V_{DD}, $125°C < T_A \le 150°C$
SID112D	A_DNL	Differential non linearity. V_{DD} = 3 V to 4.5 V, 300 ksps	–1	–	3.2	LSB	V_{REF} = 1 V to V_{DD}, $125°C < T_A \le 150°C$
SID112E	A_DNL	Differential non linearity. V_{DD} = 1.71 V to 3 V, 150 ksps	–1	–	3.3	LSB	V_{REF} = 1 V to V_{DD}, $125°C < T_A \le 150°C$
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
SID113A	A_THD	Total harmonic distortion	–	–65	–	dB	Fin = 10 kHz, $125°C < T_A \le 150°C$
SID261	$FSAR_{INTREF}$	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution

5.3.5 CSD and IDAC

Table 16 CSD and IDAC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SYS.PER#3	V_{DD_RIPPLE}	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25°C T_A, Sensitivity = 0.1 pF
SYS.PER#16	$V_{DD\_RIPPLE\_1.8}$	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75 V (with ripple), 25°C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	I_{CSD}	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} – 0.6	V	V_{DDA} – 0.06 or 4.4, whichever is lower
SID.CSD#15A	V_{REF_EXT}	External Voltage reference for CSD and Comparator	0.6		V_{DDA} – 0.6		V_{DDA} – 0.06 or 4.4, whichever is lower
SID.CSD#16	$IDAC1_{IDD}$	IDAC1 (7 bits) block current	–	–	1750	µA	–
SID.CSD#17	$IDAC2_{IDD}$	IDAC2 (7 bits) block current	–	–	1750		–
SID308	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	1.8 V ± 5% or 1.8 V to 5.5 V
SID308A	$V_{COMPIDAC}$	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6		V_{DDA} – 0.06 or 4.4, whichever is lower
SID309	$IDAC1_{DNL}$	DNL	–1	–	1	LSB	
SID310	$IDAC1_{INL}$	INL	–3	–	3		INL is ±5 LSB for V_{DDA} < 2 V
SID311	$IDAC2_{DNL}$	DNL	–1	–	1		
SID312	$IDAC2_{INL}$	INL	–3	–	3		INL is ±5 LSB for V_{DDA} < 2 V, –40°C ≤ T_A ≤ 125°C
SID312A	$IDAC2_{INL}$	INL	–	–	7		125°C < T_A ≤ 150°C
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	–	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V

Table 16 CSD and IDAC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID314	$IDAC1_{CRT1}$	Output current of IDAC1 (7 bits) in low range	4.2	–	5.2	µA	LSB = 37.5-nA typ
SID314A	$IDAC1_{CRT2}$	Output current of IDAC1 (7 bits) in medium range	34	–	41		LSB = 300-nA typ
SID314B	$IDAC1_{CRT3}$	Output current of IDAC1 (7 bits) in high range	275	–	330		LSB = 2.4-µA typ
SID314C	$IDAC1_{CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5		LSB = 37.5-nA typ. 2X output stage
SID314D	$IDAC1_{CRT22}$	Output current of IDAC1 (7 bits) in medium range, 2X mode	69	–	82		LSB = 300-nA typ. 2X output stage
SID314E	$IDAC1_{CRT32}$	Output current of IDAC1 (7 bits) in high range, 2X mode	540	–	660		LSB = 2.4-µA typ. 2X output stage
SID315	$IDAC2_{CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2	–	5.2		LSB = 37.5-nA typ.
SID315A	$IDAC2_{CRT2}$	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID315B	$IDAC2_{CRT3}$	Output current of IDAC2 (7 bits) in high range	275	–	330		LSB = 2.4-µA typ.
SID315C	$IDAC2_{CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5		LSB = 37.5-nA typ. 2X output stage
SID315D	$IDAC2_{CRT22}$	Output current of IDAC2 (7 bits) in medium range, 2X mode	69	–	82		LSB = 300-nA typ. 2X output stage
SID315E	$IDAC2_{CRT32}$	Output current of IDAC2 (7 bits) in high range, 2X mode	540	–	660		LSB = 2.4-µA typ. 2X output stage
SID315F	$IDAC3_{CRT13}$	Output current of IDAC in 8-bit mode in low range	8	–	10.5		LSB = 37.5-nA typ
SID315G	$IDAC3_{CRT23}$	Output current of IDAC in 8-bit mode in medium range	69	–	82		LSB = 300-nA typ
SID315H	$IDAC3_{CRT33}$	Output current of IDAC in 8-bit mode in high range	540	–	660		LSB = 2.4-µA typ
SID320	$IDAC_{OFFSET}$	All zeros input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode

Table 16 CSD and IDAC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±10	%	–40°C ≤ T_A ≤ 125°C
SID321A	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±11		125°C < T_A ≤ 150°C
SID322	$IDAC_{MISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	$IDAC_{MISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	4.6		LSB = 300-nA typ.
SID322B	$IDAC_{MISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	2.3		LSB = 2.4 µA typ, –40°C ≤ T_A ≤ 125°C
SID322C	$IDAC_{MISMATCH4}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.3		125°C < T_A ≤ 150°C
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10		Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor	–	2.2	–	nF	5-V rating, X7R or NP0 cap

5.3.6 10-bit CAPSENSE™ ADC

Table 17 10-bit CAPSENSE™ ADC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond.
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	–
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	–
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	–
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	–
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	–
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N + 2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N + 2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	61	–	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V_{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	kHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	–

5.4 Digital peripherals

5.4.1 Timer counter pulse-width modulator (TCPWM)

Table 18 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[8]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

Note
8. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

5.4.2 I²C

Table 19 Fixed I²C DC specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4		–

Table 20 Fixed I²C AC specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Msps	–

Note
9. Guaranteed by characterization.

5.4.3 SPI

Table 21 SPI DC specifications[10]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 22 SPI AC specifications[10]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + (3 × Tcpu)		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK valid edge	–	–	100	ns	–

Note
10.Guaranteed by characterization.

5.4.4 UART

Table 23 UART DC specifications[11]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 24 UART AC specifications[11]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

5.4.5 LCD

Table 25 LCD Direct Drive DC specifications[11]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz. 25°C
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	–	2	–		32 × 4 segments. 50 Hz. 25°C

Table 26 LCD Direct Drive AC specifications[11]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note
11.Guaranteed by characterization.

5.5 Memory

5.5.1 Flash

Table 27 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 28 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$[12]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[12]	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$[12]	Row program time after erase	–	–	4		–
SID178	$T_{BULKERASE}$[12]	Bulk erase time (64 KB)	–	–	35		–
SID180[13]	$T_{DEVPROG}$[12]	Total device program time	–	–	7	seconds	–
SID181[13]	F_{END}	Flash endurance	100K	–	–	cycles	–
SID182[13, 14]	F_{RET}	Flash retention. $T_A \leq 55°C$, 100K P/E cycles	20	–	–	years	–
SID182A[13, 14]	F_{RET}	Flash retention. $T_A \leq 85°C$, 10K P/E cycles	10	–	–		–
SID256	TWS48	Number of wait states at 48 MHz	2	–	–	–	CPU execution from Flash
SID257	TWS24	Number of wait states at 24 MHz	1	–	–	–	CPU execution from Flash

Notes

12. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
13. Guaranteed by characterization.
14. Infineon provides a retention calculator to calculate the retention lifetime based on the customers' individual temperature profiles for operation over the –40°C to +150°C ambient temperature range. For more information, visit the **Infineon community page**.

5.6 System resources

5.6.1 Power-on reset (POR)

Table 29 Power-on reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#6	SR_POWER	Power supply slew rate	1[15]	–	67	V/ms	On power-up & power-down
SID185[16]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[16]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

Table 30 Brown-out detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190[16]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[16]	$V_{FALLDPSLP}$	BOD trip voltage in deep sleep mode	1.11	–	1.5		–

5.6.2 SWD interface

Table 31 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID213	F_SWDCLK1	$3.3\ V \le V_{DD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71\ V \le V_{DD} \le 3.3\ V$	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[16]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID216[16]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–		–
SID217[16]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T		–
SID217A[16]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

Notes
15. If minimum ramp rate cannot be met, XRES should be asserted during voltage ramp ($1.5\ V > V_{DDD} > 1.0\ V$ for ramp-down or until voltage is stable for ramp-up). Note that a glitch on the I2C bus could occur during voltage ramp in this case.
16. Guaranteed by characterization.

5.6.3 Internal main oscillator

Table 32 IMO DC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 33 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	$-40°C \le T_A \le 125°C$
SID223A	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±4	%	$125°C \le T_A \le 150°C$
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

5.6.4 Internal low-speed oscillator

Table 34 ILO DC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231[17]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 35 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234[17]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[17]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Note
17.Guaranteed by characterization.

5.6.5 Watch crystal oscillator

Table 36 Watch crystal oscillator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID398	F_{WCO}	Crystal frequency	–	32.768	–	kHz	–
SID399	F_{TOL}	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive Level	–	–	1	µW	–
SID402	T_{START}	Startup time	–	–	500	ms	–
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	–
SID404	C_0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	I_{WCO1}	Operating current (high power mode)	–	–	8	µA	–
SID406	I_{WCO2}	Operating current (low power mode)	–	–	1	µA	–

5.6.6 External clock

Table 37 External clock specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID305[18]	$ExtClk_{Freq}$	External clock input frequency	0	–	48	MHz	–
SID306[18]	$ExtClk_{Duty}$	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	–

5.6.7 Block

Table 38 Block specs

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID262[18]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

5.6.8 PRGIO pass-through time

Table 39 PRGIO pass-through time (Delay in bypass mode)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID252	PRG_BYPASS	Max. delay added by PRGIO in bypass mode	–	–	1.6	ns	–

Note
18.Guaranteed by characterization.

6 Ordering information

Table 40 lists the marketing part numbers for the PSoC™ 4100S family.

Table 40 Ordering information

MPN	Features													Packages		Operating temperature		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart IOs	GPIO	28-SSOP	40-QFN	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4124PVA-S412	24	16	4	–	2	X	X	–	2	5	2	16	24	X	–	X	–	–
CY8C4124LQA-S413	24	16	4	–	2	X	X	–	2	5	2	16	34	–	X	X	–	–
CY8C4124PVA-S422	24	16	4	–	2	–	X	806 Ksps	2	5	2	16	24	X	–	X	–	–
CY8C4124LQA-S423	24	16	4	–	2	–	X	806 Ksps	2	5	2	16	34	–	X	X	–	–
CY8C4124PVA-S432	24	16	4	–	2	X	X	806 Ksps	2	5	2	16	24	X	–	X	–	–
CY8C4124LQA-S433	24	16	4	–	2	X	X	806 Ksps	2	5	2	16	34	–	X	X	–	–
CY8C4125PVA-S412	24	32	4	–	2	X	X	–	2	5	2	16	24	X	–	X	–	–
CY8C4125LQA-S413	24	32	4	–	2	X	X	–	2	5	2	16	34	–	X	X	–	–
CY8C4125PVA-S422	24	32	4	–	2	–	X	806 Ksps	2	5	2	16	24	X	–	X	–	–
CY8C4125LQA-S423	24	32	4	–	2	–	X	806 Ksps	2	5	2	16	34	–	X	X	–	–
CY8C4125PVA-S432	24	32	4	–	2	X	X	806 Ksps	2	5	2	16	24	X	–	X	–	–
CY8C4125LQA-S433	24	32	4	–	2	X	X	806 Ksps	2	5	2	16	34	–	X	X	–	–
CY8C4146PVA-S422	48	64	8	–	2	–	X	1000 Ksps	2	5	2	16	24	X	–	X	–	–
CY8C4146LQA-S423	48	64	8	–	2	–	X	1000 Ksps	2	5	3	16	34	–	X	X	–	–
CY8C4146PVA-S432	48	64	8	–	2	X	X	1000 Ksps	2	5	3	16	24	X	–	X	–	–
CY8C4146LQA-S433	48	64	8	–	2	X	X	1000 Ksps	2	5	3	16	34	–	X	X	–	–
CY8C4124PVS-S412	24	16	4	–	2	X	X	–	2	5	2	16	24	X	–	–	X	–
CY8C4124LQS-S413	24	16	4	–	2	X	X	–	2	5	2	16	34	–	X	–	X	–
CY8C4124PVS-S422	24	16	4	–	2	–	X	806 Ksps	2	5	2	16	24	X	–	–	X	–

Table 40 Ordering information *(continued)*

MPN	Features													Packages		Operating temperature		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart IOs	GPIO	28-SSOP	40-QFN	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4124LQS-S423	24	16	4	–	2	–	X	806 Ksps	2	5	2	16	34	–	X	–	X	–
CY8C4124PVS-S432	24	16	4	–	2	X	X	806 Ksps	2	5	2	16	24	X	–	–	X	–
CY8C4124LQS-S433	24	16	4	–	2	X	X	806 Ksps	2	5	2	16	34	–	X	–	X	–
CY8C4125PVS-S412	24	32	4	–	2	X	X	–	2	5	2	16	24	X	–	–	X	–
CY8C4125LQS-S413	24	32	4	–	2	X	X	–	2	5	2	16	34	–	X	–	X	–
CY8C4125PVS-S422	24	32	4	–	2	–	X	806 Ksps	2	5	2	16	24	X	–	–	X	–
CY8C4125LQS-S423	24	32	4	–	2	–	X	806 Ksps	2	5	2	16	34	–	X	–	X	–
CY8C4125PVS-S432	24	32	4	–	2	X	X	806 Ksps	2	5	2	16	24	X	–	–	X	–
CY8C4125LQS-S433	24	32	4	–	2	X	X	806 Ksps	2	5	2	16	34	–	X	–	X	–
CY8C4146PVS-S422	48	64	8	–	2	–	X	1000 Ksps	2	5	2	16	24	X	–	–	X	–
CY8C4146LQS-S423	48	64	8	–	2	–	X	1000 Ksps	2	5	3	16	34	–	X	–	X	–
CY8C4146PVS-S432	48	64	8	–	2	X	X	1000 Ksps	2	5	3	16	24	X	–	–	X	–
CY8C4146LQS-S433	48	64	8	–	2	X	X	1000 Ksps	2	5	3	16	34	–	X	–	X	–
CY8C4124PVE-S412	24	16	4	–	2	X	X	–	2	5	2	16	24	X	–	–	–	X
CY8C4124LQE-S413	24	16	4	–	2	X	X	–	2	5	2	16	34	–	X	–	–	X
CY8C4124PVE-S422	24	16	4	–	2	–	X	806 Ksps	2	5	2	16	24	X	–	–	–	X
CY8C4124LQE-S423	24	16	4	–	2	–	X	806 Ksps	2	5	2	16	34	–	X	–	–	X
CY8C4124PVE-S432	24	16	4	–	2	X	X	806 Ksps	2	5	2	16	24	X	–	–	–	X
CY8C4124LQE-S433	24	16	4	–	2	X	X	806 Ksps	2	5	2	16	34	–	X	–	–	X
CY8C4125PVE-S412	24	32	4	–	2	X	X	–	2	5	2	16	24	X	–	–	–	X
CY8C4125LQE-S413	24	32	4	–	2	X	X	–	2	5	2	16	34	–	X	–	–	X
CY8C4125PVE-S422	24	32	4	–	2	–	X	806 Ksps	2	5	2	16	24	X	–	–	–	X
CY8C4125LQE-S423	24	32	4	–	2	–	X	806 Ksps	2	5	2	16	34	–	X	–	–	X

Table 40 Ordering information *(continued)*

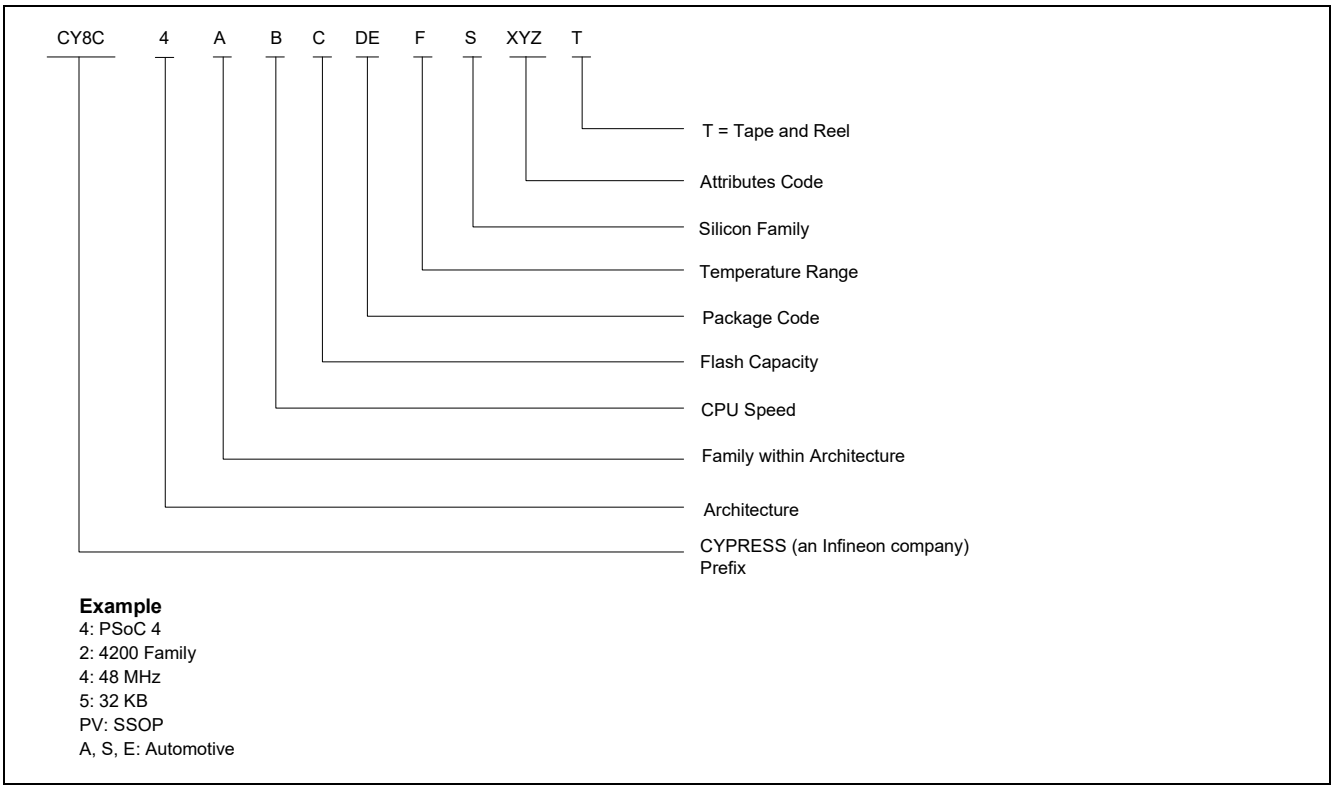
MPN	Features													Packages		Operating temperature		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart IOs	GPIO	28-SSOP	40-QFN	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4125PVE-S432	24	32	4	–	2	X	X	806 Ksps	2	5	2	16	24	X	–	–	–	X
CY8C4125LQE-S433	24	32	4	–	2	X	X	806 Ksps	2	5	2	16	34	–	X	–	–	X
CY8C4146PVE-S422	48	64	8	–	2	–	X	1000 Ksps	2	5	2	16	24	X	–	–	–	X
CY8C4146LQE-S423	48	64	8	–	2	–	X	1000 Ksps	2	5	3	16	34	–	X	–	–	X
CY8C4146PVE-S432	48	64	8	–	2	X	X	1000 Ksps	2	5	3	16	24	X	–	–	–	X
CY8C4146LQE-S433	48	64	8	–	2	X	X	1000 Ksps	2	5	3	16	34	–	X	–	–	X

The nomenclature used in the preceding table is based on the following part numbering convention:

Table 41 Nomenclature

Field	Description	Values	Meaning
CY8C	Cypress (an Infineon company) Prefix		
4	Architecture	4	PSoC™ 4
A	Family	0	4000 family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
DE	Package code	LQ	QFN
		PV	SSOP
F	Temperature range	A	Automotive (AEC-Q100: –40°C to +85°C)
		S	Automotive (AEC-Q100: –40°C to +105°C)
		E	Automotive (AEC-Q100: –40°C to +125°C)
S	Silicon family	S	PSoC™ 4A-S1, PSoC™ 4A-S2
		M	PSoC™ 4A-M
XYZ	Attributes code	000–999	Code of feature set in the specific family

The following is an example of a part number:



7 Packaging information

The PSoC™ 4100S will be offered in 40-pin QFN, and 28-pin SSOP packages.
Table 42 provides the package dimensions and Infineon drawing numbers.

Table 42 Package list

Spec ID	Package	Description	Package drawing
BID27	40-pin QFN	6 × 6 × 0.6 mm LD40A 4.6 × 4.6 mm E-Pad (Sawn) (Wettable flank package)	002-16818
BID28	28-pin SSOP	10.2 × 5.3 × 2.0 mm SP28	51-85079

Table 43 Package thermal characteristics

Parameter	Description	Package	Conditions	Min	Typ	Max	Unit
T_A	Operating Ambient temperature	–	For A-grade devices	–40	25	85	°C
		–	For S-grade devices	–40	25	105	°C
		–	For E-grade devices	–40	25	125	°C
T_J	Operating Junction temperature	–	For A-grade devices	–40	–	100	°C
		–	For S-grade devices	–40	–	120	°C
		–	For E-grade devices	–40	–	140	°C
T_{JA}	Package θ_{JA}	40-pin QFN	–	–	25	–	°C/W
T_{JC}	Package θ_{JC}	40-pin QFN	–	–	3	–	°C/W
T_{JA}	Package θ_{JA}	28-pin SSOP	–	–	66.58	–	°C/W
T_{JC}	Package θ_{JC}	28-pin SSOP	–	–	46.28	–	°C/W

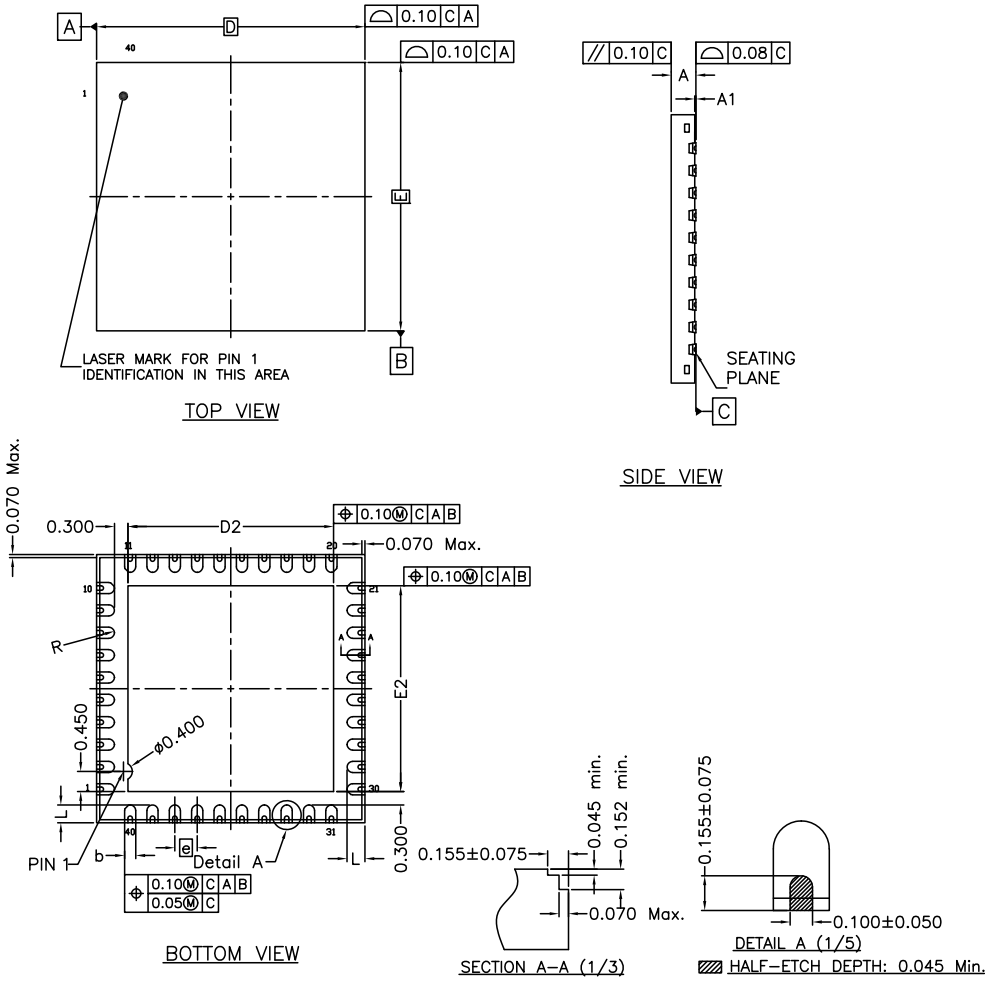
Table 44 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All	260°C	30 seconds

Table 45 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

7.1 Package diagrams



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A_1	0.00	—	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D_2	4.50	4.60	4.70
E		6.00 BSC	
E_2	4.50	4.60	4.70
L	0.30	0.40	0.50
e		0.50 BSC	
R	0.09	—	—
N		40	

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. PACKAGE WARPAGE MAX 0.08 mm.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. APPLIED ONLY TO TERMINALS.
8. JEDEC SPECIFICATION NO. REF: N.A.

002-16818 Rev. *B

Figure 6 40-pin QFN ((6.0 × 6.0 × 0.6 mm) LD40A 4.6 × 4.6 mm E-Pad (Sawn) (Wettable flank package)) package outline (PG-VQFN-40), 002-16818

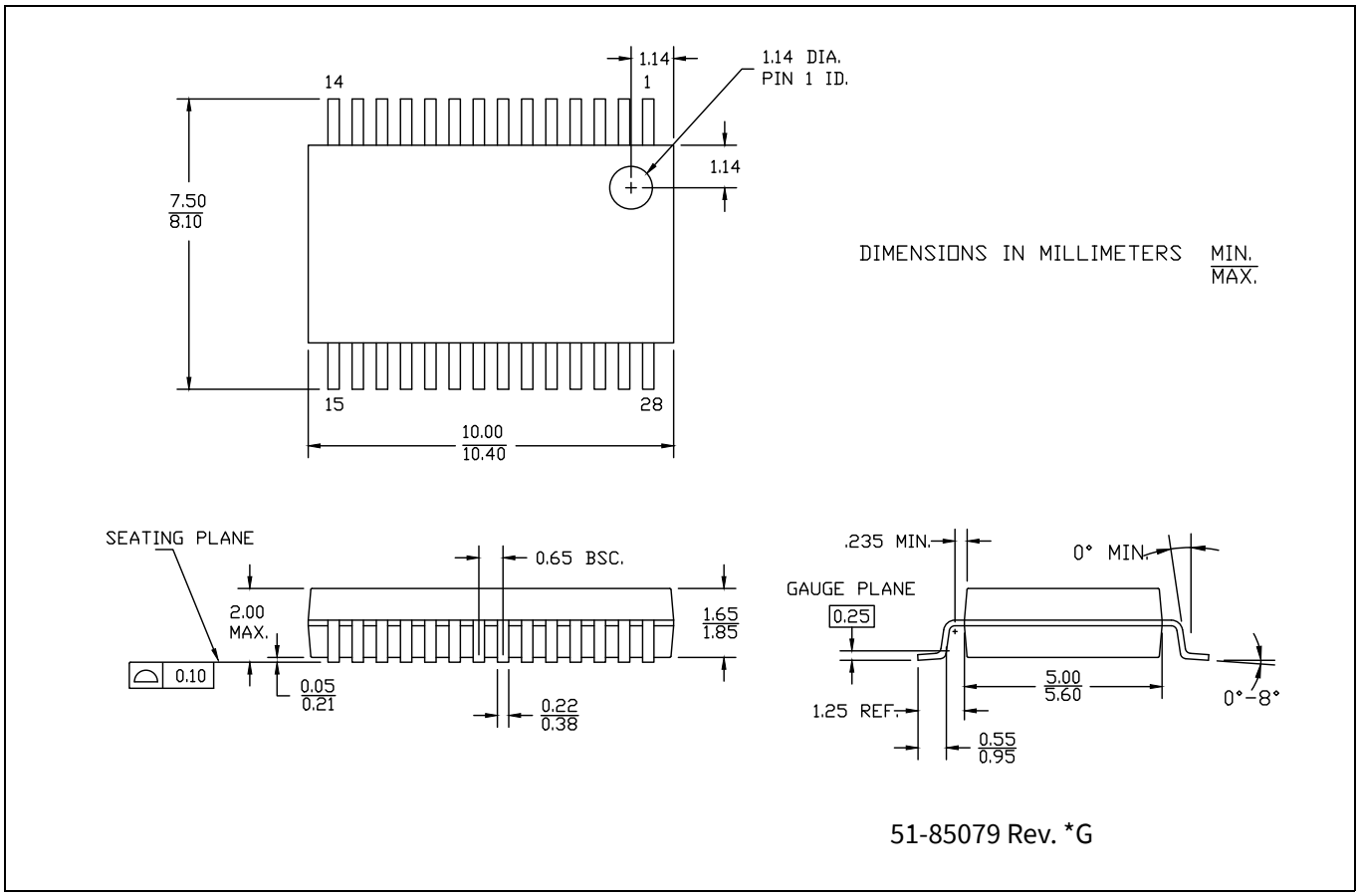


Figure 7 28-pin SSOP (10.2 × 5.3 × 2.0 mm) SP28 package outline (PG-SSOP-28), 51-85079

8 Acronyms

Table 46 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FPB	flash patch and breakpoint
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit

Table 46 Acronyms used in this document *(continued)*

Acronym	Description
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC™	Programmable System-on-Chip
PSRR	power supply rejection ratio

Table 46 Acronyms used in this document *(continued)*

Acronym	Description
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Receiver-Transmitter, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9 Document conventions

9.1 Units of measure

Table 47 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document revision	Date	Description of changes
*F	2019-04-24	Post to external web.
*G	2020-05-04	Updated **Ordering information**: No change in part numbers. Updated “part number convention”. Updated to new template.
*H	2020-09-29	Updated **Electrical specifications**: Updated **Device-level specifications**: Updated description. Updated **System resources**: Updated **Power-on reset (POR)**: Updated **Table 29**. Refer to Product Information Notice #6965423.
*I	2021-12-01	Updated **Features**: Updated description. Updated **Functional overview**: Updated **GPIO**: Updated description. Updated **Pinouts**: Updated **Table 1**. Updated **Electrical specifications**: Updated **Device-level specifications**: Updated **DC specifications**: Updated **Table 4**. Updated **System resources**: Updated **Power-on reset (POR)**: Added Note 15 and referred the same note in minimum value of SR_POWER parameter in **Table 29**. Updated **Ordering information**: Updated part numbers. Updated **Packaging information**: Updated **Table 42**. Updated **Table 43**. Updated **Package diagrams**: Added spec 002-18982 Rev. *A. Added spec 002-23807 Rev. *C. Added spec 002-34268 Rev. **. Migrated to Infineon template.
*J	2023-02-21	Replaced all references of Cypress with Infineon across the document. Updated **Ordering information**: Updated part numbers. Updated **Packaging information**: Updated **Package diagrams**: Removed spec 002-23807 Rev. *C. Removed spec 002-34268 Rev. **. Completing Sunset Review.

Revision history

Document revision	Date	Description of changes
*K	2023-10-10	Removed 24-pin QFN, 48-pin QFN packages related information in all instances across the document. Updated **Pinouts**: Updated **Table 1**. Updated **Ordering information**: Updated part numbers. Removed Note “Alternate fab available.” and its references in **Table 40**. Updated **Packaging information**: Updated **Table 42**. Updated **Package diagrams**: Removed spec 002-18982 Rev. *A. Updated to new template.

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