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CY7C1354D

9-Mbit (256K × 36) Pipelined SRAM with NoBL™ Architecture

Features

- Pin-compatible and functionally equivalent to ZBT

- Supports 200 MHz bus operations with zero wait states
  - Available speed grade is 200 MHz

- Internally self-timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$

- Fully registered (inputs and outputs) for pipelined operation

- Byte write capability

- Single 3.3 V power supply (V_{DD})

- 3.3 V or 2.5 V I/O power supply (V_{DDQ})

- Fast clock-to-output times
  - 3.2 ns (for 200 MHz device)

- Clock enable ($\overline{CEN}$) pin to suspend operation

- Synchronous self-timed writes

- Available in non Pb-free 165-ball FBGA package

- IEEE 1149.1 JTAG-compatible boundary scan

- Burst capability – linear or interleaved burst order

- "ZZ" sleep mode option and stop clock option

Functional Description

The CY7C1354D are 3.3 V, 256K × 36 synchronous pipelined burst SRAM with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1354D are equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature greatly improves the throughput of data in systems that require frequent write/read transitions. The CY7C1354D are pin compatible and functionally equivalent to ZBT devices.
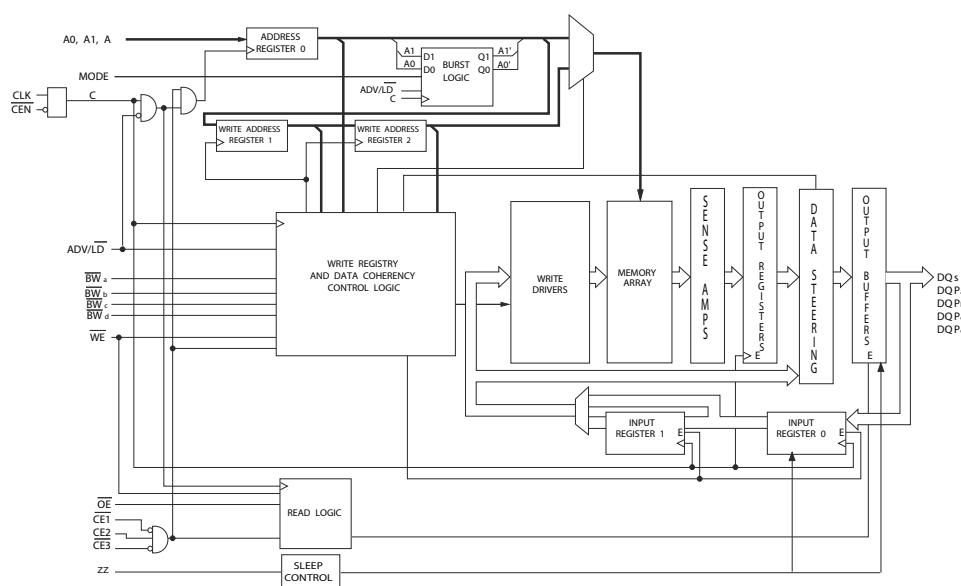
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the byte write selects (BW_a–BW_d for CY7C1354D) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. To avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

For a complete list of related documentation, click here.

Logic Block Diagram – CY7C1354D

Contents

Selection Guide

Description	200 MHz	Unit
Maximum access time	3.2	ns
Maximum operating current	220	mA
Maximum CMOS standby current	40	mA

Pin Configurations

Figure 1. 165-ball FBGA (13 × 15 × 1.4 mm) pinout

CY7C1354D (256K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_d$	$\overline{BW}_a$	CLK	$\overline{WE}$	$\overline{OE}$	NC/18M	A	NC
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Pin Name	I/O Type	Pin Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK.
$\overline{BW_a}$, $\overline{BW_b}$, $\overline{BW_c}$, $\overline{BW_d}$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW_a}$ controls DQ_a and DQP_a, $\overline{BW_b}$ controls DQ_b and DQP_b, $\overline{BW_c}$ controls DQ_c and DQP_c, $\overline{BW_d}$ controls DQ_d and DQP_d.
$\overline{WE}$	Input-synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-synchronous	**Advance/load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW to load a new address.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE_1}$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device.
$\overline{CE_3}$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-asynchronous	**Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a Write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_S	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-synchronous	**Bidirectional data parity I/O lines**. Functionally, these signals are identical to $DQ_{[a:d]}$. During write sequences, DQP_a is controlled by BW_a, DQP_b is controlled by BW_b, DQP_c is controlled by BW_c, and DQP_d is controlled by BW_d.
MODE	Input strap pin	**Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
TDO	JTAG serial output synchronous	**Serial data out to the JTAG circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG serial input synchronous	**Serial data in to the JTAG circuit**. Sampled on the rising edge of TCK.
TMS	Test mode select synchronous	**This pin controls the test access port state machine**. Sampled on the rising edge of TCK.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
TCK	JTAG-clock	**Clock input to the JTAG circuitry**.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
NC	–	**No connects**. This pin is not connected to the die.
NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**These pins are not connected**. They will be used for expansion to the 18M, 36M, 72M, 144M, 288M, 576M, and 1G densities.
ZZ	Input-asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.

Functional Overview

The CY7C1354D are synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.2 ns (200 MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If clock enable (CEN) is active LOW and ADV/LD is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable (WE). $BW_{[d:a]}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry. Three synchronous chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable (OE) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD should be driven LOW once the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (3) the write enable input signal WE is deasserted HIGH, and (4) ADV/LD is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and enables the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output

register and to the data bus within 3.2 ns (200 MHz device) provided OE is active LOW. After the first clock of the read access the output buffers are controlled by OE and the internal control logic. OE must be driven LOW for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tristates following the next clock rise.

Burst Read Accesses

The CY7C1354D has an on-chip burst counter that enables the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW to load a new address into the SRAM, as described in Single Read Accesses. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wrap around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enables inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (3) the write signal WE is asserted LOW. The address presented to A_0–A_{16} is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the OE input signal. This enables the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354D). In addition, the address for the subsequent access (read/write/deselect) is latched into

the address register if the appropriate control signals are asserted.

On the next clock rise the data presented to DQ and DQP (DQ$_{a,b,c,d}$/DQP$_{a,b,c,d}$ for CY7C1354D or a subset for byte write operations, see the table Partial Truth Table for Read/Write on page 8 for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1354D) signals. The CY7C1354D provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input ($\overline{WE}$) with the selected byte write select ($\overline{BW}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism is provided to simplify the write operations. Byte write capability is included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1354D is common I/O devices, data should not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP (DQ$_{a,b,c,d}$/DQP$_{a,b,c,d}$ for CY7C1354D) inputs. Doing so will tristate the output drivers. As a safety precaution, DQ and DQP (DQ$_{a,b,c,d}$/DQP$_{a,b,c,d}$ for CY7C1354D) are automatically tristated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1354D has an on-chip burst counter that enables the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in Single Write Accesses on page 5. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, CE$_2$, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1354D) inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation 'sleep' mode. Two clock cycles are required to enter into or exit from this 'sleep' mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}_1$, CE$_2$, and $\overline{CE}_3$, must remain inactive for the duration of t$_{ZZREC}$ after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V$_{DD}$)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I$_{DDZZ}$	Sleep mode standby current	ZZ $\geq$ V$_{DD}$ – 0.2 V	–	50	mA
t$_{ZZS}$	Device operation to ZZ	ZZ $\geq$ V$_{DD}$ – 0.2 V	–	2t$_{CYC}$	ns
t$_{ZZREC}$	ZZ recovery time	ZZ $\leq$ 0.2 V	2t$_{CYC}$	–	ns
t$_{ZZI}$	ZZ active to sleep current	This parameter is sampled	–	2t$_{CYC}$	ns
t$_{RZZI}$	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for CY7C1354D follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}$	ZZ	$\overline{ADV/LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	L	L	X	X	X	L	L–H	Tri-state
Continue deselect cycle	None	X	L	H	X	X	X	L	L–H	Tri-state
Read cycle (begin burst)	External	L	L	L	H	X	L	L	L–H	Data out (Q)
Read cycle (continue burst)	Next	X	L	H	X	X	L	L	L–H	Data out (Q)
NOP/dummy read (begin burst)	External	L	L	L	H	X	H	L	L–H	Tri-state
Dummy read (continue burst)	Next	X	L	H	X	X	H	L	L–H	Tri-state
Write cycle (begin burst)	External	L	L	L	L	L	X	L	L–H	Data in (D)
Write cycle (continue burst)	Next	X	L	H	X	L	X	L	L–H	Data in (D)
NOP/WRITE ABORT (begin burst)	None	L	L	L	L	H	X	L	L–H	Tri-state
WRITE ABORT (continue burst)	Next	X	L	H	X	H	X	L	L–H	Tri-state
IGNORE CLOCK EDGE (stall)	Current	X	L	X	X	X	X	H	L–H	–
SLEEP MODE	None	X	H	X	X	X	X	X	X	Tri-state

Notes
1. X = "Don't Care", H = Logic HIGH, L = Logic LOW, CE stands for all chip enables active. BW_X = L signifies at least one byte write select is active, BW_X = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by WE and BW_X. See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the OE signal.
5. CEN = H inserts wait states.
6. Device will power up deselected and the I/Os in a tri-state condition, regardless of OE.
7. OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = tri-state when OE is inactive or when the device is deselected, and DQs = data when OE is active.

Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1354D follows. [8, 9, 10, 11]

Function (CY7C1354D)	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X	X	X
Write – no bytes written	L	H	H	H	H
Write byte a – (DQ$_a$ and DQP$_a$)	L	H	H	H	L
Write byte b – (DQ$_b$ and DQP$_b$)	L	H	H	L	H
Write bytes b, a	L	H	H	L	L
Write byte c – (DQ$_c$ and DQP$_c$)	L	H	L	H	H
Write bytes c, a	L	H	L	H	L
Write bytes c, b	L	H	L	L	H
Write bytes c, b, a	L	H	L	L	L
Write byte d – (DQ$_d$ and DQP$_d$)	L	L	H	H	H
Write bytes d, a	L	L	H	H	L
Write bytes d, b	L	L	H	L	H
Write bytes d, b, a	L	L	H	L	L
Write bytes d, c	L	L	L	H	H
Write bytes d, c, a	L	L	L	H	L
Write bytes d, c, b	L	L	L	L	H
Write all bytes	L	L	L	L	L

Notes
8. X = "Don't Care", H = Logic HIGH, L = Logic LOW, CE stands for all chip enables active. BWx = L signifies at least one byte write select is active, BWx = valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
9. Write is defined by WE and BWX. See Write Cycle Description table for details.
10. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1354D incorporates a serial boundary scan test access port (TAP) in the BGA package. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1354D contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO should be left unconnected. Upon power-up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram on page 11. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction Codes on page 15). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 12. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Exit Order on page 16 and Boundary Scan Exit Order on page 20 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 15.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.
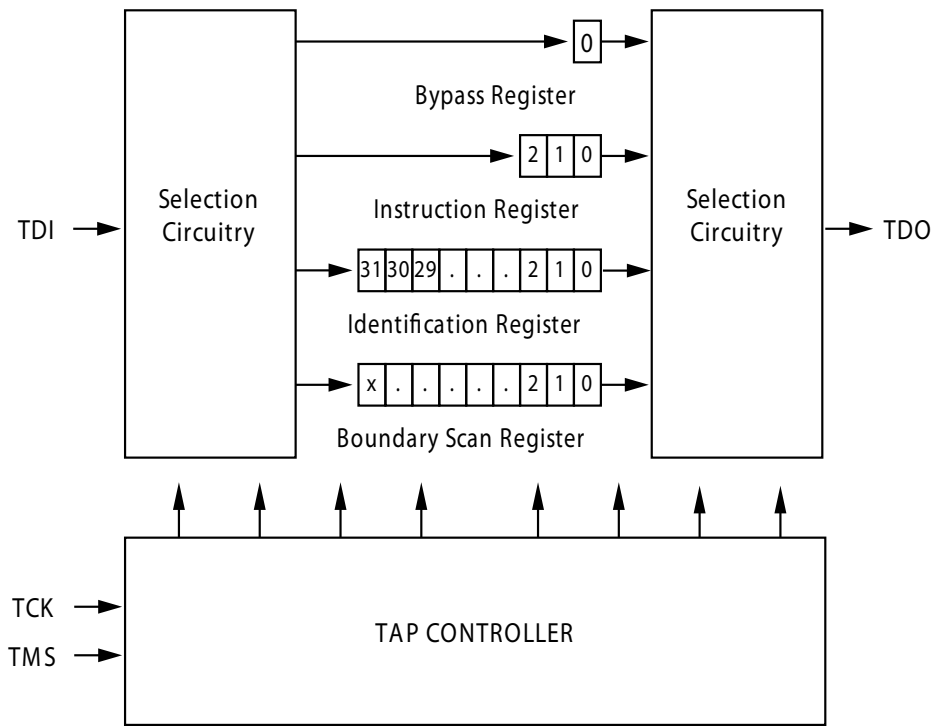
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.
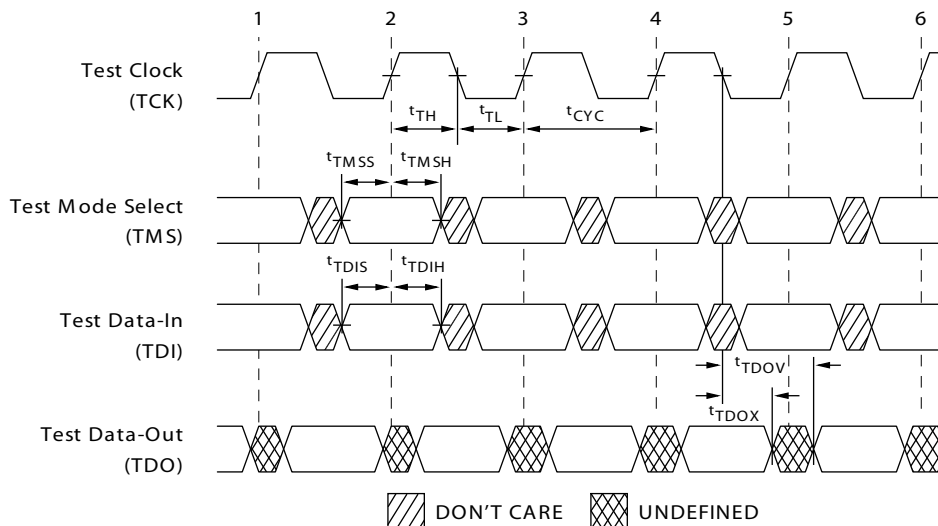
TAP Controller State Diagram
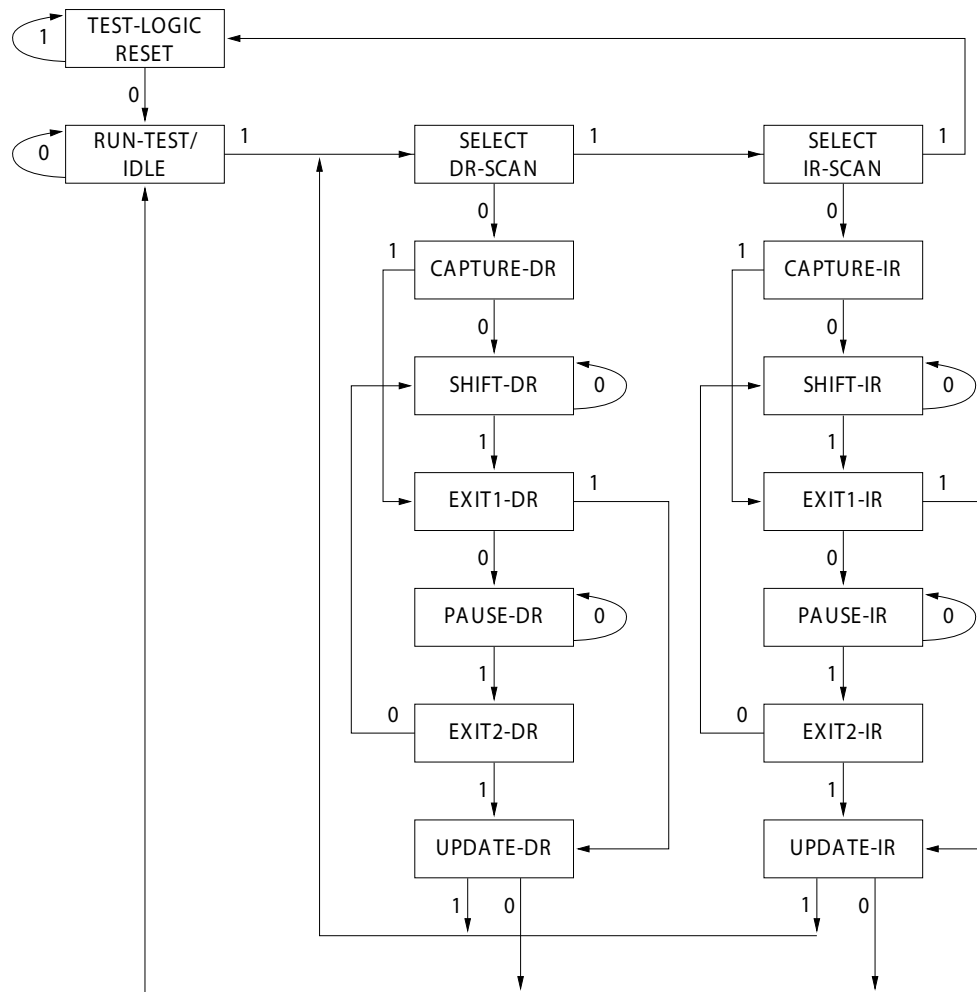
The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram


TAP Timing

TAP AC Switching Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH time	20	–	ns
t_{TL}	TCK clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns

3.3 V TAP AC Test Conditions

Input pulse levels ....V_{SS} to 3.3 V
Input rise and fall times ....1 ns
Input timing reference levels .... 1.5 V
Output reference levels .... 1.5 V
Test load termination supply voltage ....1.5 V
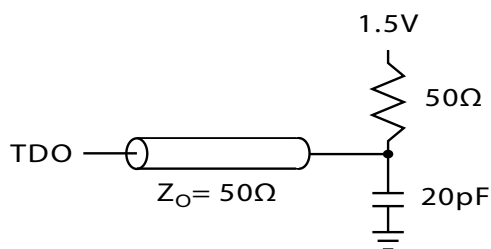
2.5 V TAP AC Test Conditions

Input pulse levels ....V_{SS} to 2.5 V
Input rise and fall time ....1 ns
Input timing reference levels .... 1.25 V
Output reference levels .... 1.25 V
Test load termination supply voltage ....1.25 V

3.3 V TAP AC Output Load Equivalent

2.5 V TAP AC Output Load Equivalent
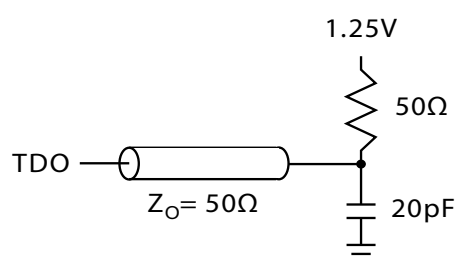
Notes
12. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
13. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

TAP DC Electrical Characteristics and Operating Conditions

$(0 \degree C < T_A < +70 \degree C; V_{DD} = 3.3\ V \pm 0.165\ V$ unless otherwise noted$)$

Parameter [14]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
			V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH voltage		V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		V_{DDQ} = 3.3 V	–0.3	0.8	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input load current	GND $\leq V_{IN} \leq V_{DDQ}$		–5	5	µA

Note
14. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1354D	Description
Revision number (31:29)	000	Reserved for version number.
Cypress device ID (28:12) [15]	01011001000100110	Reserved for future use.
Cypress JEDEC ID (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID register presence (0)	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary scan order (165-ball FBGA package)	61

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input/output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to high Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input/output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input/output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Note
15. Bit #24 is "1" in the Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Exit Order

(256K × 36)

Bit #	165-ball ID	Bit #	165-ball ID
1	B6	31	R9
2	B7	32	P9
3	A7	33	R8
4	B8	34	P8
5	A8	35	R6
6	A9	36	P6
7	B10	37	R4
8	A10	38	P4
9	C11	39	R3
10	E10	40	P3
11	F10	41	R1
12	G10	42	N1
13	D10	43	L2
14	D11	44	K2
15	E11	45	J2
16	F11	46	M2
17	G11	47	M1
18	H11	48	L1
19	J10	49	K1
20	K10	50	J1
21	L10	51	Not Bonded (Preset to 1)
22	M10	52	G2
23	J11	53	F2
24	K11	54	E2
25	L11	55	D2
26	M11	56	G1
27	N11	57	F1
28	R11	58	E1
29	R10	59	D1
30	P10	60	C1
		61	B2

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .... –0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ...... –0.5 V to +V_{DD}

DC to outputs in tri-state .... –0.5 V to V_{DDQ} + 0.5 V

DC input voltage .... –0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage
(per MIL-STD-883, method 3015) .... > 2001 V

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	320	368	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

Electrical Characteristics

Over the Operating Range

Parameter [16, 17]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage		3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage	for 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage [18]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	μA
	Input current of MODE	Input = V_{SS}	–30	–	μA
		Input = V_{DD}	–	5	μA
	Input current of ZZ	Input = V_{SS}	–5	–	μA
		Input = V_{DD}	–	30	μA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled	–5	5	μA

Notes
16. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
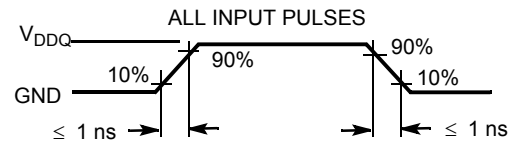17. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.
18. Tested initially and after any design or process changes that may affect these parameters.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [16, 17]	Description	Test Conditions		Min	Max	Unit
I_{DD}	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	5 ns cycle, 200 MHz	–	220	mA
I_{SB1}	Automatic CE power-down current — TTL inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} = 1/t_{CYC}	5 ns cycle, 200 MHz	–	120	mA
I_{SB2}	Automatic CE power-down current — CMOS inputs	Max V_{DD}, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0	5 ns cycle, 200 MHz	–	40	mA
I_{SB3}	Automatic CE power-down current — CMOS inputs	Max V_{DD}, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = f_{MAX} = 1/t_{CYC}	5 ns cycle, 200 MHz	–	110	mA
I_{SB4}	Automatic CE power-down current — TTL inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	5 ns cycle, 200 MHz	–	40	mA

Capacitance

Parameter [19]	Description	Test Conditions	165-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		7	pF

Thermal Resistance

Parameter [19]	Description	Test Conditions	165-ball FBGA Max	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	16.8	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.0	°C/W

Note
19. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

3.3 V I/O Test Load

OUTPUT

$Z_0 = 50\ \Omega$

$R_L = 50\ \Omega$

$V_T = 1.5\ V$

(a)

3.3 V

OUTPUT

R = 317 Ω

5 pF

INCLUDING JIG AND SCOPE

R = 351 Ω

(b)

ALL INPUT PULSES

V_{DDQ}

GND

10%

90%

90%

10%

$\leq$ 1 ns

$\leq$ 1 ns

(c)

2.5 V I/O Test Load

OUTPUT

$Z_0 = 50\ \Omega$

$R_L = 50\ \Omega$

$V_T = 1.25\ V$

(a)

2.5 V

OUTPUT

R = 1667 Ω

5 pF

INCLUDING JIG AND SCOPE

R = 1538 Ω

(b)

ALL INPUT PULSES

V_{DDQ}

GND

10%

90%

90%

10%

$\leq$ 1 ns

$\leq$ 1 ns

(c)
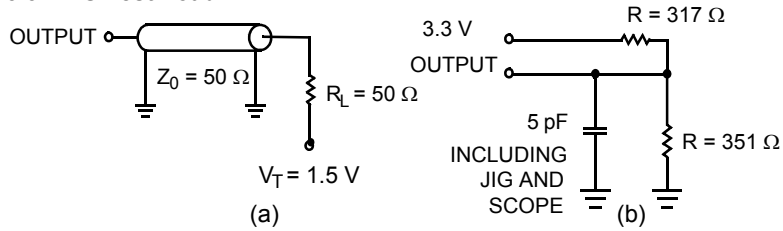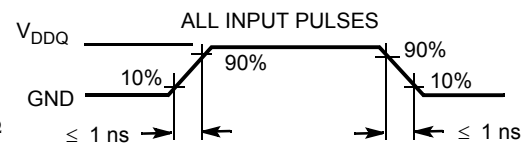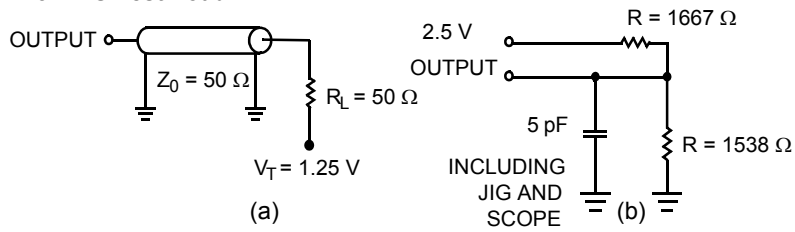
Switching Characteristics

Over the Operating Range

Parameter [20, 21]	Description	-200		Unit
		Min	Max	
t_{Power}[22]	V_{CC}(typical) to the first access read or write	1	–	ms
Clock				
t_{CYC}	Clock cycle time	5	–	ns
F_{MAX}	Maximum operating frequency	–	200	MHz
t_{CH}	Clock HIGH	2.0	–	ns
t_{CL}	Clock LOW	2.0	–	ns
t_{EOV}	$\overline{OE}$ LOW to output valid	–	3.2	ns
t_{CLZ}	Clock to low Z [23, 24, 25]	1.5	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	3.2	ns
t_{EOV}	$\overline{OE}$ LOW to output valid	–	3.2	ns
t_{DOH}	Data output hold after CLK rise	1.5	–	ns
t_{CHZ}	Clock to high Z [23, 24, 25]	1.5	3.2	ns
t_{CLZ}	Clock to low Z [23, 24, 25]	1.5	–	ns
t_{EOHZ}	$\overline{OE}$ HIGH to output high Z [23, 24, 25]	–	3.2	ns
t_{EOLZ}	$\overline{OE}$ LOW to output low Z [23, 24, 25]	0	–	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ setup before CLK rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_x$ setup before CLK rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ setup before CLK rise	1.5	–	ns
t_{CES}	Chip select setup	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_x$ hold after CLK rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.5	–	ns
t_{CEH}	Chip select hold after CLK rise	0.5	–	ns

Notes
20. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
21. Test conditions shown in (a) of Figure 2 on page 19 unless otherwise noted.
22. This part has a voltage regulator internally; t_{power} is the time power needs to be supplied above V_{DD} minimum initially, before a Read or Write operation can be initiated.
23. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
24. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
25. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 3. Read/Write Timing [26, 27, 28]
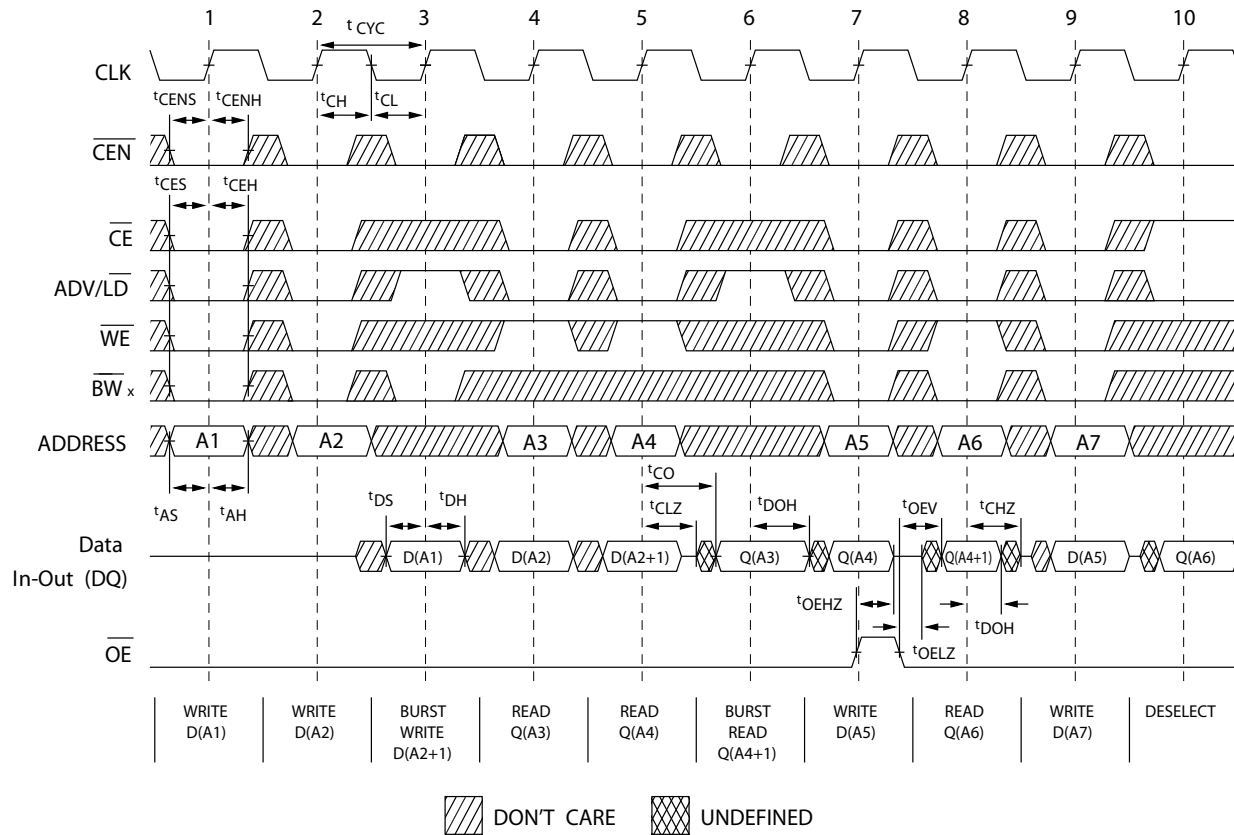
Notes
26. For this waveform ZZ is tied low.
27. When CE is LOW, CE₁ is LOW, CE₂ is HIGH and CE₃ is LOW. When CE is HIGH, CE₁ is HIGH or CE₂ is LOW or CE₃ is HIGH.
28. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms *(continued)*
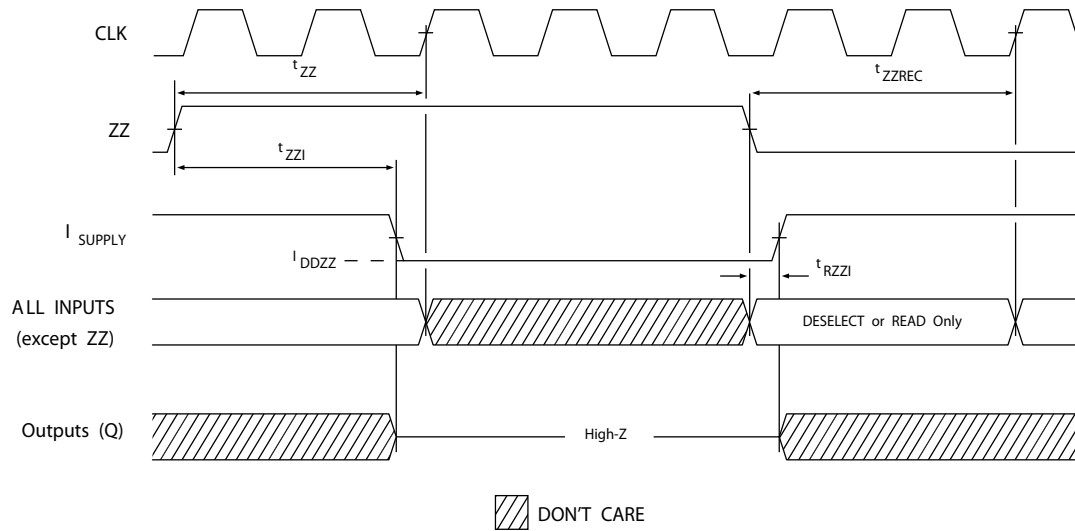
Figure 4. NOP, STALL, and DESELECT Cycles [29, 30, 31]

| | DON'T CARE | | UNDEFINED |
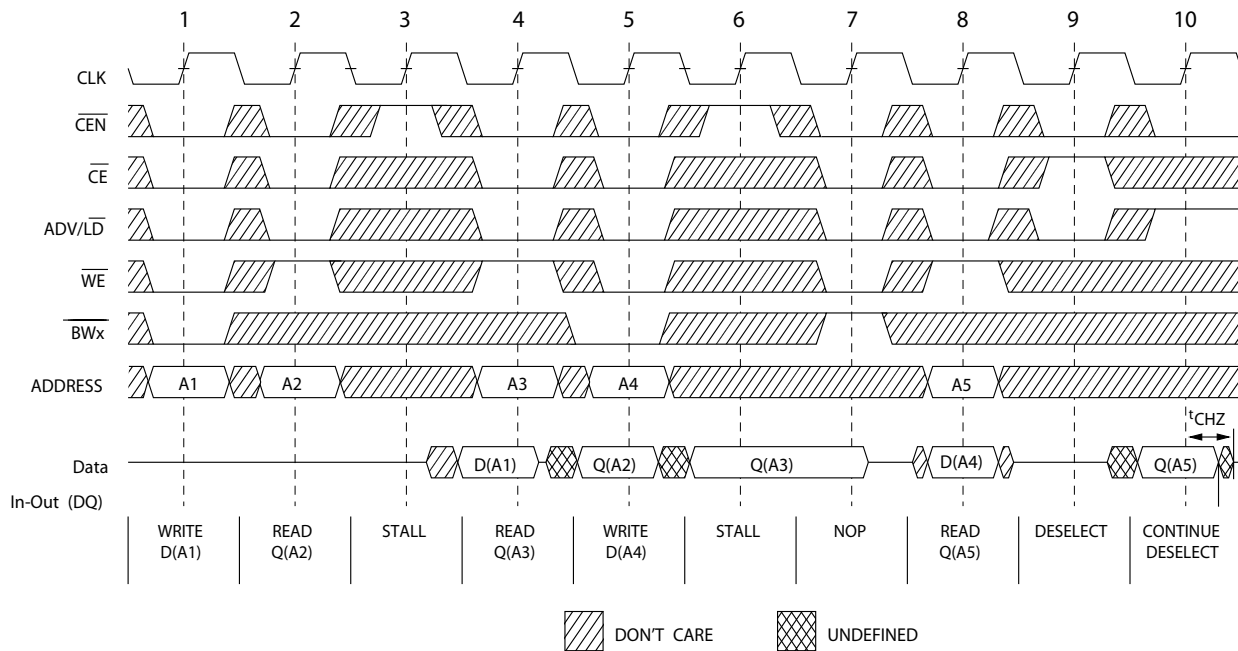
Notes
29. For this waveform ZZ is tied low.
30. When CE is LOW, CE₁ is LOW, CE₂ is HIGH and CE₃ is LOW. When CE is HIGH, CE₁ is HIGH or CE₂ is LOW or CE₃ is HIGH.
31. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.

Switching Waveforms *(continued)*

Figure 5. ZZ Mode Timing [32, 33]

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
200	CY7C1354D-200BZC	51-85180	165-ball FBGA (13 × 15 × 1.4 mm)	Commercial

Ordering Code Definitions

CY 7 C 1354 D - 200 BZ C

Temperature Range: C = Commercial;

Package Type: BZ = 165-ball FBGA

Speed Grade: 200 MHz

Process Technology ≥ 90 nm

Part Identifier: 1354 = PL, 256Kb × 36 (9Mb)

Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress
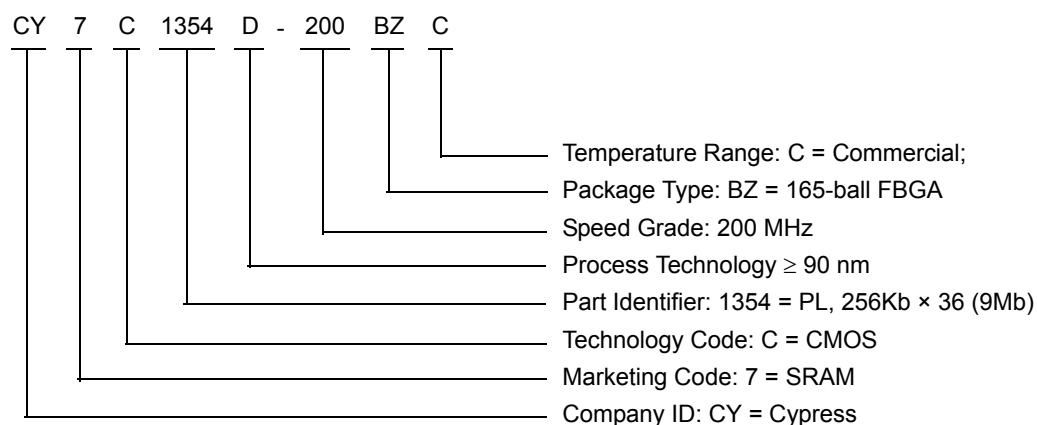
Package Diagrams

Figure 6. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180

NOTES :
SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)
JEDEC REFERENCE : MO-216 / ISSUE E
PACKAGE CODE : BB0AC/BW0AC
PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION
    DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.
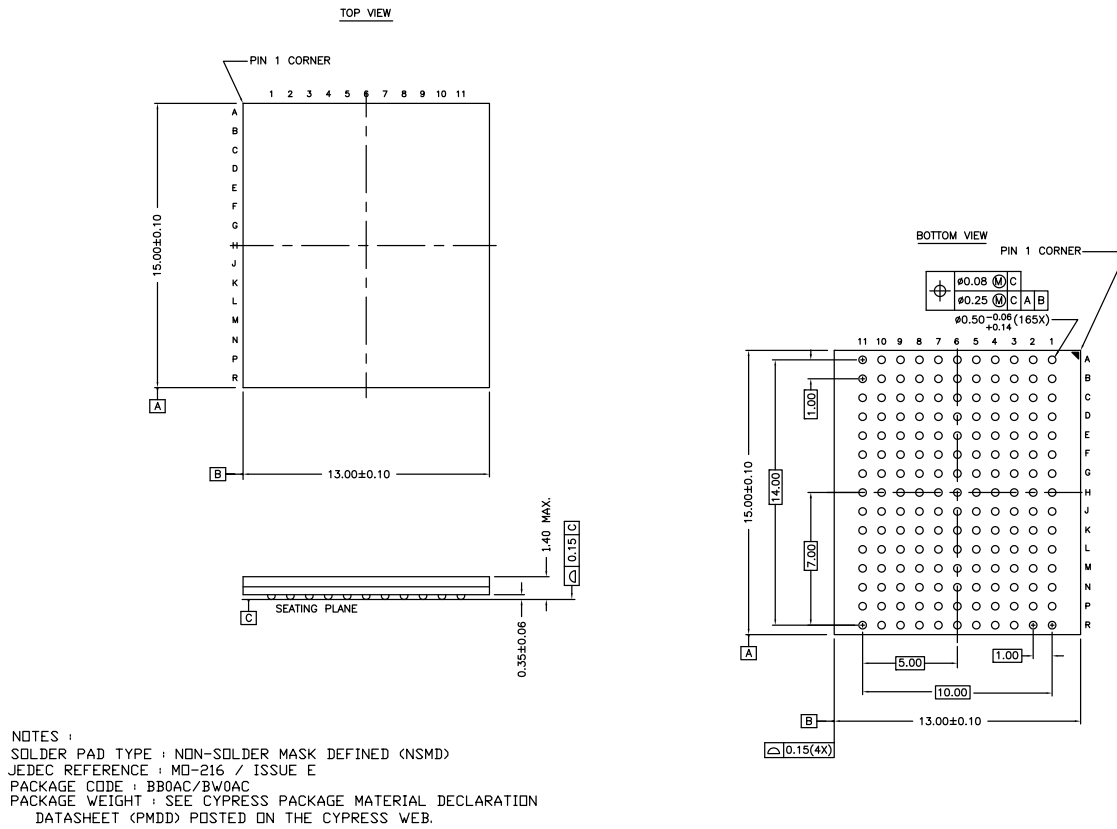
51-85180 *G

Acronyms

Acronym	Description
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
LMBU	Logical Multi-Bit Upsets
LSB	Least Significant Bit
LSBU	Logical Single-Bit Upsets
MSB	Most Significant Bit
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1354D, 9-Mbit (256K × 36) Pipelined SRAM with NoBL™ Architecture Document Number: 001-88918				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	4103005	08/23/2013	PRIT	New data sheet.
*A	4571750	11/18/2014	PRIT	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*B	5375848	07/27/2016	PRIT	Updated Package Diagrams: spec 51-85180 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*C	5980497	11/30/2017	AESATMP8	Updated logo and Copyright.

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