

## 8-Mbit (512K × 16) Static RAM

### Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical Standby current: 2  $\mu$ A
  - Maximum Standby current: 8  $\mu$ A
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

### Functional Description

The CY62157ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that significantly reduces power consumption when

addresses are not toggling. Place the device into standby mode when deselected ( $\overline{\text{CE}}$  HIGH or both  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are HIGH). The input or output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), both the Byte High Enable and the Byte Low Enable are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during an active write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

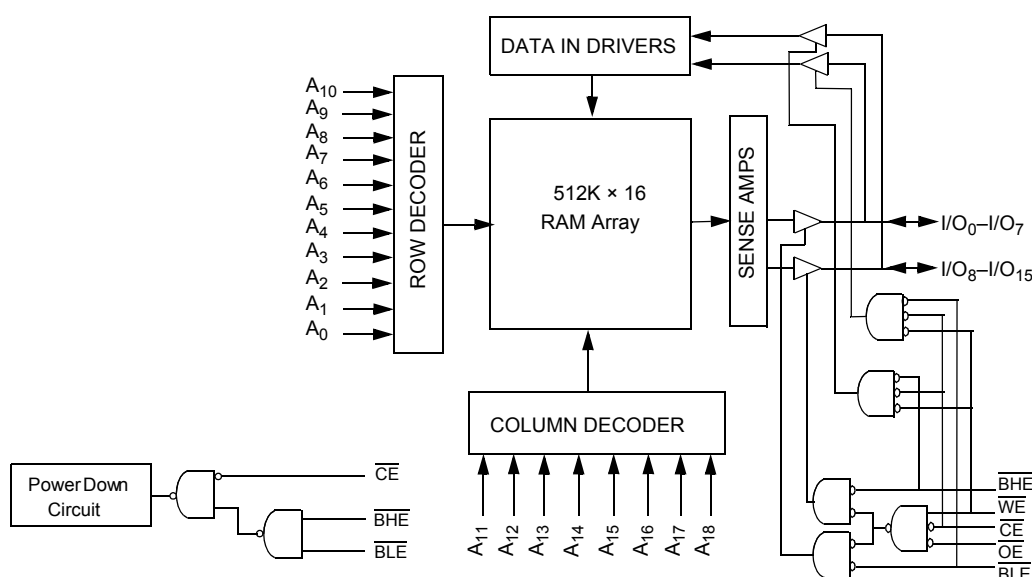
To write to the device, take Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ).

To read from the device, take Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory appears on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the [Truth Table on page 11](#) for a complete description of read and write modes.

The CY62157ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, click [here](#).

### Logic Block Diagram



## Contents

<b>Pin Configurations .....</b>	<b>3</b>	<b>Ordering Information .....</b>	<b>12</b>
<b>Product Portfolio .....</b>	<b>3</b>	Ordering Code Definitions .....	12
<b>Maximum Ratings .....</b>	<b>4</b>	<b>Package Diagram .....</b>	<b>13</b>
<b>Operating Range .....</b>	<b>4</b>	<b>Acronyms .....</b>	<b>14</b>
<b>Electrical Characteristics .....</b>	<b>4</b>	<b>Document Conventions .....</b>	<b>14</b>
<b>Capacitance .....</b>	<b>5</b>	Units of Measure .....	14
<b>Thermal Resistance .....</b>	<b>5</b>	<b>Document History Page .....</b>	<b>15</b>
<b>AC Test Loads and Waveforms .....</b>	<b>5</b>	<b>Sales, Solutions, and Legal Information .....</b>	<b>17</b>
<b>Data Retention Characteristics .....</b>	<b>6</b>	Worldwide Sales and Design Support .....	17
<b>Data Retention Waveform .....</b>	<b>6</b>	Products .....	17
<b>Switching Characteristics .....</b>	<b>7</b>	PSoC® Solutions .....	17
<b>Switching Waveforms .....</b>	<b>8</b>	Cypress Developer Community .....	17
<b>Truth Table .....</b>	<b>11</b>	Technical Support .....	17

## Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View)

A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	$\overline{\text{OE}}$
A <sub>0</sub>	5	40	$\overline{\text{BHE}}$
$\overline{\text{CE}}$	6	39	$\overline{\text{BLE}}$
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
$\overline{\text{WE}}$	17	28	A <sub>8</sub>
A <sub>18</sub>	18	27	A <sub>9</sub>
A <sub>17</sub>	19	26	A <sub>10</sub>
A <sub>16</sub>	20	25	A <sub>11</sub>
A <sub>15</sub>	21	24	A <sub>12</sub>
A <sub>14</sub>	22	23	A <sub>13</sub>

## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V) <sup>[1]</sup>	Speed (ns)	Power Dissipation					
				Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> (μA)	
				f = 1MHz		f = f <sub>max</sub>			
				Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62157ESL	Industrial	2.2 V–3.6 V and 4.5 V–5.5 V	45	1.8	3	18	25	2	8

### Notes

- Datasheet specifications are not guaranteed for V<sub>CC</sub> in the range of 3.6 V to 4.5 V.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V, and V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage to Ground Potential ..... -0.5 V to 6.0 V

DC Voltage Applied to Outputs  
in High Z State <sup>[3, 4]</sup> ..... -0.5 V to 6.0 V

DC Input Voltage <sup>[3, 4]</sup> ..... -0.5 V to 6.0 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch up Current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[5]</sup>
CY62157ESL	Industrial	-40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[6]</sup>	Max	
V <sub>OH</sub>	Output high voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7 I <sub>OH</sub> = -0.1 mA	2.0	—	—	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6 I <sub>OH</sub> = -1.0 mA	2.4	—	—	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5 I <sub>OH</sub> = -1.0 mA	2.4	—	—	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5 I <sub>OH</sub> = -0.1 mA	—	—	3.4 <sup>[7]</sup>	
V <sub>OL</sub>	Output low voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7 I <sub>OL</sub> = 0.1 mA	—	—	0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6 I <sub>OL</sub> = 2.1 mA	—	—	0.4	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5 I <sub>OL</sub> = 2.1 mA	—	—	0.4	
V <sub>IH</sub>	Input high voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	1.8	—	V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	2.2	—	V <sub>CC</sub> + 0.3	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	2.2	—	V <sub>CC</sub> + 0.5	
V <sub>IL</sub>	Input low voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	-0.3	—	0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	-0.3	—	0.8	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	-0.5	—	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	—	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	—	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CCmax</sub>	—	18	25	mA
		f = 1 MHz I <sub>OUT</sub> = 0 mA, CMOS levels	—	1.8	3	
I <sub>SB1</sub> <sup>[8]</sup>	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , f = f <sub>max</sub> (address and data only), f = 0 ( $\overline{OE}$ , $\overline{BHE}$ , $\overline{BLE}$ and $\overline{WE}$ ), V <sub>CC</sub> = V <sub>CC(max)</sub>	—	2	8	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>	—	2	8	μA

### Notes

- V<sub>IL</sub> (min) = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V, and V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.
- Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V<sub>IH</sub> of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.
- Chip enable (CE) needs to be tied to CMOS levels to meet the I<sub>SB1</sub>/I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

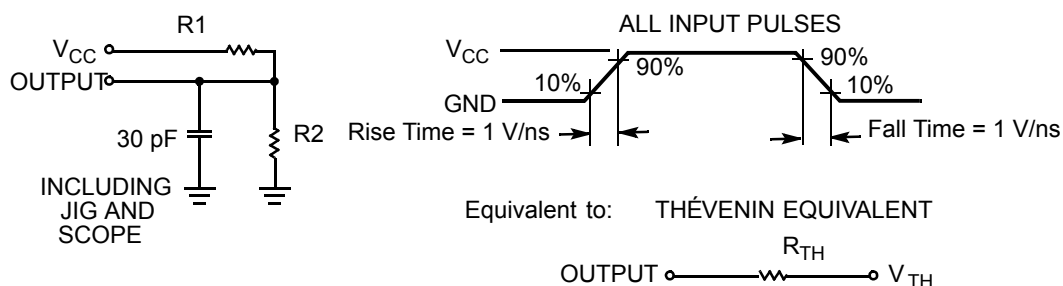
Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[9]</sup>	Description	Test Conditions	TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.92	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		17.44	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	$\Omega$
R2	15385	1554	990	$\Omega$
$R_{TH}$	8000	645	639	$\Omega$
$V_{TH}$	1.20	1.75	1.77	V

### Note

9. Tested initially and after any design or process changes that may affect these parameters.

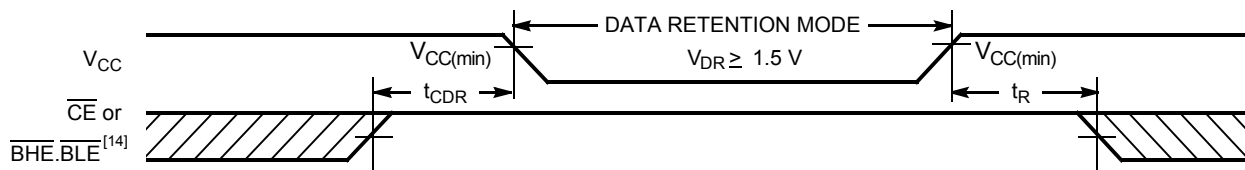
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}^{[10]}$	Data retention current	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	–	2	5	$\mu\text{A}$
		$V_{CC} = 1.5 \text{ V}$	–	2	8	
		$V_{CC} = 2.0 \text{ V}$	–	2	8	
$t_{CDR}^{[12]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[13]}$	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 3 \text{ V}$ , and  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .
11. Chip enable ( $\overline{CE}$ ) needs to be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu\text{s}$  or stable at  $V_{CC(min)} \geq 100 \mu\text{s}$ .
14.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

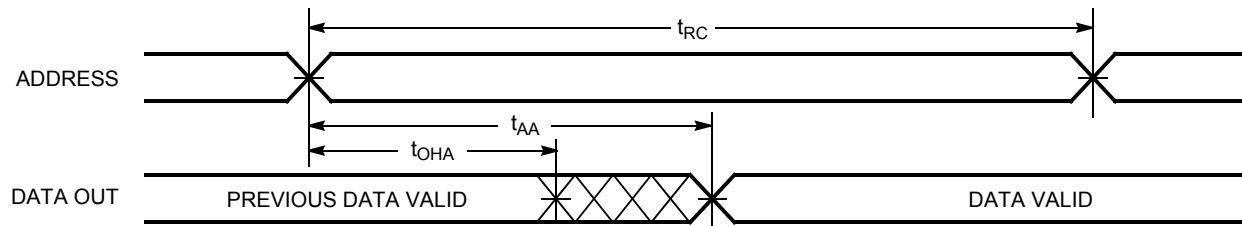
Parameter <sup>[15, 16]</sup>	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	45	–	ns
t <sub>AA</sub>	Address to data valid	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[17]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[17, 18]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[17]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[17, 18]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power up	0	–	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power down	–	45	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[17, 19]</sup>	5	–	ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to High Z <sup>[17, 18]</sup>	–	18	ns
Write Cycle <sup>[20, 21]</sup>				
t <sub>WC</sub>	Write cycle time	45	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	35	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[17, 18]</sup>	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[17]</sup>	10	–	ns

### Notes

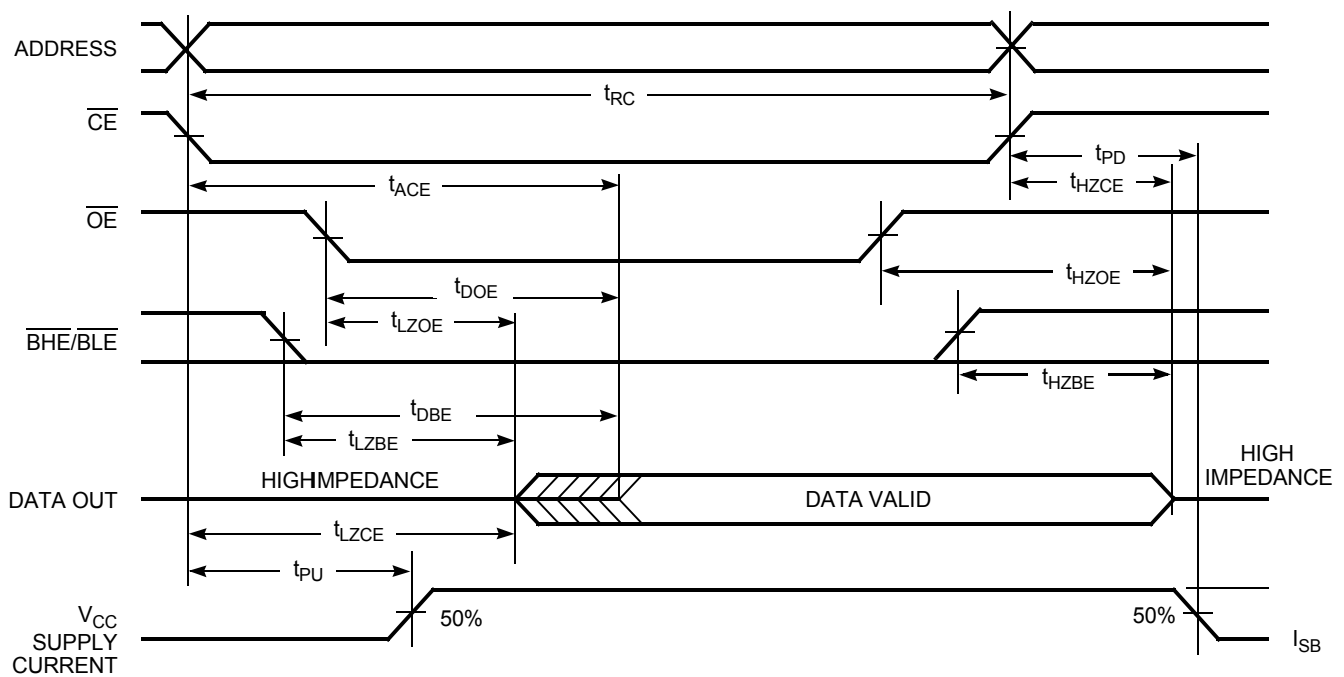
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note [AN66311](#). However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified IOL/IOH as shown in the [Figure 2 on page 5](#).
17. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
18.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
19. If both byte enables are toggled together, this value is 10 ns.
20. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for Write Cycle No. 4 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [22, 23]



**Figure 5. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [23, 24]



### Notes

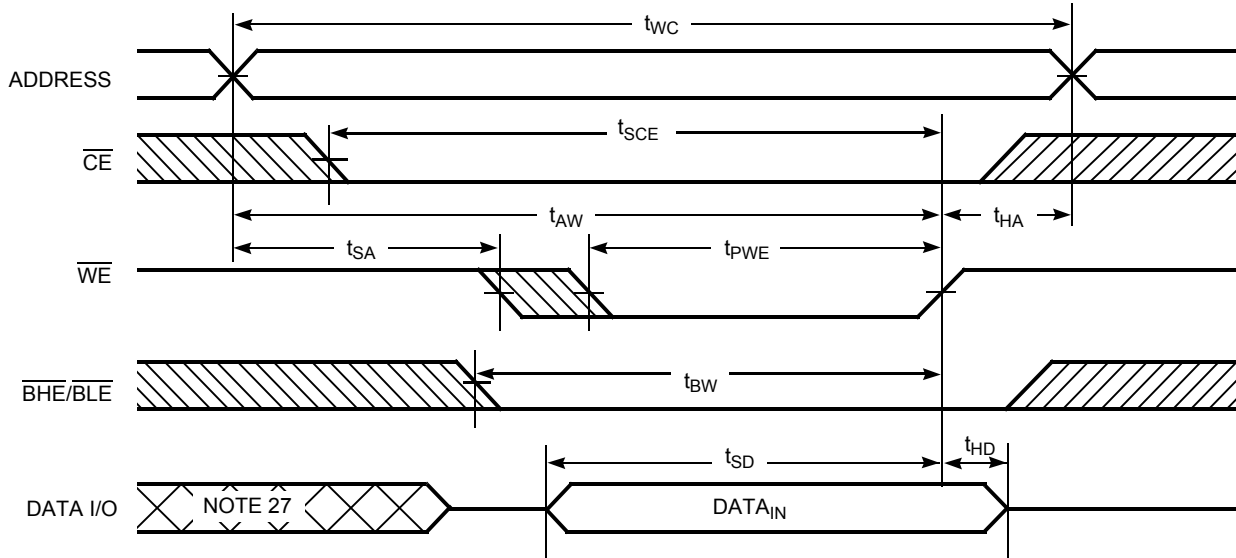
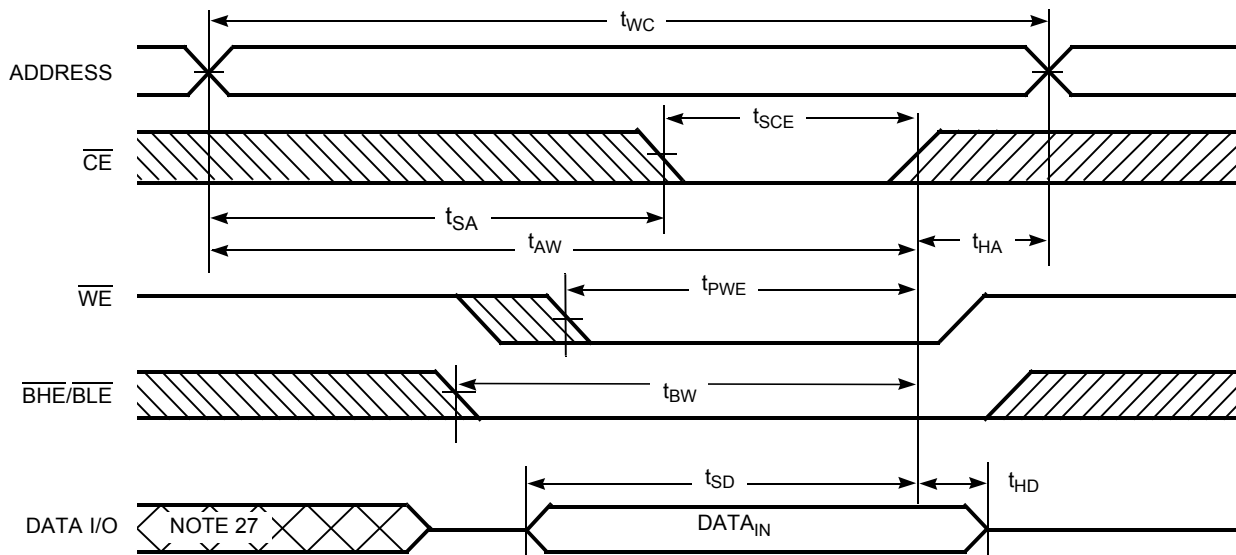
22. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$  =  $V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ .

23.  $\overline{\text{WE}}$  is HIGH for read cycle.

24. Address valid before or similar to  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW.



**Switching Waveforms** (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [25, 26]

**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [25, 26]

**Notes**

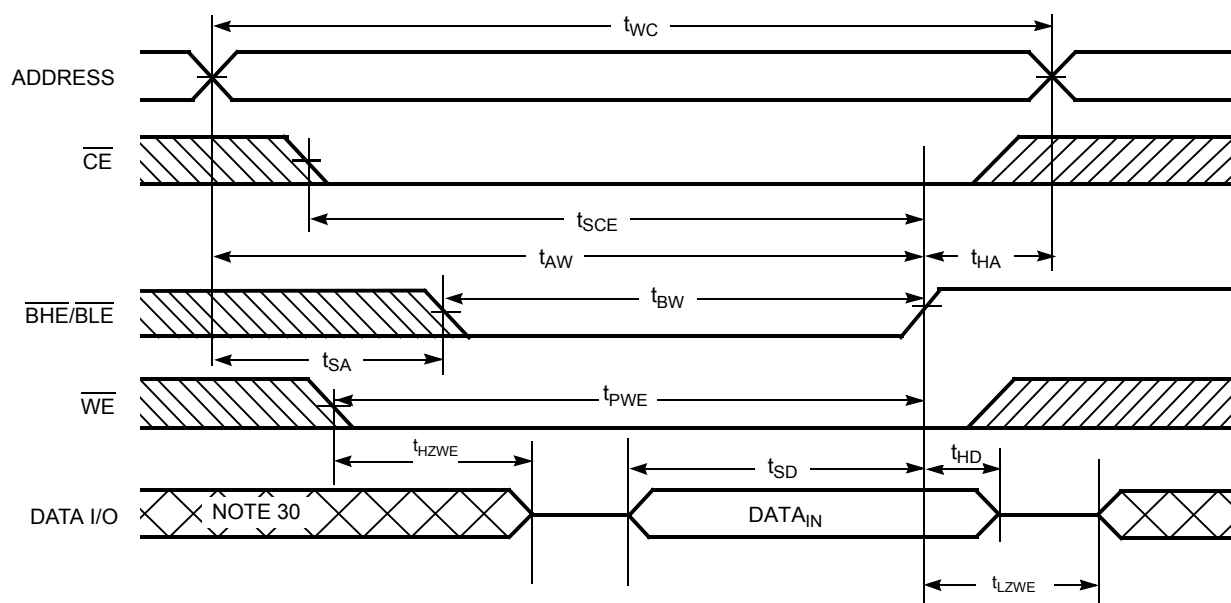
25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.

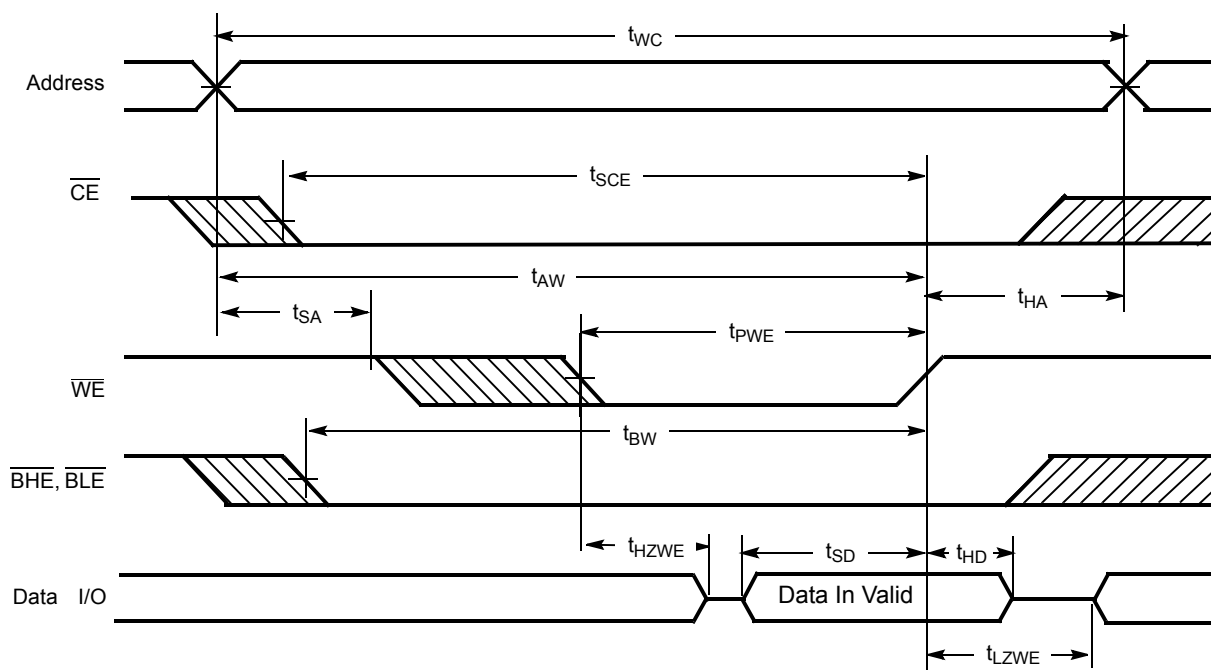
27. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled)** [28, 29]



**Figure 9. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [28, 29, 31]



### Notes

28. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

29. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high impedance state.

30. During this period, the I/Os are in output state. Do not apply input signals.

31. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/power down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	X	X	H	H	High Z	Deselect/power down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Output disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

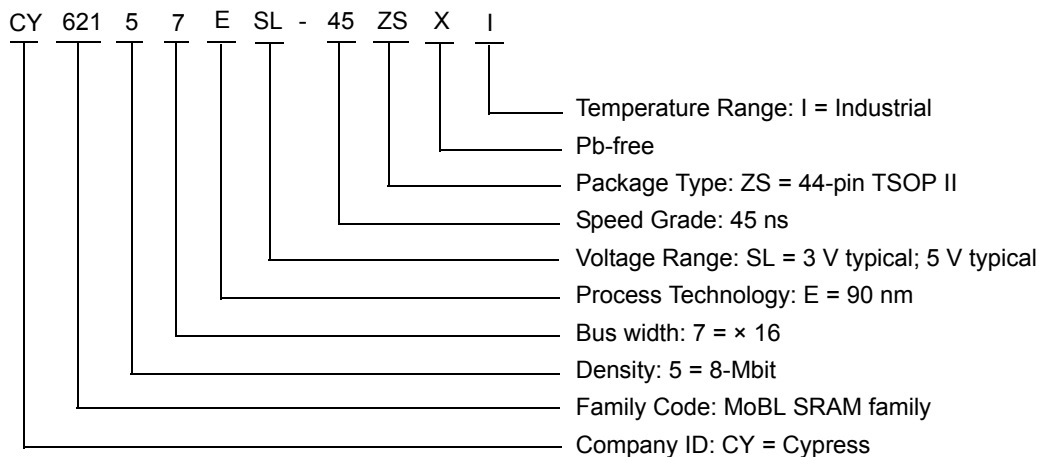
### Note

32. The 'X' (Don't care) state for the Chip enable in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on this pin is not permitted.

## Ordering Information

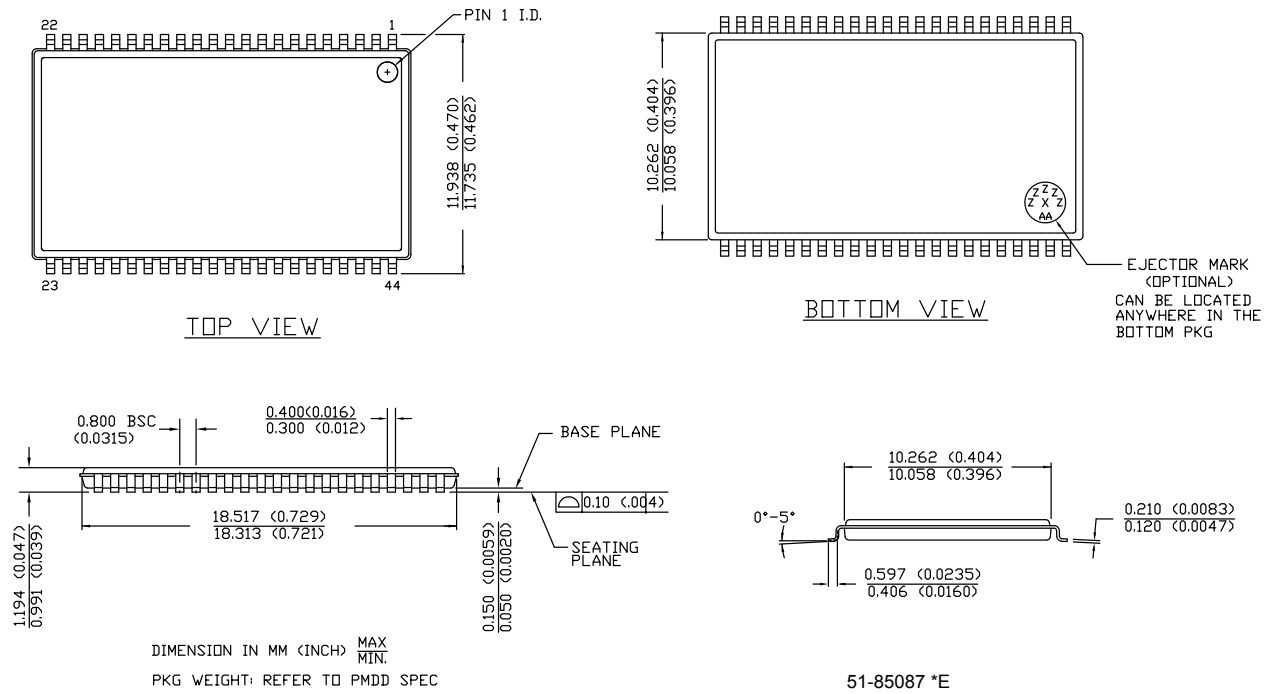
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ESL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial

## Ordering Code Definitions



## Package Diagram

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62157ESL MoBL®, 8-Mbit (512K × 16) Static RAM Document Number: 001-43141				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	1875228	See ECN	VKN / AESA	New data sheet.
*A	2943752	06/03/2010	VKN	Added <a href="#">Contents</a> . Updated <a href="#">Electrical Characteristics</a> : Added Note 8 and referred the same note in I <sub>SB2</sub> parameter. Updated <a href="#">Truth Table</a> : Added Note 32 and referred the same note in $\overline{CE}$ column. Updated <a href="#">Package Diagram</a> . Added <a href="#">Sales, Solutions, and Legal Information</a> .
*B	3109266	12/13/2010	PRAS	Changed Table Footnotes to Footnotes. Added <a href="#">Ordering Code Definitions</a> .
*C	3295175	06/29/2011	RAME	Updated <a href="#">Functional Description</a> : Remove reference to AN1064 SRAM system guidelines. Updated <a href="#">Electrical Characteristics</a> : Updated Note 8 (Added I <sub>SB1</sub> ) and referred the same note in I <sub>SB1</sub> parameter. Updated <a href="#">Capacitance</a> : Added Note 9 and referred the same note in parameter column. Updated <a href="#">Thermal Resistance</a> : Added Note 9 and referred the same note in parameter column. Updated <a href="#">Data Retention Characteristics</a> : Added Note 11 and referred the same note in I <sub>CCDR</sub> parameter. Updated <a href="#">Ordering Code Definitions</a> . Added <a href="#">Units of Measure</a> .
*D	3904207	02/14/2013	MEMJ	Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 6</a> (Removed $\overline{OE}$ signal). Updated <a href="#">Figure 7</a> (Removed $\overline{OE}$ signal). Removed the Note "Data I/O is high impedance if $\overline{OE} = V_{IH}$ ." and its reference in <a href="#">Figure 6</a> , <a href="#">Figure 7</a> . Removed the figure "Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW". Updated <a href="#">Figure 8</a> (Removed "OE LOW" in caption only). Removed the Note "Data I/O is high impedance if $\overline{OE} = V_{IH}$ ." and its reference in <a href="#">Figure 8</a> . Updated <a href="#">Package Diagram</a> : spec 51-85087 – Changed revision from *C to *E.
*E	4019657	06/04/2013	MEMJ	Updated <a href="#">Functional Description</a> : Updated description. Updated <a href="#">Electrical Characteristics</a> : Added one more Test Condition "4.5 ≤ V <sub>CC</sub> ≤ 5.5, I <sub>OH</sub> = -0.1 mA" for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition "4.5 ≤ V <sub>CC</sub> ≤ 5.5, I <sub>OH</sub> = -0.1 mA".
*F	4100920	08/21/2013	VINI	Updated <a href="#">Switching Characteristics</a> : Added Note 15 and referred the same note in "Parameter" column. Updated to new template.
*G	4576406	01/16/2015	VINI	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated <a href="#">Switching Characteristics</a> : Added Note 21 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added <a href="#">Figure 9</a> . Added Note 31 and referred the same note in <a href="#">Figure 9</a> .

**Document History Page** (continued)

Document Title: CY62157ESL MoBL®, 8-Mbit (512K × 16) Static RAM Document Number: 001-43141				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*H	5169392	03/10/2016	VINI	Updated <a href="#">Thermal Resistance</a> : Replaced “two-layer” with “four-layer” in “Test Conditions” column. Changed value of $\Theta_{JA}$ parameter from 77 °C/W to 57.92 °C/W. Changed value of $\Theta_{JC}$ parameter from 13 °C/W to 17.44 °C/W. Updated to new template. Completing Sunset Review.



## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

ARM® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Lighting & Power Control	<a href="http://cypress.com/powerpsoc">cypress.com/powerpsoc</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless/RF	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

#### PSoC® Solutions

[cypress.com/psoc](http://cypress.com/psoc)

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation 2008–2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you under its copyright rights in the Software, a personal, non-exclusive, nontransferable license (without the right to sublicense) (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units. Cypress also grants you a personal, non-exclusive, nontransferable, license (without the right to sublicense) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely to the minimum extent that is necessary for you to exercise your rights under the copyright license granted in the previous sentence. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and Company shall and hereby does release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. Company shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[CY62157ESL-45ZSXI](#) [CY62157ESL-45ZSXIT](#)