CY2545/CY2547

Quad-PLL Programmable Spread Spectrum Clock Generator with Serial I²C Interface

Features

- Four fully-integrated phase-locked loops (PLLs)
- Input frequency range
  - External crystal: 8 to 48 MHz
  - External reference: 8 to 166 MHz clock
- Wide operating output frequency range
  - 3 to 166 MHz
- Serial programmable over two-wire I²C interface
- Programmable spread spectrum with center and down spread option and Lexmark and Linear modulation profiles
- V_{DD} supply voltage options:
  - 2.5 V, 3.0 V, and 3.3 V for CY2545
  - 1.8 V for CY2547
- Selectable output clock voltages independent of V_{DD} supply:
  - 1.8 V, 2.5 V, 3.0 V, and 3.3 V for CY2545
  - 1.8 V for CY2547
- Power-down, output enable, or frequency select features
- Low jitter, high accuracy outputs
- Ability to synthesize nonstandard frequencies with Fractional-N capability
- Up to eight clock outputs with programmable drive strength
- Glitch-free outputs while frequency switching
- 24-pin QFN package
- Commercial and industrial temperature ranges
- One-time programmability
  For programming support, contact Cypress technical support or send an e-mail to clocks@cypress.com

Benefits

- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application-specific programmable EMI reduction using spread spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low-power systems

Functional Description

For a complete list of related documentation, click here.

Logic Block Diagram

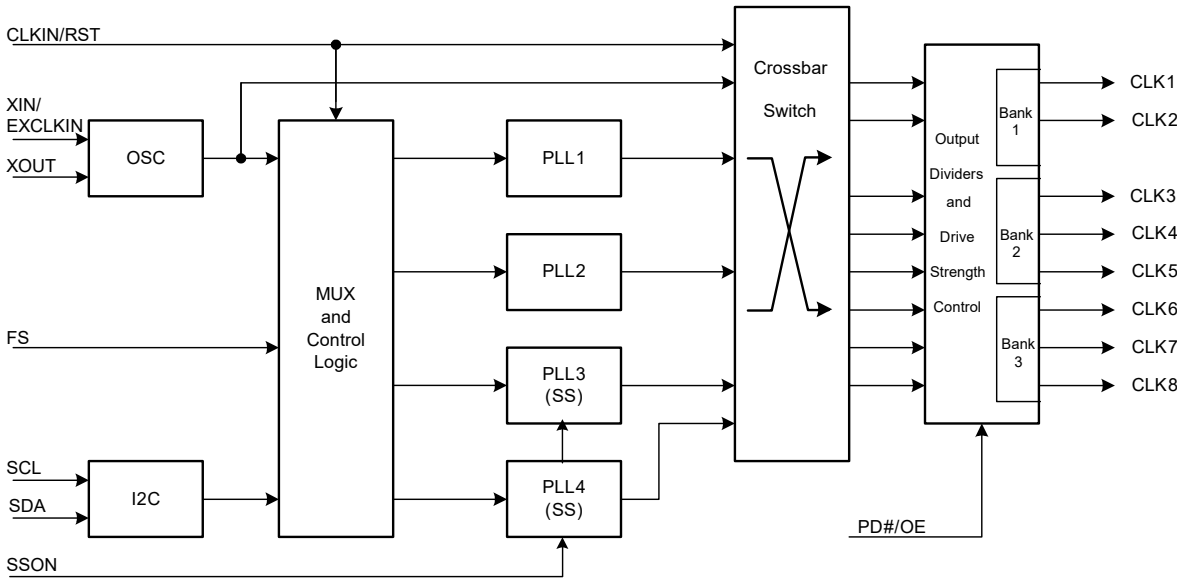

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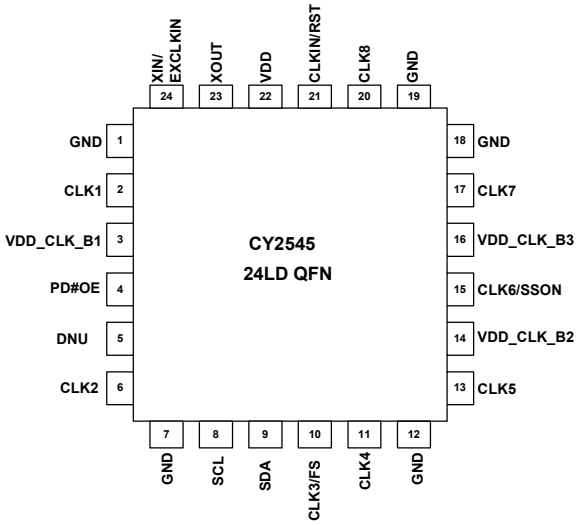
Figure 1. 24-pin QFN pinout



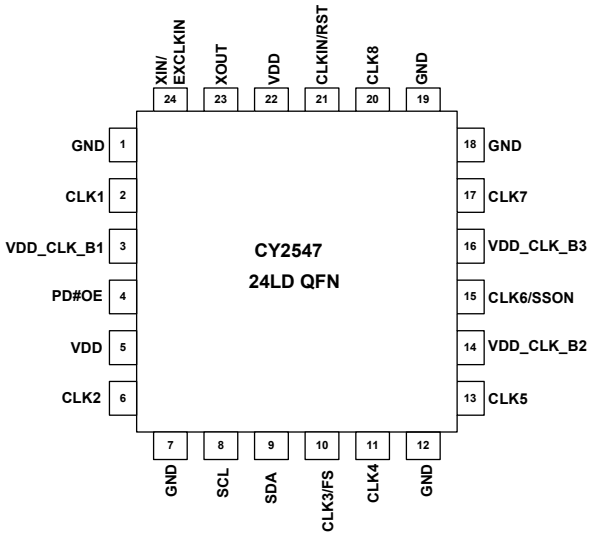
Pin Definitions

CY2545 (24-pin QFN (V_{DD} = 2.5 V, 3.0 V or 3.3 V Supply))

Pin No.	Name	I/O	Description
1	GND	Power	Power supply ground
2	CLK1	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank1 voltage
3	$V_{DD\_CLK\_B1}$	Power	Power supply for Bank1 (CLK1, CLK2) output: 2.5 V/3.0 V/3.3 V and must be equal to or more than the V_{DD} power supply.
4	PD#/OE	Input	Multifunction programmable pin: Output enable or Power-down mode
5	DNU	DNU	Do not use this pin
6	CLK2	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank1 voltage
7	GND	Power	Power supply ground
8	SCL	Input	Serial data clock
9	SDA	Input/Output	Serial data input/output
10	CLK3/FS	Output/Input	Multifunction programmable pin: Programmable clock output with no spread spectrum or frequency select input pin. Output voltage of CLK3 depends on Bank2 voltage
11	CLK4	Output	Programmable clock output with no spread spectrum. Output voltage depends on Bank2 voltage
12	GND	Power	Power supply ground
13	CLK5	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank2 voltage
14	$V_{DD\_CLK\_B2}$	Power	Power supply for Bank2 (CLK3, CLK4, CLK5) output: 1.8 V/2.5 V/3.0 V/3.3 V
15	CLK6/SSON	Output/Input	Multifunction programmable pin: Programmable clock output with spread spectrum or spread spectrum ON/OFF control input pin. Output voltage of CLK6 depends on Bank3 voltage
16	$V_{DD\_CLK\_B3}$	Power	Power supply for Bank3 (CLK6, CLK7, CLK8) output: 2.5 V/3.0 V/3.3 V
17	CLK7	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank3 voltage
18	GND	Power	Power supply ground
19	GND	Power	Power supply ground
20	CLK8	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank3 voltage
21	CLKIN/RST	Input/Input	Multifunction programmable pin. High true reset input or 2.5 V/3.0 V/3.3 V external reference clock input. The signal level of CLKIN input must track V_{DD} power supply on pin 22.
22	V_{DD}	Power	Power supply for core and inputs: 2.5 V/3.0 V/3.3 V
23	XOUT	Output	Crystal output
24	XIN/EXCLKIN	Input	Crystal input or 1.8 V external clock input

Pinouts

Figure 2. 24-pin QFN pinout



Pin Definitions

CY2547 (24-pin QFN (V_{DD} = 1.8 V Supply))

Pin No.	Name	I/O	Description
1	GND	Power	Power supply ground
2	CLK1	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank1 voltage
3	$V_{DD\_CLK\_B1}$	Power	Power supply for Bank1 (CLK1, CLK2) output: 1.8 V
4	PD#/OE	Input	Multifunction programmable pin: Output enable or Power-down mode
5	V_{DD}	Power	Power supply for core and inputs: 1.8 V
6	CLK2	Output	Programmable output clock with spread spectrum. Output voltage depends on Bank1 voltage
7	GND	Power	Power supply ground
8	SCL	Input	Serial data clock
9	SDA	Input/Output	Serial data input
10	CLK3/FS	Output/Input	Multifunction programmable pin: Programmable clock output with no spread spectrum or frequency select input pin. Output voltage of CLK3 depends on $V_{DD\_CLK\_B2}$ voltage
11	CLK4	Output	Programmable output clock with no spread spectrum. Output voltage depends on Bank2 voltage
12	GND	Power	Power supply ground
13	CLK5	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank2 voltage
14	$V_{DD\_CLK\_B2}$	Power	Power supply for Bank2 (CLK3, CLK4, CLK5) output: 1.8 V
15	CLK6/SSON	Output/Input	Multifunction programmable pin: Programmable clock output with spread spectrum or spread spectrum ON/OFF control input pin. Output voltage of CLK6 depends on $V_{DD\_CLK\_B3}$ voltage
16	$V_{DD\_CLK\_B3}$	Power	Power supply for Bank3 (CLK6, CLK7, CLK8) output: 1.8 V
17	CLK7	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank3 voltage
18	GND	Power	Power supply ground
19	GND	Power	Power supply ground
20	CLK8	Output	Programmable clock output with spread spectrum. Output voltage depends on Bank3 voltage
21	CLKIN/RST	Input/Input	Multifunction programmable pin: High true reset input or 1.8 V external low voltage reference clock input
22	V_{DD}	Power	Power supply for core and inputs: 1.8 V
23	XOUT	Output	Crystal output
24	XIN/EXCLKIN	Input	Crystal input or 1.8 V external clock input

Functional Overview

Four Configurable PLLs

The CY2545 and CY2547 have four I^2C programmable PLLs available to generate output frequencies ranging from 3 to 166 MHz. The advantage of having four PLLs is that a single device generates up to four independent frequencies from a single crystal. Two sets of frequencies for each PLL can be programmed. This enables in system frequency switching using multifunction frequency select pin, FS.

I^2C Programming

The CY2545 and CY2547 have a serial I^2C interface that programs the configuration memory array to synthesize output frequencies by programmable output divider, spread characteristics, drive strength, and crystal load capacitance. I^2C can also be used for in system control of these programmable features.

Input Reference Clocks

The input to the CY2545 and CY2547 is either a crystal or a clock signal. The input frequency range for crystals is 8 MHz to 48 MHz. There is provision for two reference clock inputs, CLKIN and EXCLKIN with frequency range of 8 MHz to 166 MHz. For both devices, when CLKIN signal at pin 21 is used as a reference input, a valid signal at EXCLKIN (as specified in the AC and DC Electrical Specification table), must be present for the devices to operate properly.

Multiple Power Supplies

The CY2545 and CY2547 are designed to operate at internal core supply voltage of 1.8 V. In the case of the high voltage part (CY2545), an internal regulator is used to generate 1.8 V from the 2.5 V/3.0 V/3.3 V V_{DD} supply voltage at pin 22. For the low voltage part (CY2547), this internal regulator is bypassed and 1.8 V at V_{DD} pin 22 is directly used.

Output Bank Settings

These devices have eight clock outputs grouped in three output driver banks. The Bank 1, Bank 2, and Bank 3 correspond to (CLK1, CLK2), (CLK3, CLK4, CLK5), and (CLK6, CLK7, CLK8), respectively. Separate power supplies are used for each of these banks and they can be any of 1.8 V, 2.5 V, 3.0 V, or 3.3 V for CY2545 and 1.8 V for CY2547 giving user multiple choice of output clock voltage levels.

Output Source Selection

These devices have eight clock outputs (CLK1 - 8). There are six available clock sources for these outputs. These clock sources are: XIN/EXCLKIN, CLKIN, PLL1, PLL2, PLL3, or PLL4. Output clock source selection is done using four out of six crossbar switch. Thus, any one of these six available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to four independent clock outputs.

Spread Spectrum Control

Two of the four PLLs (PLL3 and PLL4) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK7/SSON). It can be programmed to either center spread range from ±0.125% to ±2.50% or down spread range from –0.25% to –5.0% with Lexmark or Linear profile.

Frequency Select

The device can store two different PLL frequency configurations, output source selection and output divider values for all eight outputs in its nonvolatile memory location. There is a multifunction programmable pin, CLK3/FS which, if programmed as frequency select input, can be used to select between these two arbitrarily programmed settings.

Glitch-Free Frequency Switch

When the frequency select pin (FS) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is switched.

Device Reset Function

There is a multifunction CLKIN/RST (pin 21) that can be programmed to use for the device reset function. There are two different programmable modes of operation for this device reset function. First one (called POR like reset), when used brings the device in the default register settings loosing all configuration changes made through the I^2C interface. The second (called Clean Start), keeps the I^2C programmed values while giving all outputs a simultaneous clean start from its low pull-down state.

PD#/OE Mode

PD#/OE (Pin 4) is programmable to operate as either power-down (PD#) or output enable (OE) mode. PD# is a low true input. If activated it shuts off the entire chip, resulting in minimum device power consumption. Setting this signal high brings the device into operational mode with default register settings.

When this pin is programmed as output enable (OE), clock outputs are enabled or disabled using OE pin. Individual clock outputs can be programmed to be sensitive to this OE pin.

Keep Alive Mode

By activating the device in the keep alive mode, power-down mode is changed to power saving mode. This disables all PLLs and outputs, but preserves the contents of the volatile registers. Thus, any configuration changes made through the I^2C interface are preserved. By deactivating the keep alive mode, I^2C memory is not preserved during power-down, but power consumption is reduced relative to the keep alive mode.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 1 shows the typical rise and fall times for different drive strength settings.

Table 1. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The device, CY2545/CY2547 can be custom programmed to any desired frequencies and listed features. For customer specific programming and I^2C programmable memory bitmap definitions, contact your local Cypress Field Application Engineer (FAE) or sales representative.

Output Driver Supply and Multi-Function Input Restriction

There are two programmable Output/Input function pins for CLK3/FS and CLK6/SSON. These are configurable as clock output or select input or spread spectrum ON/OFF control input pin.

- When configured as Output, the driver supply voltage is defined by $V_{DD\_CLK\_Bx}$ and can be individually used with 1.8 V, 2.5 V, 3.0 V, or 3.3 V power supply apart from the V_{DD} supply.
- When configured as Input, the input threshold level is defined by V_{DD} supply while the protection diode is connected to the respective $V_{DD\_CLK\_Bx}$ power supply. Therefore, if $V_{DD\_CLK\_Bx}$ is less than $V_{DD} – 0.5$ V, a large leakage current would flow from the input pin to the $V_{DD\_CLK\_Bx}$ supply. The device does not permit this condition; it is required that the power supply for the bank ($V_{DD\_CLK\_Bx}$) is more than $V_{DD} – 0.5$ V.

Example: In CY2545, if $V_{DD\_CLK\_B2} = 1.8$ V, CLK3/FS is configured as FS, and $V_{DD} = 3.3$ V, there will be a leakage current from FS high to $V_{DD\_CLK\_B2}$. The multi-function pin should only be used as clock output if the $V_{DD\_CLK\_Bx}$ is less than $V_{DD} – 0.5$ V. In other words, when these multi-function programmable pins are configured as input, the power supply for the bank ($V_{DD\_CLK\_Bx}$) should be more than $V_{DD} – 0.5$ V.

Serial I²C Programming Interface Protocol and Timing

To enhance the flexibility and function of the clock synthesizer, a two signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up and therefore, use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

The CY2545 and CY2547 use a 2-wire serial interface SDA and SCL that operates up to 400 kbits/s in read or write mode. The SDA and SCL timing and data transfer sequence is shown in Figure 3. The basic write serial format is:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit. The basic serial format is illustrated in Figure 4.

Figure 3. Data Transfer Sequence on the Serial Bus

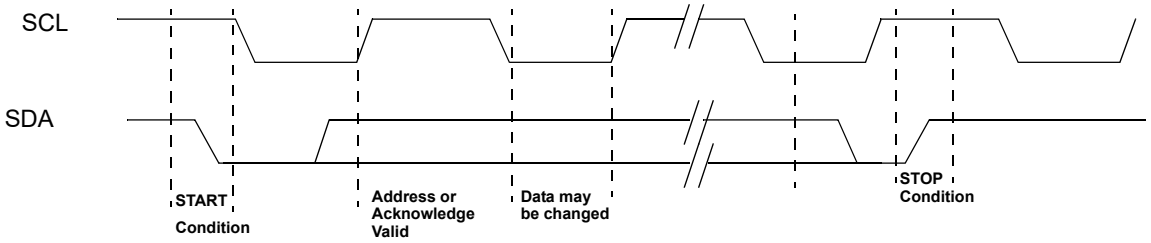
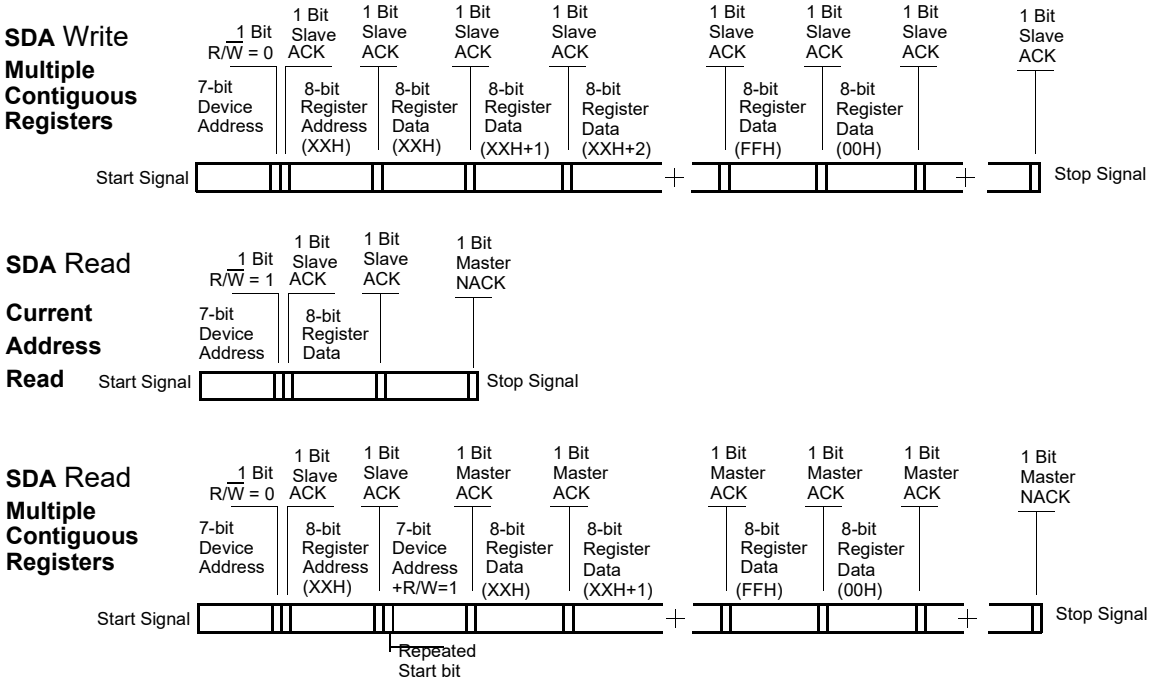


Figure 4. Data Frame Architecture



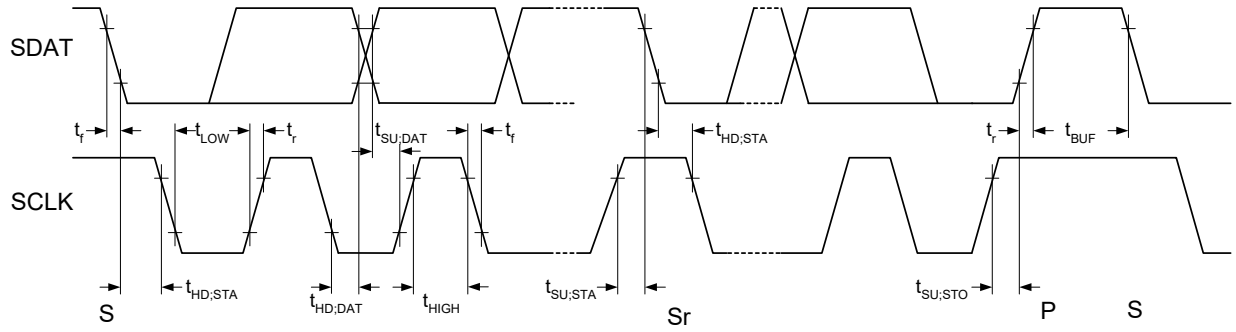
Device Address

The device serial interface address is 69H. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

Data Valid

Data is valid when the clock is HIGH, and is only transitioned when the clock is LOW, as illustrated in Figure 5.

Figure 5. Data Valid and Data Transition Periods



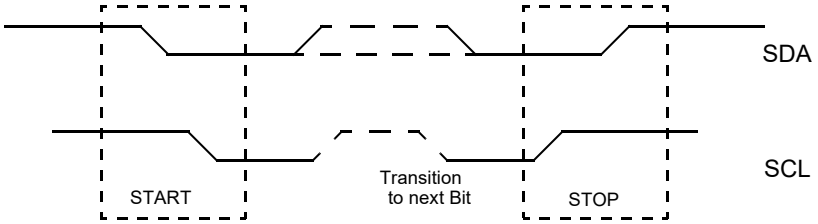
Data Frame

A start and stop sequence indicates every new data frame, as illustrated in Figure 6.

Start Sequence - The start frame is indicated by SDA going LOW when SCL is HIGH. Every time a start signal is supplied, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

Stop Sequence - The stop frame is indicated by SDA going HIGH when SCL is HIGH. A stop frame frees the bus to go to another part on the same bus or to another random register address.

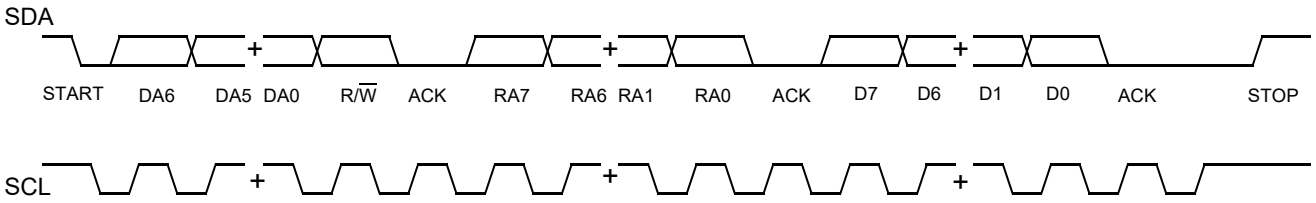
Figure 6. Start and Stop Frame



Acknowledge Pulse

During write mode the CY2545/CY2547 responds with an acknowledge pulse after every eight bits. Do this by pulling the SDA line LOW during the N × 9th clock cycle as illustrated in Figure 7 (N = the number of bytes transmitted). During read mode, the master generates the acknowledge pulse after reading the data packet.

Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (ack = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (ack = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write multiple bytes at a time, the master does not end the write sequence with a STOP condition; instead, the master sends multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, the same as after the first byte, and accepts data until the STOP condition responds to the acknowledge bit. When receiving multiple bytes, the CY2545 and CY2547 internally increment the register address.

Read Operations

Read operations are initiated the same way as write operations except that the R/W bit of the slave address is set to '1' (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY2545 and CY2547 have an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word 'n', then a current address read operation returns the value stored in location 'n+1'. When the CY2545/CY2547 receive the slave address with the R/W bit set to a '1', the CY2545/CY2547 issue an acknowledge and transmit the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the CY2545/CY2547 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is done by sending the address to the CY2545/CY2547 as part of a write operation. After sending the word address, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to '1'. The CY2545/CY2547 then issue an acknowledge and transmit the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the CY2545/CY2547 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmitting the first 8-bit data word. This action increments the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master serially reads the entire contents of the slave device memory. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

Serial I^{2}C Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	µs
t_{LOW}	Low period of the SCLK clock	1.3	–	µs
t_{HIGH}	High period of the SCLK clock	0.6	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	µs
$t_{HD:DAT}$	Data hold time	100	–	ns
$t_{SU:DAT}$	Data setup time	100	–	ns
t_R	Rise time	–	300	ns
t_F	Fall time	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	µs

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage for CY2545		–0.5	4.5	V
V_{DD}	Supply voltage for CY2547		–0.5	2.6	V
$V_{DD\_CLK\_BX}$	Output bank supply voltage		–0.5	4.5	V
V_{IN}	Input voltage for CY2545	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
V_{IN}	Input voltage for CY2547	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature and storage	Nonfunctional	–65	+150	°C
ESD_{HBM}	ESD protection (human body model)	JEDEC EIA/JESD22-A114-E	2000		V
UL-94	Flammability rating	V-0 at1/8 in.	–	10	ppm
MSL	Moisture sensitivity level		3		

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	V_{DD} operating voltage for CY2545	2.25	–	3.60	V
V_{DD}	V_{DD} operating voltage for CY2547	1.65	1.8	1.95	V
$V_{DD\_CLK\_BX}$	Output driver voltage for bank 1, 2, and 3 for CY2545	1.43	–	3.60	V
	Output driver voltage for bank 1, 2, and 3 for CY2547	1.43	–	1.98	V
T_{AC}	Commercial ambient temperature	0	–	+70	°C
T_{AI}	Industrial ambient temperature	–40	–	+85	°C
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low voltage	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output high voltage	I_{OH} = –2 mA, drive strength = [00]	$V_{DD\_CLK\_BX}$ – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{OLSD}	Output low voltage, SDA	I_{OL} = 4 mA	–	–	0.4	V
V_{IL1}	Input low voltage of PD#/OE, RST, FS, and SSON		–	–	0.2 × V_{DD}	V
V_{IL2}	Input low voltage of CLKIN for CY2545		–	–	0.2 × V_{DD}	V
V_{IL3}	Input low voltage of EXCLKIN for CY2545		–	–	0.3	V
V_{IL4}	Input low voltage of CLKIN, EXCLKIN for CY2547		–	–	0.2 × V_{DD}	V
V_{IH1}	Input high voltage of PD#/OE, RST, FS, and SSON		0.8 × V_{DD}	–	–	V
V_{IH2}	Input high voltage of CLKIN for CY2545		0.8 × V_{DD}	–	–	V
V_{IH3}	Input high voltage of EXCLKIN for CY2545		1.62	–	2.2	V
V_{IH4}	Input high voltage of CLKIN, EXCLKIN for CY2547		0.8 × V_{DD}	–	–	V
I_{ILPD}	Input low current of RST and PD#/OE	V_{IL} = 0 V	–	–	10	µA
I_{IHPD}	Input high current of RST and PD#/OE	V_{IH} = V_{DD}	–	–	10	µA
I_{ILSR}	Input low current of SSON and FS	V_{IL} = 0 V (Internal pull-down = 160 k typ)	–	–	10	µA
I_{IHSR}	Input high current of SSON and FS	V_{IH} = V_{DD} (Internal pull-down = 160 k typ)	14	–	36	µA
R_{DN}	Pull-down resistor of (CLK1-CLK8) when off, CLK6/SSON and CLK3/FS		100	160	250	kΩ
I_{DD}[1, 2]	Supply current for CY2547	PD# = high, no load	–	20	–	mA
	Supply current for CY2545	PD# = high, no load	–	22	–	mA
I_{DDS}[1]	Standby current	PD# = low, no load, with I^2C circuit not in keep alive mode	–	3	–	µA
I_{PD}[1]	Power-down current	PD# = low, no load, with I^2C circuit in keep alive mode	–	–	1	mA
C_{IN}[1]	Input capacitance	SSON, RST, PD#/OE or FS inputs	–		7	pF

Notes
1. Guaranteed by design but not 100% tested.
2. Configuration dependent.

AC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{IN} (crystal)	Crystal frequency, XIN		8	–	48	MHz
F_{IN} (clock)	Input clock frequency	Clock inputs CLKIN or EXCLKIN	8	–	166	MHz
F_{CLK}	Output clock frequency	CY2545 ($V_{DD\_CLK\_Bx}$ = 2.5 V, 3.0 V, 3.3 V) and CY2547	3	–	166	MHz
		CY2545 ($V_{DD\_CLK\_Bx}$ = 1.8 V)	3	–	50	MHz
DC1	Output duty cycle, all clocks except ref out	Duty cycle is defined in Figure 9; t_1/t_2, measured 50% of V_{DD}	45	50	55	%
DC2	Ref out clock duty cycle	Ref In Min 45%, Max 55%	40	–	60	%
T_{RF1}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 10, C_{LOAD} = 15 pF, Drive strength [00]	–	6.8	–	ns
T_{RF2}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 10, C_{LOAD} = 15 pF, Drive strength [01]	–	3.4	–	ns
T_{RF3}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 10, C_{LOAD} = 15 pF, Drive strength [10]	–	2.0	–	ns
T_{RF4}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 10, C_{LOAD} = 15 pF, Drive strength [11]	–	1.0	–	ns
T_{CCJ}[3, 4]	Cycle-to-cycle jitter max (Pk-Pk)	Configuration dependent. See Configuration Example	–	150	–	ps
T_{LOCK}[3]	PLL lock time	Measured from 90% of the applied power supply level	–	1	3	ms

Configuration Example

For C-C Jitter

Ref. Freq. (MHz)	CLK1 Output		CLK2 Output		CLK3 Output		CLK4 Output		CLK5 Output	
	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)
14.3181	8.0	134	166	103	48	92	74.25	81	Not used	
19.2	74.25	99	166	94	8	91	27	110	48	75
27	48	67	27	109	166	103	74.25	97	Not used	
48	48	93	27	123	166	137	166	138	8	103

Notes
3. Guaranteed by design but not 100% tested.
4. Configuration dependent.

Recommended Crystal Specification

For SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum frequency	8	14	28	MHz
Fmax	Maximum frequency	14	28	48	MHz
R1	Motional resistance (ESR)	135	50	30	Ω
C0	Shunt capacitance	4	4	2	pF
CL	Parallel load capacitance	18	14	12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

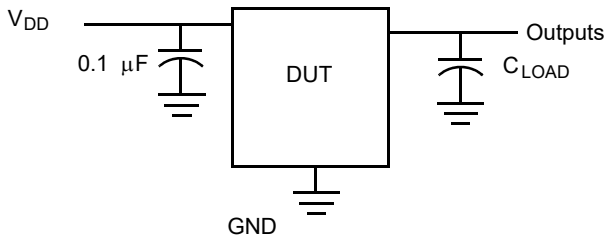
Recommended Crystal Specification

For Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum frequency	8	14	24	MHz
Fmax	Maximum frequency	14	24	32	MHz
R1	Motional resistance (ESR)	90	50	30	Ω
C0	Shunt capacitance	7	7	7	pF
CL	Parallel load capacitance	18	12	12	pF
DL(max)	Maximum crystal drive level	1000	1000	1000	µW

Test and Measurement Setup

Figure 8. Test and Measurement Setup



Voltage and Timing Definitions

Figure 9. Duty Cycle Definition

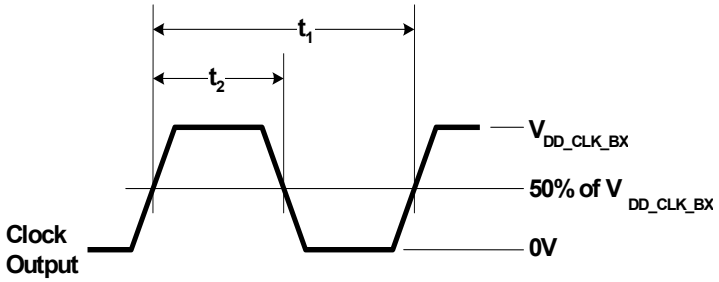
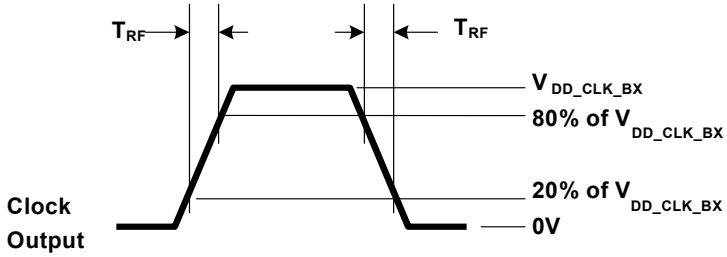


Figure 10. Rise Time = T_{RF}, Fall Time = T_{RF}



Ordering Information

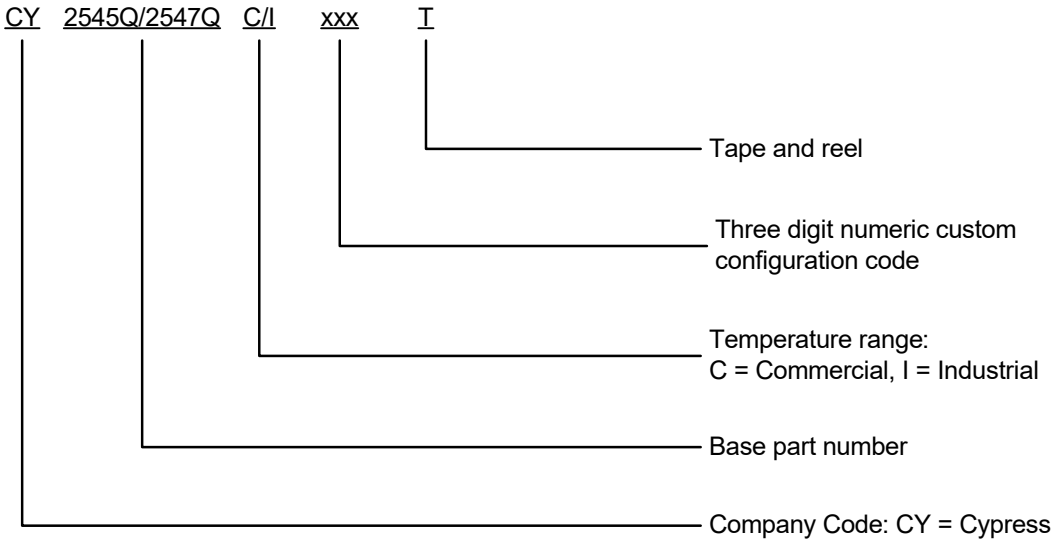
Part Number	Type	Package	Supply Voltage (V_{DD})	Production Flow
Pb-free				
CY2547QI	Field Programmable	24-pin QFN	1.8 V	Industrial, –40 °C to +85 °C
CY2547QIT	Field Programmable	24-pin QFN – Tape and Reel	1.8 V	Industrial, –40 °C to +85 °C

Products are also offered as factory programmed customer specific devices with customized part numbers. The Possible Configurations shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

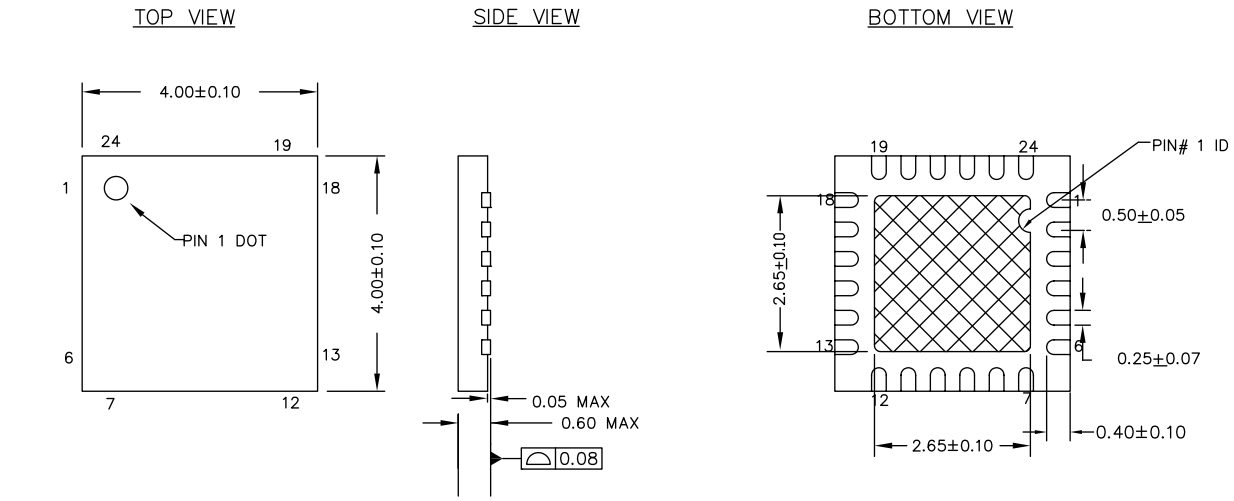
Part Number	Type	Package	Supply Voltage (V_{DD})	Production Flow
Pb-free				
CY2545QCxxx	Factory Configured	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to +70 °C
CY2545QCxxxT	Factory Configured	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to +70 °C
CY2547QCxxx	Factory Configured	24-pin QFN	1.8 V	Commercial, 0 °C to +70 °C
CY2547QCxxxT	Factory Configured	24-pin QFN – Tape and Reel	1.8 V	Commercial, 0 °C to +70 °C
CY2545QIxxx	Factory Configured	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2545QIxxxT	Factory Configured	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2547QIxxx	Factory Configured	24-pin QFN	1.8 V	Industrial, –40 °C to +85 °C
CY2547QIxxxT	Factory Configured	24-pin QFN – Tape and Reel	1.8 V	Industrial, –40 °C to +85 °C

Ordering Code Definitions



Package Diagram

Figure 11. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A (2.65 × 2.65 E-Pad (Sawn)) Package Outline, 001-13937



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
I^2C	Inter Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
PLL	Phase-Locked Loop
QFN	Quad Flat No-lead

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Units of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
µs	microsecond
µW	microwatt
mA	milliampere
ms	millisecond
ns	nanosecond
W	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2545/CY2547, Quad-PLL Programmable Spread Spectrum Clock Generator with Serial I²C Interface Document Number: 001-13196				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	870780	RGL / AESA	03/23/2007	New data sheet.
*A	1504843	RGL / AESA	10/03/2007	Replaced V_{DD_CORE} with V_{DD} in all instances across the document. Updated Serial I2C Programming Interface Timing Specifications: Changed minimum value of t_{SU} parameter from 100 ns to 250 ns. Updated Absolute Maximum Conditions: Replaced “MIL-STD-883, Method 3015” with “JEDEC EIA/JESD22-A114-E” in “Conditions” column of ESD_{HBM} parameter. Updated Recommended Operating Conditions: Updated all details of V_{DD} parameter (Combined three rows into one row for CY2545).
*B	2899681	CXQ	03/26/2010	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85203 – Changed revision from *A to *B.
*C	3302754	CXQ	07/05/2011	Added Ordering Code Definitions under Ordering Information. Added Acronyms and Units of Measure. Updated to new template.
*D	4401186	AJU	06/06/2014	Updated Package Diagram: spec 51-85203 – Changed revision from *B to *D. Updated to new template. Completing Sunset Review.
*E	4586478	TAVA	12/03/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Serial I2C Programming Interface Protocol and Timing: Updated Figure 4 (Updated the last ACK in SDA Read-Current Address Read and SDA Read-Multiple Contiguous Registers to “NACK”).
*F	5140921	TAVA	03/14/2016	Updated Serial I2C Programming Interface Protocol and Timing: Updated Data Valid: Updated Figure 5. Updated Serial I2C Programming Interface Timing Specifications: Updated all details. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated Package Diagram: Removed spec 51-85203 *D. Added spec 001-13937 *F. Updated to new template.
*G	5475518	BPIN	10/14/2016	Updated Ordering Information: Updated part numbers. Updated to new template.

Document History Page (continued)

Document Title: CY2545/CY2547, Quad-PLL Programmable Spread Spectrum Clock Generator with Serial I²C Interface Document Number: 001-13196				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	5778174	PSR	06/19/2017	Updated Features: Added one-time programmability. Updated Pin Definitions: Updated details in “Description” column corresponding to pin numbers 2, 6, 11, 13, 17, and 20. Updated Pin Definitions: Updated details in “Description” column corresponding to pin numbers 2, 6, 11, 13, 17, and 20. Updated Functional Overview: Added Output Driver Supply and Multi-Function Input Restriction. Updated to new template.
*I	5955034	XHT	11/02/2017	Updated DC Electrical Specifications: Updated details in “Max” column corresponding to V_{IL2}, V_{IL3}, and V_{IL4} parameters. Updated details in “Min” column corresponding to V_{IH2}, and V_{IH4} parameters. Updated to new template.

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