MOSFET

SIPMOS® Small-Signal-Transistor

SC59-3

Features

- P-Channel
- Enhancement mode / Logic level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- Footprint compatible to SOT23
- Halogen free according to IEC61249-2-21

Product validation

Qualified according to AEC Q101

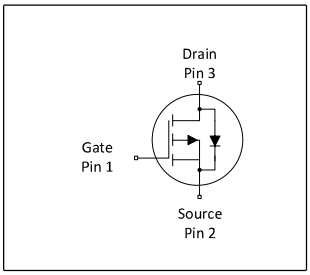


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-100	V
$R_{DS(on),max}$	1.8	Ω
I_D	-0.36	A

Type / Ordering Code	Package	Marking	Related Links
BSR316P	PG-SC59-3	LC	-

Table of Contents

1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	-0.36 -0.29	A	T_A=25 °C T_A=70 °C
Pulsed drain current	$I_{D,pulse}$	-	-	-1.44	A	T_A=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	25	mJ	I_D=-0.36 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	0.5	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56
ESD class	-	-	1A (250V to 500V)	-	-	JESD22-A114-HBM
Soldering temperature	-	-	260 °C	-	-	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - ambient, minimal footprint, steady state	R_{thJA}	-	-	250	K/W	-

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-100	-	-	V	V_{GS}=0 V, I_D=-250 µA
Gate threshold voltage	$V_{GS(th)}$	-2	-1.5	-1	V	V_{DS}=V_{GS}, I_D=-170 µA
Zero gate voltage drain current	I_{DSS}	- -	-0.1 -10	-1 -100	µA	V_{DS}=-100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-100 V, V_{GS}=0 V, T_j=150 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.8 1.3	2.2 1.8	Ω	V_{GS}=-4.5 V,I_D=-0.33 A V_{GS}=-10 V,I_D=-0.36 A
Transconductance	g_{fs}	0.3	0.5	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-0.29 A

Table 5 Dynamic characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	124	165	pF	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz
Output capacitance	C_{oss}	-	25	33	pF	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	13	20	pF	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5	8	ns	V_{DD}=-50 V, V_{GS}=-10 V, I_D=-0.36 A, $R_{G,ext}$=6 Ω
Rise time	t_r	-	6	9	ns	V_{DD}=-50 V, V_{GS}=-10 V, I_D=-0.36 A, $R_{G,ext}$=6 Ω
Turn-off delay time	$t_{d(off)}$	-	71	106	ns	V_{DD}=-50 V, V_{GS}=-10 V, I_D=-0.36 A, $R_{G,ext}$=6 Ω
Fall time	t_f	-	26	39	ns	V_{DD}=-50 V, V_{GS}=-10 V, I_D=-0.36 A, $R_{G,ext}$=6 Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.3	0.4	nC	V_{DD}=-80 V, I_D=-0.36 A, V_{GS}=0 to -10 V
Gate to drain charge	Q_{gd}	-	1.6	2.4	nC	V_{DD}=-80 V, I_D=-0.36 A, V_{GS}=0 to -10 V
Gate charge total	Q_g	-	5.3	7.0	nC	V_{DD}=-80 V, I_D=-0.36 A, V_{GS}=0 to -10 V
Gate plateau voltage	$V_{plateau}$	-	-2.7	-	V	V_{DD}=-80 V, I_D=-0.36 A, V_{GS}=0 to -10 V

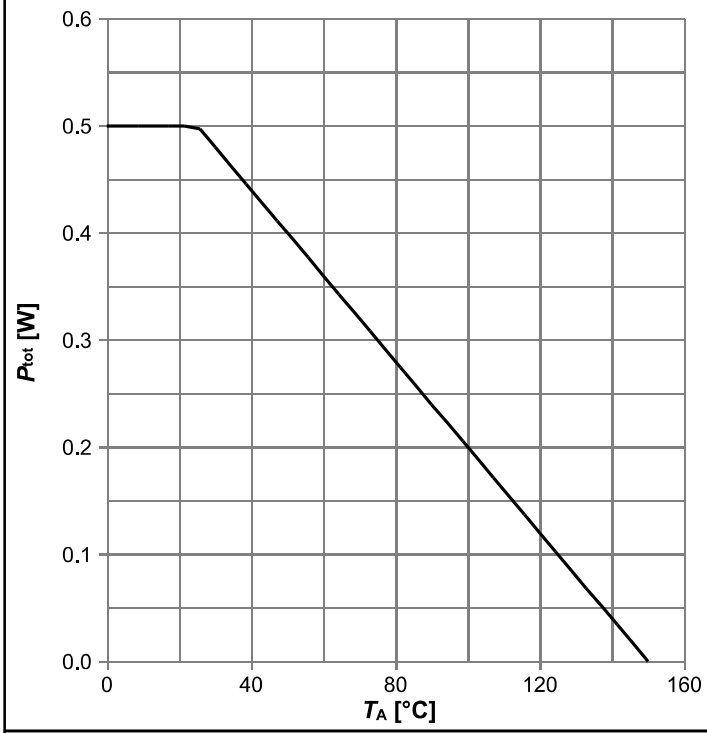
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-0.36	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-1.44	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-0.8	-1.1	V	V_{GS}=0 V, I_F=0.36 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	40.6	-	ns	V_R=-50 V, I_F=|I_S|, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	46.4	-	nC	V_R=-50 V, I_F=|I_S|, di_F/dt=100 A/µs

[1)] >Defined by design. Not subjected to production test

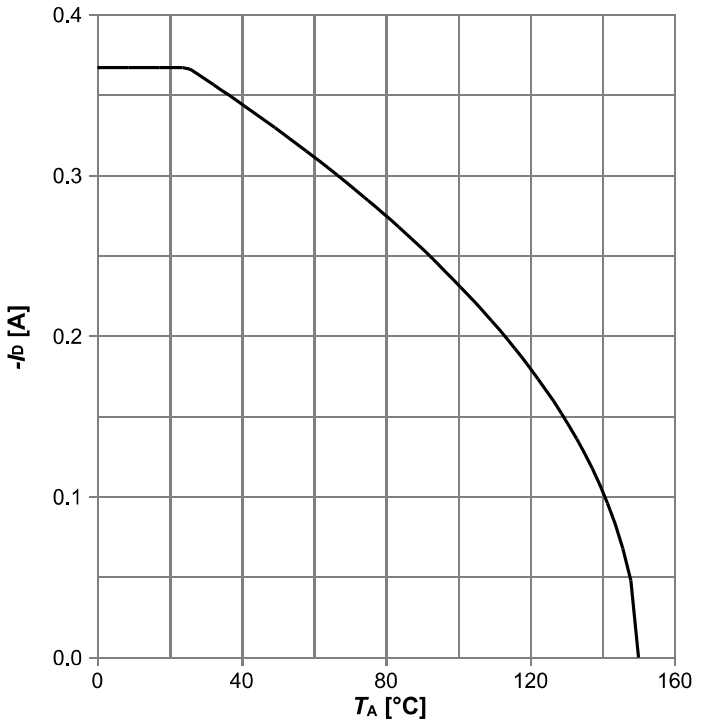
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



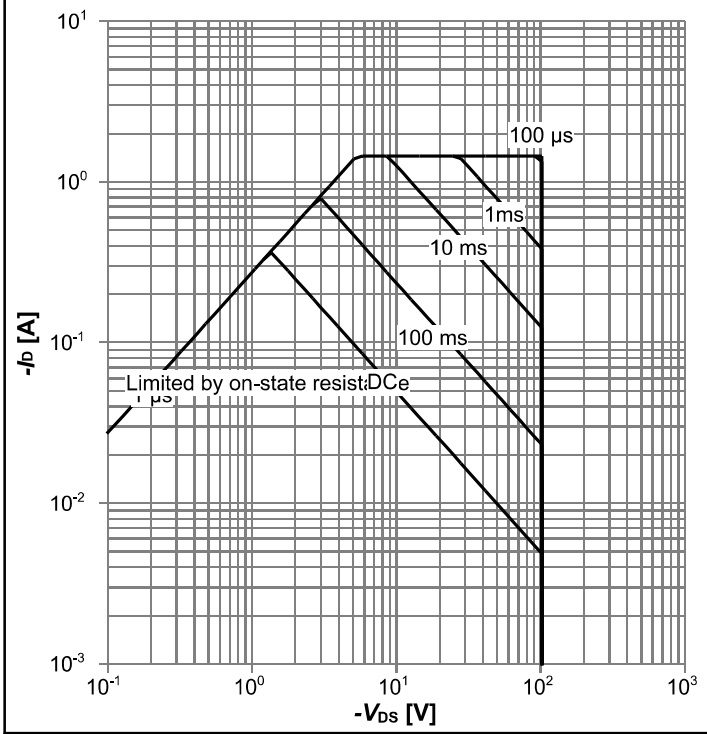
$P_{tot}=f(T_C)$

Diagram 2: Drain current



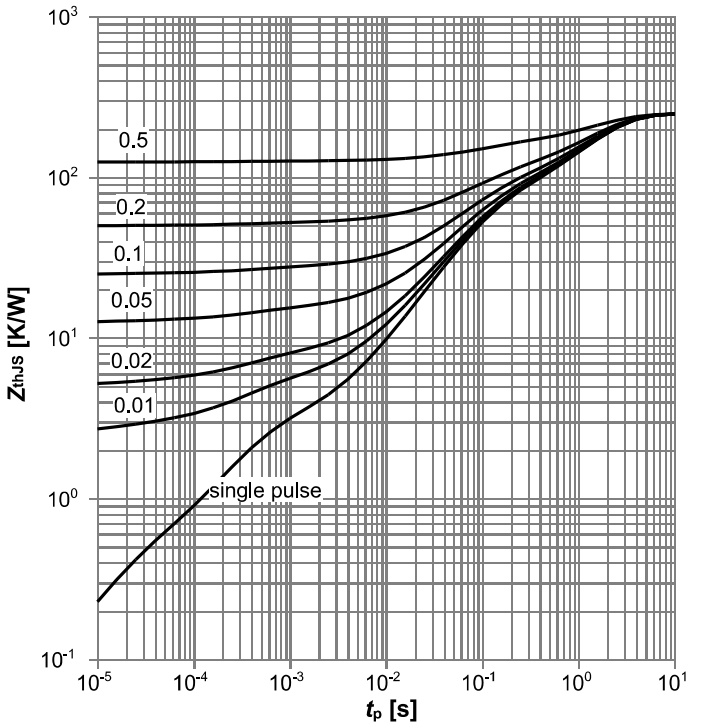
$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V

Diagram 3: Safe operating area



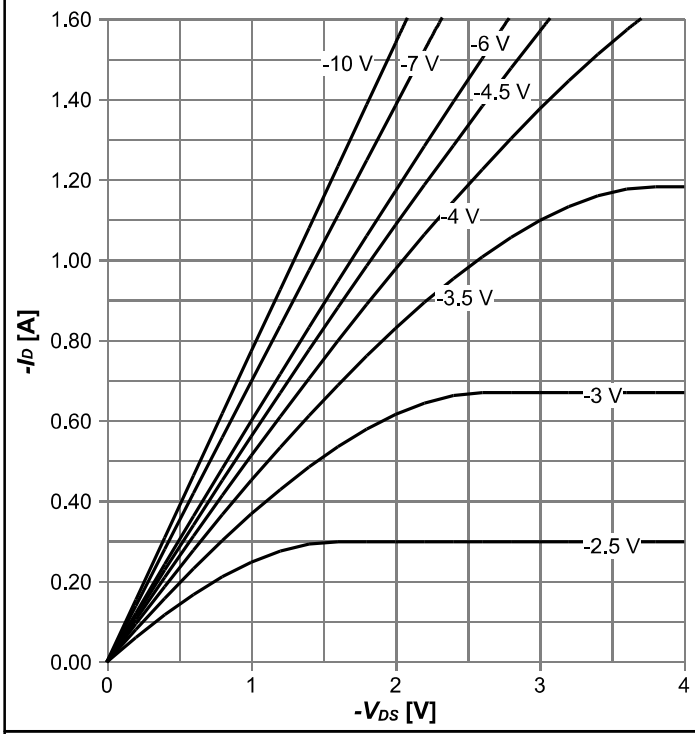
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



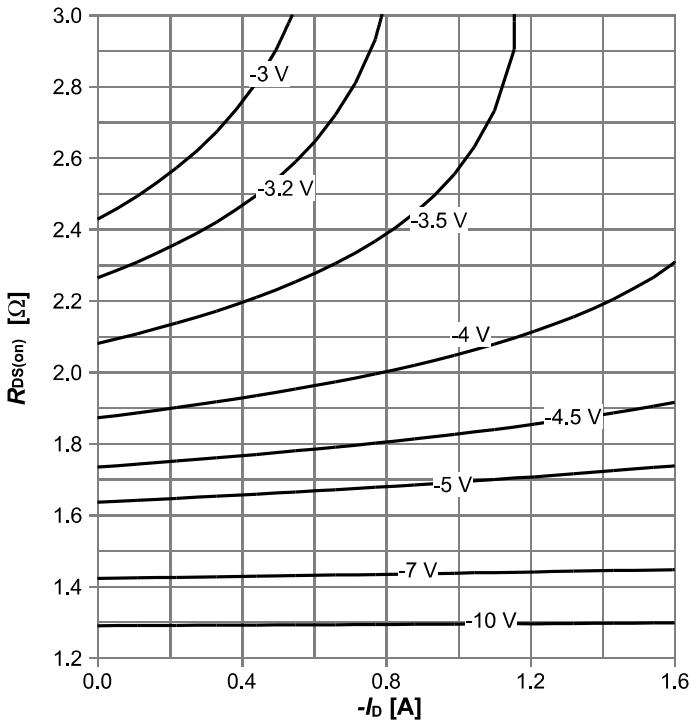
$Z_{thJA}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



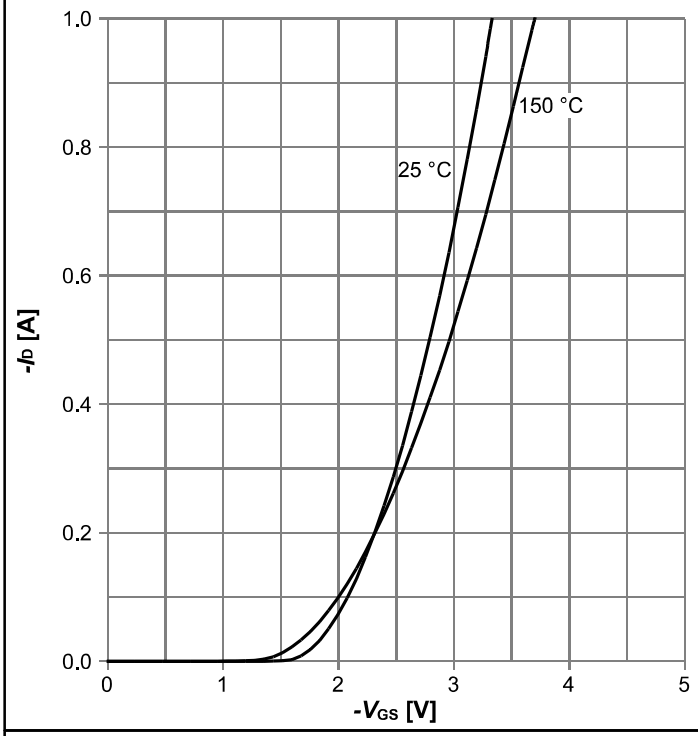
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



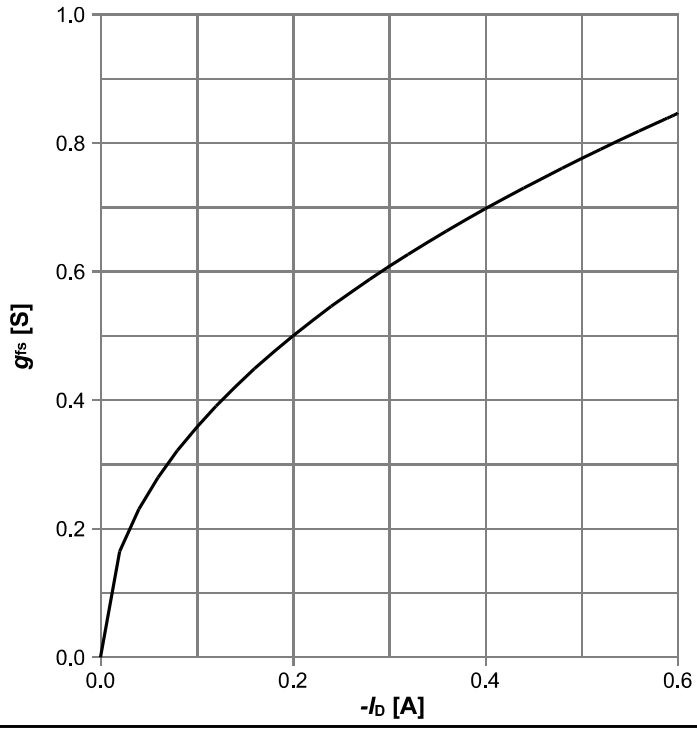
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



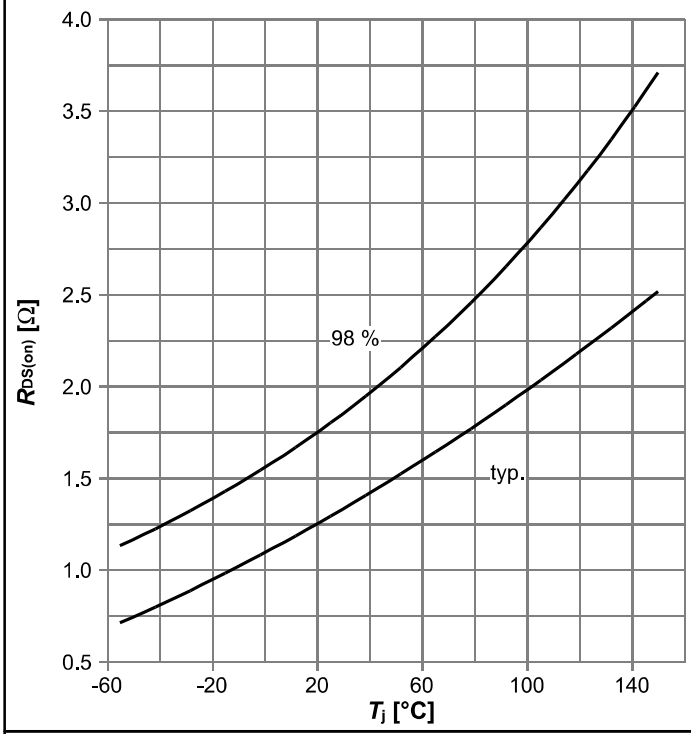
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



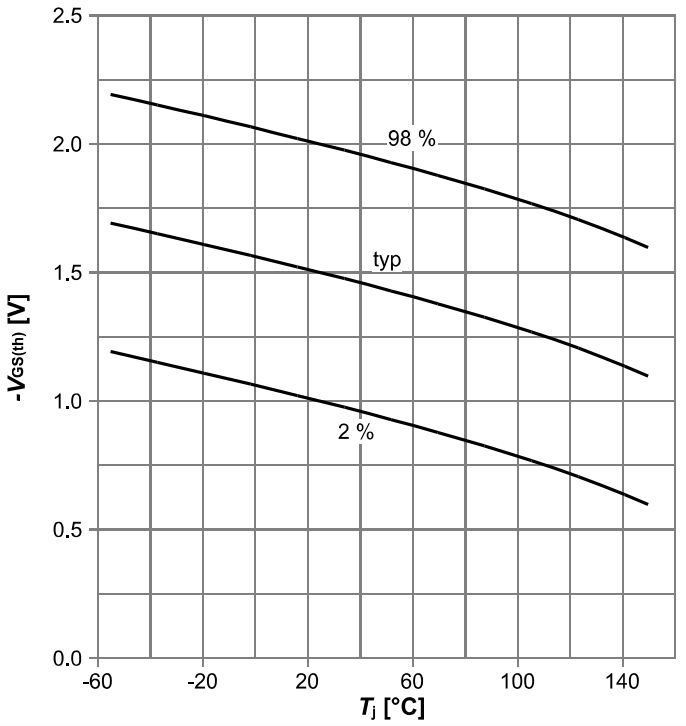
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



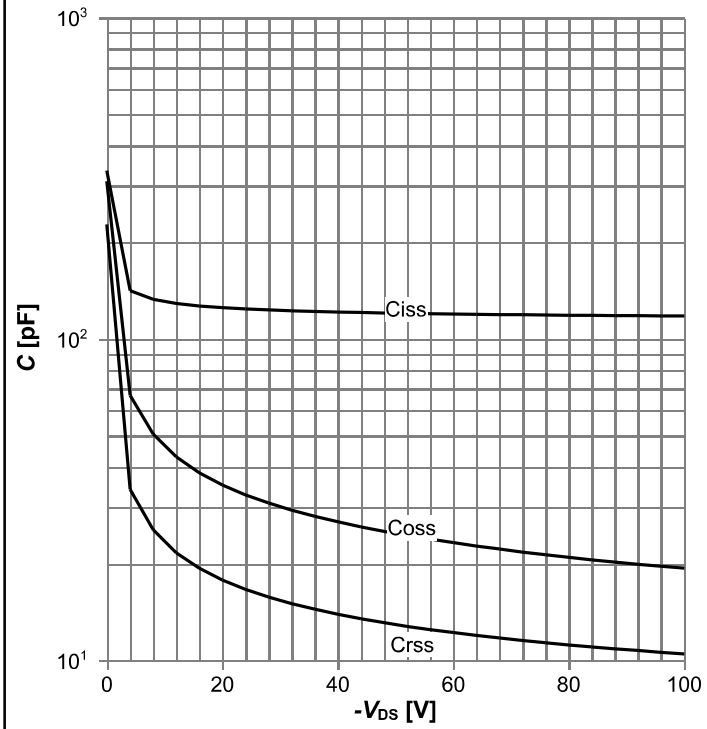
$R_{DS(on)}$=f(T_j); I_D=-0.36 A; V_{GS}=-10 V

Diagram 10: Typ. gate threshold voltage



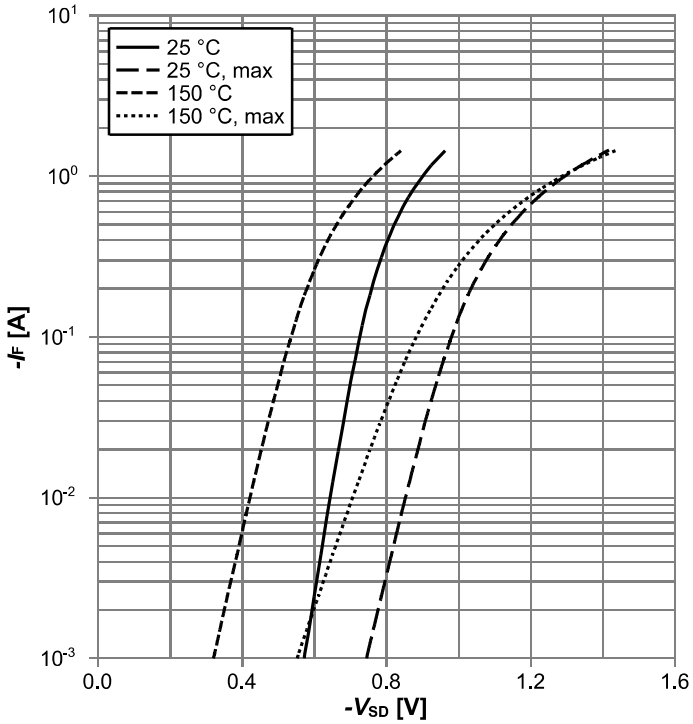
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=-170 µA

Diagram 11: Typ. capacitances



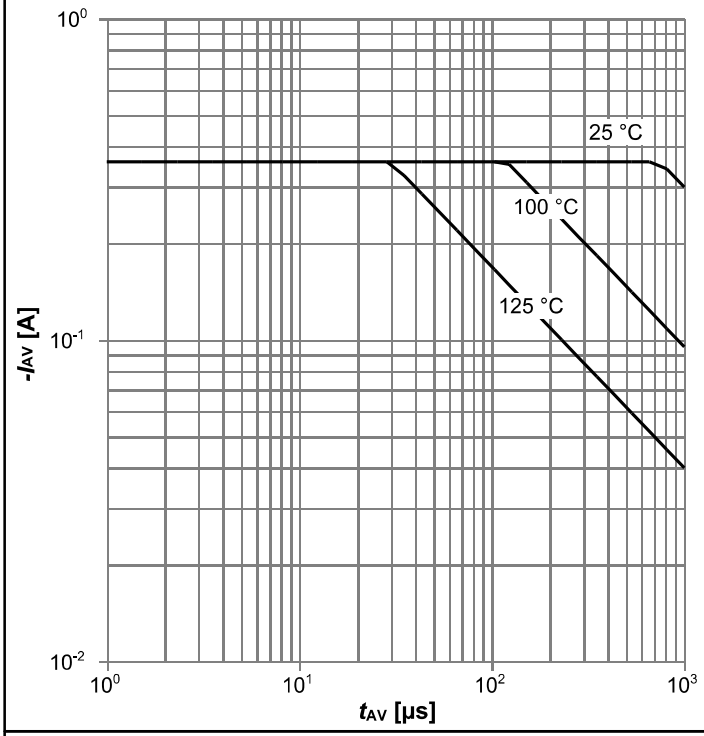
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



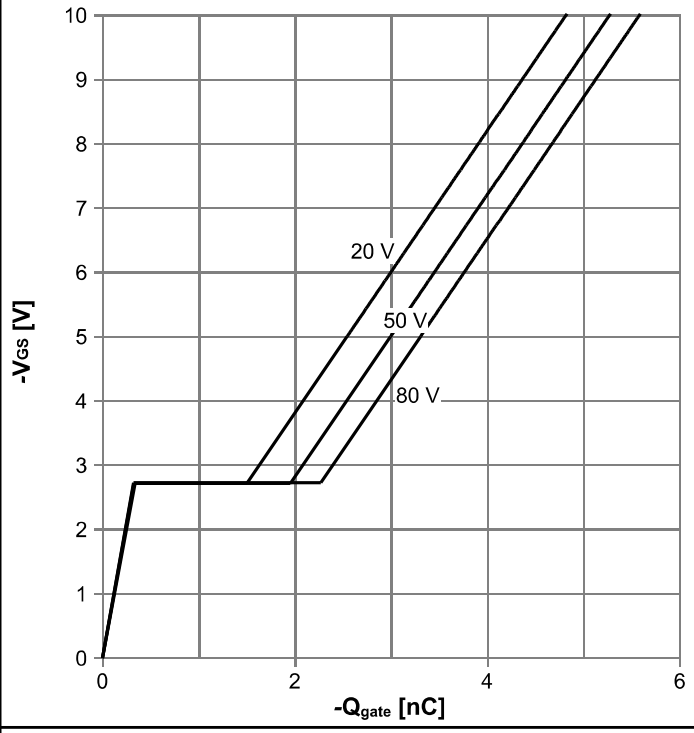
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



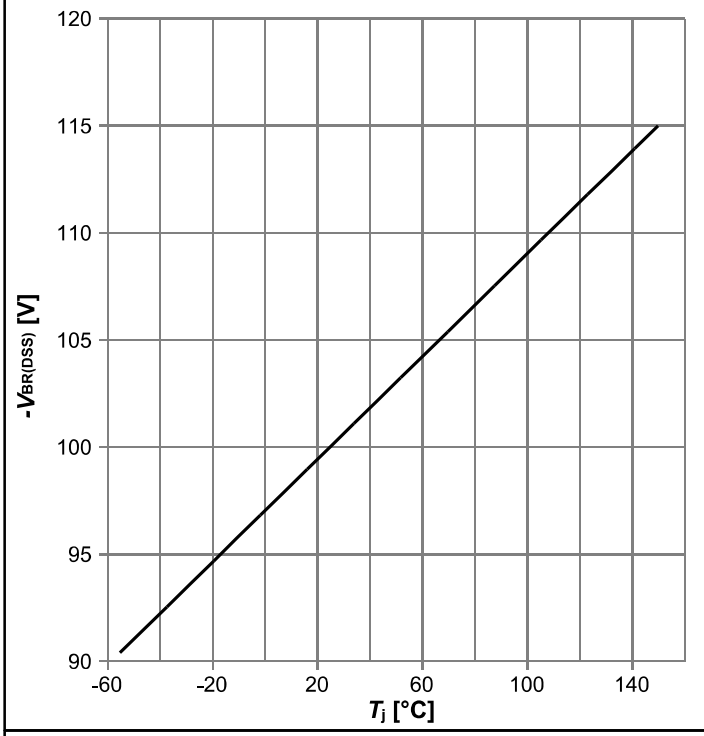
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



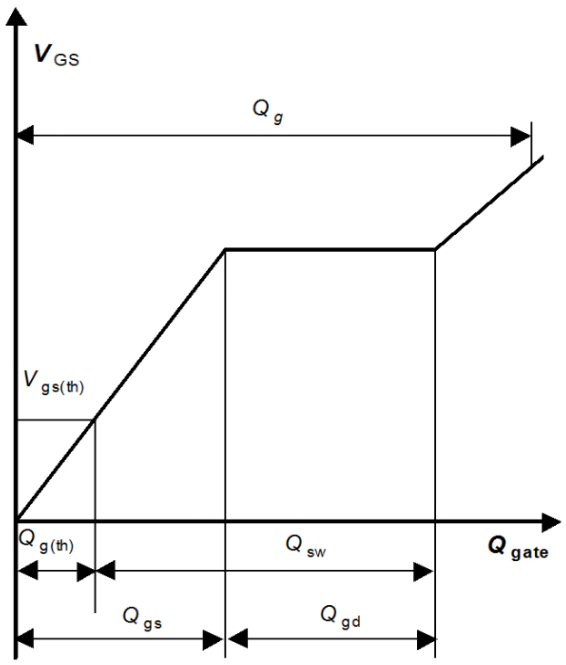
V_{GS}=f(Q_{gate}); I_D=-0.36 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



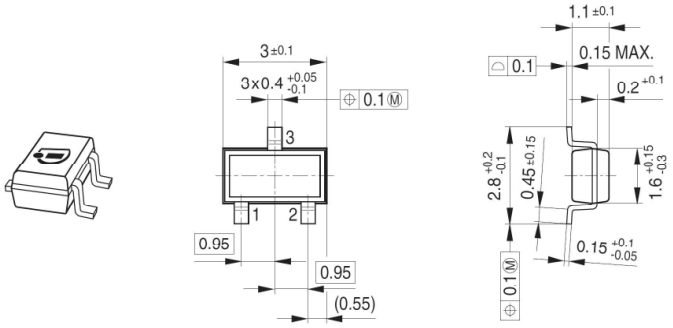
$V_{BR(DSS)}$=f(T_j); I_D=-250 µA

Diagram Gate charge waveforms



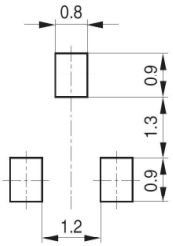
5 Package Outlines

Package Outline

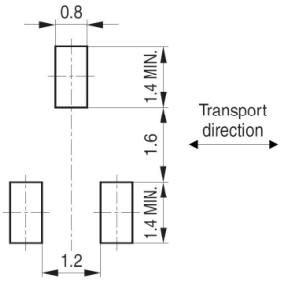


Foot Print

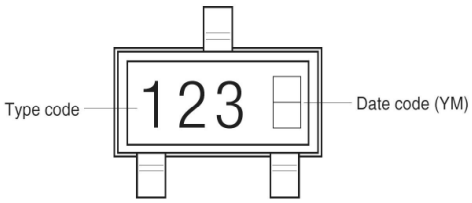
Soldering Type: Reflow Soldering



Soldering Type: Wave Soldering



Marking Layout



Tape and Reel

Reel ø180 mm: 3.000 Pieces/Reel
Reels/Box: 1 x 3.000 = 3.000

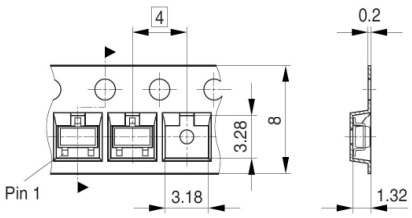


Figure 1 Outline PG-SC59-3, dimensions in mm/inches

Revision History

BSR316P

Revision: 2021-05-27, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2020-11-10	Breakdown voltage max to min
2.1	2021-05-27	Update schematic and legend Diagram 4

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