

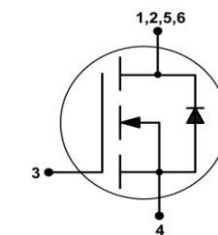
OptiMOS™ -3 Small-Signal-Transistor

Features

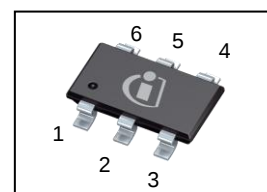
- N-channel
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100%lead-free; Halogen-free; RoHS compliant



Halogen-Free



PG-TSOP-6



Type	Package	Tape and Reel Info	Marking	Halogen-free	Package
BSL606SN	PG-TSOP-6	H6327: 3000 pcs/reel	sPW	Yes	Non-dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	4.5	A
		$T_A=70\text{ °C}$	3.6	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	18.1	
Avalanche energy, single pulse	E_{AS}	$I_D=4.5\text{ A}$, $R_{GS}=25\text{ }\Omega$	14	mJ
Reverse diode dv/dt	dv/dt	$I_D=4.5\text{ A}$, $V_{DS}=16\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
Power dissipation ¹⁾	P_{tot}	$T_A=25\text{ °C}$	2.0	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	°C
ESD Class		JESD22-A114 -HBM	class 0 (<250V)	
Soldering Temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

SMD version, device on PCB	R_{thJA}	@6cm ² cooling area ¹⁾	-	-	62.5	
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Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=0\text{ V}$, $I_D=15\text{ }\mu\text{A}$	1.3	1.8	2.3	
Drain-source leakage current	I_{DSS}	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$, $I_D=3.6\text{ A}$	-	69	95	m Ω
		$V_{GS}=10\text{ V}$, $I_D=4.5\text{ A}$	-	49	60	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=3.6\text{ A}$		7.1	-	S

¹⁾ Performed on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air; $t \leq 5\text{ sec}$.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	494	657	pF
Output capacitance	C_{oss}		-	131	174	
Reverse transfer capacitance	C_{rss}		-	10.2	15.3	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=4.5\text{ A}, R_{G,ext}=6\text{ }\Omega$	-	6.8	-	ns
Rise time	t_r		-	3.0	-	
Turn-off delay time	$t_{d(off)}$		-	18	-	
Fall time	t_f		-	3.1	-	

Gate Charge Characteristics

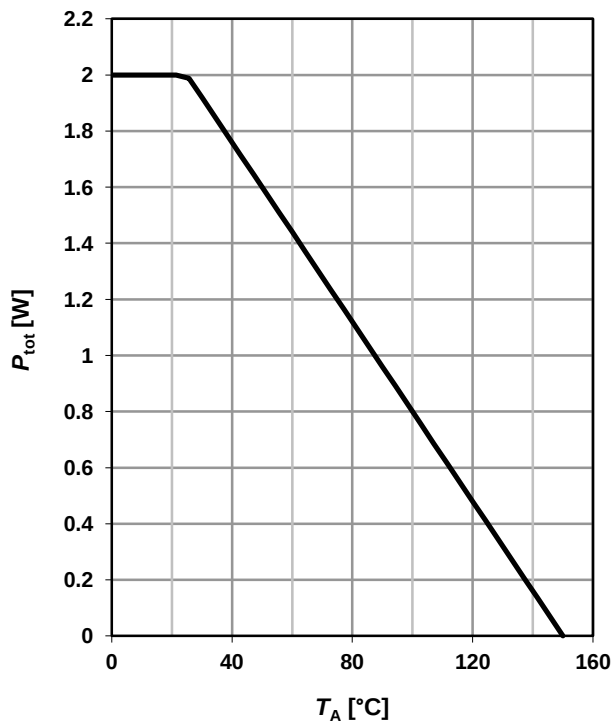
Gate to source charge	Q_{gs}	$V_{DD}=48\text{ V}, I_D=4.5\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	1.7	2.2	nC
Gate to drain charge	Q_{gd}		-	1.0	1.5	
Gate charge total	Q_g		-	3.7	5.6	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	0.9	A
Diode pulse current	$I_{S,pulse}$		-	-	18.1	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=4.5\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.1	V
Reverse recovery time	t_{rr}	$V_R=10\text{ V}, I_F=4.5\text{ A},$ $di_F/dt=200\text{ A}/\mu\text{s}$	-	21	-	ns
Reverse recovery charge	Q_{rr}		-	24	-	nC

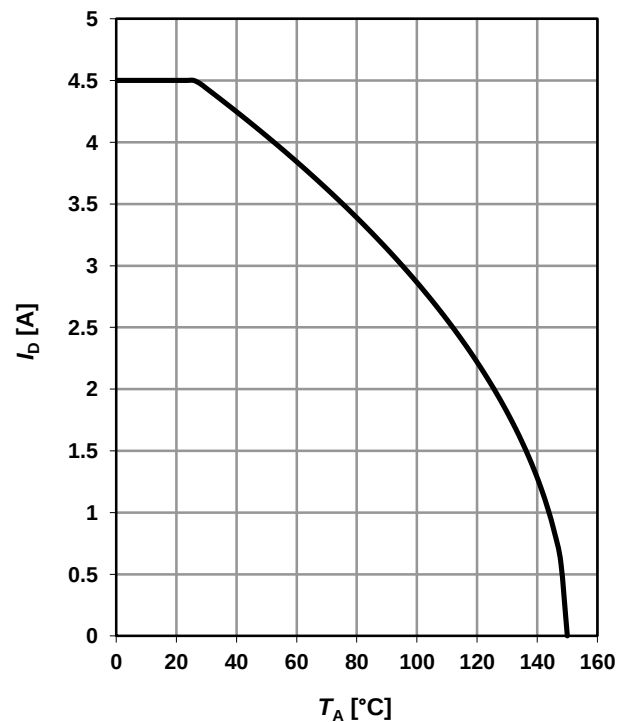
1 Power dissipation

$$P_{\text{tot}} = f(T_A)$$



2 Drain current

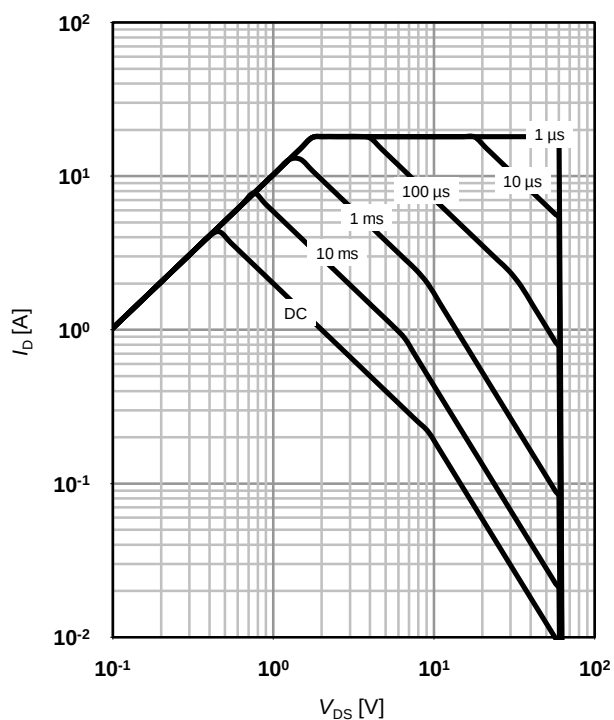
$$I_D = f(T_A); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_A = 25 \text{ °C}; D = 0$$

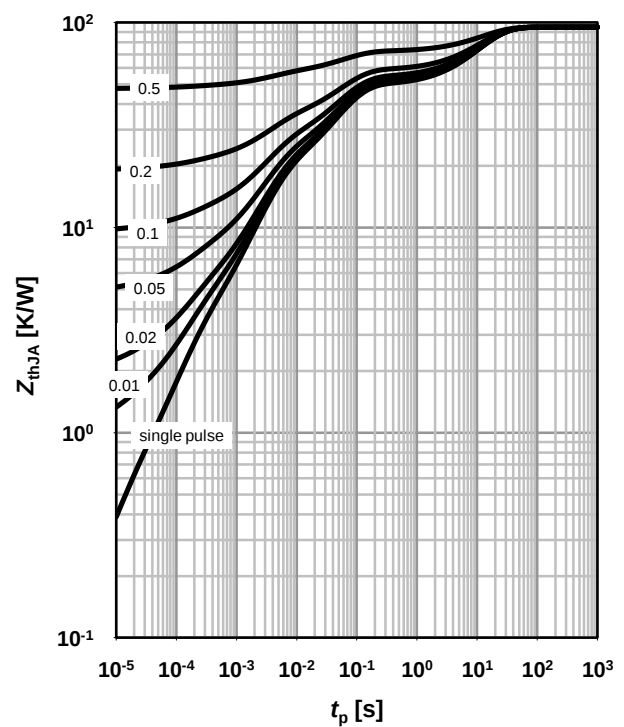
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJA}} = f(t_p)$$

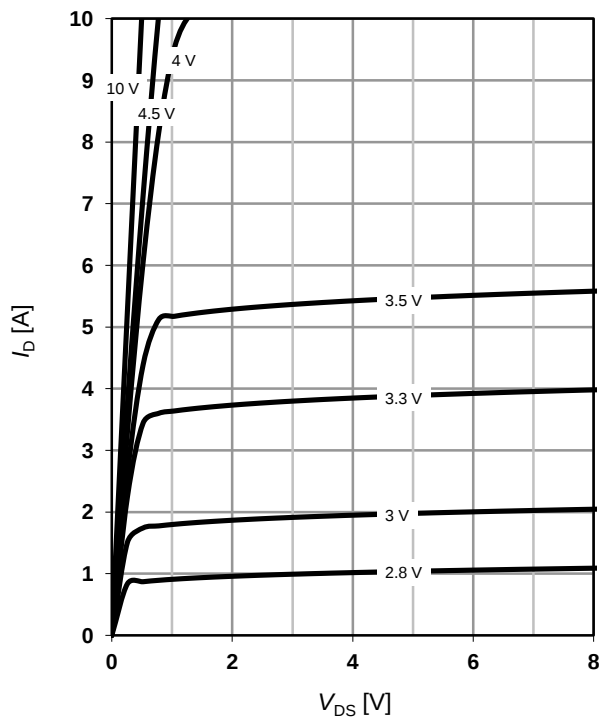
parameter: $D = t_p/T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

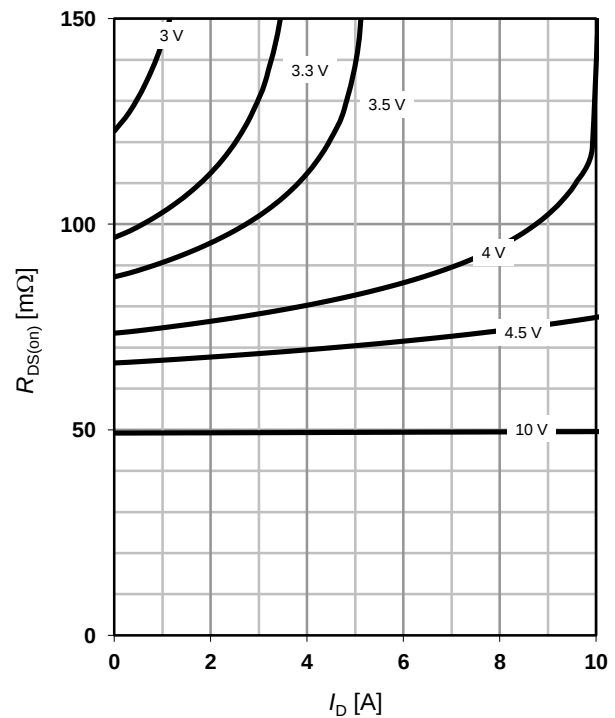
parameter: V_{GS}



6 Typ. drain-source on resistance

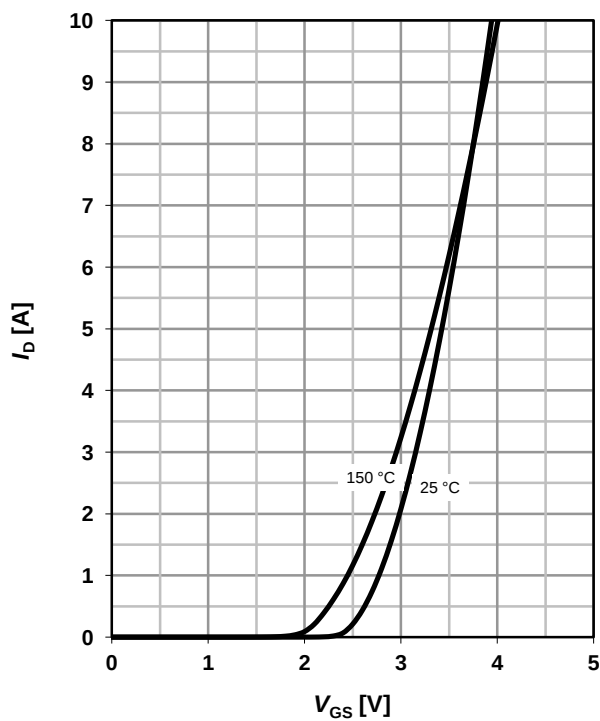
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

parameter: V_{GS}



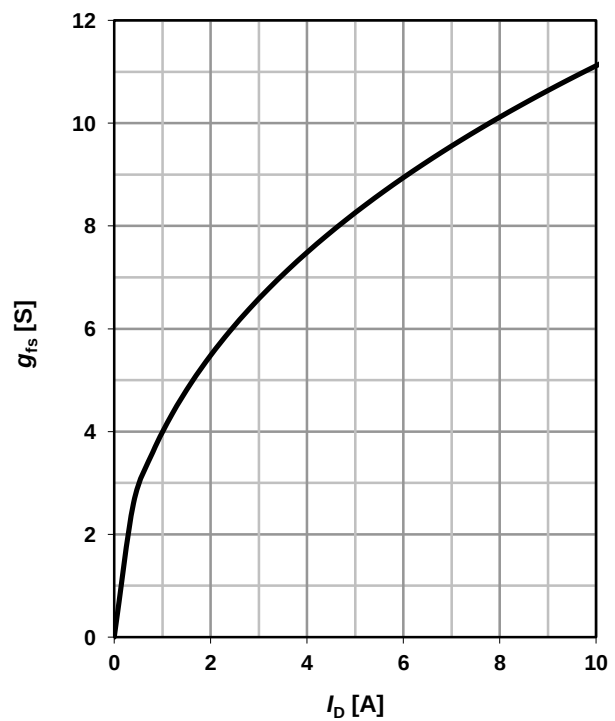
7 Typ. transfer characteristics

$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$



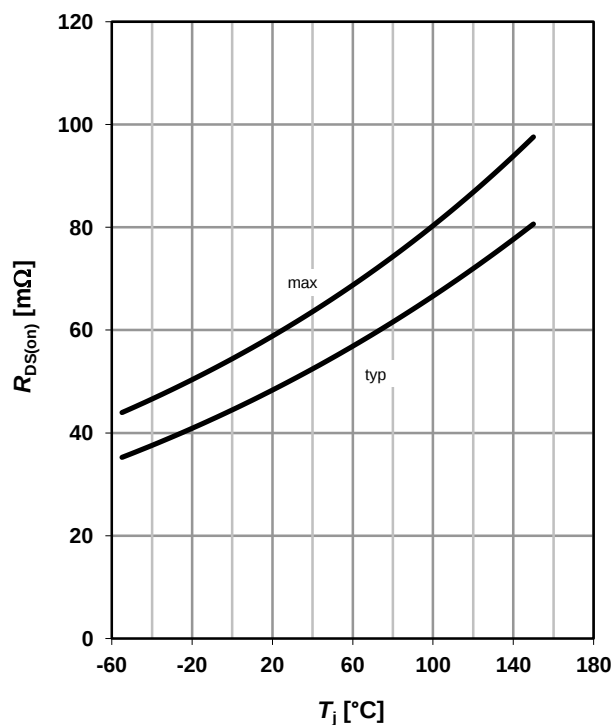
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



9 Drain-source on-state resistance

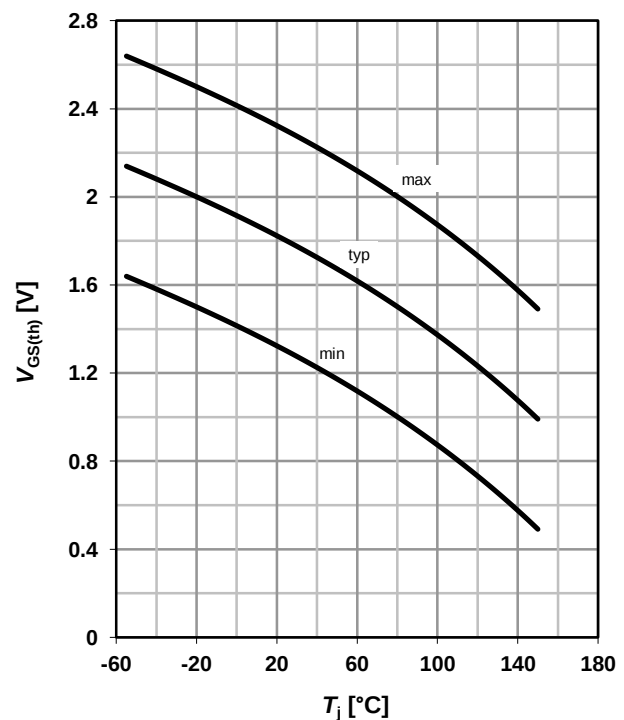
$$R_{DS(on)} = f(T_j); I_D = 4.5 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

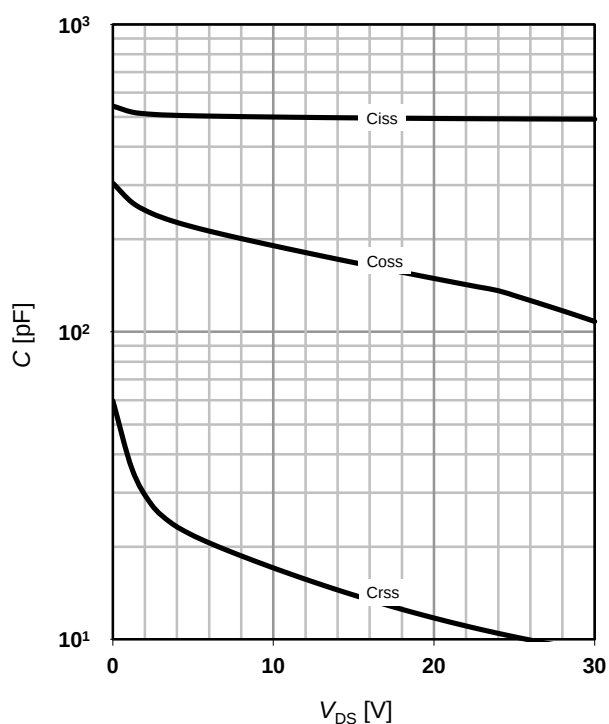
$$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 15 \mu\text{A}$$

parameter: I_D



11 Typ. capacitances

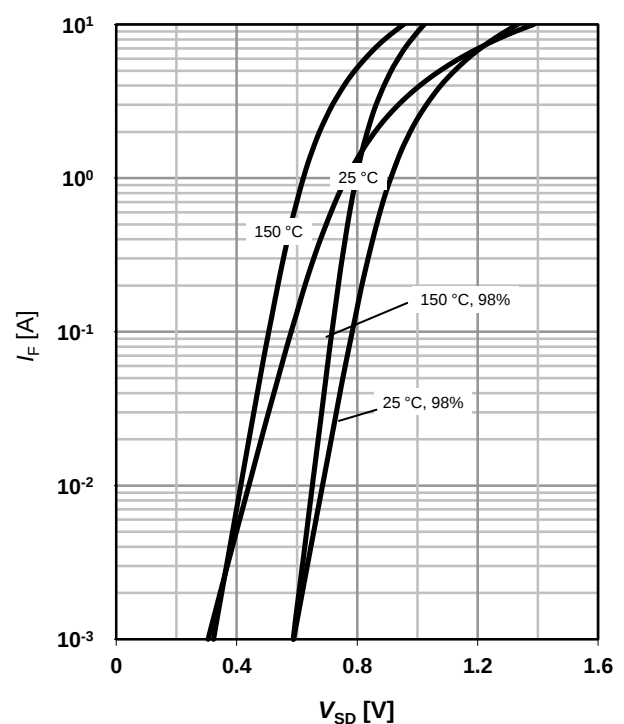
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ\text{C}$$



12 Forward characteristics of reverse diode

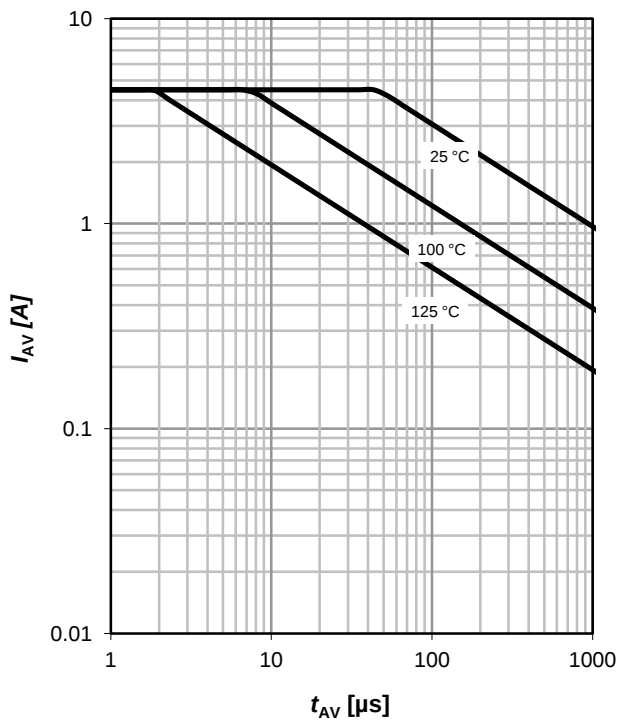
$$I_F = f(V_{SD})$$

parameter: T_j



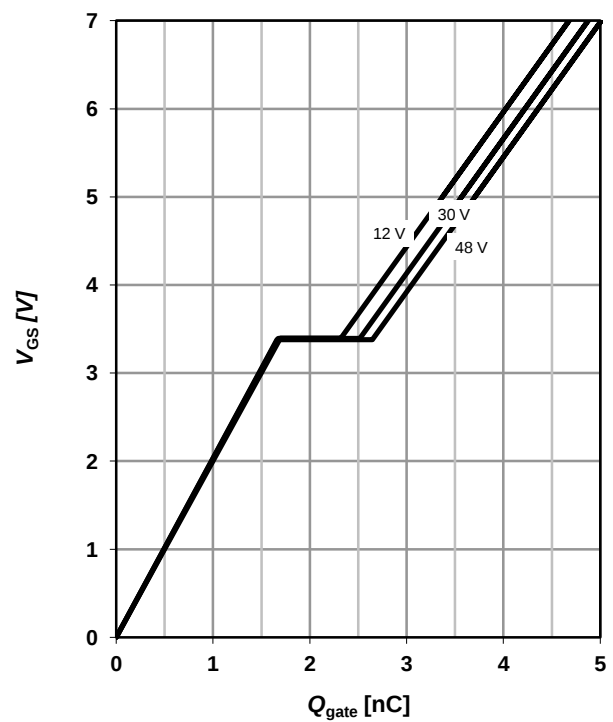
13 Avalanche characteristics

 $I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$

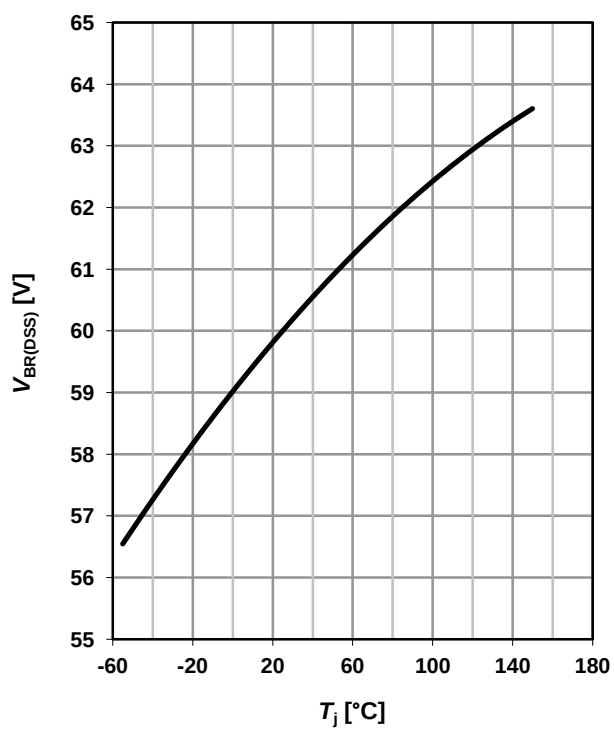
parameter: $T_{j(start)}$


14 Typ. gate charge

 $V_{GS}=f(Q_{gate}); I_D=4.5\text{ A pulsed}$

parameter: V_{DD}


15 Drain-source breakdown voltage

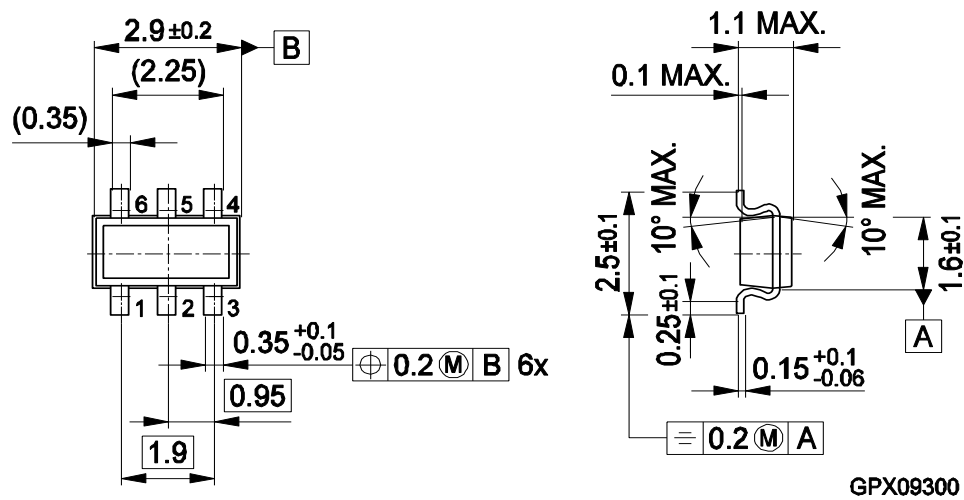
 $V_{BR(DSS)}=f(T_j); I_D=250\ \mu\text{A}$


16 Gate charge waveforms



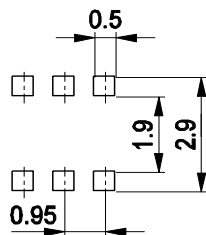
Package Outline:

TSOP-6



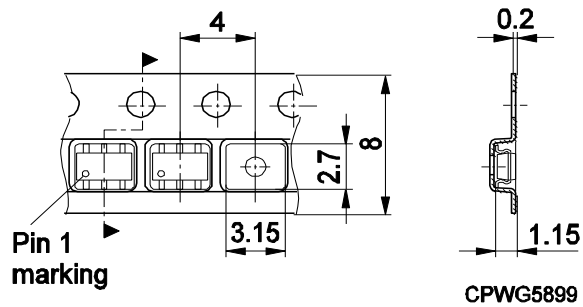
Footprint:

Packaging:



Remark: Wave soldering possible dep.
on customers process conditions

HLG09283



Dimensions in mm

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Infineon Technologies AG
81726 Munich, Germany
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