MOSFET

OptiMOS™ Power-MOSFET, 30 V

Features

- Optimized for high performance synchronous rectification
- Monolithically integrated schottky-like diode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
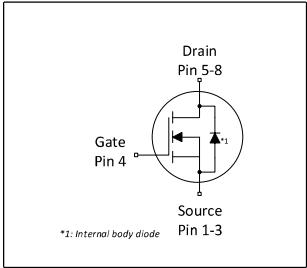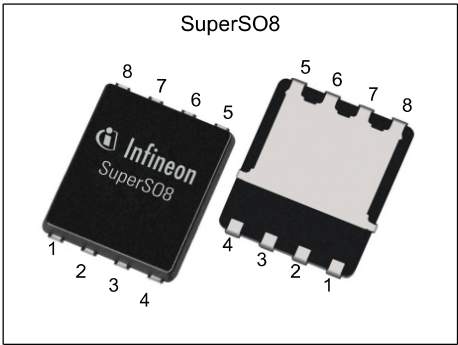- Halogen-free according to IEC61249-2-21

SuperSO8

Drain
Pin 5-8

Gate
Pin 4

Source
Pin 1-3

*1: Internal body diode

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	2.0	mΩ
I_D	145	A
Q_{OSS}	28	nC
Q_G(0V..10V)	41	nC

Type / Ordering Code	Package	Marking	Related Links
BSC0901NSI	PG-TDSON-8	0901NSI	-

[1] J-STD20 and JESD22

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - - -	- - - - -	145 92 127 81 28	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10V,T_A=25°C,R_{thJA}=50K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	580	A	T_C=25 °C
Avalanche current, single pulse[4]	I_{AS}	-	-	50	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	45	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	69 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.8	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	50	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=10 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/K	I_D=10 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	- 3	0.5 -	mA	V_{DS}=24 V, V_{GS}=0 V V_{DS}=24 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.1 1.7	2.6 2.0	mΩ	V_{GS}=4.5 V, I_D=30 A V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	0.4	0.8	1.6	Ω	-
Transconductance	g_{fs}	65	130	-	S	$|V_{DS}|$>2$|I_D|R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	2600	3500	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	1000	1300	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	140	280	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5.0	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Rise time	t_r	-	7.2	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Fall time	t_f	-	4.6	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω

[1] Defined by design. Not subject to production test

Table 6   Gate charge characteristics[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6.3	8.4	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	4.1	5.4	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge[2]	Q_{gd}	-	6.5	11	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	8.8	14	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	20	27	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	41	54	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	16	22	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[2]	Q_{oss}	-	28	37	nC	V_{DD}=15 V, V_{GS}=0 V

Table 7   Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	80	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	580	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.55	0.7	V	V_{GS}=0 V, I_F=7 A, T_j=25 °C
Reverse recovery charge[2]	Q_{rr}	-	2.0	-	nC	V_R=15 V, I_F=7 A, di_F/dt=400 A/µs

[1] See ″Gate charge waveforms″ for parameter definition
[2] Defined by design. Not subject to production test

4   Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot}=f(T_C)

Diagram 2: Drain current

I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D=t_p/T
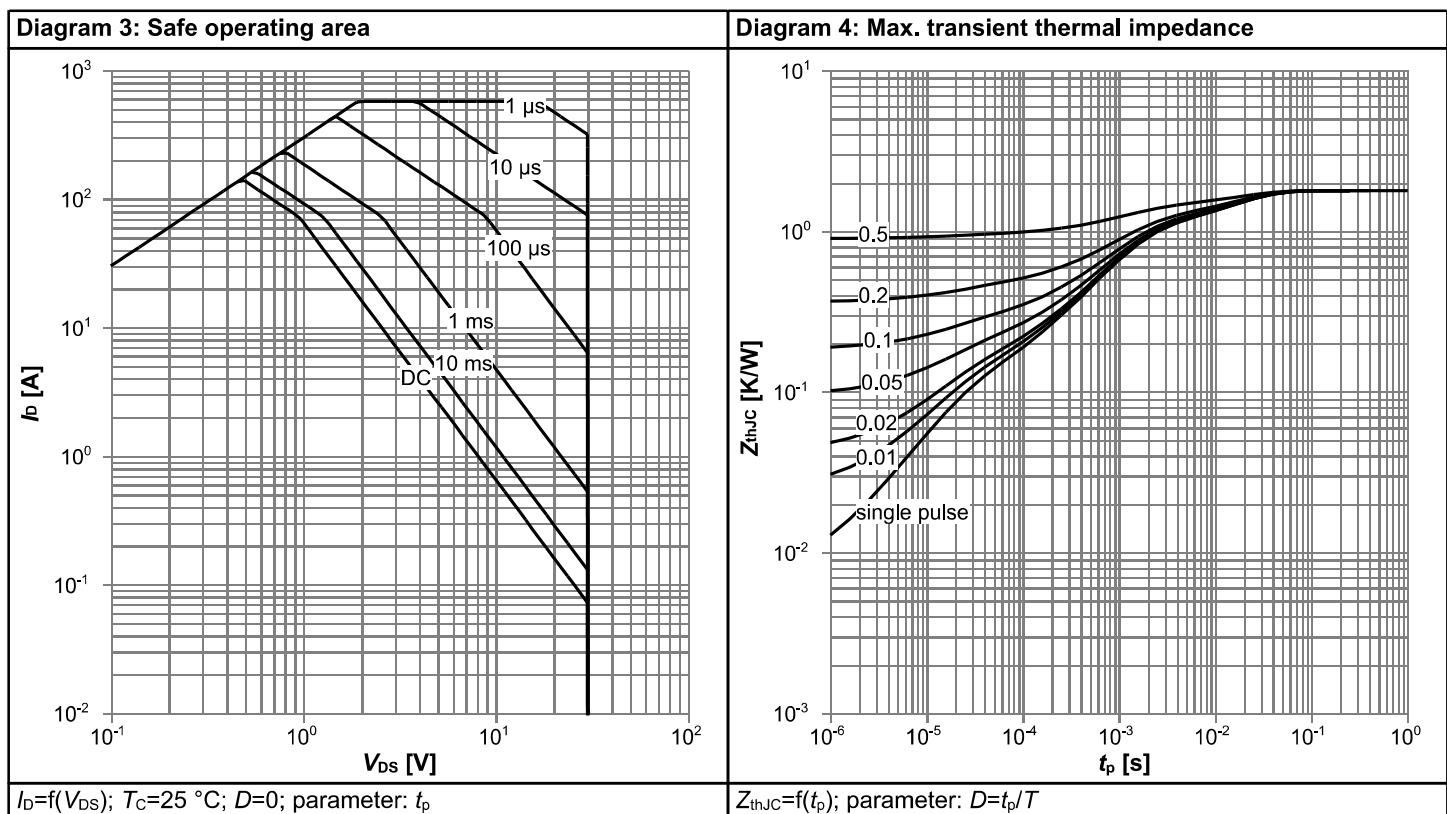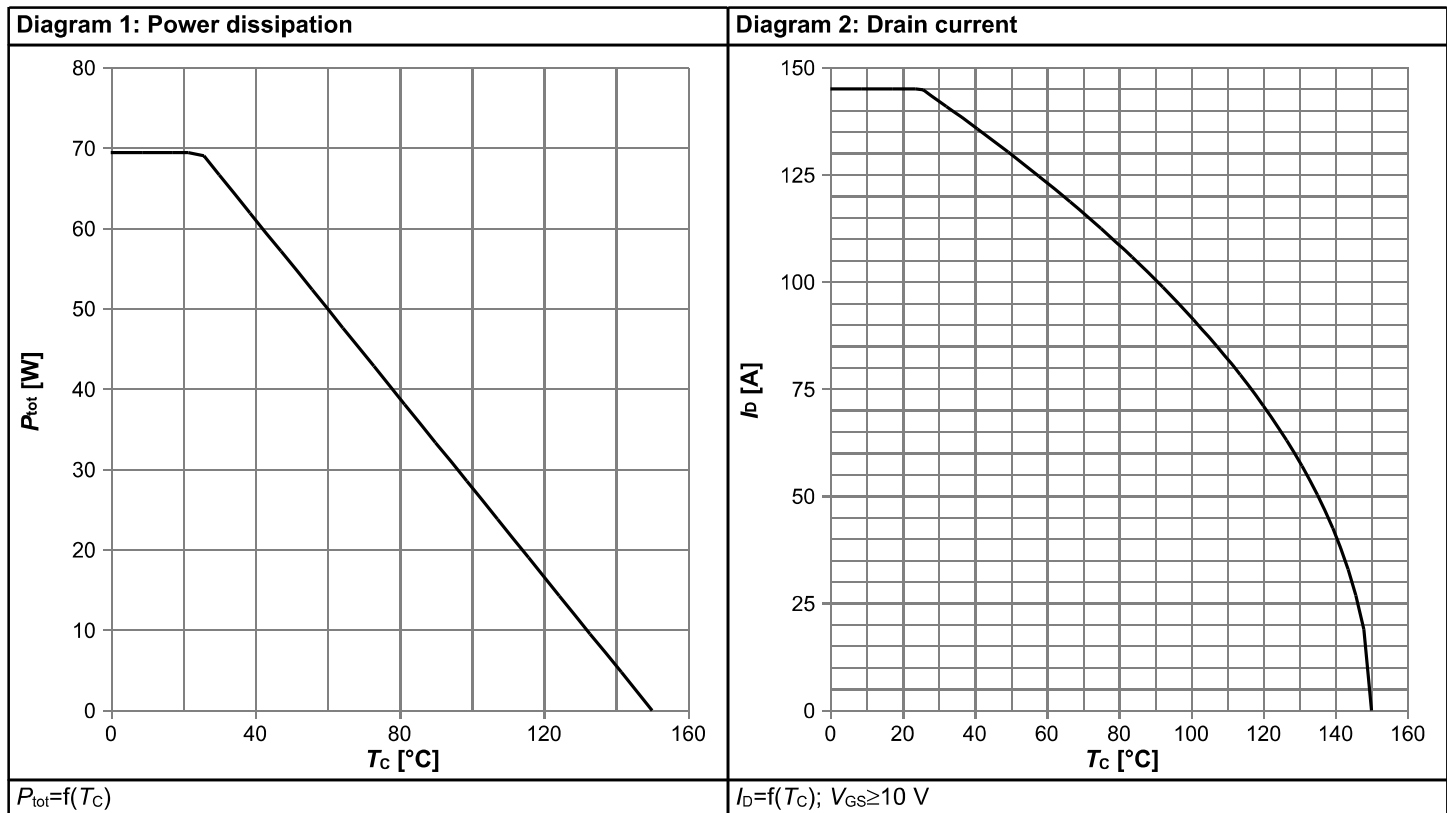
Diagram 5: Typ. output characteristics
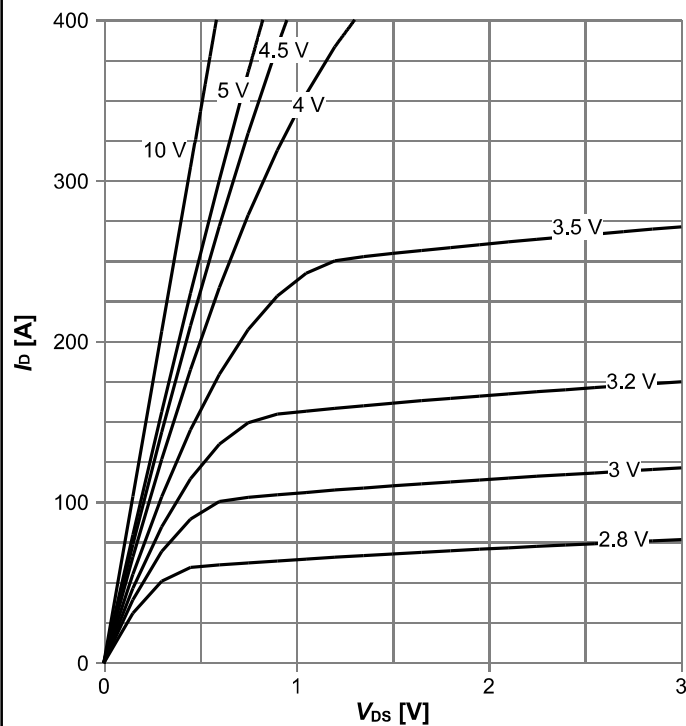
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance
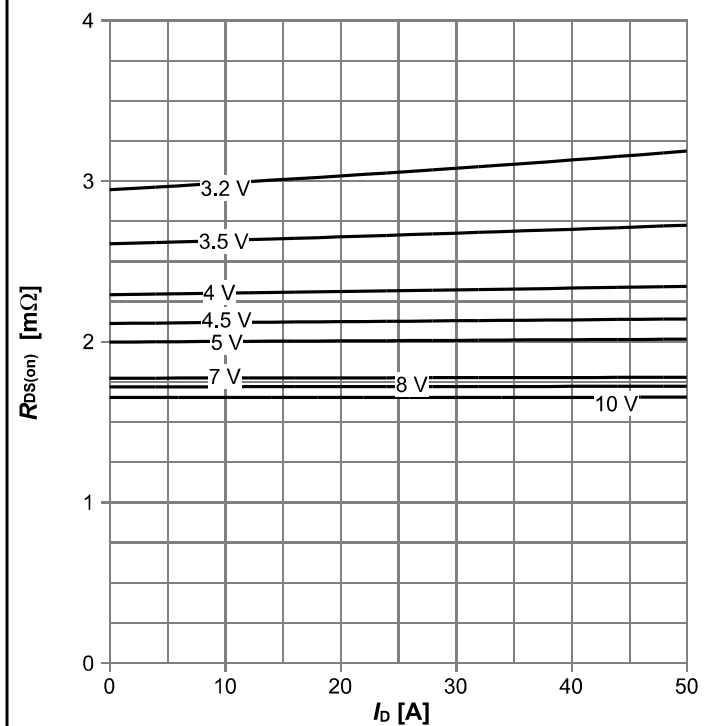
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
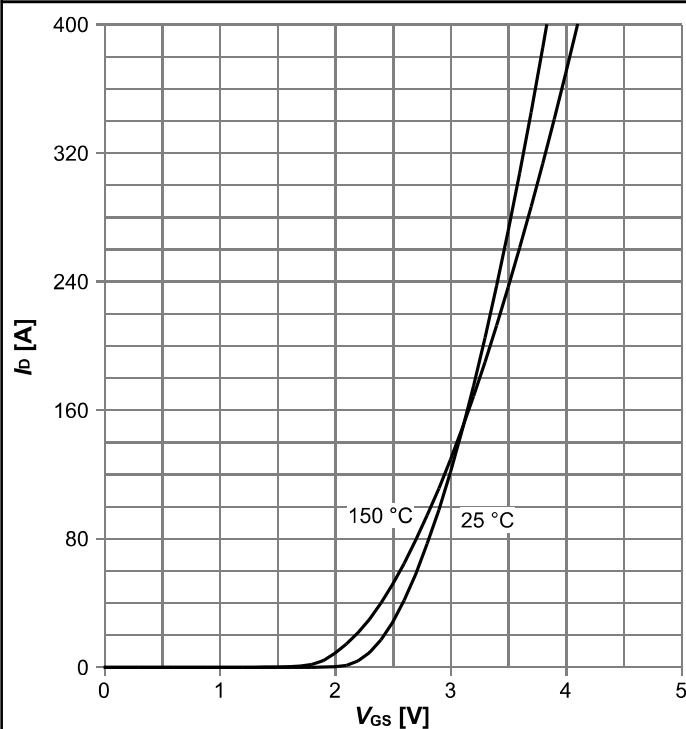
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance
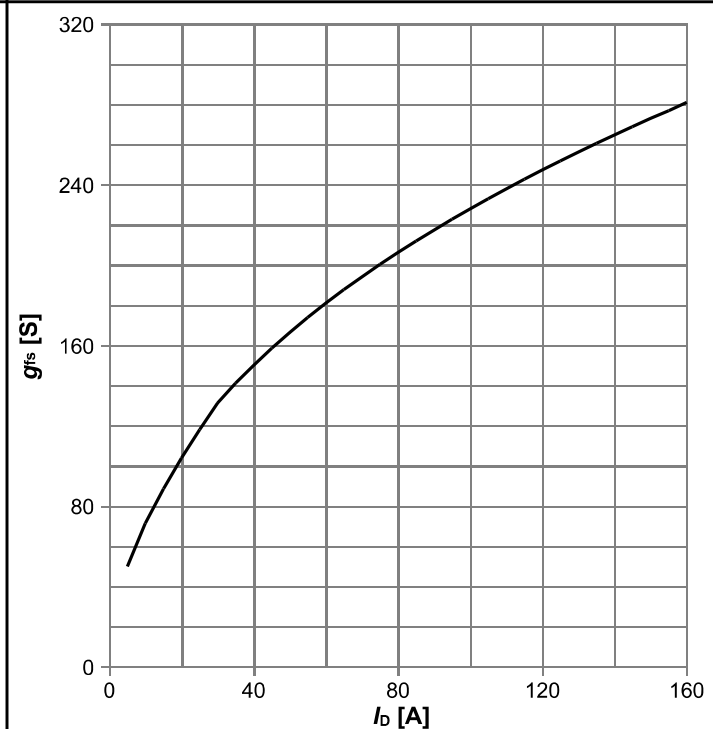
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance
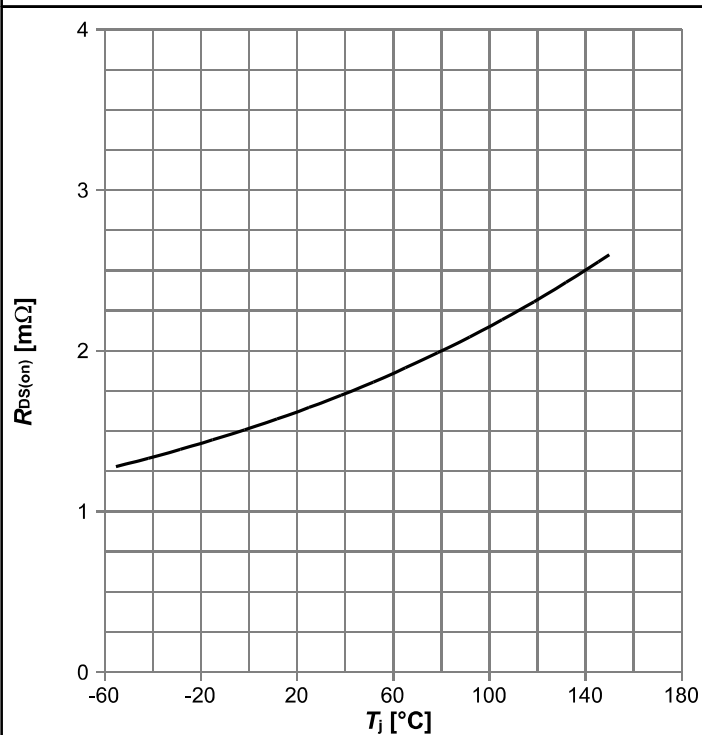
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage
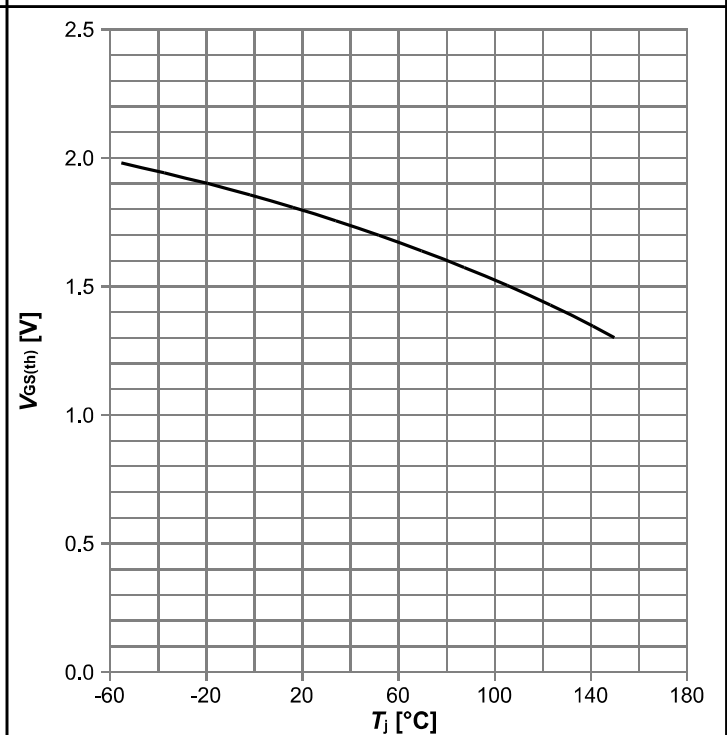
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=10 mA

Diagram 11: Typ. capacitances
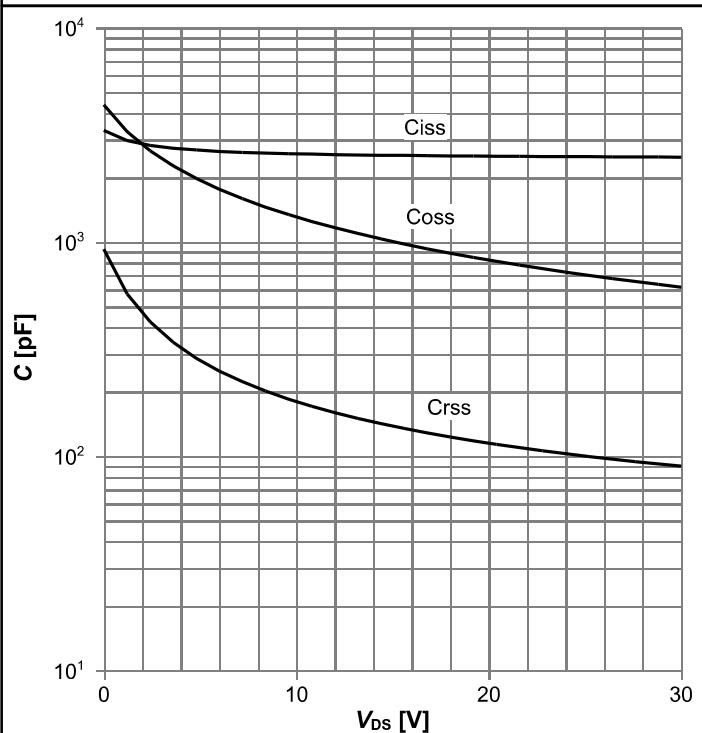
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode
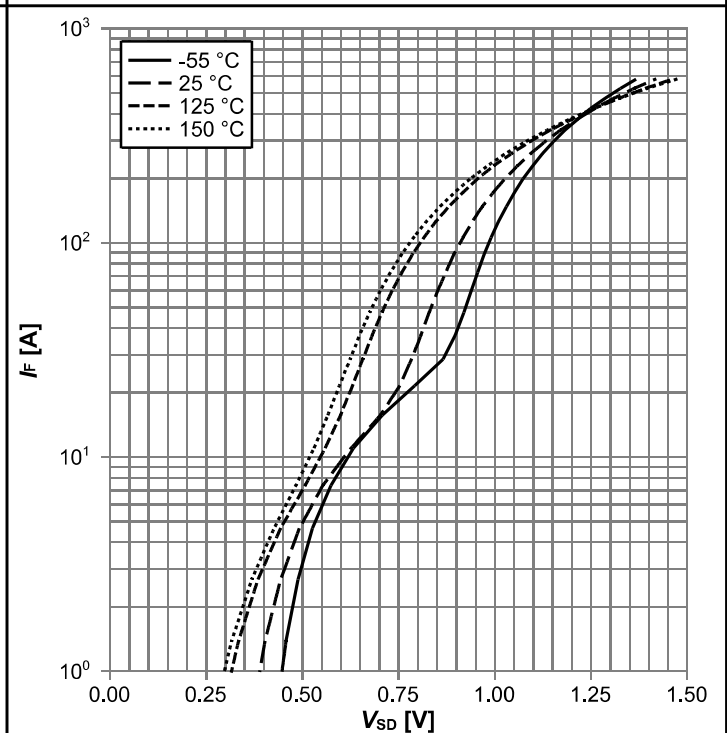
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics
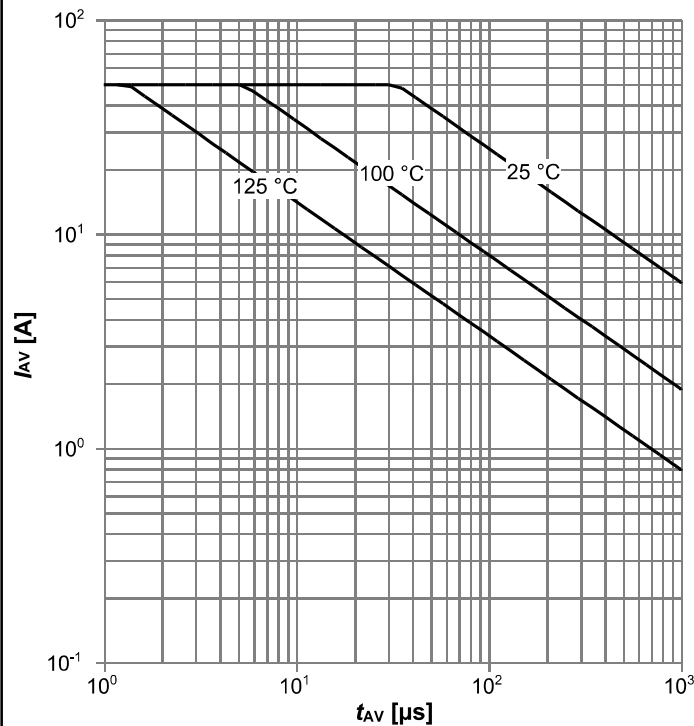
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge
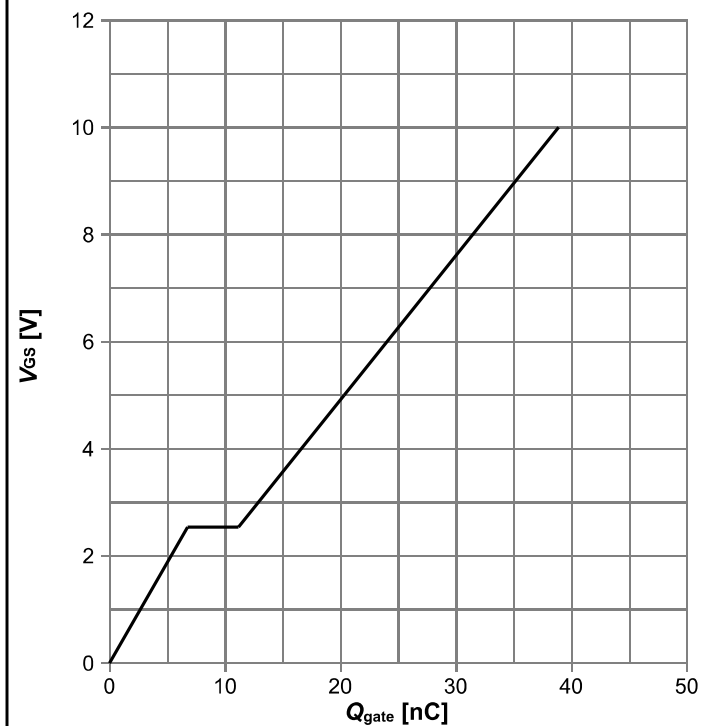
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Typ. drain-source leakage current
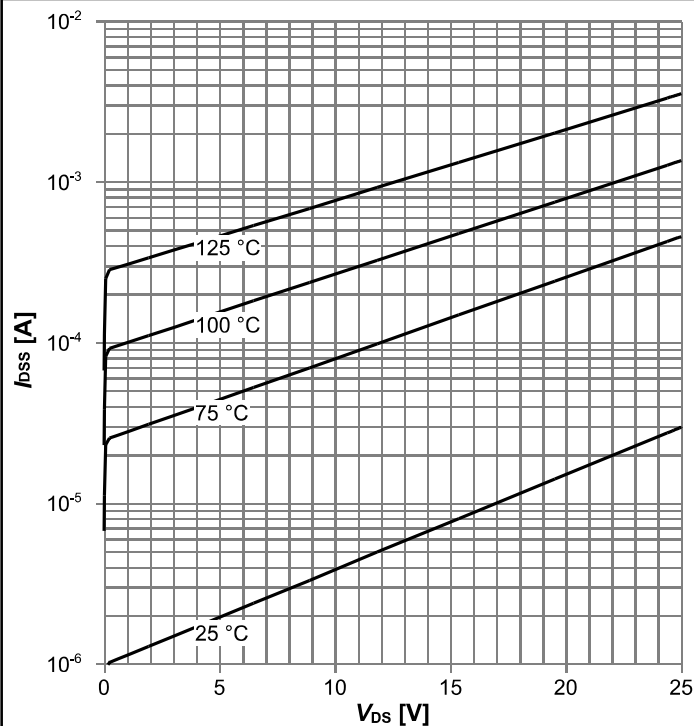
I_{DSS}=f(V_{DS}); V_{GS}=0 V; parameter: T_j

Diagram Gate charge waveforms
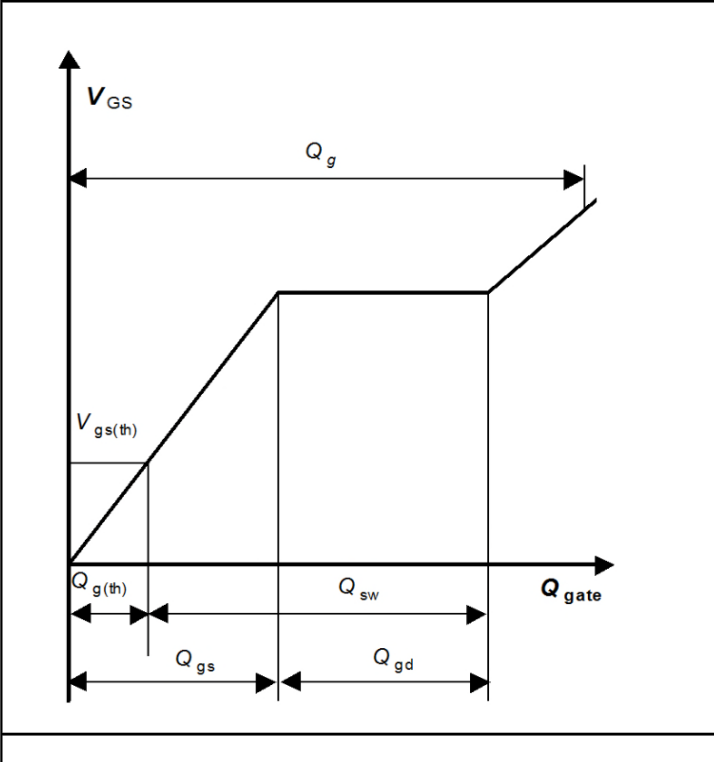
5   Package Outlines
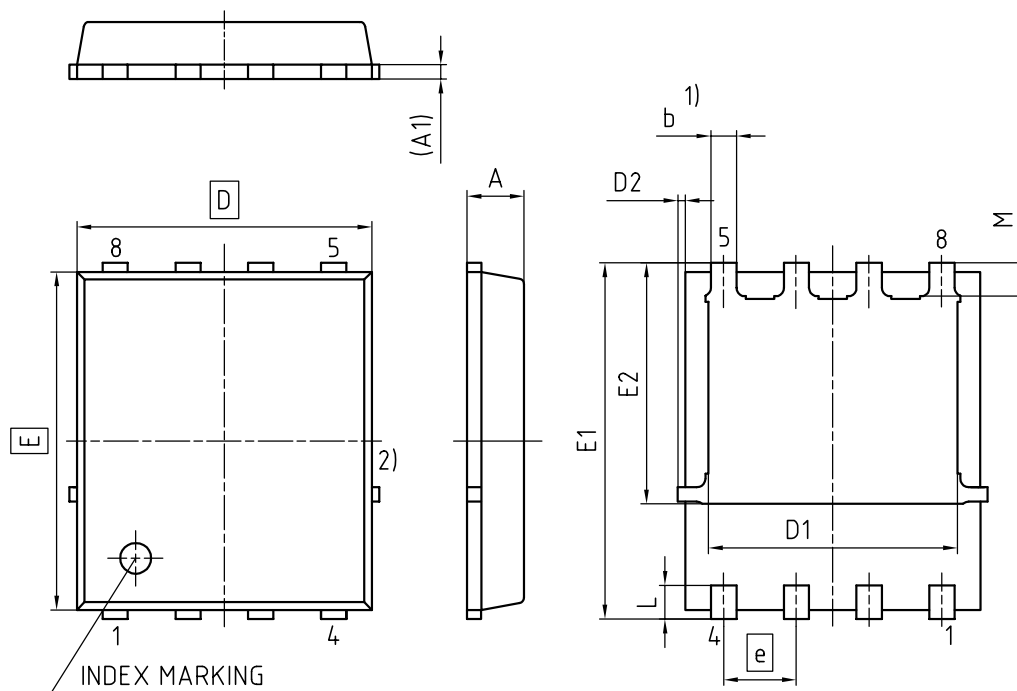
1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO.
Z8B00003332

REVISION
07

SCALE 10:1

0   1   2   3mm

EUROPEAN PROJECTION

ISSUE DATE
06.06.2019

Figure 1   Outline PG-TDSON-8, dimensions in mm

PG-TDSON-8: Recommended Boardpads & Apertures
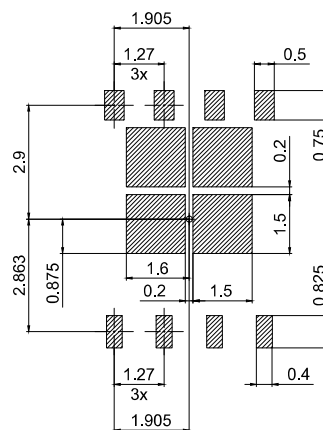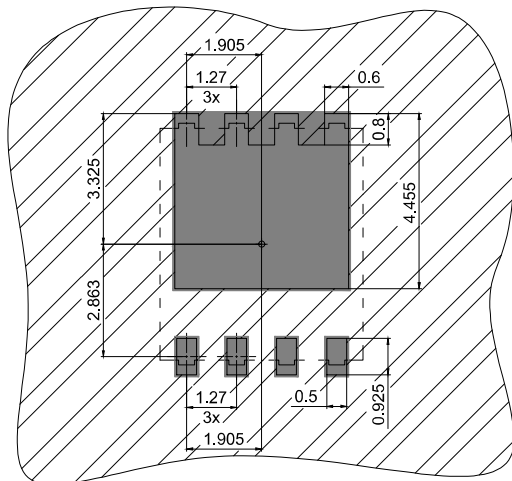
copper   solder mask   stencil apertures

all dimensions in mm

Figure 2   Outline Boardpads (TDSON-8), dimensions in mm

Dimension in mm

Figure 3   Outline Tape (TDSON-8)

Revision History

BSC0901NSI

Revision: 2021-06-07, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.4	2019-10-31	Update package drawings and add max. Capacitances and Charges
2.5	2021-06-07	Update current rating and footnotes

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