BGT60ATR24C

60 GHz radar sensor

Datasheet V1.5

Features

- 60 GHz radar sensor for FMCW operation
- 4 GHz bandwidth
- 2 TX / 4 RX channels
- Digital interface for chip configuration and radar data acquistion
- Optimized power modes for low-power operation
- Integrated state machine for independent operation

Potential applications

- Radar frontend for gesture sensing
- High resolution FMCW radars
- Short range sensing operations
- Hidden sensing applications behind radome

Product validation

Qualified for Automotive Applications.
Product Validation according to AEC-Q100/101

AEC Qualified RoHS Halogen-free

Description

BGT60ATR24C, an automotive 60 GHz radar sensor, enables ultra-wide bandwidth FMCW operation in a small package. Sensor configuration and data acquisition are enabled with a digital interface and the integrated state machine enables independent data acquisition with power mode optimization for lowest power consumption.

Table of contents

1 Introduction

New smart sensors for gesture recognition can be based on radar systems, in special case, FMCW radars. Those systems can comprise several blocks: Radio Frequency (RF) front-end, Analog Base Band (ABB), Analog to Digital Converter (ADC), Phase Locked Loop (PLL), memory (FIFO e.g.) and Serial Peripheral Interface (SPI). Smart sensors require a high level of integration, thus, the components listed above should be integrated in a single chip solution. BGT60ATR24C offers this level of integration in a single chipset.

1.1 Product Overview

The core functionality of BGT60ATR24C is to transmit frequency modulated continuous wave (FMCW) signal via one of the two transmitter channel (TX) and receive the echo signals from the target object on the four receiving channels (RX). Each receiver path includes a baseband filtering, a VGA, as well as an ADC. The digitized output is stored in a FIFO. The data are transferred to an external host, microcontroller unit (MCU) or application processor (AP), to run radar signal processing. A typical implementation of a sensor system consists of two main blocks only (see Figure 1):

- BGT60ATR24C handles the RF signals and provides the sampled IF signals
- Application Processor which captures and processes the radar signals

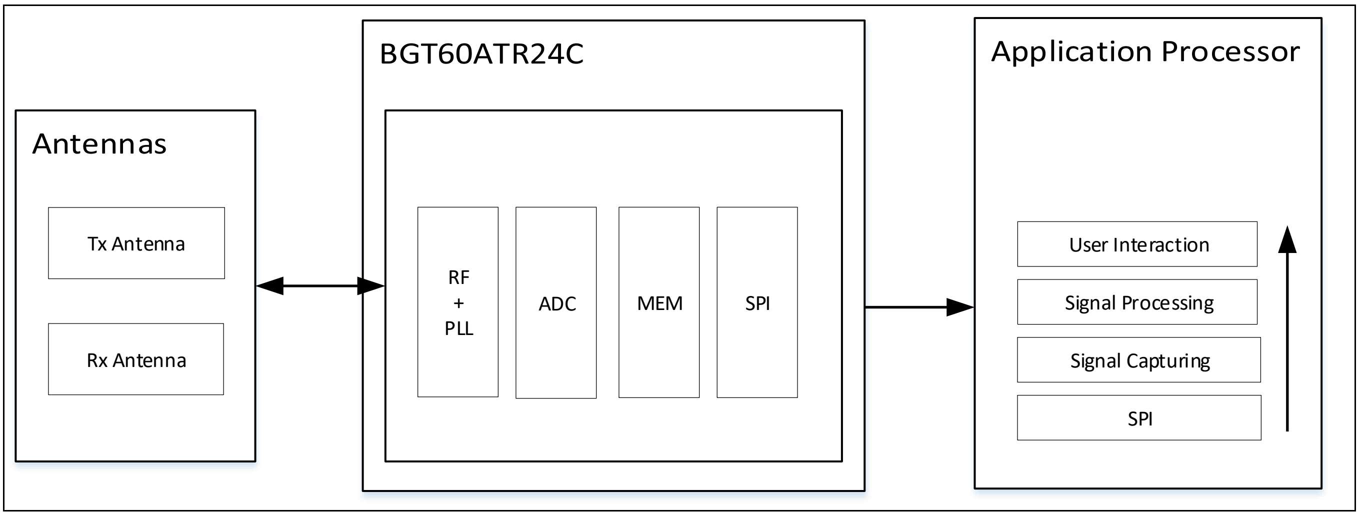


Figure 1 Data flow in the complete radar sensor system

1.2 Potential Applications

The chipset has been designed to address mainly the following potential applications:

- Radar frontend for gesture sensing
- High resolution FMCW radars
- Short range sensing operations
- Hidden sensing applications behind radome

1.3 BGT60ATR24C Bare Die Block Diagram

BGT60ATR24C block diagram is presented in Figure 2.

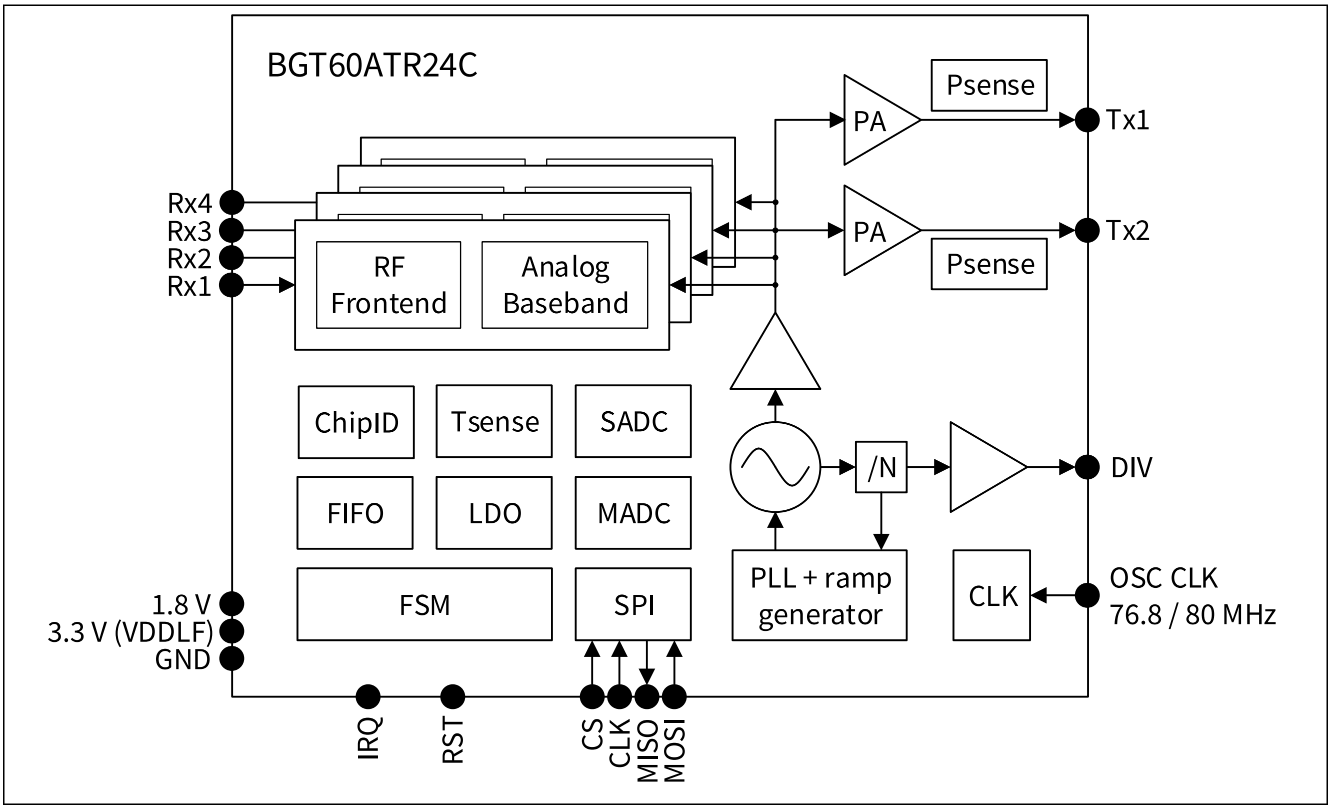


Figure 2 BGT60ATR24C Bare die block diagram

Feature List:

- Integrated LDOs from 1.8 V to 1.5 V to supply the digital domain
- RF-Frontend at 60 GHz covering frequencies from 58.0 to 62.0 GHz with two TX and four RX channels
- Baseband chain consisting of high pass filter, low noise voltage gain amplifier (VGA), and antialiasing filters
- Four ADC channels with 12 bits resolution and up to 4 MSps sampling rate to sample the RX-IF channels
- Integrated RF-PLL, timers, counters, and FSM to run set of frames in standalone mode (no communication with AP required except first trigger and raw data transfer)
- Full duplex FIFO structure as data buffer (196 kbit = 8192 words x 24 bits)
- Linear Feedback Shift Register (LFSR) test pattern generator on chip for data transfer check
- 8 to 10 bits sensor ADC for power and temperature measurement
- Standard SPI mode for configuration and status register read accesses
- Dedicated power modes for power reduction
- An external 80 MHz reference oscillator is used as a system clock source
- BITE (Built in test equipment) for EOL test in production at Infineon to verify RF performance
- ChipID block provides info regarding the digital code version, the RF block version, and the RF configuration
- Fabricated with BiCMOS Infineon process technology
- Housed in a eWLB package

1.4 BGT60ATR24C Pin Definition and Function (ES)

Figure 3 shows the pin definition the PG-VFWLB-76-1 eWLB package in top view. The function of each pin is described in Figure 3 and Figure 4 .

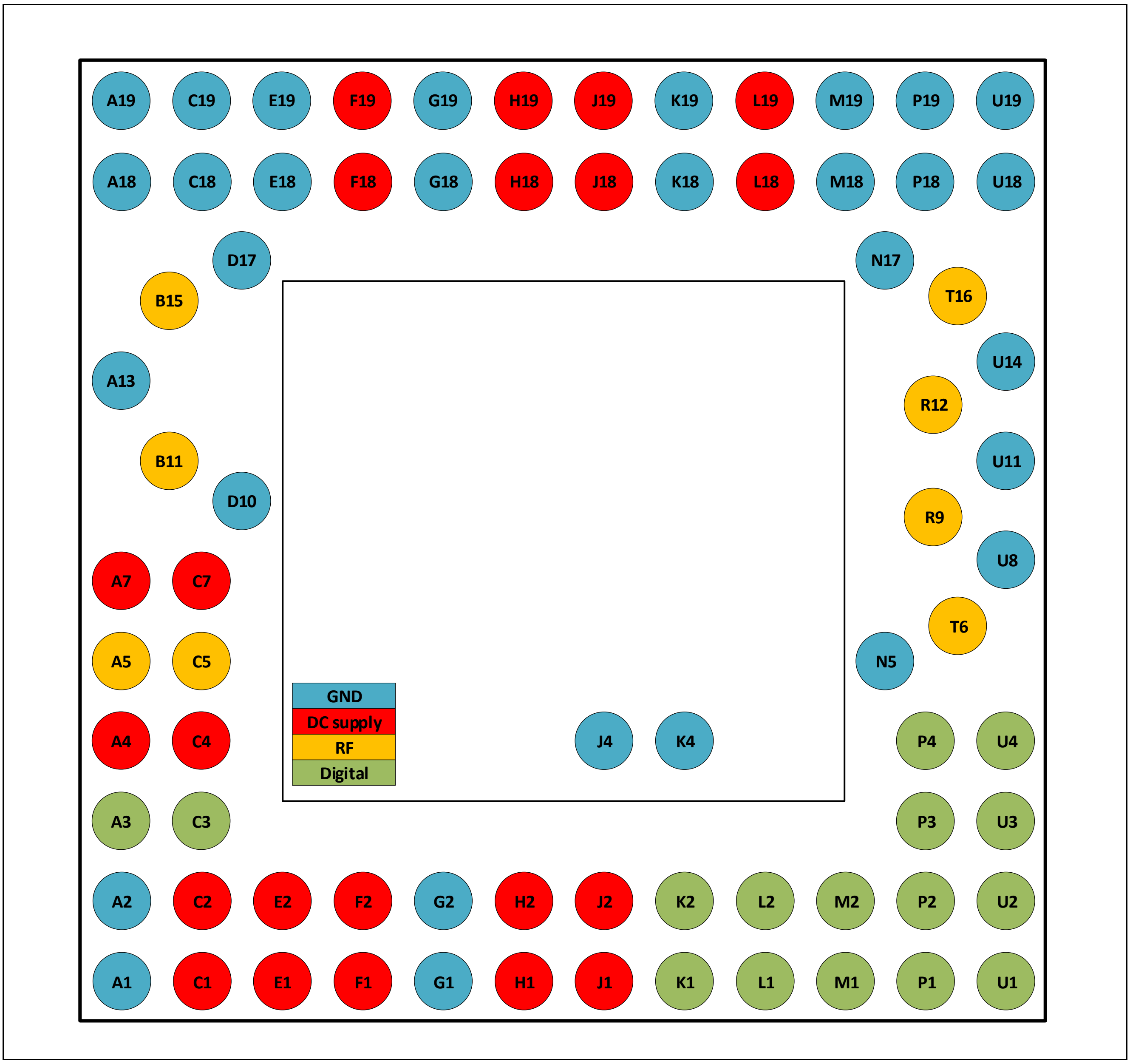


Figure 3 Pin Definition (transparent top view)

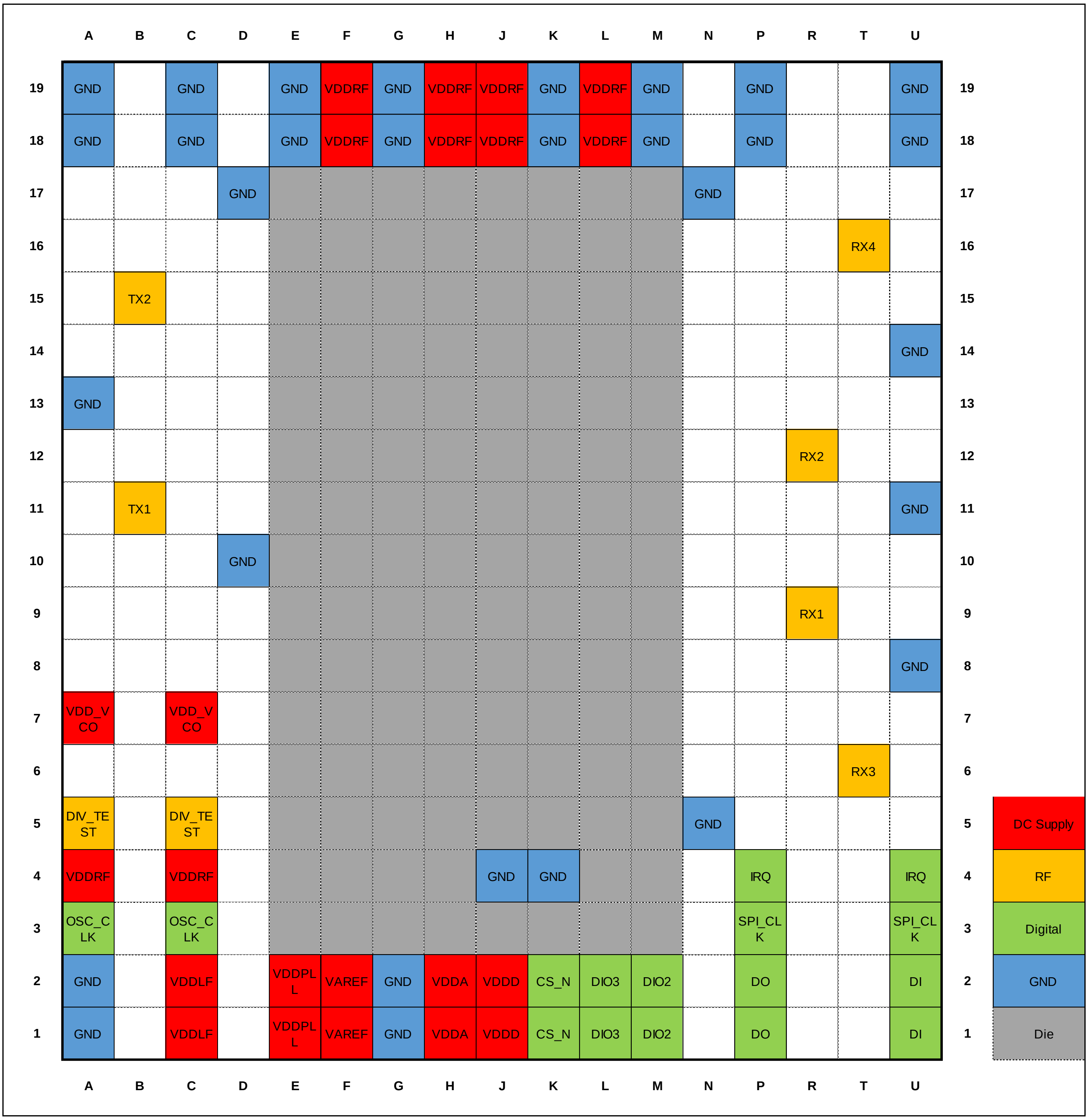


Figure 4 Pin Function (transparent top view)

Table 1 Ball Definition (ES)

Ball No.	Name	Function
B11	TX1	RF transmit output 1
B15	TX2	RF transmit output 2
R9	RX1	RF receive input 1
R12	RX2	RF receive input 2
T6	RX3	RF receive input 3

Ball No.	Name	Function
T16	RX4	RF receive input 4
A4, C4	VDDRF	Power supply RF
A7, C7	VDD_VCO	Power supply VCO
C1, C2	VDDLF	Power supply level shifter loop filter
E1, E2	VDDPLL	Power supply PLL
F1, F2	VAREF	Positive reference voltage output
F18, F19	VDDRF	Power supply RF
H1, H2	VDDA	Power supply ADC
H18, H19	VDDRF	Power supply RF
J1, J2	VDDD	Power supply digital domain
J18, J19	VDDRF	Power supply RF
L18, L19	VDDRF	Power supply RF
A3, C3	OSC_CLK	80 MHz reference input for PLL
A5, C5	DIV_TEST	VCO divided by 16 output
K1, K2	CS_N	SPI chip select
L1, L2	DIO3	HW Reset (I/O pin for Quad-SPI)
M1, M2	DIO2	I/O pin for Quad-SPI
P1, P2	DO	SPI data out (I/O pin for Quad-SPI)
P3, U3	SPI_CLK	SPI clock in
P4, U4	IRQ	Interrupt output
U1, U2	DI	SPI data in (I/O pin for Quad-SPI)
A1, A2, A13, A18, A19, C18, C19, D10, D17, E18, E19, G1, G2, G18, G19, J4, K4, K18, K19, M18, M19, N5, N17, P18, P19, U8, U11, U14, U18, U19	GND	Ground

1.4.1 IO and Supply Pins

Table 2 Input/Output Pins

Symbol	Type	Domain	Description	Domain
DIV_TEST	A_{OUT}	VDDRF	VCO divided by 16 output	Analog-RF
OSC_CLK	A_{IN}	VDDRF	80MHz Xtal input (SYS_CLK) for PLL	Analog-RF
IRQ	D_{OUT}	VDDD	Interrupt output	Control FSM
SPI_CLK	D_{IN}	VDDD	SPI CLK input	SPI
CS_N	D_{IN}	VDDD	SPI chip select input, active low	SPI
DI	D_{IN} / D_{OUT}	VDDD	SPI signal from the host output (I/O pin for Quad-SPI)	SPI
DO	D_{IN} / D_{OUT}	VDDD	SPI signal to the host input (I/O pin for Quad-SPI)	SPI
DIO2	D_{IN} / D_{OUT}	VDDD	I/O pin for Quad-SPI	SPI
DIO3	D_{IN} / D_{OUT}	VDDD	HW reset pin (I/O pin for Quad-SPI)	SPI
TX1	A_{OUT}	VDDRF	Transmitter 1 output	Analog-RF
TX2	A_{OUT}	VDDRF	Transmitter 2 output	Analog-RF
RX1	A_{IN}	VDDRF	Receiver 1 input	Analog-RF
RX2	A_{IN}	VDDRF	Receiver 2 input	Analog-RF
RX3	A_{IN}	VDDRF	Receiver 3 input	Analog-RF
RX4	A_{IN}	VDDRF	Receiver 4 input	Analog-RF

Table 3 Supply Pins

Symbol	Type	Domain	Description	Domain
VDDD	V_{IN}	1.8 V	Digital supply voltage	Digital
VDDA	V_{IN}	1.8 V	Analog supply voltage	ADC
VAREF	V_{OUT}	1.2 V	Positive reference voltage output; for bypass cap	ADC
VDDVCO	V_{IN}	1.8 V	Analog supply voltage to the VCO	Analog-RF
VDDRF	V_{IN}	1.8 V	Analog supply voltage	Analog-RF
VDDLF	V_{IN}	3.3V	Analog supply voltage for the level shifter of the PLL loop filter	Analog-RF
VDDPLL	V_{IN}	1.8 V	Analog supply voltage to the PLL	Analog-RF
VSSRF	GNDA	0 V	Analog ground connection	Analog-RF
VSSA	GNDA	0 V	Analog ground connection	ADC
VSSD	GNDD	0 V	Digital ground connection	Digital

Abbreviations:

V_{IN} … supply voltage input pin

D_{IN} … digital input pin

D_{OUT} … digital output pin

V_{OUT} … supply voltage output pin

A_{OUT} … analog output pin

A_{IN} … analog input pin

GNDA … analog ground connection

GNDD … digital ground connection

1.5 BGT60ATR24C Functional Block Diagram

BGT60ATR24C consists of some main functional blocks:

- **RF Frontend** consisting of 4ch Rx, 2ch Tx, LO generation, and divider by 4/5, see paragraph 7.1
- **ABB**, analog baseband consisting of high pass filter (HPF), VGA, anti-aliasing filter (AAF), see paragraph 7.2
- **PLL**, 3rd order sigma-delta based to perform FMCW ramp
- **MADC**, 4ch 12 bits differential SAR ADCs interfaced to the ABB via a driver and to the FIFO via a mux, see paragraph 8
- **SADC**, 8 to 10 bits single-ended SAR ADC used to sense the sensor data, see section 9
- **FIFO**, 196 kbit= 8192 words x 24 bits
- **Register banks**, 97 registers, see paragraph 4
- **SPI**, up to 50 MHz clock
- **FSM**, finite state machine which manage the complete chip
- **Clock wise, two domains** can be identified:
  80 MHz system clock (SYS_CLK) domain for PLL, MADC, SADC, and FIFO
  50 MHz (e.g.) SPI clock
  The main FSM syncs those two domains.

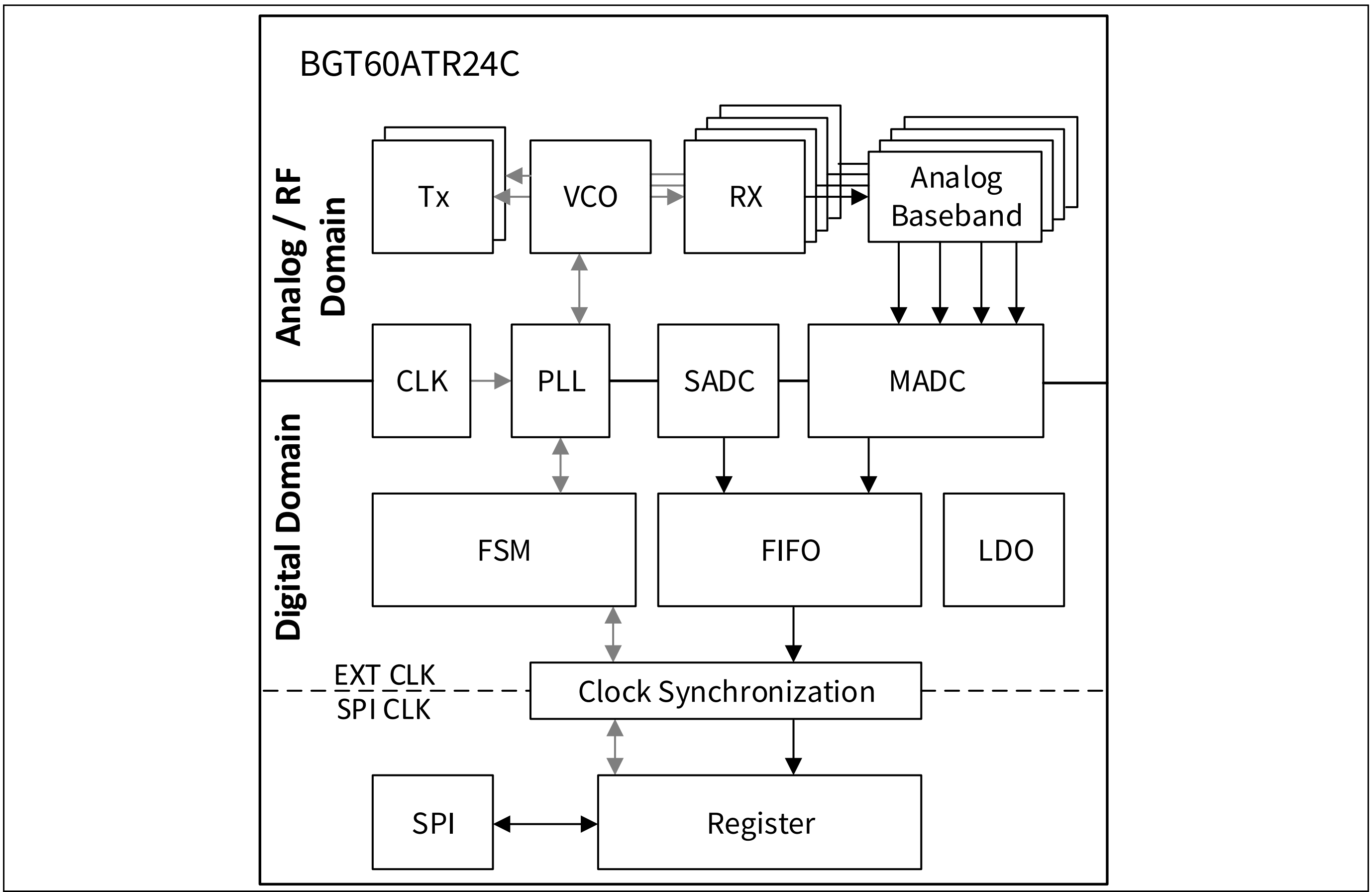


Figure 5 **BGT60ATR24C functional overview**

2 General Product Specification

The reference for all specified data is the Infineon application board, available on request.

2.1 Absolute Maximum Ratings

Table 4 **Absolute Maximum Ratings T_b= -40°C to 105°C,** all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Parameters not subject to production test

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Supply Voltage	VDDD	V	-0.3		+2	2.1.1	
Supply Voltage	VDDA	V	-0.3		+2	2.1.2	
Supply Voltage	VDDRF	V	-0.3		+2	2.1.3	
Supply Voltage	VDDVCO	V	-0.3		+2	2.1.4	
Supply Voltage	VDDPLL	V	-0.3		+2	2.1.5	
Supply Voltage	VDDLF	V	-0.3		+3.7	2.1.6	
DC Voltage at all I/O Pins	$V_{I/O}$	V	-0.3		VDD+0.3	2.1.7	Not exceeding 2V
RF Input Power Level	PRF	dBm			+10	2.1.8	At the Rx input-port
Junction Temperature	Tj	°C	-40		+145	2.1.9	
Storage Temperature	Tstg	°C	-40		+150	2.1.10	

Warning: Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.

2.2 Range of Functionality

Table 5 **Range of Functionality,** VDDD= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Supply Voltage	VDDD	V	1.71	1.8	1.89	2.2.1	Noise on each supply domain should not exceed the level of 20µVpp in the frequency range 20kHz-700kHz[1)]
Supply Voltage	VDDA	V	1.71	1.8	1.89	2.2.2	
Supply Voltage	VDDRF	V	1.71	1.8	1.89	2.2.3	
Supply Voltage	VDDVCO	V	1.71	1.8	1.89	2.2.4	
Supply Voltage	VDDPLL	V	1.71	1.8	1.89	2.2.5	
Supply Voltage	VDDLF	V	2.5	3.3	3.63	2.2.6	
Chip Backside Temperature	Tb	°C	-40		105	2.2.7	Measured with the on-chip temperature sensor
Frequency Range	f_{RF}	GHz	58.0		62.0	2.2.8	
System Reference Frequency	f_{SYS_CLK}	MHz	75	80	85	2.2.9	1.8 V CMOS clock; 78 MHz not allowed

Duty cycle of f_{SYS_CLK}	f_{DUTSYS}	%	45	50	55	2.2.10	
Rise and Fall Time of f_{SYS_CLK}	$t_{RS,FS,SYS}$	ns			6	2.2.11	
Phase Jitter of f_{SYS_CLK}	J_{PHSYS}	ps		1		2.2.12	BW: 12kHz to 20MHz

1) This value will guarantee no artifact/false target in the Range-Doppler map when it is calculated with a minimum of 8 chirps.

2.3 Current Consumption

Table 6 **Overall Current Consumption,** VDD (all except LF) = 1.71 to 1.89 and Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Idd Deep Sleep[1)]	Idd_{ds}	mA	0.03	0.12	5.10	2.3.1	
Idd Idle[2)]	Idd_{idle}	mA	2.86	3.6	9.12	2.3.2	
Idd Init0, 4Rx + 2Tx	Idd_{int0}	mA	158	206	275	2.3.3	
Idd Init1, 4Rx + 2Tx[3)]	Idd_{int1}	mA	164	215	279	2.3.4	
Idd Active, 4Rx + 2Tx[4)]	Idd_{act}	mA	201	259	336	2.3.5	

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

5) The value at max refers to the max temperature, +105°C, and the max supply, 1.89 V

Table 7 **VDDD Domain Current Consumption,** VDD (any except LF) = 1.71 to 1.89 and Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Idd Deep Sleep[1)]	$DIdd_{ds}$	mA	0.03	0.1	4.93	2.3.6	
Idd Idle[2)]	$DIdd_{idle}$	mA	2.3	3.1	8.4	2.3.7	
Idd Init0, 4Rx + 2Tx	$DIdd_{int0}$	mA	2.5	3.4	8.8	2.3.8	
Idd Init1, 4Rx + 2Tx[3)]	$DIdd_{int1}$	mA	2.8	3.8	9.3	2.3.9	
Idd Active, 4Rx + 2Tx[4)]	$DIdd_{act}$	mA	3.0	4.1	9.6	2.3.10	

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, FIFO in low power mode, DAC Tx set to #31 for an output power of +5dBm

5) The value at max refers to the max temperature, +105°C, and the max supply, 1.89 V

Table 8 **VDDA Domain Current Consumption,** VDD (any except LF) = 1.71 to 1.89 and Tb= -40 to +105°C

Spec	**Symbol**	**Unit**	**Value**			**Number**	**Condition**
Parameter			Min	Typ	Max		
Idd Deep Sleep[1]	$AIdd_{ds}$	µA	0	0.05	10	2.3.11	
Idd Idle[2]	$AIdd_{idle}$	mA	0.27	0.41	0.53	2.3.12	
Idd Init0, 4Rx + 2Tx	$AIdd_{int0}$	mA	1.8	2.3	2.8	2.3.13	
Idd Init1, 4Rx + 2Tx[3]	$AIdd_{int1}$	mA	1.8	2.3	2.8	2.3.14	
Idd Active, 4Rx + 2Tx[4]	$AIdd_{act}$	mA	1.8	2.3	2.9	2.3.15	

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

Table 9 **VDDPLL Domain Current Consumption,** VDD (any except LF) = 1.71 to 1.89 and Tb= -40 to +105°C

Spec	**Symbol**	**Unit**	**Value**			**Number**	**Condition**
Parameter			Min	Typ	Max		
Idd Deep Sleep[1]	$PLLIdd_{ds}$	µA	0	0.02	30	2.3.16	
Idd Idle[2]	$PLLIdd_{idle}$	mA	0.03	0.04	0.10	2.3.17	
Idd Init0, 4Rx + 2Tx	$PLLIdd_{int0}$	mA	0.7	0.86	1.1	2.3.18	
Idd Init1, 4Rx + 2Tx[3]	$PLLIdd_{int1}$	mA	6.8	7.8	9.3	2.3.19	
Idd Active, 4Rx + 2Tx[4]	$PLLIdd_{act}$	mA	6.9	8.0	9.0	2.3.20	

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

Table 10 **VDDLF Domain Current Consumption,** VDD (any except LF) = 1.71 to 1.89 and Tb= -40 to +105°C

Spec	**Symbol**	**Unit**	**Value**			**Number**	**Condition**
Parameter			Min	Typ	Max		
Idd Deep Sleep[1]	$LFIdd_{ds}$	µA	0	0.02	10	2.3.21	
Idd Idle[2]	$LFIdd_{idle}$	µA	0	0.04	10	2.3.22	
Idd Init0, 4Rx + 2Tx	$LFIdd_{int0}$	mA	0.32	0.41	0.51	2.3.23	
Idd Init1, 4Rx + 2Tx[3]	$LFIdd_{int1}$	mA	0.06	0.4	0.51	2.3.24	
Idd Active, 4Rx + 2Tx[4]	$LFIdd_{act}$	mA	0.32	0.4	0.51	2.3.25	

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

Table 11 **VDDRF + VDDVCO Domain Current Consumption,** VDD (any except LF) = 1.71 to 1.89 and Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Idd Deep Sleep[1]	$RFIdd_{ds}$	µA	0	2.6	160	2.3.26	
Idd Idle[2]	$RFIdd_{idle}$	mA	0	0.1	0.21	2.3.27	
Idd Init0, 4Rx + 2Tx	$RFIdd_{int0}$	mA	150	200	268	2.3.28	
Idd Init1, 4Rx + 2Tx[3]	$RFIdd_{int1}$	mA	150	200	268	2.3.29	
Idd Active, 4Rx + 2Tx[4]	$RFIdd_{act}$	mA	188	244	321	2.3.30	

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

2.4 ESD Robustness

Table 12 **ESD Robustness,** VDD (any)= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
ESD robustness, HBM[1]	$V_{ESD\text{-}HBM}$	V	-2000		+2000	2.4.1	All pins
ESD robustness, CDM[2]	$V_{ESD\text{-}CDM}$	V	-750 -500		+750 +500	2.4.2	Corner pins All other pins

1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kOhm, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

2) According to ANSI/ESDA/JEDEC JS-002 Field-Induced Charged-Device Model (CDM). Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

Please note that this result is subject to:
- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

2.5 Thermal Resistance

Table 13 **Thermal Resistance,** VDD (any)= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	**Symbol**	**Unit**	**Value**			**Number**	**Condition**
Parameter			Min	Typ	Max		
Package Rth-JB	$R_{th\text{-}JB}$	K/W		44.2		2.5.1	Simulated junction to balls. Conditions: package only, bottom side of balls fixed to ambient temperature

2.6 Product Validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

3 Shapes, Frames, and Channel Set Definition

This section is intended to provide the user with an overview on the overall modulation and power modes capabilities of BGT60ATR24C. Specifically the structure of timers, counters, shapes, channel set and frames will be presented. The section gives also a description of how the main FSM is setting and controlling the PLL for the expected modulation shapes and sequences programmed by the host.

3.1 Shapes and Frames

The shape is the modulation chirp that should be performed by the PLL. Two basic shapes are allowed (see Figure 6):

- triangular shape: consisting of a frequency Upchirp and a frequency Downchirp
- saw-tooth shape: consisting of a frequency Upchirp followed by a fast-down chirp

The shapes are set and enabled in the PLLx[0..7] registers (see section 4.16 and 4.17) by the bit PLLx7_SH_EN. Up to four different shapes can be programmed. If more than one shape is used, the lower shapes must be programmed (eg. 3 shapes are needed by the application than x= 1...3).

N_SHAPE_EN is the number of shapes enabled.

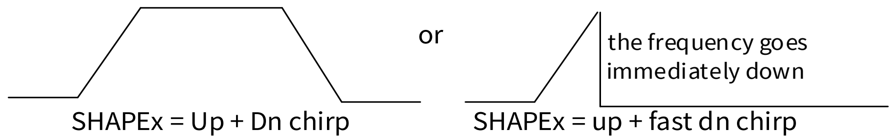


Figure 6 Shape definition

Shape Group

Each shape defined above can be repeated several times (see Figure 7). The same shape repeated several times represents a shape group. The repetition factor for the shape is called REPSx and described in 4.17. Each shape is repeated up to RSx=2^REPSx times.

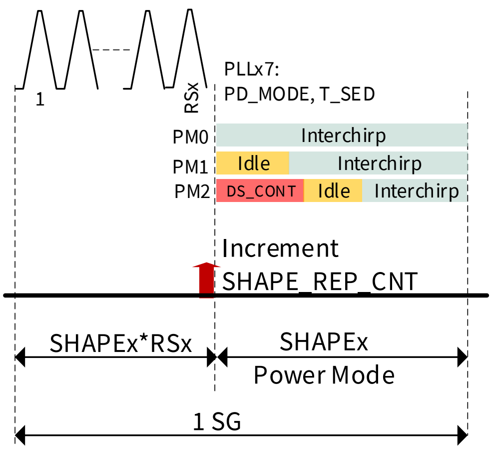


Figure 7 Shape group

After the last repetitions the FSM will enter, for a period PLLx7:T_SED (see section 4.17), the power mode programmed according to what specified in PLLx7:PD_MODE (see section 4.17).

After a shape group, the shape groups counter STAT1: SHAPE_GRP_CNT is incremented (see section 4.5). In Figure 8 an example of four programmed shape groups is reported. It represents a shape set.

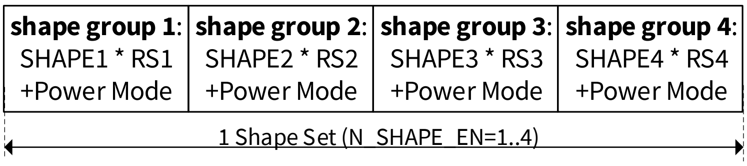


Figure 8 Shape set

Frame

A frame, as shown in Figure 9, is a sequence of shape sets followed by a specific power mode. Each shape set can be then repeated several times. The repetition factor for the shape set is called REPTx and described in 4.12. Each shape is repeated up to RTx= 2^REPTx times.

The length of a frame is defined through CCR2: FRAME_LEN (see section 4.14), which is the number of shape groups to be executed.

At each start of a frame, the first shape SHAPE1 together with the first channel set, CSU1+CSC1 in 0, is loaded.

The number of frame groups the FSM will execute will be:

$$\min(\text{FRAME\_LEN}, \text{N\_SHAPE\_EN} * \text{RT})$$

With RT ≤ (4096/shape groups) and 4095 maximum value allowed for CCR2: FRAME_LEN.

After the last shape group in a frame, the power mode from CCR1: PD_MODE is used for the period programmed in CCR1: T_FED instead of PPLx7: MODE for period PLLx7: T_SED.

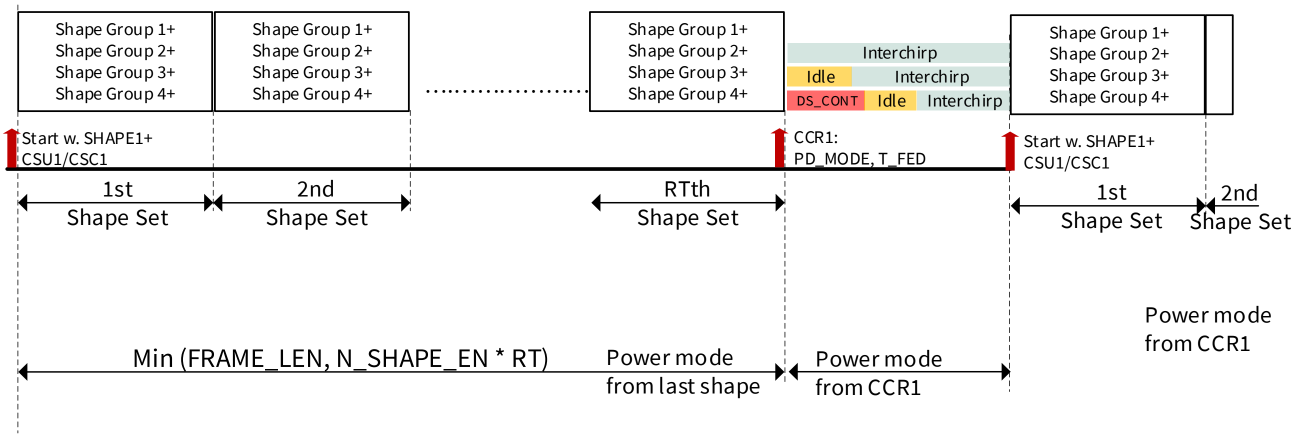


Figure 9 Example of one frame

Maximum Number of Frames

- The overall frame generation starts after the wake-up period with the first frame
- After the last frame CCR2: MAX_FRAME_CNT (see section 4.14) is reached, the FSM will enter the Deep Sleep mode instead of the power mode defined at the end of the last frame
  - In order to trigger the chip again, an FSM reset is required.

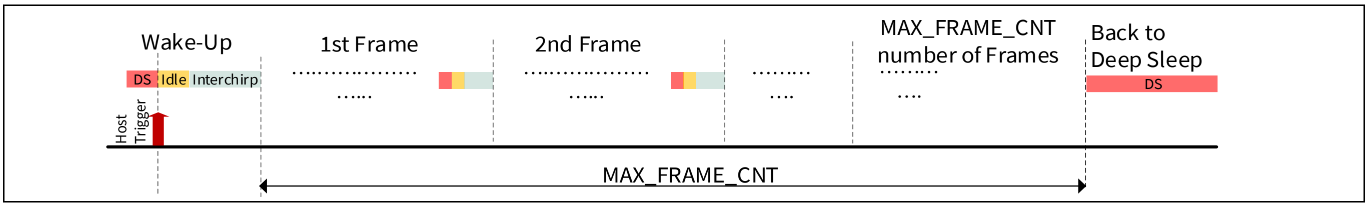


Figure 10 Maximum number of frames

3.2 Channel Set

Each channel set can be then repeated several times. The repetition factor for the channel set is called REPCx and described in 4.11. Each shape is repeated up to RCx=2^REPCx times. There are in total 10 channel set registers and 6 channel set control registers of 3 different types acting in the specific “modes”. 8 channel sets relate to the shapes (4 shapes x “up” and “down” segment settings) and two to the power modes, Idle and Deep Sleep, respectively:

- Deep Sleep power mode is related to channel set CSDS and CSCDS
- Idle mode is related to channel set CSI and CSCI
- 8 channel sets are defined for the shapes:
  - CSU1 … CSU4 registers for Upchirp
  - CSD1 … CSD4 registers for Downchirp
  - CSC1 … CSC4 channel set registers for up- and Downchirp
- Each shape from above has up to 2 channel sets CSUx and CSDx
  - In case triangular shape is used, CSUx and CSDx are applied
  - In case sawtooth shape is used, CSD is skipped
- Channel sets are repeating independent of the shapes
- Channel set repetition factor tells how often a single channel set is repeated until the next channel set is loaded
- On the channel set sequence:
  - The lower channel set number is followed by the next higher channel set number
  - In case the highest channel set number is reached, the next channel set loaded is channel set 1
- On the enabling sequence of channel sets:
  - In case not all channel sets are used, the lower number channel sets have to be used
  - In between the enabled channel sets must not be a disabled channel set
  - Eg: 2 channel sets expected: use only CS1 and CS2. In case 3 channel sets are expected, use only CS1, CS2, and CS3
- Start and end of channel set sequences:
  - After reset, the FSM is set to Deep Sleep and the first channel sets loaded are CSDS and CSCDS.
  - After a frame starts the first channel set loaded will be CS1

Note:

It would be preferable to have REPS=REPC. This is the actual implementation in the driver.

3.3 Power Modes

The following Figure 11 shows the flow chart on all possible power modes for the FSM.

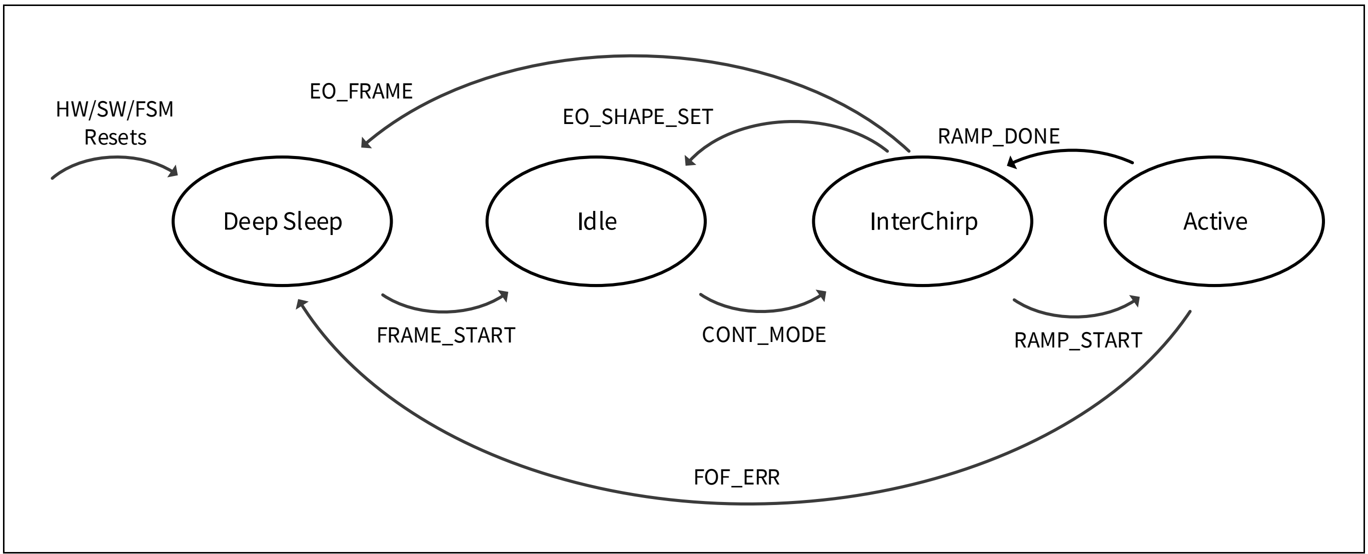


Figure 11 FSM flow chart

Power Management through the Power Modes

The power modes enable the host to have full flexibility on power consumption during each state of radar frame generation. A set of isolation registers (CSCx see section 4.11) enables/disables the different blocks on chip. The power modes are managed by the FSM.

3.3.1 Mode Descriptions

In Active, Idle, and Deep Sleep mode the power mode can be defined in the CSCx register, see section 4.11, for all channel sets: CSC1..4, CSI, CSCDS (CSUx= Channel Set Upchirp, CSDx= Channel Set Downchirp, CSI= Channel Set Idle, CSDS= Channel Set Deep Sleep).

Active Mode Definition:

- During a shape: PLLx7: PD_MODE= 0_D
- Power mode defined through registers CSx (CS1..CS4), same mode for Up/Downchirp
- Default Setting: all expected settings are enabled by the host.

Interchirp Mode Definition:

- During a shape: PLLx7: PD_MODE= 0_D
- Power mode basically same as Active mode, exception: TX1 off (PAOFF).

Idle Mode Definition:

- After a shape: PLLx7: PD_MODE= 1_D
- After a frame: CCR1: PD_MODE= 1_D

- Idle mode is defined through CSCI
- Wakeup from Deep Sleep for MAIN:TR_WKUP

The Idle mode can be used as a low-power mode in between Interchirp modes or after Deep Sleep mode to further reduce the overall power consumption while not entering the Deep Sleep mode. The wake-up times after Idle mode are faster compared to the ones after Deep Sleep mode.

Entering Deep Sleep Mode:

- After a shape: PLLx7: PD_MODE= 2_D and PLLx7: CONT_MODE= 0_B
- After a frame: CCR1: PD_MODE= 2_D and CCR0: CONT_MODE= 0_B
- Deep sleep mode is defined through CSCDS register (see section 4.11)
- All blocks can be turned off
- Internal 80 MHz clock is also turned off - to achieve extra power saving - when Cont Mode= 0_B otherwise (Cont Mode= 1_B) the clock is kept up to count the internal timer T_FED/T_SED during the deep sleep.
- In order to wake up the FSM from the Deep Sleep, the host has to program:
  - PACR1: OSCCLKEN= 1_B to enable the clock gating
  - Then the first trigger can be applied via FRAME_START.

Entering Deep Sleep Cont Mode:

- After a shape: PLLx7: PD_MODE= 2_D and PLLx7: CONT_MODE= 1_B
- After a frame: CCR1: PD_MODE= 2_D and CCR0: CONT_MODE= 1_B

In case CCR0: CONT_MODE= 1_B is enabled the wake-up from deep sleep is done automatically. The internal system clock is kept running.

In case of Errors:

If a FIFO overflow condition occurs, the FSM will bring the sensor into the Deep Sleep power mode even if the internal counters are holding the previous value, i.e., the FSM is not reset and a reset is required. In order to reset the FIFO, the host should send at least a MAIN: FIFO_RESET command (see section 4.2).

If the FIFO overflow occurs, the event is reported in FSTAT: FOF_ERR (see section 4.23) or in GSR0: FOF_ERR (see section 4.24).

In this case the data inside a FIFO can be read from the host as long as no reset occurs. “

The flags FSTAT: FOF_ERR and GSR0: FOF_ERR are cleared after a reset.

Note:

Each time the SPI will access the chip, the 80 MHz clock will be enabled internally for synchronization reasons.

3.3.2 Power Modes and Timings

This section presents the power modes and states that can be entered by the BGT60ATR24C FSM.

3.3.3 Wake-Up Phase from "Deep Sleep" to "Idle"

After VDDD power up the main LDO will require 20 µs to settle VDDC. After the reset, the chip will change to a Deep Sleep state. The following figure describes the timing for waking up the chip.

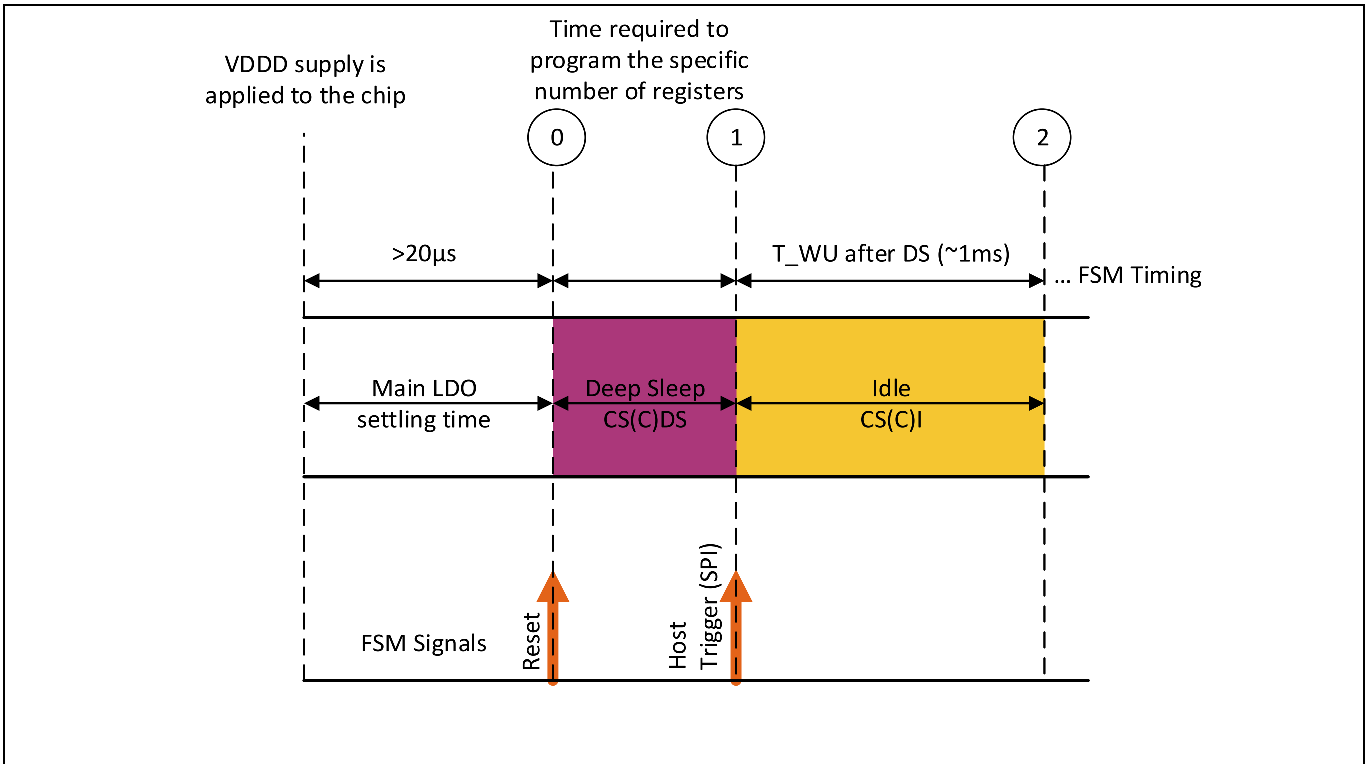


Figure 12 Deep Sleep to Idle transition

Table 14 Transitions from Deep Sleep into Idle

From #	To #	Description	Signals	Related time
#0		Chip is reset by host (see section 5.10).		
#0	#1	Host programs all registers needed for expected functionality.		
#1		Host enables the oscillator: PACR1: OSCCLKEN= 1_B to enable the clock gating.		
#1		Host starts the first trigger; it can be applied via FRAME_START.		
#1		Activate bandgap for MADC.		
#1	#2	Time required to settle the ADC BG (charge of external cap).		T_WU
#2		Enable PLL, MADC, and SADC.		
#2		MADC sends ready signal to FSM.	madc_rdy	

3.3.4 Idle to Interchirp then Active

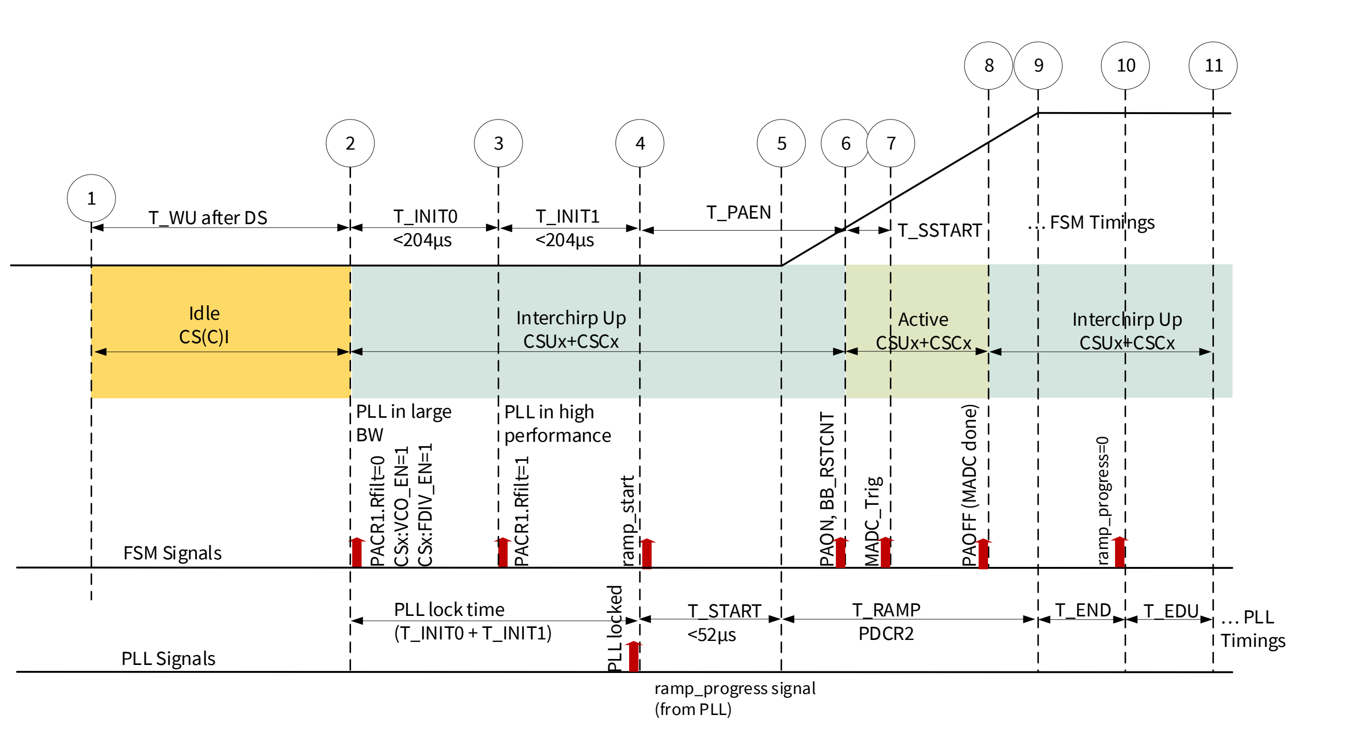


Figure 13 Transition from Idle to Interchirp to Active to Interchirp again

Table 15 Transition from Idle to Interchirp to Active to Interchirp

From #	To #	Description	Signals	Related time
#1		**Idle mode** is activated.		
#1		Host has to enable the bandgap (CSCI:BG_EN= 1_B in section 0).		
#1	#2	If Idle mode comes after a Deep Sleep (see transition from Deep Sleep to Idle).		T_WU
#1	#2	If Idle mode comes after an Interchirp mode, the bandgap is already running.		T_SED
#2		**Interchirp Up mode** is activated by selecting CSUx + CSCx register depending on the actual channel set (see section 0).		
#2		Host already enabled the blocks required by the PLL: CSx:VCO_EN = 1_B CSx:FDIV_EN = 1_B		
#2		FSM sets power mode from CSUx + CSCx.		
#2		FSM sets PACR1.RFILTSEL = 0_B.		
#2	#3	The PLL needs some time to initialize the filter settings, 75 µs typ.		T_INIT0
#3		FSM sets PACR1.RFILTSEL = 1_B.		
#3	#4	The PLL needs again some time to settle the mode, 15 µs typ.		T_INIT1
#4		PLL sends lock signal to FSM.	PLL_lock	
#4		FSM give ramp_start signal to PLL.	RAMP_START	

From #	To #	Description	Signals	Related time
#4	#5	PLL needs some settling time before chirp can start. The PLL timer is running in parallel to the FSM timer. T_START will be evaluated during system testing.		T_START (PLL)
#5	#9	PLL will run the frequency chirp.		T_RAMP (PLL)
#4	#6	Some programmable delay		T_PAEN
#6		**Active mode** starts here.		
#6		PA is enabled (PAON). Host makes sure that PA is not ON before the chirp starts (>#5).	PAON	
#6		Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value.		
#6	#7	During this phase the baseband can settle.		T_SSTART
#7		MADC is triggered for the active segment (Up).	MADC_TRIG	
#7		SADC is triggered once here.		
#7	#8	MADC starts acquiring the given number of samples (PLLx:APU in section 4.16). See section 3.4.		T_ACQUx
#8		MADC has completed the acquisition of the expected number of samples.	MADC_ DONE	
#8		PA is disabled (PAOFF) This condition must be reached before #9 The condition is: T_PAEN + T_SSTART + T_ACQUx > T_START + T_RAMPx.	PAOFF	
#8		**Interchirp Up mode** is activated again here (CSUx + CSCx).		
#9		PLL has completed the Upchirp.		
#9	#10	Programmable delay time (eg. 3 µs).		T_END
#10		Ramp completed.	RAMP_DONE	
#10	#11	Programmable delay time (eg. 1 µs).		T_EDU
#11		**Interchirp Up** mode ends here.		
#11		**Interchirp Down** mode is programed here.		

3.3.5 Saw-tooth Shape Timing

In the saw-tooth mode, after a normal Upchirp segment there will be a fast ramp down segment. The saw-tooth shape should be enabled in the bitfield PACR2: FSTDNEN (see section 4.7). For the sawtooth only CSU (Upchirp) is used (see section 4.10). The time T_EDU (see section 4.16, PLLx2#) is applied after the segment is completed. See Figure 14.

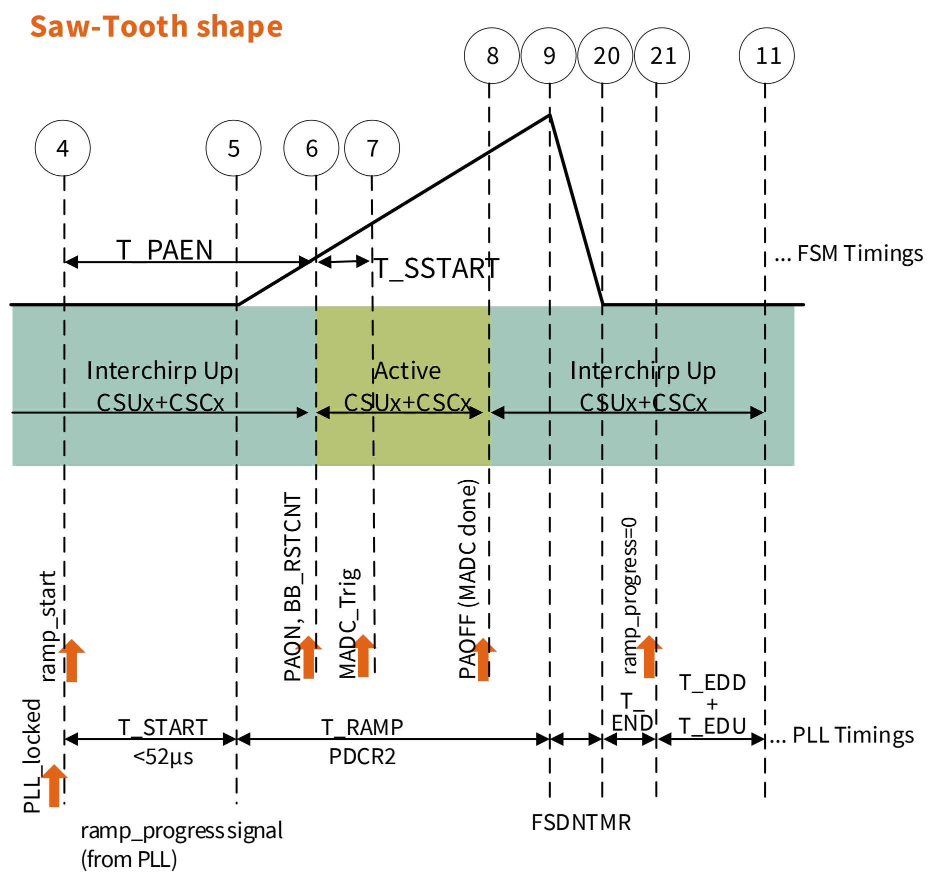


Figure 14 **Saw-tooth shape timing**

3.3.6 Different Power Modes after Shapes and Shape Groups

After the shape ends with Downchirp, the chip can enter different power modes based on the settings (PLLx, CSx, CSCx, ...):

- Interchirp mode in-between shapes – for fast chirp repetitions
- Idle mode after shape groups – in case of longer delay between shape groups and max power saving is required
- Deep Sleep + Idle mode after shape groups in case if very long delays are expected.

3.3.6.1 Idle after Shape or Shape Groups

The Idle mode after a shape or shape groups can be set when a long time in low power mode between shapes is required. Figure 15 represents a time behavior continuation of what presented in Figure 13.

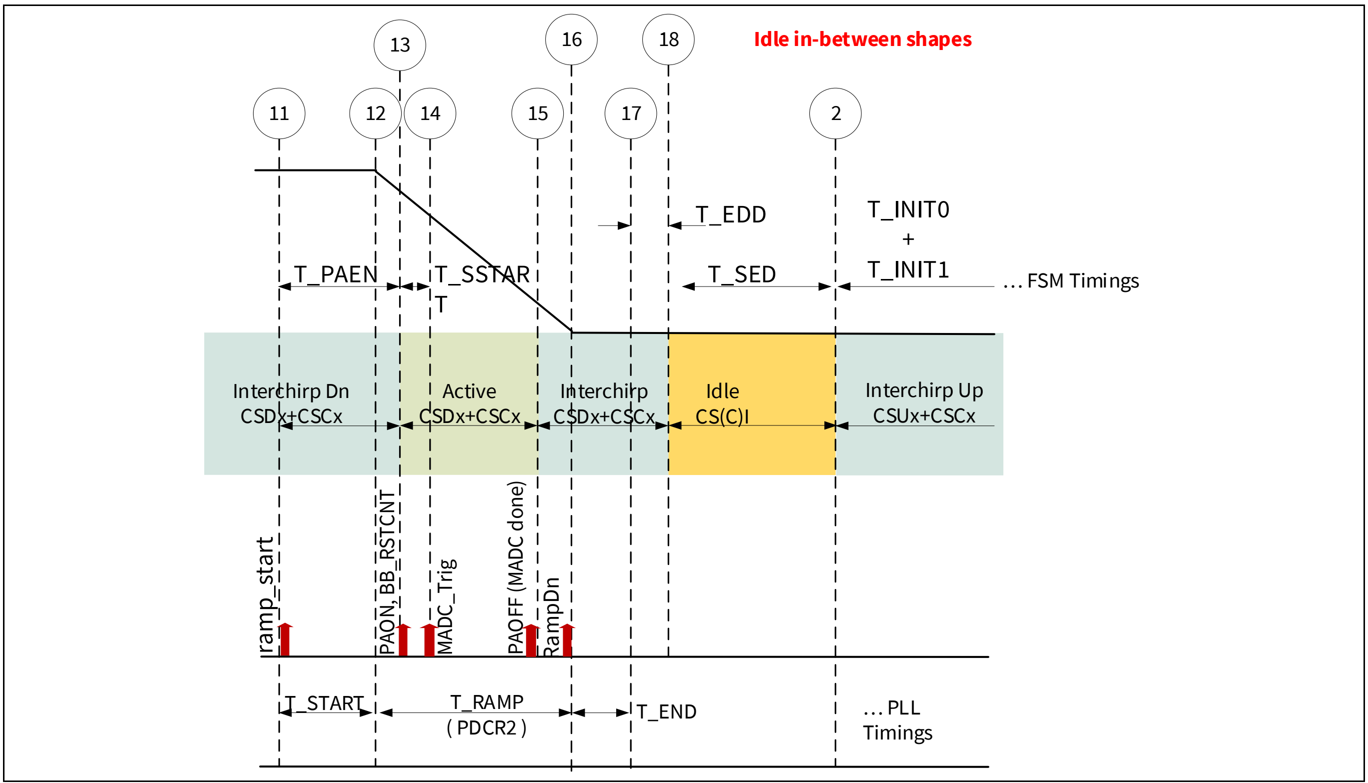


Figure 15 Idle mode after shape groups

Table 16 End of shape and interchirp in-between shapes

From #	To #	Description	Signals	Related time
#11		Interchirp Dn mode is programed here (CSDx + CSCx).		
#11		FSM generates ramp_start signal.	Ramp_start	
		PLL related:		
#11	#12	Preparation for Downchirp.		T_START
#12	#16	Downchirp time.		T_RAMP
#16	#17	Some delay after Downchirp is completed.		T_END
		FSM related:		
#11	#13	Some delay (see above T_PAEN).		T_PAEN
#13		**Active mode** is entered with settings from previous Interchirp Dn mode (CSDx+CSCx).		
#13		PA is enabled (PAON). Host make sure that PA is not ON before the chirp starts (>#12).	PAON	
#13		Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value.		
#13	#14	During this phase the baseband can settle		T_SSTART
#14	#15	MADC starts acquiring the given number of samples (PLLx:APD in section 4.16). See section 3.4.	MADC_TRIG	T_ACQDx
#15		MADC has completed the acquisition of the expected number of samples.	MADC_ DONE	
#15		PA is disabled (PAOFF)	PAOFF	

From #	To #	Description	Signals	Related time
		This condition must be reached before #16 The condition is: T_PAEN + T_SSTART + T_ACQDx > T_START + T_RAMPx.		
#15		**Interchirp Dn mode** is activated again here (CSDx + CSCx).		
#14	#16	FSM waits for PLL if ramp down to calculate #17 (TMREND).		
#16		PLL signals the end of the Downchirp (ramp progress).	RampDN	
#17	#18	Time delay programmed by the host.		T_EDD
#18	#2	Time programed by the host to stay in Idle mode.		T_SED
#2		Same state #2 as in Figure 13 starts here.		

3.3.6.2 Interchirp in-between Shapes

Interchirp between shapes can be set when the required gap between two shapes is relativly small (< 25 µs).

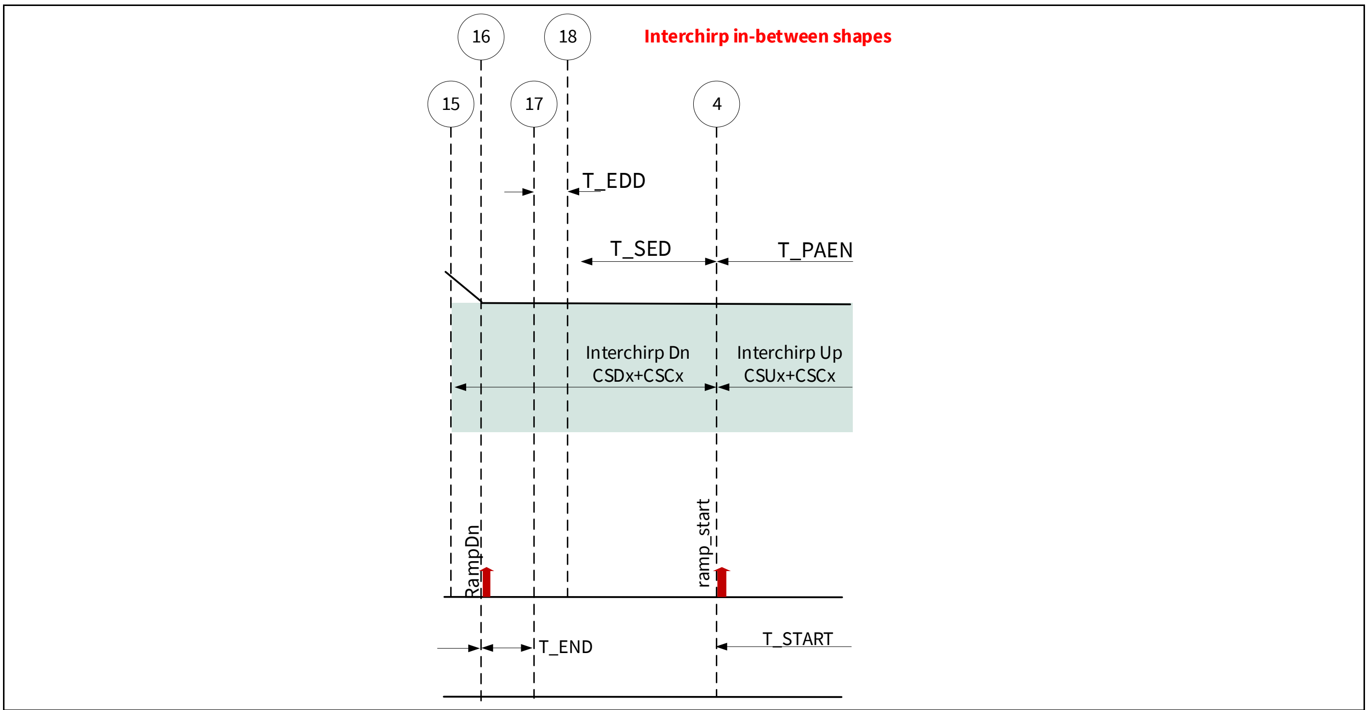


Figure 16 Interchirp in-between shapes

Table 17 Interchirp in-between shapes

From #	To #	Description	Signals	Related time
#15		Interchirp Dn (CSDx + CSCx) is activated after Active mode.		
#16		PLL signals the end of the Downchirp (ramp progress).	RampDN	
#16	#17	Some delay after Downchirp is completed.		T_END
#17		PLL has completed its action.		
#17	#18	Time delay programmed by the host.		T_EDD
#18	#4	The chip will remain in the same interchirp power state for the provided amount of time (T_EDD).		T_SED
#4		Same state #4 as in Figure 13 starts here.		

From #	To #	Description	Signals	Related time
#4		Interchirp Up mode programed by FSM here (CSUx + CSCx).		

3.3.6.3 Deep Sleep Continuous + Idle wake-up after shape groups

In Deep Sleep Cont(inuous) mode after the shape group is completed, the FSM wakes up automatically after the programed time T_SED. The internal clock is kept running during this time. Deep Sleep Cont is the only deep sleep power mode possible between shape groups.

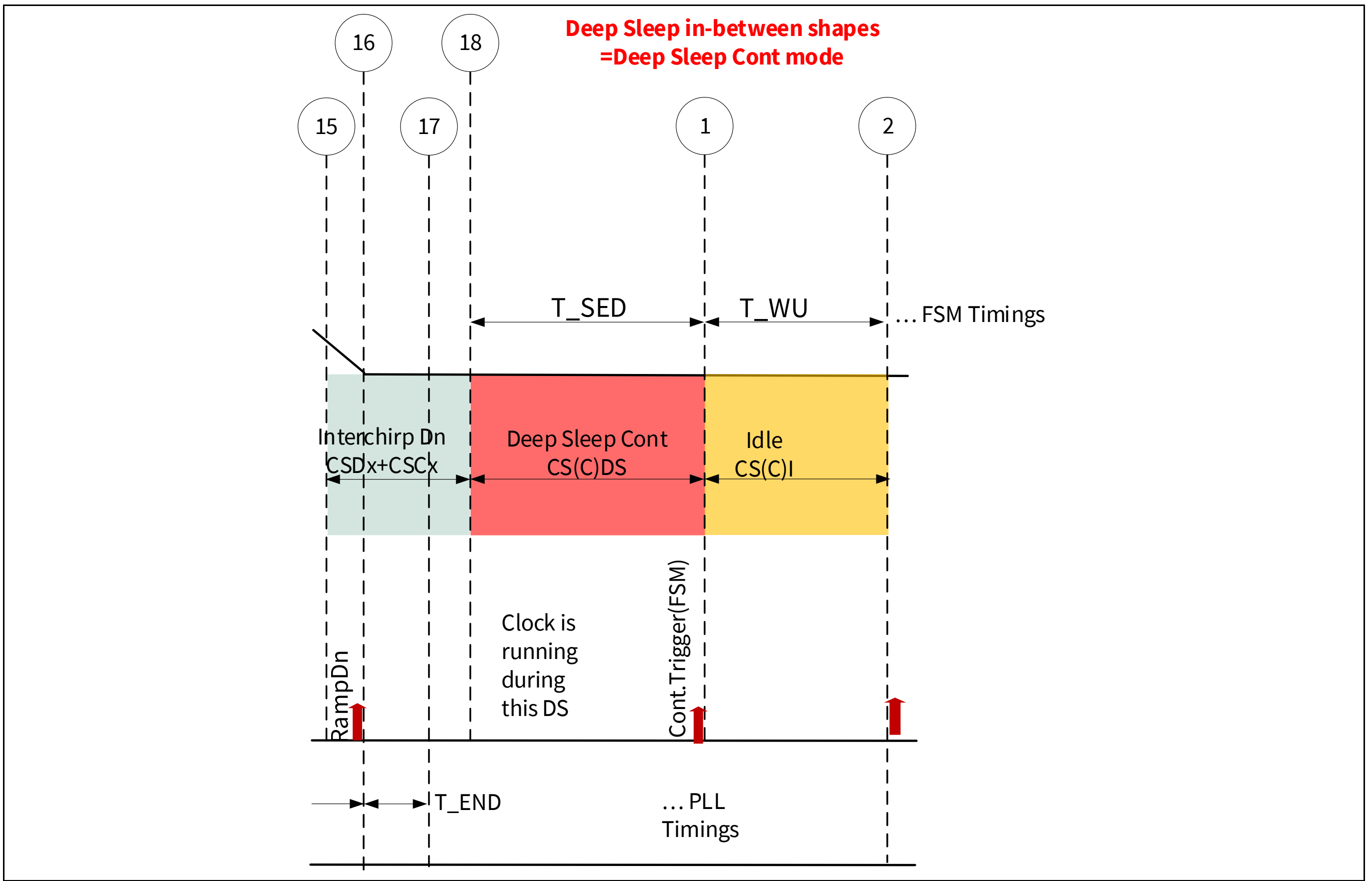


Figure 17 **Deep Sleep + Idle wake-up after shape groups**

Table 18 Deep Sleep Cont + Idle wake-up after shape groups

From #	To #	Description	Signals	Related time
#16	#17	Some delay after Downchirp is completed.		T_END
#17		PLL is completed its action.		
#17	#18	Time delay programmed by the host.		T_EDD
#17		Deep Sleep Cont mode is enabled. The difference to the normal Deep Sleep mode is, the f_{SYS_CLK} is kept running to count the internal timers.		
#17		The internal system clock f_{SYS_CLK} is kept running.		
#18	#1	The chip will be in Deep Sleep Cont mode.		T_SED
#1		Continuous trigger coming from the FSM.		
#1		Same start-up procedure as Figure 13starts here.		

3.4 System Constraints

3.4.1 MADC Sampling Timing Conditions and Calculations

The number of MADC samples during a frequency chirp (up or down segment of the shape) shall fulfil some specific requirements.

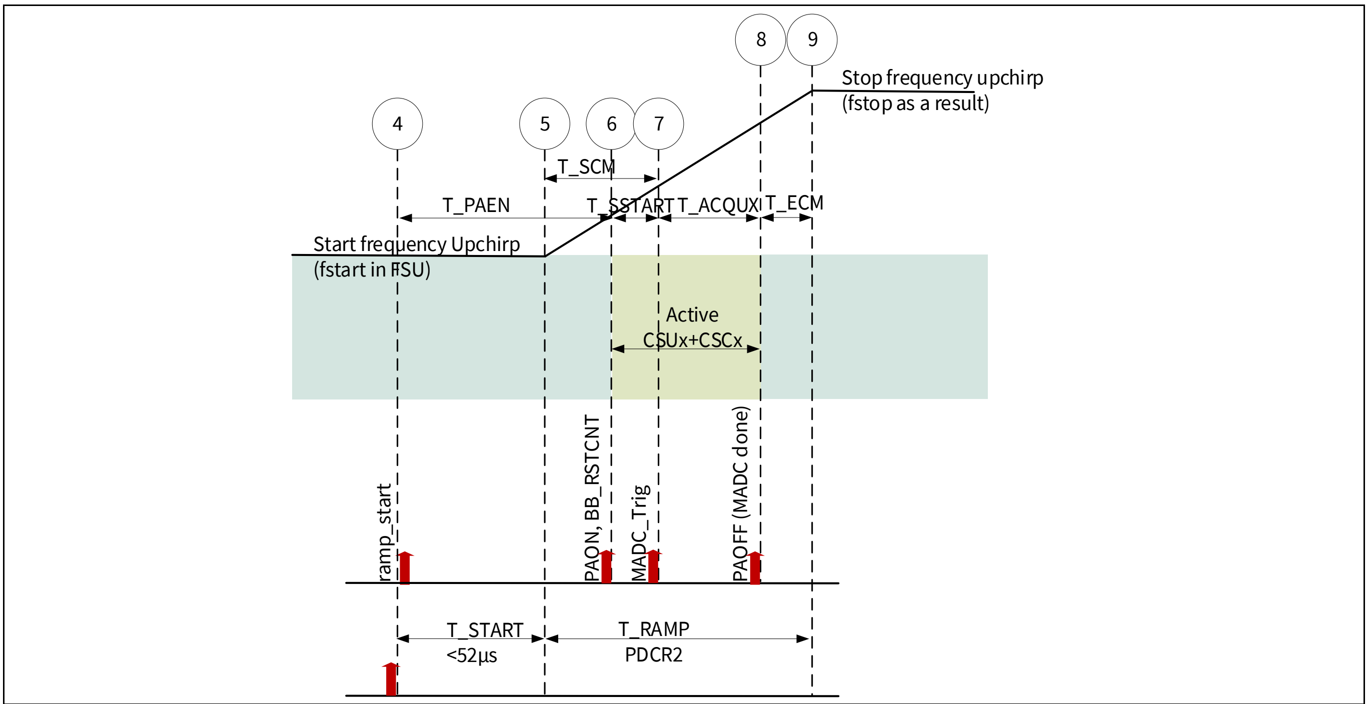


Figure 18 T_RAMP timing conditions

Table 19 T_RAMP Timing Conditions

From #	To #	Description	Signals	Related time
#4		PLL starts counting.		
#4	#5	PLL starts.		T_START
#5	#9	PLL performs the frequency Upchirp, chirp from fstart (PLLx[1]:FSU) to fstop.		T_RAMP
#6	#8	Active Phase.		
#4	#7	Time to start the MADC.		T_PAEN+T_SSTART
#7	#8	MADC sampling time for Upchirp raw data.		T_ACQUX
#8	#9	End chirp margin T_ECM is needed to avoid transmission out of band. Empirically derived in System.		T_ECM
#5	#7	Start chirp margin T_SCM is needed to avoid transmission out of band. Empirically derived in System.		T_SCM

ADC Sampling Rate f_{ADC_SAMP} (see section 8.5.5):

$$f_{ADC\_SAMP} = f_{ADC\_CLK} / ADC\_DIV$$

ADC acquisition time for Upchirp T_ACQUx:

$$T\_ACQUx = APUx / f_{ADC\_SAMP}$$

Where APU is the number of samples.

End chirp margin T_ECM is tested in system but assumed to be more than 0 µs:

$$T\_ECM > 0\mu s,\ T\_SCM > 0\ \mu s$$

Condition on the data acquisition start time:

$$T\_PAEN + T\_SSTART > T\_START$$

Considering the start chirp margin TCM at the beginning:

$$T\_PAEN + T\_SSTART - T\_SCM = T\_START$$

Overall timing equation:

$$T\_PAEN + T\_SSTART + T\_ACQUx + T\_ECM = T\_START + T\_RAMP$$

Example, Fixed number of samples:

In case the user expects a fixed number of samples, the APU is set and T_RAMP is calculated.

The time for a frequency ramp T_RAMP is:

T_RAMP (PLLx2#:RTU in section 4.16) **= T_PAEN + T_SSTART + T_ACQUx + T_ECM – T_START**

Example, Fixed chirp-time (T_RAMP):

$$T\_ACQUx = T\_RAMP - (T\_SCM + T\_ECM)$$

$$APU = (T\_ACQUx * f_{ADC\_SAMP}),$$

APU (PLLx3#:APU in section 4.16) **= (T_RAMP – (T_SCM + T_ECM)) *(f_{SYS_CLK} / ADC_DIV)**

3.4.2 PLL Frequency Ramp Setup

The RF frequency ramps generated by the PLL are controlled through the PLLx registers (see section 4.16), where the bit fields FSU, RSU and RTU control the Upchirp of a shape and the registers FSD, RSD and RTD control the down chirp of a shape. The following description refers only to up chirp ramp setup. The given formulas can be adopted to down chirp ramps by replacing FSU by FSD, RSU by RSD and RTU by RTD.

Each RF frequency ramp is defined by the start frequency programmed to FSU, the ramp slope programmed to RSU and the ramp time programmed to RTU. It must be noted that the slope in RSU is specified as frequency increment per clock cycle while the ramp time in RTU is specified as number of steps where a single step means 8 clock cycles. The relation between RSU and RTU is shown in Figure 19.

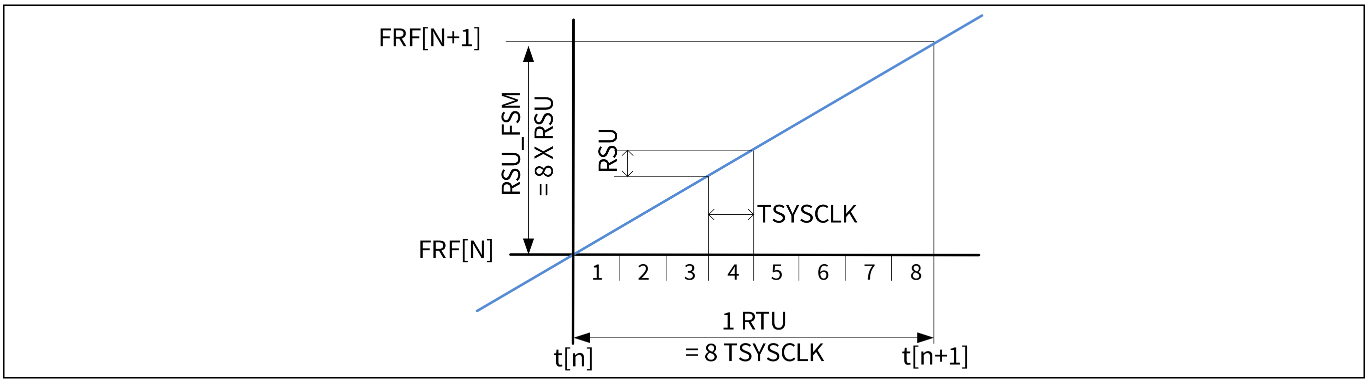


Figure 19 Relationship between RTU and RSU

The value N_{FSU} that is programmed to FSU bit field to control the ramp start frequency is a signed 2's complement number in the range of $[-2^{23} \dots (2^{23}-1)]$. The relation between the RF frequency f_{RF} and N_{FSU} is given by:

$$f_{RF} = 8 f_{SYSCLK} \left[4(N_{DIVSET} + 2) + 8 + \frac{N_{FSU}}{2^{20}} \right]$$

where f_{SYSCLK} is the frequency of the reference clock oscillator (typically 80 MHz) and N_{DIVSET} is the value programmed to the bit field DIVSET in register PACR2 (default 20, see section 4.7). Accordingly the value N_{FSU} can be calculated by this formula:

$$N_{FSU} = 2^{20} \left[\frac{f_{RF}}{8 f_{SYSCLK}} - 4(N_{DIVSET} + 2) - 8 \right]$$

The value N_{RSU} that is programmed to RSU bit field to control the frequency increment per clock cycle is also a signed 2's complement number in the range of $[-2^{23} \dots (2^{23}-1)]$. The relation between the RF frequency increment Δf_{RF} and N_{RSU} is given by:

$$\Delta f_{RF} = 8 f_{SYSCLK} \frac{N_{RSU}}{2^{20}}$$

or

$$N_{RSU} = 2^{20}\frac{\Delta f_{RF}}{8f_{SYSCLK}}.$$

Note:

Both slope bit fields RSU and RSD can hold positive and negative values, so an up chirp can also be programmed with a falling ramp and a down chirp can be programmed with a rising ramp. The naming convention "up chirp" and "down chirp" are based on the assumption that a triangle shape always starts with the rising ramp. Therefore, regardless of the actual ramp slope the up-chirp registers always refer to the first chirp of a shape and the down chirp registers always refer to the 2nd chirp of a shape in triangle mode.

PLL Setup Example 1 ($f_{SYSCLK} = 80MHz$)

With a reference clock frequency of 80 MHz the recommended value for N_{DIVSET} is 20, the default values. With these parameters the conversion formulas simplify to:

$$N_{FSU} = 2^{20}\left[\frac{f_{RF}}{640\ \text{MHz}} - 96\right]$$

and

$$N_{RSU} = 2^{20}\frac{\Delta f_{RF}}{640\ \text{MHz}}$$

.

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is $56.32\ GHz \leq f_{RF} \leq 66.559\ GHz$. This may be a wider range than the effectively achievable frequency range (see section 6 for PLL specification).

To achieve a frequency ramp from 58 GHz to 62 GHz in 36 µs, the FSU register is programmed to:

$$N_{FSU} = 2^{20}\left[\frac{58\ \text{GHz}}{640\ \text{MHz}} - 96\right] = -5636096 \mathrel{\widehat{=}} AA0000_{hex}.$$

The ramp time bit field RTU is programmed to:

$$N_{RTU} = \frac{t_{ramp}}{8T_{SYSCLK}} = 36\ \mu s\frac{80\ MHz}{8} = 360.$$

The frequency increment per clock cycle result to:

$$\Delta f_{RF} = \frac{f_{RF,end} - F_{RF,start}}{8N_{RTU}} = \frac{62\ GHz - 58\ GHz}{8*360} = \frac{4\ GHz}{2880} = 1.389MHz.$$

Accordingly the bit field RSU is programmed to:

$$N_{RSU} = 2^{20}\frac{1.389MHz}{640\ \text{MHz}} = 2275.8 \cong 2276 \mathrel{\widehat{=}} 0008E4_{hex}$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{RF,end} = f_{RF,start} + 8 * N_{RTU} * \frac{640\ MHz}{2^{20}} N_{RSU} = 62.000781GHz.$$

PLL Setup Example 2 ($f_{SYSCLK} = 76.8MHz$)

With a reference clock frequency of 76.8 MHz the recommended value for N_{DIVSET} is 21. With these parameters the conversion formulas simplify to:

$$N_{FSU} = 2^{20}\left[\frac{f_{RF}}{614.4\ \text{MHz}} - 100\right]$$

and

$$N_{RSU} = 2^{20}\frac{\Delta f_{RF}}{614.4\ \text{MHz}}$$

.

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is $56.5248\ GHz \leq f_{RF} \leq 66.3552\ GHz$. This may be a wider range than the effectively achievable frequency range (see section 6 for PLL specification).

To achieve a frequency ramp from 58 GHz to 62.0 GHz in 36 µs, the FSU register is programmed to:

$$N_{FSU} = 2^{20}\left[\frac{58\ \text{GHz}}{614.4\ \text{MHz}} - 100\right] = -5870933.\overline{3} \cong -5870933 \mathrel{\widehat{=}} A66AAB_{hex}.$$

The ramp time bit field RTU is programmed to:

$$N_{RTU} = \frac{t_{ramp}}{8T_{SYSCLK}} = 36\mu s\frac{76.8\ MHz}{8} = 345.6 \cong 346.$$

The frequency increment per clock cycle result to:

$$\Delta f_{RF} = \frac{f_{RF,end} - F_{RF,start}}{8N_{RTU}} = \frac{62\ GHz - 58\ GHz}{8*346} = \frac{4\ GHz}{2768} = 1.44509MHz.$$

Accordingly the bit field RSU is programmed to:

$$N_{RSU} = 2^{20}\frac{1.44509\ MHz}{614.4\ \text{MHz}} = 2466.28 \cong 2466 \mathrel{\widehat{=}} 0009A2_{hex}.$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{RF,start} = 614.4\ \text{MHz}\left[100 + \frac{N_{FSU}}{2^{20}}\right] = 58.0000002GHz$$

$$f_{RF,end} = f_{RF,start} + 8 * N_{RTU} * \frac{614.4MHz}{2^{20}}N_{RSU} = 61.99954GHz.$$

4 BGT60ATR24C Registers

An array of registers visible via the SPI is used to control and program the states of the different blocks inside the chip.

4.1 Register List

The registers are arranged in blocks of 24 bits each. Each block is identified by its unique address. The registers are accessed from the SPI module. The bit fields from each register are arranged in MSB first order.

Table 20 The following table gives an overview on the BGT60ATR24C registers. Register Overview / Address Table

Register Address	Register Name	Description	RST	Section
0x00	MAIN	Main register		4.2
0x01	ADC0	MADC control register		4.3
0x02	CHIP_VERSION	Digital and RF version		4.4
0x03	STAT1	Status register 1		4.5
0x04	PACR1	PLL analog control register 1		4.6
0x05	PACR2	PLL analog control register 2		4.7
0x06	SFCTL	SPI and FIFO Control		4.8
0x07	SADC_CTRL	Sensor ADC ctrl reg		4.9
0x08	CSI_0	Channel set idle mode 0		4.10
0x09	CSI_1	Channel set idle mode 1		4.10
0x0A	CSI_2	Channel set idle mode 2		4.10
0x0B	CSCI	Channel set control idle mode		4.11
0x0C	CSDS_0	Channel set deep sleep mode 0		4.10
0x0D	CSDS_1	Channel set deep sleep mode 1		4.10
0x0E	CSDS_2	Channel set deep sleep mode 2		4.10
0x0F	CSCDS	Channel set control deep sleep mode		4.11
0x10	CSU1_0	Channel set 1 (up)		4.10
0x11	CSU1_1	Channel set 1 (up)		4.10
0x12	CSU1_2	Channel set 1 (up)		4.10
0x13	CSD1_0	Channel set 1 (down)		4.10
0x14	CSD1_1	Channel set 1 (down)		4.10
0x15	CSD1_2	Channel set 1 (down)		4.10
0x16	CSC1	Channel set control 1 (up/dn)		4.11
0x17	CSU2_0	Channel set 2 (up)		4.10
0x18	CSU2_1	Channel set 2 (up)		4.10
0x19	CSU2_2	Channel set 2 (up)		4.10
0x1A	CSD2_0	Channel set 2 (down)		4.10
0x1B	CSD2_1	Channel set 2 (down)		4.10
0x1C	CSD2_2	Channel set 2 (down)		4.10

0x1D	CSC2	Channel set control 2 (up/dn)		4.11
0x1E	CSU3_0	Channel set 3 (up)		4.10
0x1F	CSU3_1	Channel set 3 (up)		4.10
0x20	CSU3_2	Channel set 3 (up)		4.10
0x21	CSD3_0	Channel set 3 (down)		4.10
0x22	CSD3_1	Channel set 3 (down)		4.10
0x23	CSD3_2	Channel set 3 (down)		4.10
0x24	CSC3	Channel set control 3 (up/dn)		4.11
0x25	CSU4_0	Channel set 4 (up)		4.10
0x26	CSU4_1	Channel set 4 (up)		4.10
0x27	CSU4_2	Channel set 4 (up)		4.10
0x28	CSD4_0	Channel set 4 (down)		4.10
0x29	CSD4_1	Channel set 4 (down)		4.10
0x2A	CSD4_2	Channel set 4 (down)		4.10
0x2B	CSC4	Channel set control 4 (up/dn)		4.11
0x2C	CCR0	Chirp control register 0		4.12
0x2D	CCR1	Chirp control register 1		4.13
0x2E	CCR2	Chirp control register 2		4.14
0x2F	CCR3	Chirp control register 3		4.15
0x30	PLL1_0	FSU1 – shape 1		4.16
0x31	PLL1_1	RSU1 – shape 1		4.16
0x32	PLL1_2	RTU1 – Shape 1		4.16
0x33	PLL1_3	AP1 – shape 1		4.16
0x34	PLL1_4	FSD1 – shape 1		4.16
0x35	PLL1_5	RSD1 – shape 1		4.16
0x36	PLL1_6	RTD1 – shape 1		4.16
0x37	PLL1_7	SCR – shape 1		4.17
0x38	PLL2_0	FSU1 – shape 2		4.16
0x39	PLL2_1	RSU1 – shape 2		4.16
0x3A	PLL2_2	RTU1 – shape 2		4.16
0x3B	PLL2_3	AP1 – shape 2		4.16
0x3C	PLL2_4	FSD1 – shape 2		4.16
0x3D	PLL2_5	RSD1 – shape 2		4.16
0x3E	PLL2_6	RTD1 – shape 2		4.16
0x3F	PLL2_7	SCR – shape 2		4.17
0x40	PLL3_0	FSU1 – shape 3		4.16
0x41	PLL3_1	RSU1 – shape 3		4.16
0x42	PLL3_2	RTU1 – shape 3		4.16
0x43	PLL3_3	AP1 – shape 3		4.16
0x44	PLL3_4	FSD1 – shape 3		4.16
0x45	PLL3_5	RSD1 – shape 3		4.16

0x46	PLL3_6	RTD1 – shape 3		4.16
0x47	PLL3_7	SCR – shape 3		4.17
0x48	PLL4_0	FSU1 – shape 4		4.16
0x49	PLL4_1	RSU1 – shape 4		4.16
0x4A	PLL4_2	RTU1 – shape 4		4.16
0x4B	PLL4_3	AP1 – shape 4		4.16
0x4C	PLL4_4	FSD1 – shape 4		4.16
0x4D	PLL4_5	RSD1 – shape 4		4.16
0x4E	PLL4_6	RTD1 – shape 4		4.16
0x4F	PLL4_7	SCR – shape 4		4.17
0x55	RFT0	RF test register 0		4.19
0x56	RFT1	RSVD		4.20
0x57	DFT0	DFT register 0		4.21
0x58	DFT1	DFT register 1		4.22
0x59	PLL_DFT0	PLL DFT register 0		4.18
0x5D	STAT0	Status register 0		4.23
0x5E	SADC_RESULT	Sensor ADC result register		4.24
0x5F	FSTAT	FIFO status register		4.25
0x60	CHIP ID #1	Chip ID #1 register		4.26
0x61	CHIP ID #2	Chip ID #2 register		4.27
>= 0x62		FIFO access		

Note: Reserved bits (RSVD) in the registers should not be modified. They should be kept in the default/reset state unless otherwise specified.

4.1.1 Abbreviations

Access modes on the registers:

- R … Readable register or bit field
- W … Writeable register or bit field
- W1C … Writeable register or bit field, cleared by Hardware
- RSVD … Reserved value which is not assigned at the moment

4.2 MAIN – Main Register

This register controls the top-level behavior of the chip.

Register MAIN

<table>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>LDO_MODE</td><td colspan="2">LOAD_STRENGTH</td><td colspan="2">MADC_BG_CLK_DIV</td><td colspan="2">SADC_BG_CLK_DIV</td><td>CW_MODE</td><td colspan="4">TR_WKUP_MUL</td><td colspan="8">TR_WKUP</td><td>FIFO_RESET</td><td>FSM_RESET</td><td>SW_RESET</td><td>FRAME_START</td></tr>
</table>

Figure 20 MAIN register

Table 21 MAIN: Register Description

Symbol	**Bits**	**Type**	**Description**	**RST**
LDO_MODE	23	RW	The LDO settling time is defined by the LDO_MODE: 0_B … Low power (50 µA), slow settling time 1_B … High power (100 µA), fast settling time	0_B
LOAD_STRENGTH	22:21	RW	Current spikes, overshoots and undershoots can occur on the VDDC during FSM transitions. Those can be smooth by applying a dummy load at the output of the LDO: 0_D … Disabled 1_D … 100 µA (current in the dummy load) 2_D … 200 µA (current in the dummy load) 3_D … 400 µA (current in the dummy load)	0_D
MADC_BG_CLK_DIV	20:19	RW	MADC Bandgap clock divider Bandgap clock frequency divider value: 0_D … Bandgap clock off 1_D … Divider value is 1 2_D … Divider value is 2 3_D … Divider value is 4 Note: not “clock tree balanced”	3_D
SADC_BG_CLK_DIV	18:17	RW	SADC Bandgap clock divider Bandgap clock frequency divider value: 0_D … SADC clock off 1_D … Divider value is 1 2_D … Divider value is 2 3_D … Divider value is 4 Note: not “clock tree balanced”	3_D

Symbol	Bits	Type	Description	RST
CW_MODE	16	RW	Set to 1_B: “Continuous Wave” mode: no shapes are executed but PLL / RF / ADC runs with values programmed in PDFT [0,1] registers and CS1.	0_B
TR_WKUP_MUL	15:12	RW	Timer multiplier factor for wake-up time delay T_WU. Precise formula provided under MAIN:TR_WKUP	0_D
TR_WKUP	11:4	RW	Coefficient to calculate T_WU: 0_D … T_{SYS_CLK} From 1_D to 255_D the time delay T_WU is calculated as follows: If TR_WKUP > 0, then the time delay is T_WU = (TR_WKUP x 2^TR_WKUP_MUL x 8 + TR_WKUP_MUL +3) x $_{TSYS\_CLK}$. In typical use-case T_WUTYP = 1ms.	0_D
FIFO_RESET	3	W1C	Clears and resets data_fifo: 0_B … No change 1_B … Reset the FIFO and return back to 0	0_B
FSM_RESET	2	W1C	Control FSM reset: 0_B … No change 1_B … Reset the control FSM and return back to 0_B	0_B
SW_RESET	1	W1C	Software reset: 0_B … No change 1_B … Reset the register settings and return back to 0_B	0_B
FRAME_START	0	W1C	Starts frame generation. After the frame generation is started writing 1_B: 0_B … No effect 1_B … Starts the frame generation It can be stopped by an FSM_RESET.	0_B

4.3 ADC0 – MADC Control Register

The bits in this register are used to set properly the ADCs in the Rx chain.

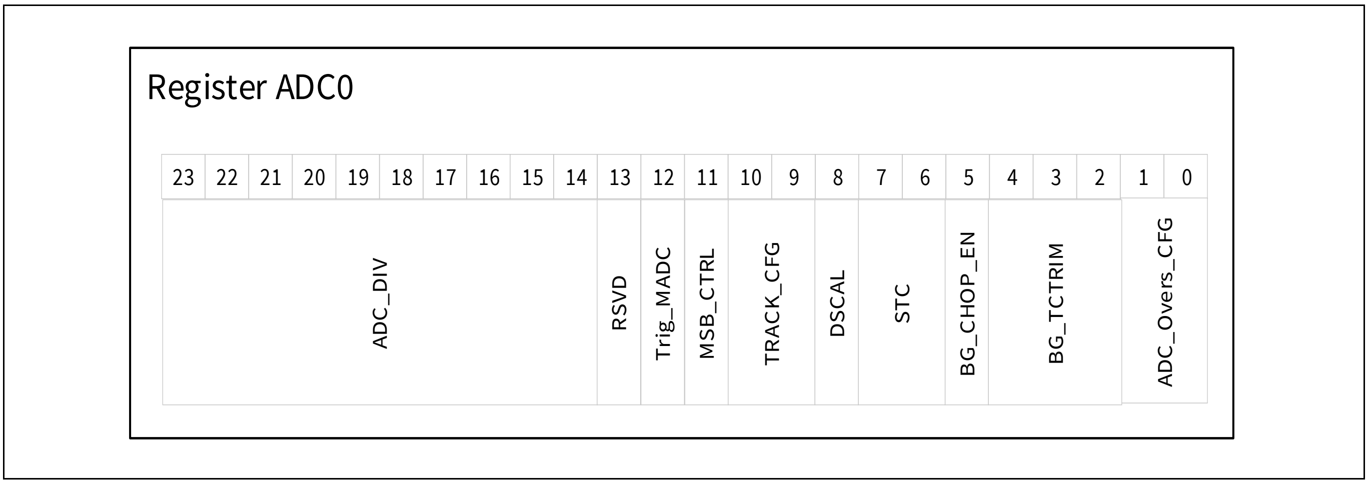


Figure 21 ADC0 register

Table 22 **ADC0: Register Description**

Symbol	Bits	Type	Description	RST
ADC_DIV	23:14	RW	Sampling frequency divider value. The actual sampling frequency will be $f_{ADC\_SAMP} = f_{ADC\_CLK} / ADC\_DIV$: 20_D … minimum divider value → f_{ADC_SAMP}= 4 Msps 33_D … typical value → f_{ADC_SAMP}= 2.42 Msps 1023_D … max divider value → f_{ADC_SAMP}= 78.201 ksps	40_D
RSVD	13	RW	RSVD	0_B
TRIG_MADC	12	W1C	Test mode feature for single measurement acquisition. The results can be read through the test bits in registers ADC1 to ADC5: 0_B … Return value after trigger is captured internally 1_B … Single trigger event	0_B
MSB_CTRL	11	RW	MSB decision time selection during calibration and conversion: 0_B … Single MSB decision time 1_B … Doubled MSB decision time	0_B
TRACK_CFG	10:9	RW	Tracking conversion configuration bits: 0_D … No sub conversions are executed and averaged 1_D … 1 sub conversion 2_D … 3 sub conversions 3_D … 7 sub conversions	1_D
DSCAL	8	RW	Disable Startup calibration: 0_B … startup calibration is enabled 1_B … startup calibration is disabled	0_B
STC	7:6	RW	Sample time control: 0_D … 50 ns 1_D … 100 ns 2_D … 200 ns 3_D … 400 ns	1_D
BG_CHOP_EN	5	RW	Enable chopping within the bandgap. 0_B … No chopping enabled 1_B … Chopping enabled	0_B
BG_TC_TRIM	4:2	RW	Static temperature coefficient trimming 0_D … Min. value 7_D … Max. value	0_D
ADC_OVERS_CFG	1:0	RW	Oversampling configuration: $=00_B$ Standard single 11 bits conversion Note: Oversampling must be set to “00_B”	00_B

4.4 CHIP_VERSION

The register CHIP_VERSION provides information regarding the digital code version, the RF block version, and the RF configuration (number of TX/RX channels).

It is used by the driver to configure the device properly according to the info above.

Register CHIP_ID

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								DIGITAL_ID								RF_ID							

Figure 22 CHIP_ID register

Table 23 CHIP_ID: Register Description

Symbol	Bits	Type	Description	RST
RSVD	23:16	R	Reserved	0_D
DIGITAL_ID	15:8	R	5_D … BGT60ATR24C	5_D
RF_ID	7:0	R	4_D … 2ch Tx, 4ch Rx	4_D

4.5 STAT1 - Status Register1

The status register provides internal counter values for the actual number of frames and shapes. They are also provided to the data header. However, it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 µs.

Register STAT1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_CNT												SHAPE_GRP_CNT											

Figure 23 STAT1: status register 1

Table 24 STAT1: Register Description

Symbol	Bits	Type	Description	RST
FRAME_CNT	23:12	R	Frame counter value: 0_D … Reset value / after max. value rollover 4095_D … Max. value *Note: This field is for debug only. FRAME_CNT info should not be used when endless mode enabled (please check CCR2:MAX_FRAME_CNT)*	0_D
SHAPE_GRP_CNT	11:0	R	Shape group counter counts the actual shape groups:	0_D

Symbol	Bits	Type	Description	RST
			0_D … Reset value / after max. value for SHAPE_GRP_CNT reached 4095_D … Max. value	

Note:

1. *A shape consists of an "Up Chirp" segment and a "Down Chirp" segment.*
2. *A sawtooth shape is generated by an "Up Chirp" and a "Fast Down Chirp".*
3. *There is no data acquisition in the "Fast Down Chirp".*

4.6 PACR1: PLL Analog Control Registers 1

The bits in this register are used to properly set the PLL.

Register PACR1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSCCLKEN	LFEN	CPEN	BIASFORC	ICPSEL			LOCKFORC	LOCKSEL			RSVD	RLFSEL	RFILTSEL	VREFSEL		U2IEN	BGAPEN	VDIGREG		DIGPON	VANAREG		ANAPON

Figure 24 PACR1 register

Table 25 PACR1: Register Description

Symbol	Bits	Type	Description	RST
OSCCLKEN	23	RW	Enable clock path for system clock: 0_B … Clock off 1_B … Clock path active by default this is disabled This bit is controlled by FSM during operation. After deep sleep this bit should be enabled by the host. Before the MAIN: FRAME_START is raised the OSCCLKEN should be enabled!	0_B
LFEN	22	RW	Enable loop filter: 0_B … Off(default) 1_B … On	0_B
CPEN	21	RW	Enable charge pump: 0_B … Off(default) 1_B … On	0_B
BIASFORC	20	RW	Use fixed biasing inside charge pump (= disable bias reg. loop): 0_B … Fixed biasing off = bias regulation loop active (default) 1_B … Fixed biasing on = bias regulation loop deactivated	1_B

ICPSEL	19:17	RW	Select charge pump current: 0_D … 40 µA 1_D … 80 µA 2_D … 120 µA 3_D … 160 µA 4_D … 200 µA (default) 5_D … 240 µA 6_D to 7_D … 280 µA	4_D
LOCKFORC	16	RW	Force lock signal to high: 0_B … Lock signal not forced 1_B … Lock forced to high	1_B
LOCKSEL	15:13	RW	Select lock detection range/window: 0_B … 265 ps 4_B … 2 ns 1_B … 500 ps 5_B … 2.8 ns 2_B … 1 ns 6_B … 3.8 ns 3_B … 1.5 ns (default) 7_B … 4.6 ns	3_D
RSVD	12	RW	Reserved Read as 0_B, must be written with 0_B.	0_B
RLFSEL	11	RW	Select Rlf inside the loop filter: 0_B … Rlf= 5 kOhm (default) 1_B … Rlf= 7 kOhm	0_B
RFILTSEL	10	RW	Select Rfilt of the reference filter: 0_B … Rfilt= 100 kOhm 1_B … Rfilt= 1 MOhm (default) Switch together with CPEN from 0_d to 1_d to improve start-up time!	1_B
VREFSEL	9:8	RW	Select reference voltage/common mode level of loop filter: 0_D … 433mV 1_D … 506mV (default) 2_D … 578mV 3_D … 650mV	1_D
U2IEN	7	RW	Enable voltage-to-current-converter: 0_B … off (default) 1_B … on	0_B
BGAPEN	6	RW	Enable bandgap reference: 0_B … off (default) 1_B … on	0_B
VDIGREG	5:4	RW	Program output voltage of dig-regulator: 0_D … 1.44 V 1_D … 1.5 V 2_D … 1.55 V(default) 3_D … 1.60 V (@Vbg=1.2 V)	2_D
DIGPON	3	RW	Enable dig-regulator: 0_B … Power off (default) 1_B … Power on	0_B

VANAREG	2:1	RW	Program output voltage of ana-regulator: 0_D ... 1.44 V 1_D ... 1.5 V 2_D ... 1.55 V (default) 3_D ... 1.60 V (@Vbg=1.2 V)	2_D
ANAPON	0	RW	Enable analog-regulator: 0_B … Power off (default) 1_B … Power on	0_B

4.7 PACR2: PLL Analog Control Registers 2

The bits in this register are used to properly set the PLL.

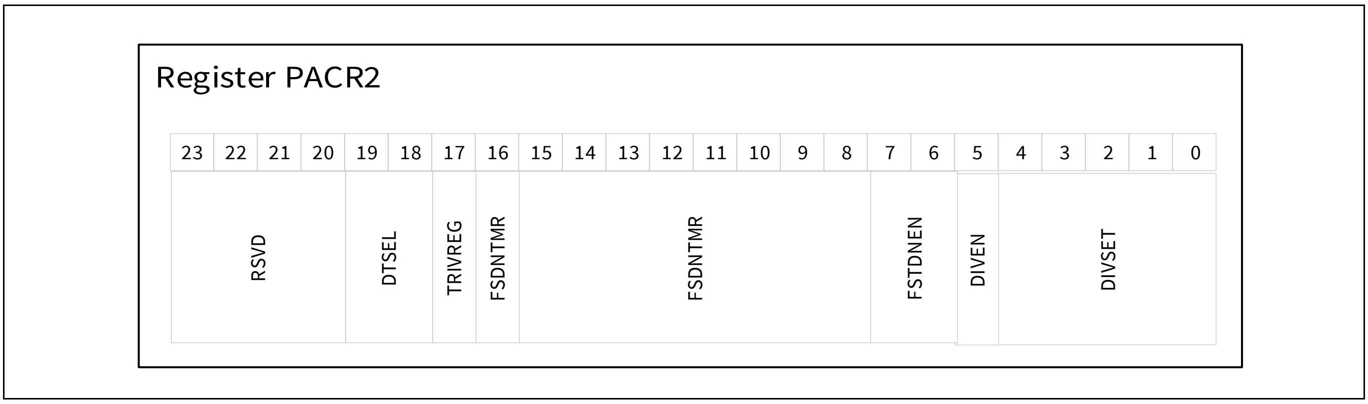


Figure 25 PACR2 PLL register

Table 26 PACR2: Register Description

Symbol	Bits	Type	Description	RST
RSVD	23:20	RW	Reserved	0_D
DTSEL	19:18	RW	Set PFD dead time / dead zone: 0_D ... 180ps to 350ps 1_D ... 270ps to 510ps (default) 2_D ... 360ps to 680ps 3_D ... 450ps to 840ps	1_D
TRIVREG	17	RW	Set regulator off-state to tristate (for both ana- & dig-regulator): 0_B ... Off state is 0.0V (default) 1_B ... Off state is to tristate (setting active for dig-regulator if DIGPON = 0_B; setting active for ana-regulator if ANAPON= 0_B)	0_B
FSDNTMR	16:8	RW	Defines the time for the PLL loop filter discharge during fast down chirp operation. When FSTDNTMR = 0_D and FSTDNEN is ≠ 0_D, the fast down chirp length is internally assigned to a default value (@typ f_{SYS_CLK}): 0_D ... 500 ns if FSTDNEN = 1_D (discharge of the loop filter to the reference voltage set to PACR2:VREFSEL)	0_D

			0_D ... 700 ns if FSTDNEN = 2_D (discharge of the loop filter in a defined time window) 0_D ... 300 ns if FSTDNEN = 3_D For FSTDNTMR > 0_D the discharge time will be T_{SYS_CLK} × (FSDNTMR+1):1_D ... 25 ns 2_D ... 37.5 ns … 511_D ... 6.4 µs Suggested settings for the discharge time: PACR2: FSDNTMR= 5_D Together with: PACR2: FSTDNEN= 2_D Depending on the specific modulation bandwidth set, specific settings can be defined.	
FSTDNEN	7:6	W	FAST DOWN CHIRP enable (see Note below): 00_B ... Disable (default) 01_B ... Enable fast down chirp (mode 1) 10_B ... Enable fast down chirp (mode 2) 11_B ... Enable fast down chirp (mode 3) Suggested settings for the fast-down mode (active mode between chirps): PACR2: FSDNTMR= 5_D Together with: PACR2: FSTDNEN= 2_D Depending on the specific modulation bandwidth set, specific settings can be defined.	00_B
DIVEN	5	RW	Enable divider: 0_B ... Off: Input clock of divider and 80 MHz clock gated 1_B ... On: clocks released	0_B
DIVSET	4:0	RW	Set fixed part of integer division factor (consider offset of |2|). Default = 20_D, valid for a 80 MHz system clock. 21_D should be used for a 76.8 MHz system clock.	20_D

Note:

This bit field is typically used by the FSM. In case not used, the FSM switches the bit field back to the default value.

4.8 SFCTL – SPI and FIFO Control Register

This register is used to configure the SPI and FIFO.

Register SFCTL

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QSPI_WT				RSVD	PREFIX_EN	LFSR_EN	MISO_HS_RD	RSVD		FIFO_LP_MODE	FIFO_CREF												

Figure 26 SPI and FIFO Control Register

Table 27 SPI and FIFO Control: Register Description

Symbol	Bits	Type	Description	RST
QSPI_WT	23:20	RW	Number of QSPI wait cycles (see QSPI section): 0_D … 1 cycle delay 15_D … 16 cycles delay	7_D
RSVD	19	RW	RSVD	0_B
PREFIX_EN	18	RW	Enables the data header written into the FIFO prior to the sampling data of each chirp: 0_B … No prefix data header prior to chirp data 1_B … Prefix data header added prior to chirp data (see section 5.1 for data header)	0_B
LFSR_EN	17	RW	Enable LFSR register data generation: 0_B … Normal data acquisition, LFSR reset 1_B … LFSR data generation started LFSR should be enabled after a FIFO reset to ensure an empty FIFO (see also 5.11).	0_B
MISO_HS_RD	16	RW	0_B … MISO data is sent with falling edge of SPI CLK 1_B … MISO data is sent with rising edge (½ cycle earlier) Note: HS_RD = 0_B can only be used for a SPI clock < 25 MHz. For HS-transfer please check the timing of the SPI Master and adjust settings accordingly. The setting becomes active when the last bit of FSCTL is clocked out and it affects MISO immediately. See also section 5.3.1.	1_B
RSVD	15:14	RW	RSVD	0_B
FIFO_LP_MODE	13	RW	FIFO power mode: 0_B … FIFO permanently enabled 1_B … FIFO activated dynamically	0_B
FIFO_CREF	12:0	RW	FIFO compare reference: it defines the compare filling status for interrupt and CREF reporting When filling status is > FIFO_CREF an interrupt is issued:	0_D

Symbol	Bits	Type	Description	RST
			0_D … minimum value is 0, interrupt generated in case first sample is written into FIFO 8191_D … maximum value in case FIFO is full with 8192 memory locations eg. CREF = 0x1000 represents a 50% compare reference	

4.9 SADC_CTRL Sensor ADC Control Register

The bits in this register are used to properly set the sensor ADC (SADC) used to monitor the on chip sensor outputs, temperature and power, as well as some internal voltage nodes.

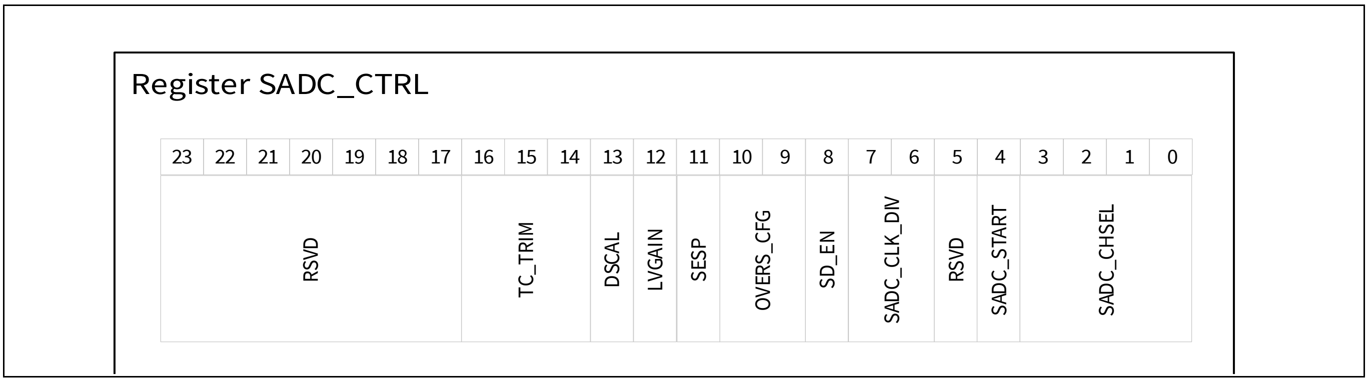


Figure 27 SADC_CRTL registers

Table 28 SADC_CRTL: Register Description

Symbol	Bits	Type	Description	RST
RSVD	23:17	RW	RSVD	0_D
TC_TRIM	16:14	RW	Bandgap trim value: 0_D … Min. trim value 7_D … Max. trim value	0_D
DSCAL	13	RW	Disable startup calibration: 0_B … Startup calibration enabled 1_B … startup calibration disabled	0_B
LVGAIN	12	RW	Sample configuration for LV channels: 0_B … Gain = 1.0 1_B … Gain = 0.75	0_B
SESP	11	RW	Spreaded early sampling point enable: 0_B … Disabled 1_B … Enabled	0_B
OVERS_CFG	10:9	RW	Oversampling configuration: 0_D … No oversampling → 8 bits resolution 1_D … Oversampling by 2 2_D … Oversampling by 4 → 9 bits resolution 3_D … Oversampling by 32 → 10 bits resolution	0_D
SD_EN	8	RW	Sigma delta loop enable: 0_B … Disabled	0_B

Table 28 SADC_CRTL: Register Description

Symbol	Bits	Type	Description	RST
			1_B … Enabled	
SADC_CLK_DIV	7:6	RW	SADC clock divider sets the clock for the sensing ADC. The divider value is defined as: 0_D … divider value is 1 (80MHz e.g.) 1_D … divider value is 1 (40MHz e.g.) 2_D … divider value is 1 (26MHz e.g.) 3_D … divider value is 1 (20MHz e.g.)	3_D
RSVD	5	RW	RSVD	0_D
SADC_START	4	WC1	SADC trigger: 1_B … Trigger the SADC to start a measurement 0_B … Default value or value after the trigger is captured; internally the value is set back to SADC_START= 0_B.	0_B
SADC_CHSEL	3:0	RW	Analog multiplexer input for channel selection into the SADC: 0_D … Temperature Sensor 1_D ... RSVD 2_D … Temperature Sensor reference 3_D … ifx_mix4 4_D … if_mix4 5_D … ifx_mix3 6_D … if_mix3 7_D … ifx_mix2 8_D … if_mix2 9_D … ifx_mix1 10_D … if_mix1 11_D … pd1_outx 12_D … pd1_out 13_D … pd2_outx 14_D … pd2_out 15_D … RSVD	0_D

4.10 CSx: Channel Set Registers

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes. CSUx= Channel Set Upchirp, CSDx= Channel Set Downchirp, CSI= Channel Set Idle, CSDS= Channel Set Deep Sleep.

#0

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	BBCHGLOB_EN	RX4MIX_EN	RX4LOBUF_EN	RX3MIX_EN	RX3LOBUF_EN	RX2MIX_EN	RX2LOBUF_EN	RX1MIX_EN	RX1LOBUF_EN	LO_DIST1_EN	LO_DIST2_EN	RESERVED_9	RESERVED_8	RESERVED_7	FDIV_EN	TEST_DIV_EN	VCO_EN	PD2_EN	TX2_EN	PD1_EN	TX1_EN

#1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBCH_SEL				BB_RSTCCNT							TEMP_MEAS_EN	RSVD	MADC_EN	TX2_DAC					TX1_DAC				

#2

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP_GAIN				VGA_GAIN4			HPF_SEL4		VGA_GAIN3			HPF_SEL3		VGA_GAIN2			HPF_SEL2		VGA_GAIN1			HPF_SEL1	

Figure 28 Channel Set Registers

Table 29 **CSx#0: Register Description**

Symbol	Bits	Type	Description	RST
RSVD	23:21	RW	RSVD	0_D
BBCHGLOB_EN	20	RW	Enables the baseband chain together with the bit BBCH_SEL: 0_B … Baseband channels are disabled 1_B … Baseband channels are enabled	0_B
RX4MIX_EN	19	RW	Enable the mixer on ch4: 0_B … Disabled 1_B … Enabled	0_B
RX4LOBUF_EN	18	RW	Enable the local oscillator buffer to the mixer on ch4: 0_B … Disabled 1_B … Enabled	0_B
RX3MIX_EN	17	RW	Enable the mixer on ch3: 0_B … Disabled 1_B … Enabled	0_B
RX3LOBUF_EN	16	RW	Enable the local oscillator buffer to the mixer on ch3: 0_B … Disabled 1_B … Enabled	0_B
RX2MIX_EN	15	RW	Enable the mixer on ch2: 0_B … Disabled 1_B … Enabled	0_B
RX2LOBUF_EN	14	RW	Enable the local oscillator buffer to the mixer on ch2:	0_B

Table 29 CSx#0: Register Description

Symbol	Bits	Type	Description	RST
			0_B … Disabled 1_B … Enabled	
RX1MIX_EN	13	RW	Enable the mixer on ch1: 0_B … Disabled 1_B … Enabled	0_B
RX1LOBUF_EN	12	RW	Enable the local oscillator buffer to the mixer on ch1: 0_B … Disabled 1_B … Enabled	0_B
LO_DIST1_EN	11	RW	Enable the local oscillator distribution buffer to both TX channels: 0_B … Disabled 1_B … Enabled	0_B
LO_DIST2_EN	10	RW	Enable the local oscillator distribution buffer to all four RX channels: 0_B … Disabled 1_B … Enabled	0_B
RSVD	9:7	RW	RSVD	0_D
FDIV_EN	6	RW	Enable the VCO frequency divider: 0_B … Disable the DIV output 1_B … Enable the DIV output	0_B
TEST_DIV_EN	5	RW	Frequency divider test control bit: 0_B … Disable the divider 1_B … Enable the divider	0_B
VCO_EN	4	RW	Enable the VCO: 0_B … Disabled 1_B … Enabled	0_B
PD2_EN	3	RW	Enable the power detector from TX2: 0_B … Disabled 1_B … Enabled	0_B
TX2_EN	2	RW	Enable the DAC and power amplifier of TX2 0_B … Disabled 1_B … Enabled	0_B
PD1_EN	1	RW	Enable the power detector from TX1: 0_B … Disabled 1_B … Enabled	0_B
TX1_EN	0	RW	Enable the DAC and power amplifier of TX1 0_B … Disabled 1_B … Enabled	0_B

Table 30 CSx#1: Register Description

Symbol	Bits	Type	Description	RST
BBCH_SEL	23:20	RW	Enable the baseband filters, baseband amplifiers and ADCs on channel BBCHx, where x can be 1..4: BBCHx = 0_D … channel disabled BBCHx = 1_D … channel enabled CSx#1[23] … BBCH4 CSx#1[22] … BBCH3 CSx#1[21] … BBCH2 CSx#1[20] … BBCH1	0_D
BB_RSTCNT	19:13	RW	Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. BB_RSTCNT = T_{BBRST} * f_{SYS_CLK}: 0_D … No analog baseband reset 1_D … Min. reset time is T_{BBRST} = 12.5 ns 127_D … Max. reset counter, T_{BBRST} = 1.5875 µs	0_D
TEMP_MEAS_EN	12	RW	Enables the temperature sensor: 0_B … Disabled 1_B … Enabled	0_B
RSVD	11	RW	RSVD	0_B
MADC_EN	10	RW	Enable the three channel ADC module at once: 0_B... ADC module powered down 1_B … ADC module powered up	0_B
TX2_DAC	9:5	RW	TX2 power setting: 0_D … Min. TX output power 31_D … Max. TX output power	0_D
TX1_DAC	4:0	RW	TX1 power setting: 0_D … Min. TX output power 31_D … Max. TX output power	0_D

Table 31 CSx#2: Register Description

Symbol	Bits	Type	Description	RST
HP_GAIN	23:20	RW	Set the gain of the first stage: HPF GAIN[x]= 1_D … 18dB Gain HPF GAIN[x]= 0_D … 30dB gain bit20→ch1, bit21→ch2, bit22→ch3, bit23→ch4	0_D
VGA_GAIN4	19:17	RW	VGA gain setting channel 4: 0_D… 0dB gain 1_D … 5dB gain 2_D … 10dB gain 3_D … 15dB gain	0_D

Table 31 **CSx#2: Register Description**

Symbol	Bits	Type	Description	RST
			4_D … 20dB gain 5_D … 25dB gain 6_D … 30dB gain 7_D … RSVD	
HPF_SEL4	16:15	RW	High pass filter channel 4 cutoff setting: 0_D … 20kHz 1_D … 45kHz 2_D … 70kHz 3_D … 80kHz	0_D
VGA_GAIN3	14:12	RW	VGA gain setting channel 3: 0_D… 0dB gain 1_D … 5dB gain 2_D … 10dB gain 3_D … 15dB gain 4_D … 20dB gain 5_D … 25dB gain 6_D … 30dB gain 7_D … RSVD	0_D
HPF_SEL3	11:10	RW	High pass filter channel 3 cutoff setting: 0_D … 20kHz 1_D … 45kHz 2_D … 70kHz 3_D … 80kHz	0_D
VGA_GAIN2	9:7	RW	VGA gain setting channel 2: 0_D … 0dB gain 1_D … 5dB gain 2_D … 10dB gain 3_D … 15dB gain 4_D … 20dB gain 5_D … 25dB gain 6_D … 30dB gain 7_D … RSVD	0_D
HPF_SEL2	6:5	RW	High pass filter channel 2 cutoff setting: 0_D … 20kHz 1_D … 45kHz 2_D … 70kHz 3_D … 80kHz	0_D
VGA_GAIN1	4:2	RW	VGA gain setting channel 1: 0_D … 0dB gain 1_D … 5dB gain 2_D … 10dB gain 3_D … 15dB gain	0_D

Table 31 **CSx#2: Register Description**

Symbol	Bits	Type	Description	RST
			4_D … 20dB gain 5_D … 25dB gain 6_D … 30dB gain 7_D … RSVD	
HPF_SEL1	1:0	RW	High pass filter channel 1 cutoff setting: 0_D … 20kHz 1_D … 45kHz 2_D … 70kHz 3_D … 80kHz	0_D

4.11 CSCx - Channel Set Control Register

The channel set control register CSCx is related to the channel set register CSUx and CSDx as well as to CSI and CSDS, see description in section 4.10.

Besides REPC, all other bits are used to define a specific power mode.

"_ISOPD" represent a logical isolation layer and are used to disable one main block (MADC e.g.) preserving its configuration (no change in the ADC0 register configuration e.g.).

REPC is one parameter used to define the modulation sequence, see also 3.2.

CSCx: Channel Set Control Register x

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												PLL_ISOPD	BG_TMRF_EN	SADC_ISOPD	MADC_ISOPD	BG_EN	RF_ISOPD	ABB_ISOPD	CS_EN	REPC			

Figure 29 Channel Set Control Register

Table 32 **CSCx: Register Description**

Symbol	Bits	Type	Description	RST
RSVD	23:12	RW	RSVD	0_D
PLL_ISOPD	11	RW	Isolation pin to disable the PLL: 0_B … PLL is connected 1_B … PLL is isolated	1_B
BG_TMRF_EN	10	RW	Required for temperature sensor readout:	0_B

Symbol	Bits	Type	Description	RST
			0_B … Disabled 1_B … Enabled	
SADC_ISOPD	9	RW	Enable the isolation of all control signals towards the sensor ADC: 0_B … SADC connected 1_B … SADC isolated	1_B
MADC_ISOPD	8	RW	Enable the isolation of all control signals towards the MADC: 0_B … MADC connected 1_B … MADC isolated	1_B
BG_EN	7	RW	Enable bandgap in MADC: 0_B … Disabled 1_B … Enabled	0_B
RF_ISOPD	6	RW	Enable the isolation of all control signals towards the RF block: 0_B … RF connected 1_B … RF isolated	1_B
ABB_ISOPD	5	RW	Enable the isolation of all control signals towards the analog baseband (BB) block: 0_B … BB connected 1_B … BB isolated	1_B
CS_EN	4	RW	Enable channel set (CS): 0_B … CS is not used 1_B … CS is used In case of CSCI or CSCDS this bit is ignored. In the application at least the first channel set should be used by the host (CSC1:CS_EN= 1_B).	0_B
REPC	3:0	RW	Repetition factor for Channel set: RC= 2^REPC: 0_D … RC= 1 repetition 1_D … RC= 2 repetitions 2_D … RC= 4 repetitions … 10_D … RC= 1024 repetitions 15_D … RC= 32768 repetitions In case of CSCI or CSCDS this bit is ignored.	0_D

4.12 CCR0 - Chirp Control Registers 0

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

Register CCR0

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_INIT1 MUL		TR_INIT1								REPT				CONT MODE	TR_END								

Figure 30 Chirp Control Register 0

Table 33 CCR0: Register Description

Symbol	Bits	Type	Description	RST
TR_INIT1_MUL	23:22	RW	Timer multiplier factor for T_INIT1. Precise timing provided under CCR0:TR_INIT1.	0_D
TR_INIT1	21:14	RW	Coefficient to calculate T_INIT1: 0_D … T_{SYS_CLK} From 1_D to 255_D the time delay for T_INIT1 is calculated as follows: T_INIT1 = (TR_INIT1 x 2^TR_INIT1_MUL x 8 + TR_INIT1_MUL +3) x T_{SYS_CLK}. See note below.	0_D
REPT	13:10	RW	Repetition factor for shape sets in a frame: RT= 2^ REPT: 0_D … 1 repetition 1_D … 2 repetitions 2_D … 4 repetitions … 15_D … 32768 repetitions **The host should program as default value 15_D.**	0_D
CONT_MODE	9	RW	After last repetition of RT, the CONT_MODE is enabled. 0_B … only in case if deep sleep power mode is enabled (CCR1: PD_MODE= 2_D). The system clock is disabled internally. 1_B … goes to specified power mode (CCR1: PD_MODE) and after T_FED next shapes will run.	0_B
TR_END	8:0	RW	Coefficient to calculate T_END. T_END Ramp End Delay defines the waiting time after generation of the ramp. T_END= (TR_END x 8 +5) x T_{SYS_CLK}: 0_D … 5*T_{SYS_CLK} 511_D … Max. delay	0_D

Note:

These values are used for every up and every down-ramp.

4.13 CCR1 - Chirp Control Registers 1

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

Register CCR1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_FED_MUL					TR_FED								PD_ MODE		TR_START								

Figure 31 Chirp Control Register 1

Table 34 CCR1: Register Description

Symbol	Bits	Type	Description	RST
TR_FED_MUL	23:19	RW	Timer multiplier factor for frame end delay T_FED. Precise timing provided under CCR1:TR_FED. Note: only values TR_FED_MUL<= 10_D are verified.	0_D
TR_FED	18:11	RW	Coefficient to calculate T_FED: 0_D … T_{SYS_CLK} From 1_D to 255_D the time delay T_FED is calculated as follows: T_FED = (TR_FED x 2^TR_FED_MUL x 8 + TR_FED_MUL +3) x T_{SYS_CLK}.	0_D
PD_MODE	10:9	RW	After last RT repetition the chip enters this power mode for the time T_FED: 0_D … Keep power mode same (CSx, CSCx) 1_D … Idle Mode (CSI + CSCI) 2_D … Deep Sleep Mode (CSDS + CSCDS) 3_D … RSVD	0_D
TR_START	8:0	RW	Coefficient to calculate T_START. T_START Ramp Start Delay defines the waiting time before generation of the ramp. T_START= (TR_START x 8 +10) x T_{SYS_CLK}: 0_D … 10*T_{SYS_CLK} 511_D … Max. delay	0_D

4.14 CCR2 - Chirp Control Registers 2

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

Register CCR2

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_LEN												MAX_FRAME_CNT											

Figure 32 Chirp Control Register 2

Table 35 CCR2: Register Description

Symbol	Bits	Type	Description	RST
FRAME_LEN	23:12	RW	Frame Length specifies the number of shape groups in a frame. When specified frame length is reached frame counter will be incremented and shape group counter reset: 0_D … 1 shape group 1_D … 2 shape group 4095_D … Max. value (=4096).	0_D
MAX_FRAME_CNT	11:0	RW	Maximum number of frames to be executed. When MAX_FRAME_CNT is reached, shape generation will stop and the chip will go into deep sleep power mode. The next frame can be triggered only after a reset (eg. FSM_RESET). The frame generation can be stopped any time by the FSM reset (see MAIN: FSM_RESET). 0_D … Endless generation 1_D … 1 frame will be generated 4095_D … Max. number of frames generated (=4095).	0_D

4.15 CCR3 - Chirp Control Registers 3

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

Register CCR3

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_INIT0 MUL		TR_INIT0								TR_SSTART					TR_PAEN								

Figure 33 Chirp Control Register 3

Table 36 CCR3: Register Description

Symbol	Bits	Type	Description	RST
TR_INIT0_MUL	23:22	RW	Timer multiplier for delay T_INIT0.Precise timing provided under CCR3:TR_INIT0.	0_D
TR_INIT0	21:14	RW	Coefficient to calculate T_INIT0: 0_D … T_{SYS_CLK} From 1_D to 255_D the time delay for T_INIT0 is calculated as follows: T_INIT0 = (TR_INIT0 x 2^TR_INIT0_MUL x 8 + TR_INIT0_MUL +3) x T_{SYS_CLK}. See Note 3.	0_D
TR_SSTART	13:9	RW	Coefficient to calculate T_SSTART. T_SSTART Sampling Start Delay Time after PA enable until 1st trigger to MADC. T_SSTART= (TR_SSTART x 8 +1) x T_{SYS_CLK}: 0_D … T_{SYS_CLK} 31_D … Max. delay	0_D
TR_PAEN	8:0	RW	Coefficient to calculate T_PAEN. T_PAEN Delay Time after PLL Start to PA enable. T_PAEN= TR_PAEN x 8 x T_{SYS_CLK}: 0_D … RSVD 1_D … Min. delay 511_D … Max. delay	0_D

Note:

1. *One single step is equal to 8 x T_{SYS_CLK} system clock cycles (= 100 ns)*
2. *The delay values are used for every up and every down-ramp*
3. *T_INIT0 and T_INIT1 should be programmed to a minimum value according to the ADC calibration time. See also Table 15 and Table 64.*

4.16 PLLx [0...6] - Chirp Shape Registers

Registers PLLx, where x can be 1 to 4, are used to program the parameters for the modulation sequence inside the PLL local FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL Chirp Shape Registers

	Bits 23 … 12	Bits 11 … 0
#0	FSU[1..4] Chirp Start Freq Upchirp	
#1	RSU[1..4] Ramp Step Upchirp	
#2	T_EDU End Delay Upchirp	RTU[1..4] Ramp Time Upchirp
#3	APD_Numsamp[1..4] NumberOfSamples Dnchirp	APU_Numsamp[1..4] NumberOfSamples Upchirp
#4	FSD[1..4] Chirp Start Freq Downchirp	
#5	RSD[1..4] Ramp Step Downchirp	
#6	T_EDD End Delay Downchirp	RTD[1..4] Ramp Time Downchirp

Figure 34 PLL Chirp Shape Registers 1-6

Table 37 PLLx#0 … PLLx#6 Chirp Shape: Register Description

Symbol	Bits	Type	Description	RST
FSU[1..4] FSD[1..4]	23:0	RW	Chirp Start Freq Upchirp / Downchirp. SDM start frequency for the ramp generator: FSD = 0_D for sawtooth shape In case FSD=0, RSD=0, and RTD=0, then the fast sawtooth shape is enabled. In all other cases the triangular shape is enabled.	0_D
RSU[1..4] RSD[1..4]	23:0	RW	Ramp Step Upchirp / Downchirp. A ramp step is the RF frequency difference added to the actual frequency during single clock cycle time of T_{SYS_CLK}= 12.5 ns. In case the value is zero the RF frequency will be almost constant during the RTU/RTD time. bit (23) represents the sign for the ramp: 0_D … Upchirp 1_D … Downchirp	0_D
TR_EDU[1..4] TR_EDD[1..4]	23:16	RW	Coefficients to calculate T_EDU and T_EDD, respectively. T_EDU and T_EDD are End of Chirp Delay applied after every Upchirp and Downchirp. If TR_EDU/D = 0: T_EDU/D = 2 x T_{SYS_CLK}. If TR_EDU/D > 0: T_EDU/D = (8 x TR_EDU/D + 5) x T_{SYS_CLK}. 255D … Max. delay	0_D
RSVD	15:14		Reserved on register #2 and #6.	0_D
RTU[1..4] RTD[1..4]	13:0	RW	Ramp Time Upchirp / Downchirp. RTU/D defines the number of clock cycles for the Upchirp (RTU) or Downchirp (RTD). The actual ramp time is T_RAMP[U|D] = [RTU|RTD] * 8 x T_{SYS_CLK}: 0_D … Timer disabled. Disabling the timer is useful when doing Downchirp operation with fast down chirp enabled. 1_D … T_RAMP = 100 ns 16383_D … T_RAMP = 2^14 x 100 ns = 1.6383 ms	0_D
APU[1..4] APU[1..4]	23:12 11:0	RW	Number of samples for Upchirp (APU) or Downchirp (APD) for the results of a single ADC: 0_D … No sampling during chirp 1_D … Number of samples = 1 4095_D … Max. number of samples is 4095	0_D

Note:

IRQ FIFO interrupt is generated based on FIFO words. One FIFO word of 24 bit captures two ADC samples of 12 bit. For dual and quad ADC operation all samples result in 1 or more FIFO words. In single ADC mode, if an odd number of samples are selected, the FIFO interrupt will be generated after the following (even) sample. For single channel mode an even number of samples is recommended.

4.17 PLLx[7] – SCR Shape Control Register

Registers PPLx[7], where x can be 1 to 4, are used to program the parameters for the modulation sequence inside the PLL local FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

Register PLLx#7

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_SED_MUL					TR_SED								PD_ MODE		CONT_MODE	RSVD			SH_EN	REPS			

Figure 35 PLLx#7 SCR shape control register

Table 38 PLLx#7 SCR **Shape Control: Register Description**

Symbol	**Bits**	**Type**	**Description**	**RST**
TR_SED_MUL	23:19	RW	Timer multiplier factor for shape end delay T_SED. Precise timing provided under PLLx#7:TR_SED. Note: only values TR_SED_MUL<= 10_D are verified.	0_D
TR_SED	18:11	RW	Coefficient to calculate T_SED: 0_D … T_{SYS_CLK} From 1_D to 255_D the time delay T_SED is calculated as follows: T_SED = (TR_SED x 2^TR_SED_MUL x 8 + TR_SED_MUL +3) x T_{SYS_CLK}.	0_D
PD_MODE	10:9	RW	After last shape repetition, FSM goes to a specified Power Down Mode (run this mode during T_SED): 0_D … Keep power mode same (CSx, CSCx) 1_D … Idle Mode (CSI + CSCI) 2_D … Deep Sleep Mode (CSDS + CSCDS) 3_D … RSVD	0_D
CONT_MODE	8	RW	After last shape repetition REPS, FSM: 0_B … goes to a specified Power Down Mode and stop immediately 1_B … goes to a specified Power Down Mode and after T_SED it runs the next shapes	0_B
RSVD	7:5	RW	RSVD	0_D
SH_EN	4	RW	Enables the specific shape x (see Note 3): 0_B … shape is not used regardless if shape parameters of PLLx[1..7] are programed with values different from default value. 1_B … shape is used	0_B

Symbol	Bits	Type	Description	RST
REPS	3:0	RW	Repetition factor for a single shape x: RSx= 2^REPSx: 0_D … RSx= 1 repetition 1_D … RSx= 2 repetitions 2_D … RSx= 4 repetitions … 15_D … RSx= 32768 repetitions	0_D

Note:

1. *When chirp shapes are not used FSU/RSU/RTU register fields must be programmed to 0_D (see also Table 37.*
2. *A “sawtooth” chirp can be defined by setting field FSD= 0_D, and programming the fields for Upchirp (see also Table 37.*
3. *At least the first shape needs to be enabled (PLL1[7]:SH_EN=1_B)*

4.18 PLL DFT0 Register

The setting in this register should be used when the CW mode is enabled (see also 10.3).

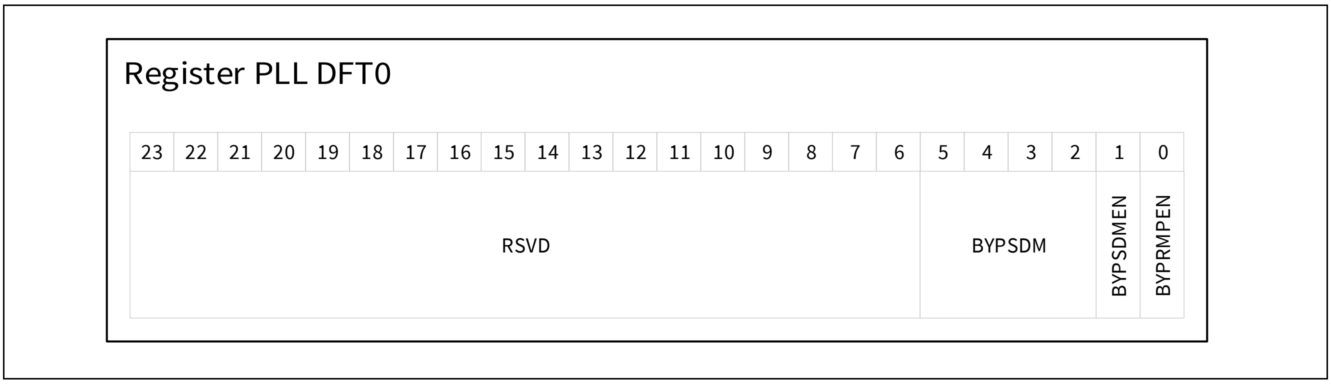


Figure 36 PLL DFT0 register

Table 39 PLL DFT0: Register Description

Symbol	Bits	Type	Description	RST
RSVD	23:6	RW	RSVD	0_D
BYPSDM	5:2	RW	Word used when SDM bypassed	0_D
BYPSDMEN	1	RW	0_B … SDM module drives the PLL 1_B … Value of BYPSDM drives the PLL	0_B
BYPRMPEN	0	RW	0_B … Ramp generator enabled 1_B … Ramp generator disabled	0_B

4.19 RFT0 – RF Test Register 0

Register contains several bits used to enable dedicated paths for self-test.

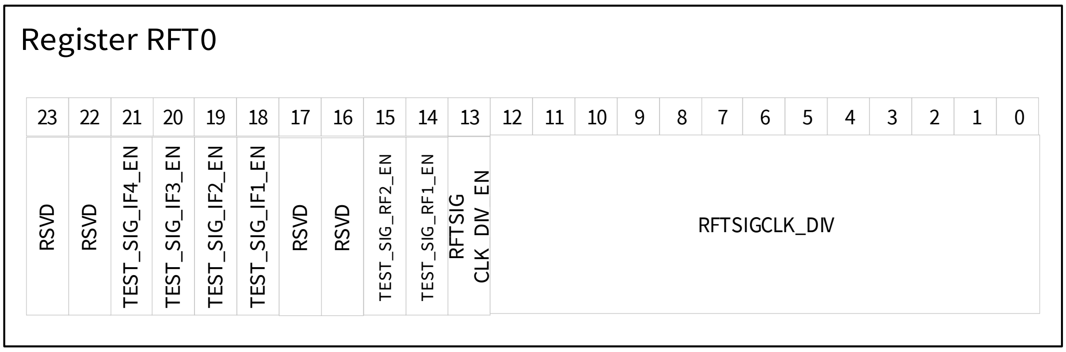


Figure 37 RFT0 RF test register 0

Table 40 RFT0: Register Description

Symbol	Bits	Type	Description	RST
RSVD	23:22	RW	RSVD	0_D
TEST_SIG_IF4_EN	21	RW	Enable the test signal output for IF channel 4	0_D
TEST_SIG_IF3_EN	20	RW	Enable the test signal output for IF channel 3	0_D
TEST_SIG_IF2_EN	19	RW	Enable the test signal output for IF channel 2	0_D
TEST_SIG_IF1_EN	18	RW	Enable the test signal output for IF channel 1	0_D
RSVD	17:14	RW	RSVD	0_B
RFTSIGCLK_DIV_EN	13	RW	Enable the RF test tone signal output to the baseband module: 0_B … Disable the divider output 1_B … Enable the divider output	0_B
RFTSIGCLK_DIV	12:0	RW	RF test tone signal divider value: $f_{RFTST}= f_{SYS\_CLK}$ / RFTSIGCLK_DIV. 2_D … Min. divider value 8191_D … Max. divider value	8000_D

4.20 RFT1 – RSVD

Reserved register

4.21 DFT0 – Design for Test Register 0

Register contains several bits needed for sensing eFuses.

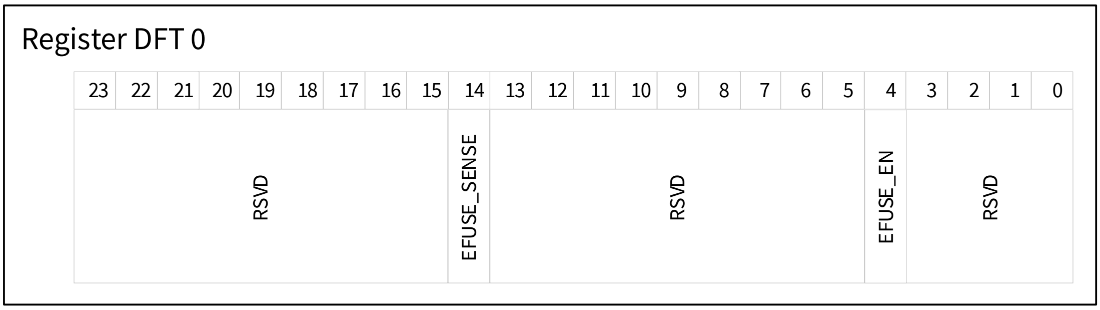


Figure 38 DFT0

Table 41 **DFT0: Register Description**

Symbol	Bits	Type	Description	RST
RSVD	23:15	RW	RSVD	0_D
EFUSE_SENSE	14	W1C	Start EFUSE read out	0_B
RSVD	13:5	RW	RSVD	0_D
EFUSE_EN	4	RW	Enable EFUSE functionality	0_B
RSVD	3:0	RW	RSVD	0_D

4.22 DFT1 – Design for Test Register 1

Register contains one bit needed for sensing eFuses.

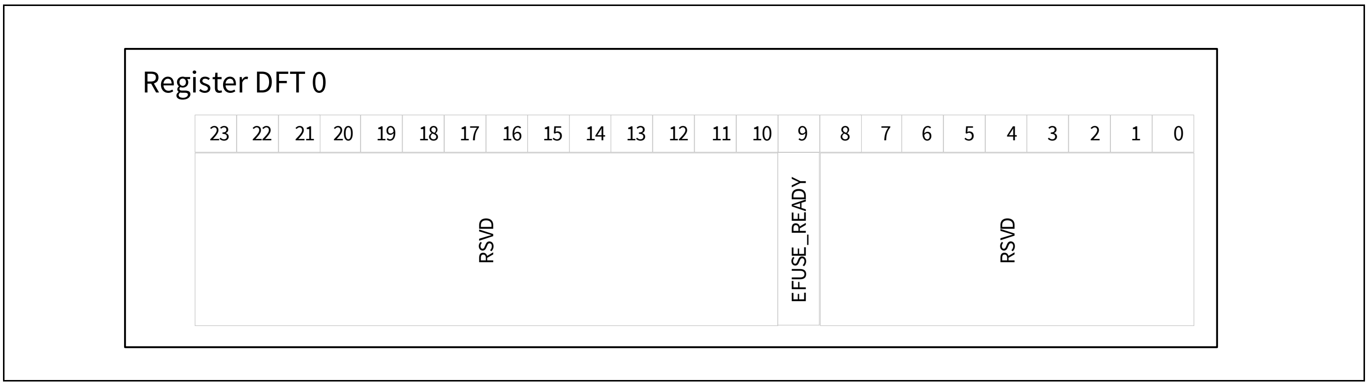


Figure 39 **DFT1**

Table 42 **DFT1: Register Description**

Symbol	Bits	Type	Description	RST
RSVD	23:10	RW	RSVD	0_D
EFUSE_READY	9	R	EFUSE ready signal. Register CHIP ID #1 and CHIP ID #2 are valid if EFUSE_READY is set to 1.	0_B
RSVD	8:0	RW	RSVD	0_D

4.23 STAT0 - Status Register 0

The status register STAT0 provides the actual value of some specific internal states. However, it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 µs.

Register STAT0

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										SH_IDX			CH_IDX			PM			RSVD	LDO_RDY	MADC_BGUP	MADC_RDY	SADC_RDY

Figure 40 STAT0: Control FSM Status Register

Table 43 STAT0: Register Description

Symbol	Bits	Type	Description	RST
RSVD	23:14	R	RSVD	0_D
SH_IDX	13:11	R	Actual chirp shape enabled by the FSM: 0_D … PLLU1 1_D … PLLD1 2_D … PLLU2 3_D … PLLD2 4_D … PLLU3 5_D … PLLD3 6_D … PLLU4 7_D … PLLD4	0_D
CH_IDX	10:8	R	Actual channel set enabled by the FSM: 0_D … CSU1 1_D … CSD1 2_D … CSU2 3_D … CSD2 4_D … CSU3 5_D … CSD3 6_D … CSU4 7_D … CSD4	0_D
PM	5:7	R	Power Mode is the current power mode status of FSM: 1_D … Active Mode 2_D … Interchirp Mode 3_D … Idle Mode 5_D … Deep Sleep Mode 0_D,4_D,6_D,7_D … RSVD	5_D
RSVD	4	R	RSVD	0_B
LDO_RDY	3	R	LDO output level, i.e. VDDC, above the threshold: 0_B … LDO output level below threshold 1_B … LDO output level above threshold, ready	0_B
MADC_BGUP	2	R	MADC bandgap reference power up status: 0_B … Status down	0_B

Table 43 **STAT0: Register Description**

Symbol	Bits	Type	Description	RST
			1_B … Up and running	
MADC_RDY	1	R	MADC status: 0_B … Status down 1_B … Up and running	0_B
SADC_RDY	0	R	SADC startup / calibration status: 0_B … Status down 1_B … Up and running	0_B

4.24 SADC_RESULT Sensor ADC Result Register

The sensor ADC register SADC_RESULT is used to monitor the SADC as well as to read out the output from the conversion.

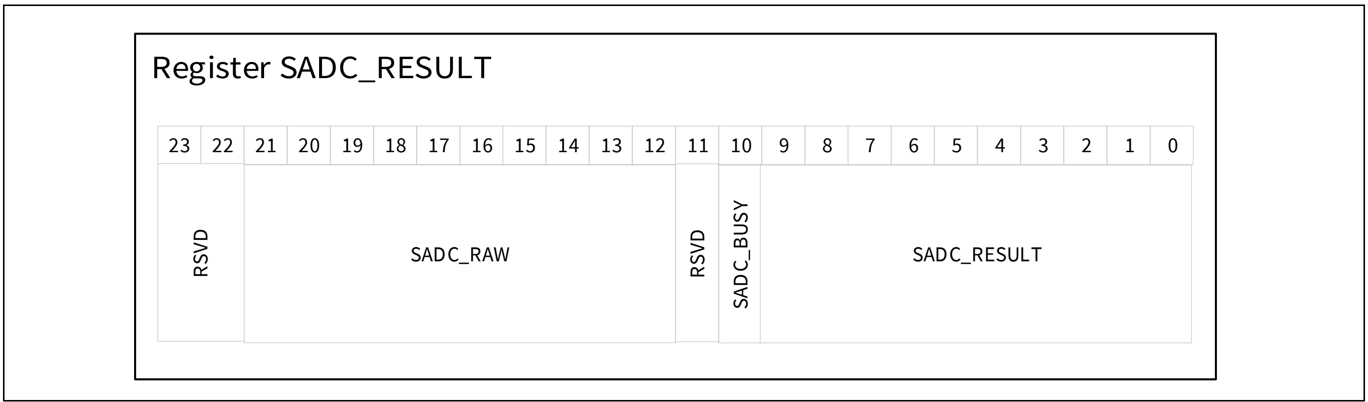


Figure 41 SADC_RESULT register

Table 44 **SADC: Register Description**

Symbol	Bits	Type	Description	RST
RSVD	23:22	R	RSVD	0_D
SADC_RAW	21:12	R	SADC Raw data (for test only)	0_D
RSVD	11	R	RSVD	0_B
SADC_BUSY	10	R	Shows if SADC is busy: 0_B … SADC not busy 1_B … SADC busy	0_B
SADC_RESULT	9:0	R	10 bits measurement result. In case just 8 bits are converted, the 8-bit value is left-shifted by two (multiplied by 4). In case 9 bit are converted, the 9-bit result is left-shifted by 1 (multiplied by 2).	0_B

4.25 FSTAT - FIFO Status Register

The global status register FSTAT is used to monitor the FIFO. It should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 µs.

Register FSTAT

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOF_ERR	FULL	CREF	EMPTY	FUF_ERR	BURST_ERR	CLK_NUM_ERR	RSVD			FILL_STATUS													

Figure 42 **FSTAT Register**

Table 45 **FSTAT: Register Description**

Symbol	Bits	Type	Description	RST
FOF_ERR	23	R	FIFO overflow error bit shows if more sample data are transferred to the FIFO than FIFO memory locations are available to store the data. The flag will be shown also in GSR0 as a part of FIFO over or underflow error bit FOU_ERR: 0_B … No FIFO overflow 1_B … FIFO had an overflow condition	0_B
FULL	22	R	The FULL bit shows if the FIFO has fully filled up: 0_B … FIFO is not full 1_B … FIFO is full	0_B
CREF	21	R	0_B … FIFO filling status below CREF 1_B … FIFO filling status is > CREF	0_B
EMPTY	20	R	The FIFO empty bit EMPTY signals if the FIFO is empty: 0_B … FIFO stores at least one sample 1_B … FIFO is empty	1_B
FUF_ERR	19	R	FIFO under flow error signals if the host was reading more sampling data from the FIFO than available. The flag will be shown also in GSR0 as a part of FIFO over or underflow error bit FOU_ERR: 0_B … No error 1_B … FIFO underflow occurred	0_B
SPI BURST_ERR	18	R	In case of burst error this bit is set. Further details in the Note below and in 5.8: 0_B … No error 1_B … Burst error occurred. Bit will be reset after HW or SW reset condition. See also section 5.8.	0_B

Symbol	Bits	Type	Description	RST
CLK_NUM_ERR	17	R	Clock number error bit is set when SPI clocks do not fit the expected clock cycles. Further details in the Note below and in 5.8: 0_B … No error 1_B … Burst error occurred. Bit will be reset after HW or SW reset condition. See also section 5.8.	0_B
RSVD	16:14	R	Not used	0_D
FILL_STATUS	13:0	R	FIFO filling status: 0x0 … FIFO empty 0x1000 … FIFO 50% filled 0x2000 … FIFO full This bit field is for de-bugging only. It should not be evaluated while the MADC sampling and filing up the FIFO. It can be evaluated when the FSM status is held, for example, after an FSM reset or in a specific power mode, Deep Sleep e.g.	0_D

Note:

FOF/FUF will be cleared after these resets:

- FIFO reset
- SW reset
- HW reset

4.26 Register CHIP ID #1

The unique CHIP ID consists of 48 bits. Register CHIP ID #1 provides the lower 24 bits of the ID.

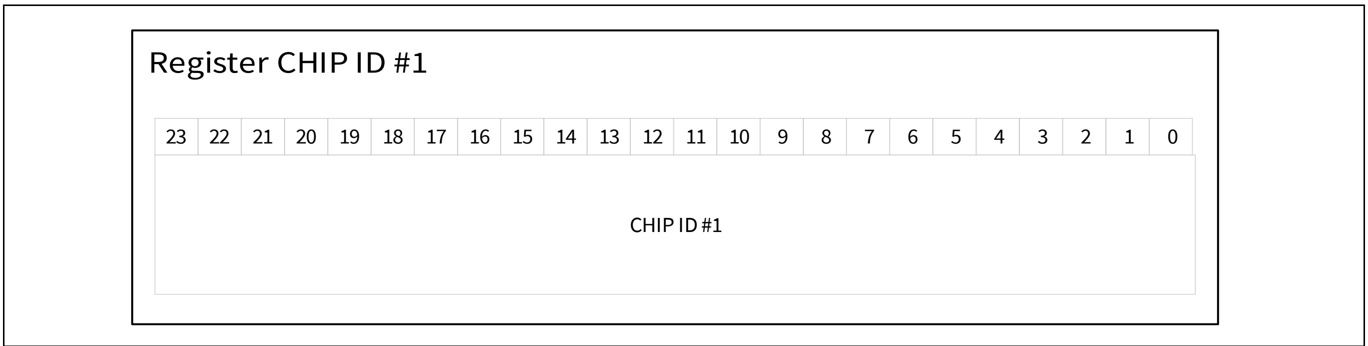


Figure 43 CHIP ID #1 Register

Table 46 CHIP ID #1: Register Description

Symbol	Bits	Type	Description	RST
CHIP ID #1	23:0	R	Lower 24 bits of the CHIP ID (23:0)	

4.27 Register CHIP ID #2

The unique CHIP ID consists of 48 bits. Register CHIP ID #2 provides the upper 24 bits of the ID.

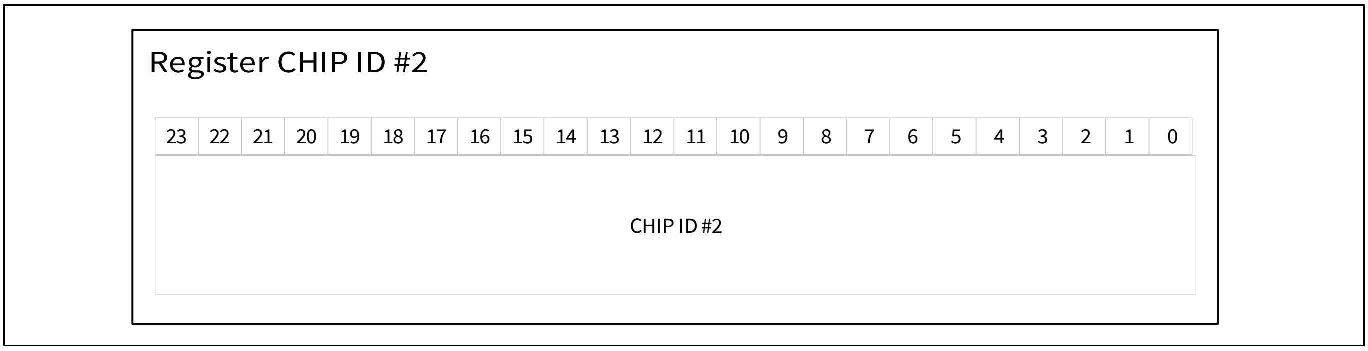


Figure 44 CHIP ID #2 Register

Table 47 CHIP ID #2: Register Description

Symbol	Bits	Type	Description	RST
CHIP ID #2	23:0	R	Upper 24 bits of the CHIP ID (47:24)	

4.28 GSR0 - Global Status Register

The global status register GSR0 is related to SPI read/write monitoring.

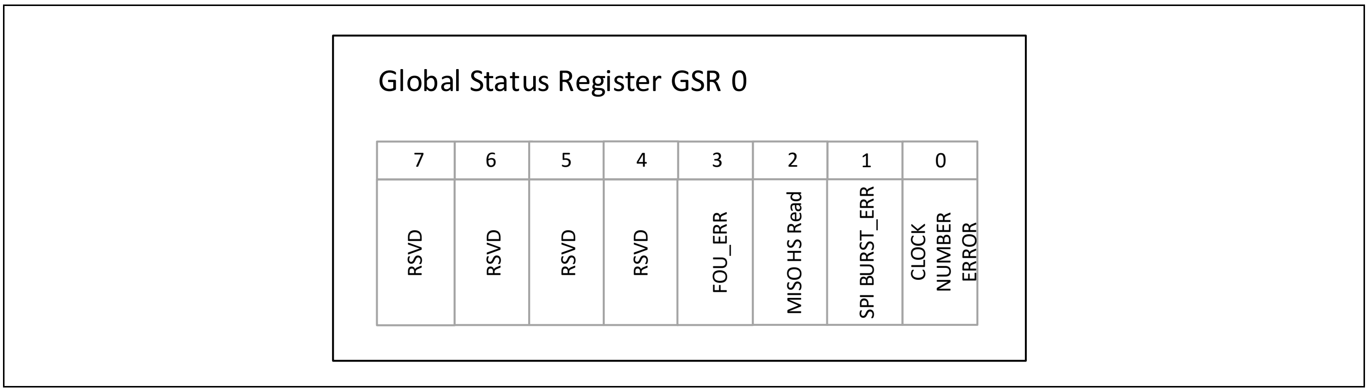


Figure 45 GSR0 Register

Table 48 GSR0: Register Description

Symbol	Bits	Type	Description	RST
RSVD	7:4	R	RSVD	1111_B
FOU_ERR	3	R	Shows if FIFO overflow or underflow condition occurred. The error will be cleared after the following resets: FIFO reset or SW reset or HW reset: 1_B … Error condition occurred 0_B … No error	0_B
MISO HS Read	2	R	SPI: MISO high speed mode activated	1_B

Symbol	Bits	Type	Description	RST
SPI BURST_ERR	1	R	SPI burst error, defined within the SPI spec (see section 5.8): 0_B … No burst read/write error 1_B … Burst error	0_B
CLOCK NUMBER ERROR	0	R	Defined within the SPI Spec: 0_B … No clock number error 1_B … Error condition occurred	0_B

5 Data Organization and SPI Interface

5.1 Data Header

The main FSM is capable of generating a data header to be attached to the actual radar raw data. The structure of the header is shown in Figure 46 and in Table 49. The data header can be disabled by controlling the bit SFCTL: PREFIX_EN (see section 4.8).

A sync-word is sent at the beginning of each acquisition to make the radar raw-data from each shape unique. This can be useful in case of broken communication with the application processor or in case of errors. Supposing the FIFO will generate a “FIFO overflow flag” the sync-word 0x000000 can be evaluated by the host controller and used to resync with the BGT60ATR24C and discard the data received before this sync word (if header or sync-word not used then the controller should reset the FIFO, discarding the actual FIFO data). On “FIFO underflow flag”, the received data bits from the host are 111111111111_B.

Following, the header includes also the frame counter and shape group counter, as well as the actual APU/APD value (see section 4.16) and temperature value.

Data Header

#0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SYNC_WORD1 = 0x000												SYNC_WORD0 = 0x000											
#1	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRAME_CNT[11:0]												SHAPE_GRP_CNT[11:0]											
#3	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHIRP_LEN[11:0]												SADC_VAL[9:0]										CS[1:0]	
#4	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data 0												Data 1											
...																								

Figure 46 Data header

Table 49 Data Header Description

Symbol	Reg	Bits	Description	RST
SYNC_WORD1	#0	23:12	The sync-word can be used to identify the start of a new chirp. In case the MADC will output also a sequence of 0x000000, to make the sync-word unique, the data from the MADC will be automatically changed to 0x001 before transferring it to the FIFO.	0_D
SYNC_WORD0	#0	11:0	See SYNC_WORD1.	0_D
FRAME_CNT	#1	23:12	Same as STAT1: FRAME_CNT (see section 4.5). *Note: FRAME_CNT info should not be used by the host when endless mode is enabled (please check CCR2:MAX_FRAME_CNT).*	0_D
SHAPE_GRP_CNT	#1	11:0	Same as STAT1: SHAPE_GRP_CNT (see section 4.5).	0_D
CHIRP_LEN	#2	23:12	Number of MADC samples inside the chirp (APU/APD value of related chirp).	0_D
SADC_VAL	#2	11:2	10 bits of sensor ADC output data (eg. temperature).	0_D
CS	#2	1:0	Indicates the channel shape number to which the following sampling data belongs to.	
Data 0	#3	23:12	MSB data (see section 5.2).	
Data 1	#3	11:0	LSB data (see section 5.2).	

5.2 FIFO and Dataflow

The memory in the BGT60ATR24C is based on a FIFO. The FIFO consists of a circular shift register organized in 8192 words of 24 bits each. Four dataflow modes from MADC to the FIFO are supported by the FSM (see Figure 47):

- Mode 1: Only one ADC active (can be any ADC from 1 to 3)
    - Data from 1st sample, 12 bits, are temporarily stored in a buffer
    - When the 2nd sample, 12 bits, are available, both, 1st and 2nd, 24 bits, are stored into one data word
- Mode 2: Two ADCs active (can be any ADC from 1 to 3)
    - Data from active ADCs, 12+12 bits, are occupying one data word in the FIFO
- Mode 3: Three ADCs active
    - Data from first two channels are stored into a data word while data from third channel is buffered. On the consecutive trigger the buffered data and the one from first channel are stored in a data word while the data of the second channel is buffered. On the next trigger the buffered data plus the data from the third channel are stored in a third data word, etc.
- Mode 4: Four ADCs active
    - Data from active ADCs are occupying 2 subsequent datawords in memory

Mode 1

	23 … 12	11 … 0
0x00	Trig1:ADC1	Trig2:ADC1
0x01	Trig3:ADC1	Trig4:ADC1

Mode 2

	23 … 12	11 … 0
0x00	Trig1:ADC1	Trig1:ADC2
0x01	Trig2:ADC1	Trig2:ADC2

Mode 3

	23 … 12	11 … 0
0x00	Trig1:ADC1	Trig1:ADC2
0x01	Trig1:ADC3	Trig2:ADC1
0x02	Trig2:ADC2	Trig2:ADC3

Mode 4

	23 … 12	11 … 0
0x00	Trig1:ADC1	Trig1:ADC2
0x01	Trig1:ADC3	Trig1:ADC4
0x02	Trig2:ADC1	Trig2:ADC2
0x02	Trig2:ADC3	Trig2:ADC4

Figure 47 FIFO organization

Readout from the FIFO is done from the SPI block. Due to max frequency of SPI clock, 50 MHz, the readout rate from the FIFO is:

- 50 MHz / SPI Mode / 24 bit = 480 ns = 40 cycles (in the 80 MHz domain)

Readout from the FIFO should be executed from the host controller using memory address with correct data length and SPI burst reads. Data length can be derived from the data header or based on the “sync-word”.

Note:

An illegal write to memory address space will lead to lost FIFO data!

5.3 SPI – Serial Peripheral Interface Module

The SPI is the basic communication interface between the host and the BGT60ATR24C. It enables the host to read to, or write (program) from the registers as well as reading from the FIFO.

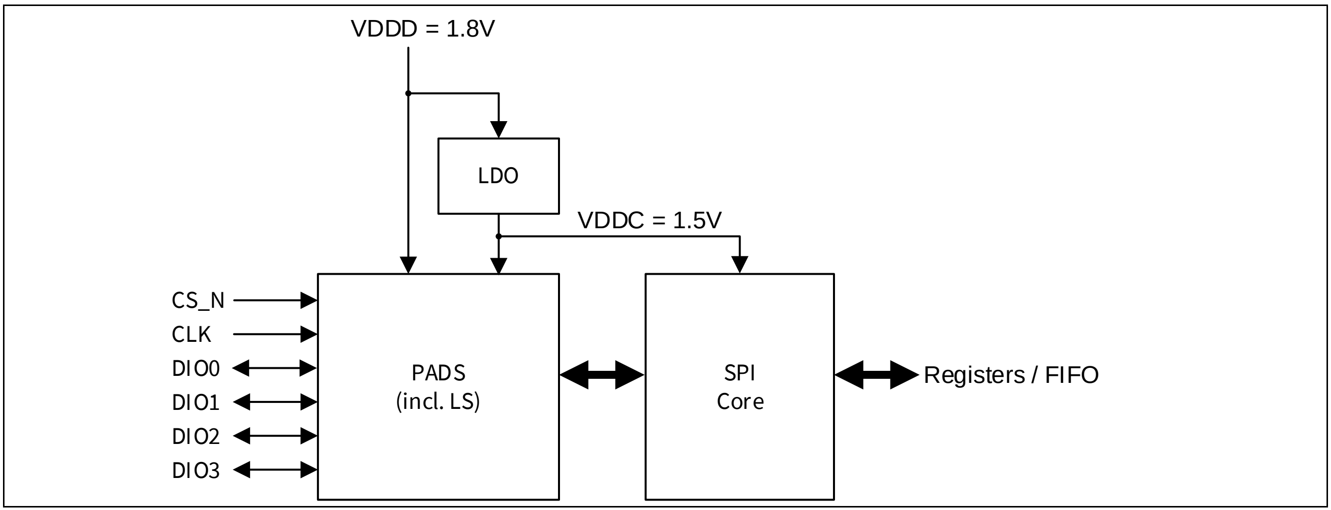


Figure 48 SPI module

The device supports two different SPI modes,

- Normal SPI
- Quad-SPI (QSPI)

In order to enter the expected mode, do the following.

Normal SPI

BGT60ATR24C features four I/O pins for SPI communication and one for chip reset. DIO[x] pins are pulled up to logic high inside the pad.

- CS_N to be connected to $\overline{SS}$ of the SPI master
- CLK to be connected to CLK of the SPI master
- DIO0, DI to be connected to MOSI of the SPI master
- DIO1, DO to be connected to MISO of the SPI master
- DIO2 not available in normal SPI mode
- DIO3 to be connected to reset

Table 50 SPI pins

Pin Name	Standard SPI Mode Function	Remarks
CS_N	CS_N	Chip select or Slave Select
CLK	CLK	SPI clock
DIO0	DI	HiZ, biderectional
DIO1	DO	HiZ, bidirectional
DIO2	N.A.	Not available in normal SPI mode
DIO3	RESET	HiZ, bidirectional

The SPI interface can be clocked up to 50 MHz. To meet the timing requirements for higher SPI clock frequencies (e.g. > 25MHz) BGT60ATR24C offers an additional high speed mode (SFCTL:MISO_HS_RD) which increases the timing budget on SPI master side by sending out data via DO with the rising edge instead of the falling edge of the CLK.

Quad SPI (QSPI)

After SPI_CSN is active low, the address is transferred. Therefore, the first working edge of SPI_CLK transfers the four upper MSB address bits from SPI_DIO[3:0] into the shift register. On the second working edge of SPI_CLK, the four LSB address bits are transferred into the shift register.

In case if the received address in the shiftregister is address < 0xC0, then the QSPI mode is activated and the normal SPI mode is disabled during SPI_CSN is active low.

An address ≥ 0xC0 is not allowed.

For details of Quad SPI operation see section 5.9

5.3.1 Standard SPI Timing

The timing diagram for normal SPI mode (SFCTL: MISO_HS_RD = 0_B) is presented in Figure 49. A SPI transfer is started with a falling edge of chip select signal CSN generated by the SPI master. At the same time the SPI master shall drive the level of the data input signal DI /MOSI (Master Output Slave Input) according to the first bit. Also with the falling edge of the chip select signal CSN the SPI slave applies the level of the data on the output signal DO / MISO (Master Input Slave Output) according to the first bit which shall be transferred to the SPI master, the level becomes stable after the period t(ds). The SPI master has to wait for the time t(L) before the clock signal CLK can be generated.

With the rising edge of CLK the SPI slave captures the level of DI. The SPI master must keep the DI level stable for t(sis) before and for t(sih) after the rising edge of CLK to ensure valid setup and hold time of the SPI slave. With the falling edge of CLK the SPI master shall set the level of DI according to the next bit the master wants to send.

The SPI master is supposed to read the level of DO with the rising edge of CLK. The SPI slave keeps the DO level stable for t(soh) after the falling edge of CLK. With the falling edge of CLK the SPI slave drives the level of DO according to the next bit, DO becomes stable after latest t(sov).

After the last bit has been transferred and CLK has gone to low level, the SPI master must set CSN to high level to stop the transfer. The master must take care that the period between the last rising edge of CLK and the rising edge of CSN is not shorter than t(T). Within the period t(dh) after the rising edge of CSN the SPI slave drives DO to high impedance state again.

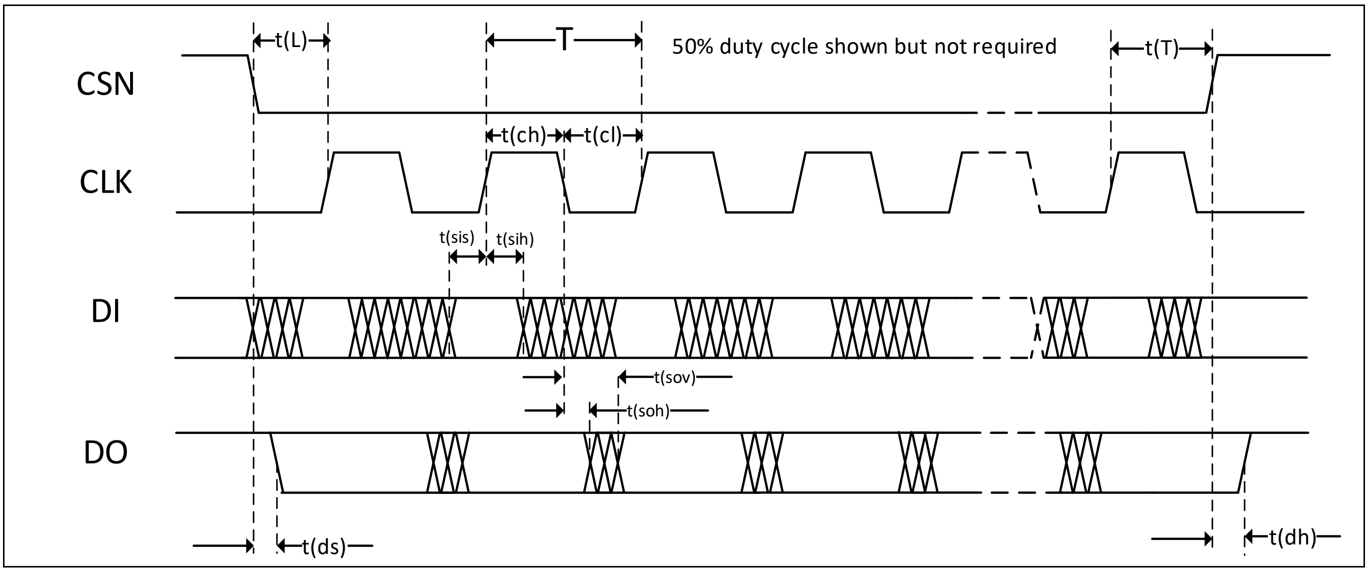


Figure 49 SPI interface timing diagram for SFCTL: MISO_HS_RD = 0_b

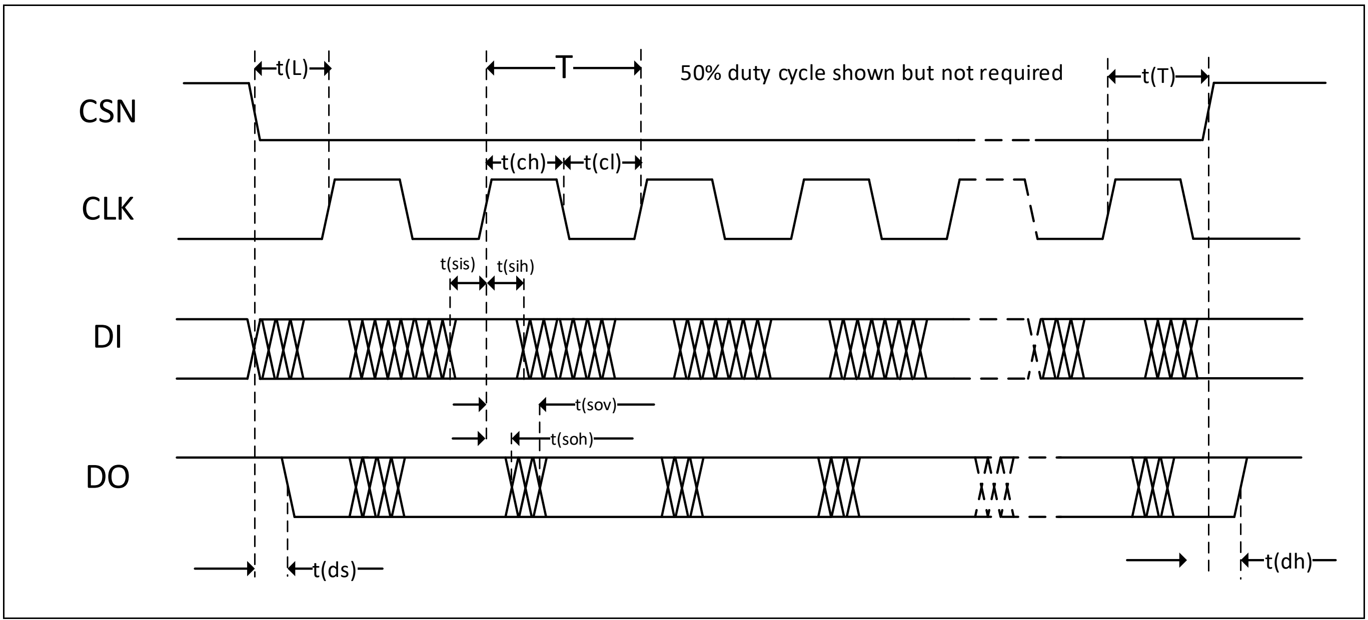


Figure 50 SPI interface timing diagram for SFCTL: MISO_HS_RD = 1_b

BGT60ATR24C can operate at SPI clock frequencies up to 50MHz, but the maximum achievable SPI clock frequency is limited by DI related setup and hold times of SPI master and SPI slave. If for example the SPI master requires a longer setup time than T/2-t(sov), the SPI clock speed in normal SPI mode must be reduced. Alternatively BGT60UTR11DAiP can be switched to SPI high speed mode by setting SFCTL: MISO_HS_RD = 1_B.

The timing diagram for high speed SPI mode is presented in Figure 50Figure 50. In this mode the SPI master is still supposed to capture the level of DO with the rising edge of CLK. The SPI slave keeps the level of DO stable for t(soh) after the rising edge of CLK, and then sets the level of DO according to the next bit which is send out.

Table 51 SSPI Timing Requirements, VDDD= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
SPI clock period: 50 MHz, with 1% clock jitter	T	ns	20			5.3.1	
Clock high	t(ch)	ns	9.0			5.3.2	
Clock low	t(cl)	ns	9.0			5.3.3	
Slave input setup	t(sis)	ns	5.0			5.3.4	
Slave input hold	t(sih)	ns	5.0			5.3.5	
Slave output valid	t(sov)	ns			15.0	5.3.6	(see Note 2)
Slave output hold	t(soh)	ns	1.0			5.3.7	
Lead time before the first working clock edge occurs	t(L)	ns	9.0			5.3.8	
Tailing time after the last working clock edge	t(T)	ns	1			5.3.9	
Data setup time after the DO goes in low impedance state	t(ds)	ns			5.0	5.3.10	Guaranteed by design
Data hold time before DO goes in high impedance state.	t(dh)	ns			5.0	5.3.11	Guaranteed by design

Note:

1. *If SFCTL: MISO_HS_RD is not set properly then data read on MISO may not be correct.*
2. *The timing is guaranteed for worst case condition: VDDD = 1.71 V, Tb=+70°C, output load of Cload = 50 pF.*

5.3.2 Logic Levels

The digital inputs and outputs are fully CMOS compatible (reported in Table 52). All IO input / output timings are based on 50% voltage reference levels (see Figure 51). I/O interfaces are shown in Figure 54, input pins, and Figure 55, output pins, which include internal pull-ups.

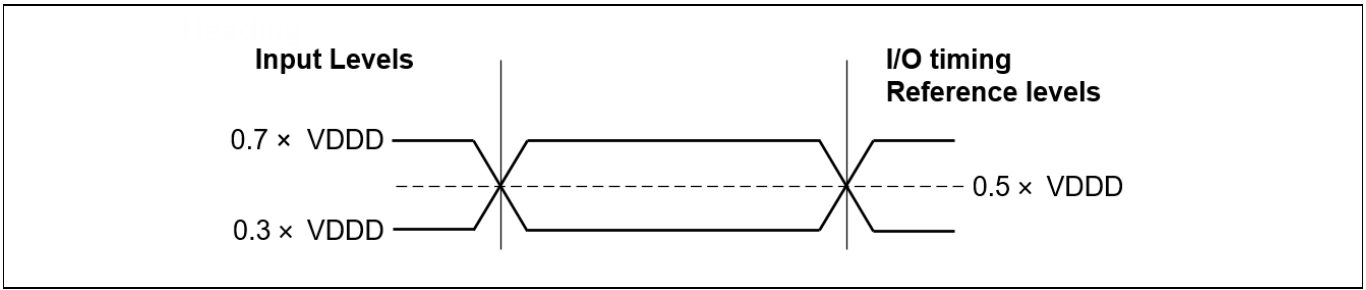


Figure 51 AC timing input/output reference levels

The input logic hysteresis prevents input buffers from oscillation. The minimum hysteresis range V_{HYST} is in between the lower (0.3 × VDDD) and upper logic level (0.7 × VDDD) boundaries (see Figure 52). Above 0.7 × VDDD the input signal is a logical '1' while below 0.3 × VDDD it is a logical '0' regardless of hysteresis. Due to temperature drifts and device variation the hysteresis range V_{HYST} can be up to 0.7 × VDDD or down to 0.3 × VDDD but typically around 0.5 × VDDD. Parameters are reported in Table 52 and Table 53.

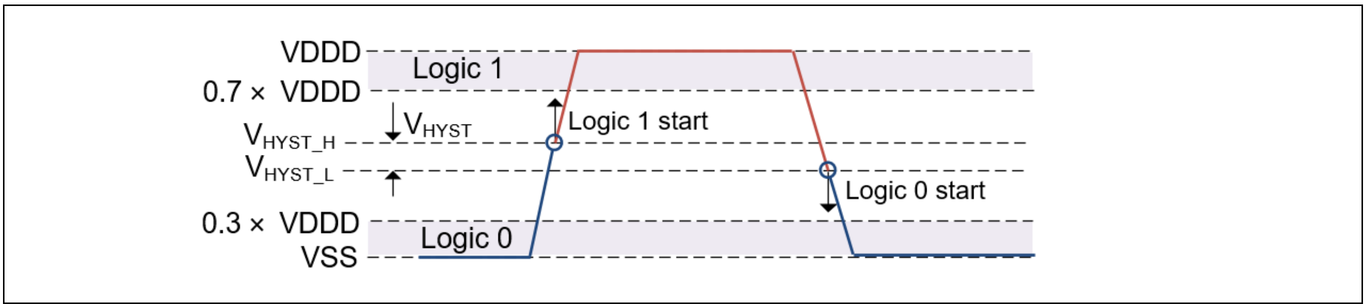


Figure 52 Logic input levels and hysteresis

The digital output pads have a fixed output pad strength that gives a specific slew-rate for rising signals, dV_{TR}, and falling signals, dV_{TF} (see Figure 53). Minimum slew rates were simulated considering a total capacitive load of 15pF. Results reported in Table 52 and Table 53.

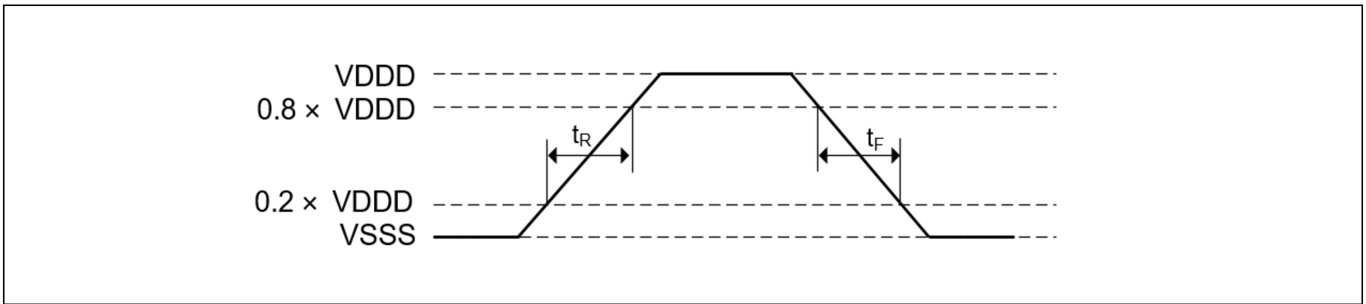


Figure 53 Rise/Fall Time, Slew Rate specified between 0.2 × VDDD and 0.8 × VDDD

Table 52 **Logical Levels for Pins SPI_CLK, CS_N, DI, DO, DIO2, DIO3,** VDDD= 1.71 to 1.89 V, Tb= -40 to +105°C, ambient temperature not below -40°C; all voltages with respect to VSSD digital ground, positive current flowing into pin (unless otherwise specified)

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
LOW level	$V_{IN(L)}$	V	0		0.3 × VDDD	5.3.12	
HIGH level	$V_{IN(H)}$	V	0.7 × VDDD		VDDD	5.3.13	
Input current (0 V < VIN <VDDD)	I_{IN}	µA	-150		150	5.3.14	
Input capacitance SPI_CLK/CSN	C_{IN}	pF	1.8			5.3.15	
Input capacitance DI/DO/DIO2/DIO3	C_{IN}	pF	3.1			5.3.16	
Minimum hysteresis voltage range between 0.3*VDDD and 0.7*VDDD	V_{HYST}	V	0.175			5.3.17	V_{HYST_H} - V_{HYST_L}
Upper hysteresis signal level	V_{HYST_H}	V		0.5 × VDDD + V_{HYST} / 2	0.7 × VDDD	5.3.18	
Lower hysteresis signal level	V_{HYST_L}	V	0.3 × VDDD	0.5 × VDDD - V_{HYST} / 2		5.3.19	

Table 53 **Logic Levels for Pins IRQ, DI, DO, DIO2, DIO3,** VDDD= 1.71 to 1.89 V, Tb= -40 to +105°C, ambient temperature not below -40°C; all voltages with respect to VSSD digital ground, positive current flowing into pin (unless otherwise specified)

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
LOW level	$V_{OUT(L)}$	V	0		0.3 ×VDDD	5.3.20	
HIGH level	$V_{OUT(H)}$	V	0.7 ×VDDD		VDDD	5.3.21	
Output current (LOW)	$I_{OUT(L)}$	mA	-5			5.3.22	
Output current (HIGH)	$I_{OUT(H)}$	mA			5	5.3.23	
Allowed load capacitance to provide maximum signal frequency on DO	C_{LOAD}	pF			15	5.3.24	
Output pad slew rate for rising wave form	dV_{TR}	V/ns	0.32			5.3.25	0.2 × VDDD to 0.8 × VDDD

Spec	Symbol	Unit	Value			Number	Condition
Output pad slew rate for falling wave form	dV_{TF}	V/ns	0.33			5.3.26	0.2 × VDDD to 0.8 × VDDD

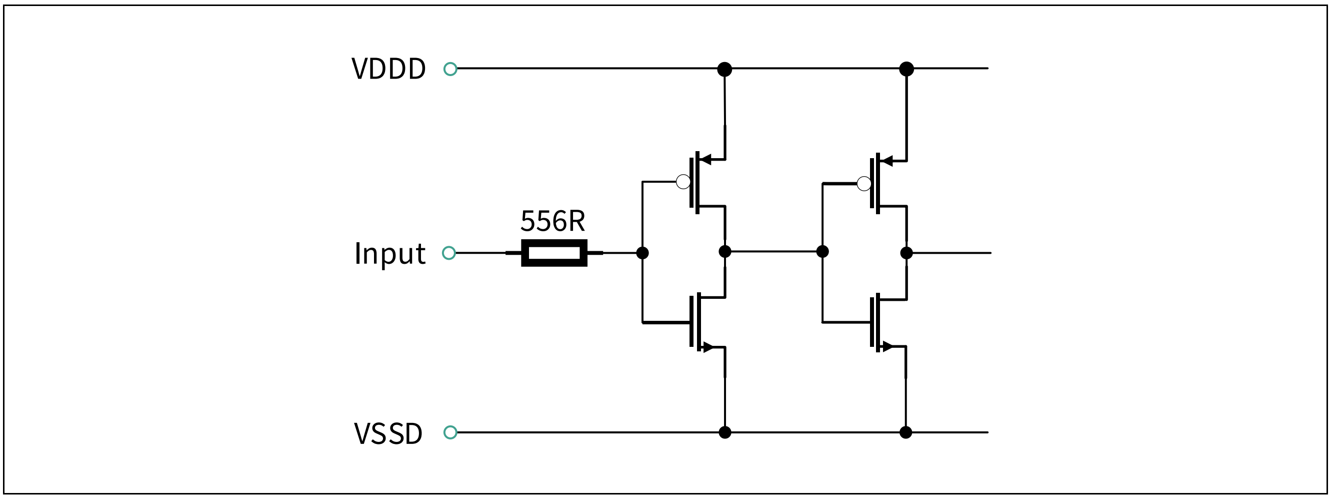


Figure 54 Interface for input pins CLK, CS_N, DI, DO, DIO2, DIO3

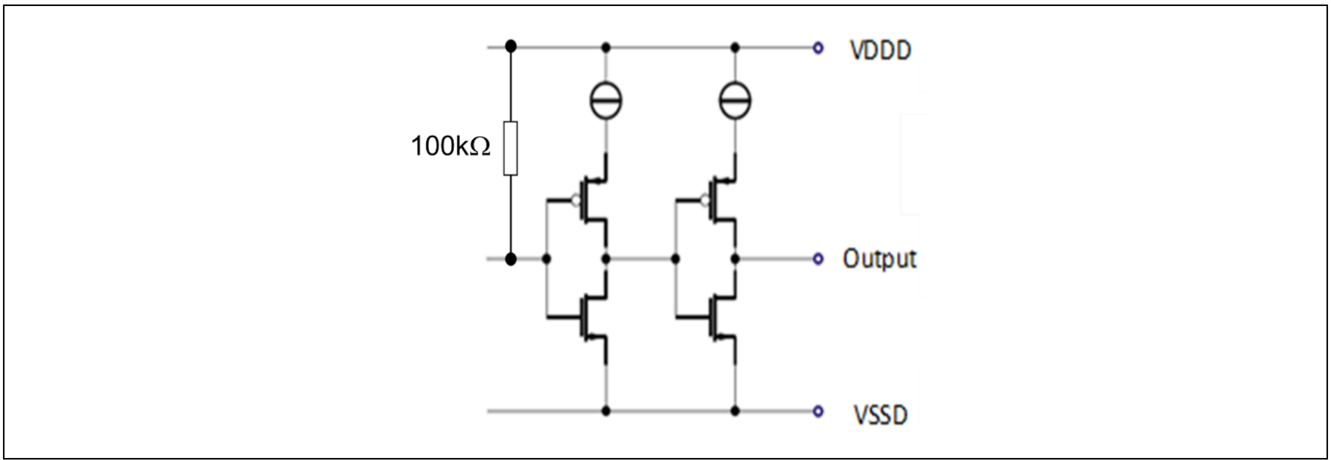


Figure 55 Interface for output pins IRQ, DI, DO, DIO2, DIO3

5.4 Overshoot and Undershoot Waveform Definition

During operation the applied signals and supply levels should not exceed absolute maximum DC levels specified in datasheet. Digital signals can have positive or negative overshoots due to inductive and/or capacitive loads. The following Table 54 reports the allowed overshoot timings and signal levels for all logic signals.

Table 54 Overshoot and Undershoot Signal Levels

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Maximum absolute overshoot voltage level	Vos	V			VDDD+ 0.5 V	5.4.1	see Note:
Maximum absolute undershoot voltage level	Vus	V			VSS – 0.5 V	5.4.2	see Note:

Note: Maximum pad current not exceeding ±5 mA (see alsoTable 53). No slew rate limitation existing on digital signals for overshoots / undershoots.

5.5 IBIS Model

A BGT60ATR24C IBIS Model is available under NDA upon reqest. It is based on timing simulations. In order to better reflect the real timing behavior, different pad models for input/output signals are used and summarized in Table 55. The driver strength for all pads are fix (PRG0=0).

Table 55 IBIS Pad Types and Models (see Ibis model)

Pin	Ibis PAD Model
CSN	IN: MODEL_654_7345_110
CLK	IN: MODEL_654_7345_110
DIO0 / DI	IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59
DIO1 / DO	IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59
DIO2	IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59
DIO3 / Reset	IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59
IRQ	OUT: MODEL_8138_4982_55

5.6 SPI Functionality

Each word transferred over the SPI bus has a length of 1 command byte + 3 data Bytes. The communication is done bitwise. First the address is transferred with MSB first. The address is followed by the R/W-bit and then followed by the data which is sent MSB first, too. At the same time, while command byte is received, a freely from system level configurative global status register (8 bits, GSR0) is serial shifted out on DO (MSB first). On the following 24 clock cycles the selected register content is shifted out on DO, MSB first.
Depending on sent R/W-bit there are two different operation modes available, the write mode and the read mode. Every write mode is a read mode too.

Write-Mode

After the start condition the desired address is sent. The address is 7 bits long followed by a bit that is a data direction bit (read/write). A one indicates a write operation (see Figure 56).

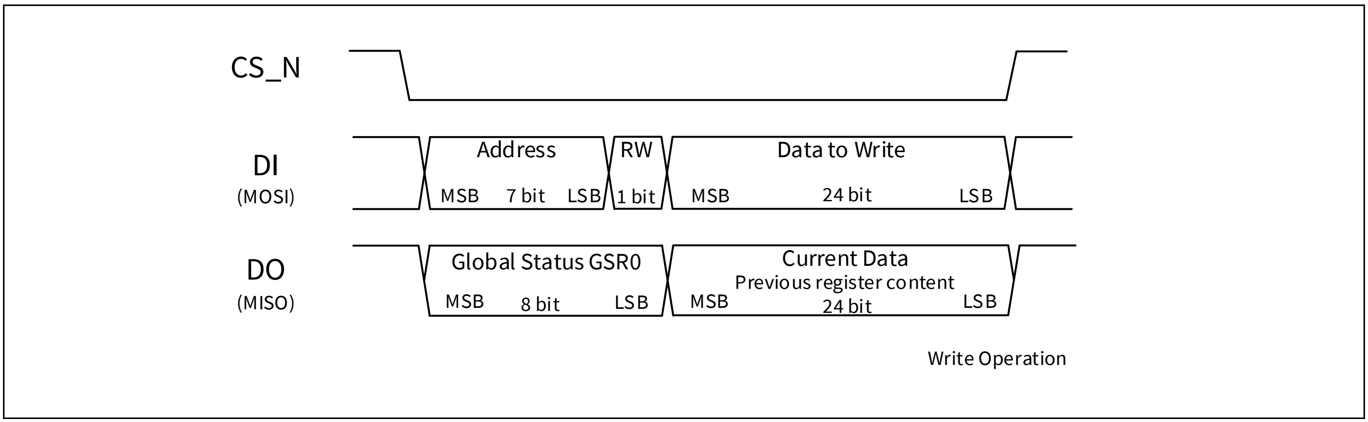


Figure 56 SPI timing write mode

Read-Mode

After the start condition, the desired address is sent like in the write operation. A zero of the R/W-bit indicates a read access. The data on DI after the command byte may contain any value. The DO behavior is the same as in write mode.

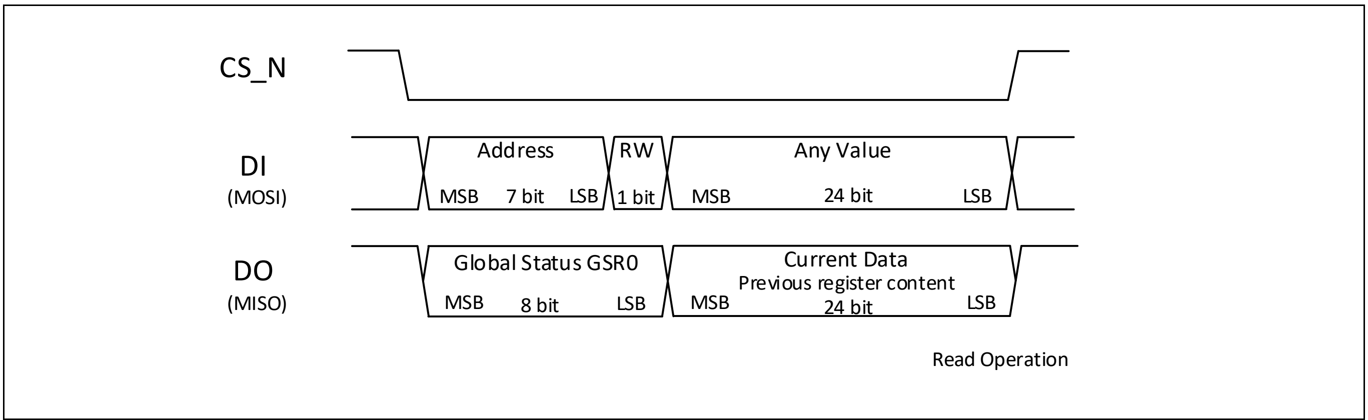


Figure 57 SPI timing read mode

5.7 SPI Burst Mode

The burst mode can be used to read or write out several registers or some data from the FIFO instead of reading just single registers or data. The burst mode command is sent by the host. The burst mode command consists of several bit fields and is shown in Figure 58.

Burst Mode Command

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR							RW	SADDR							RWB	NBURSTS							RSVD								

Figure 58 Burst mode command

The following Table 56 shows a detailed description on the burst mode command bit fields.

Table 56 Burst Mode Command Bit Field Description

Bit field	Bit	Description	RST
ADDR	31:25	To enter the burst mode the following address is used: 0x7F … request the burst read/write.	
RW	24	Read/Write register access: Fixed to 1_B … write to address 0x7F	
SADDR	23:17	Starting address where the burst starts processing: < 0x62 Register access == 0x62 FIFO access > 0x62 Reserved - Address is incremented automatically inside a burst.	
RWB	16	Burst read or write: 0_B … Perform a read burst 1_B … Perform a write burst, (writes to FIFO not supported)	
NBURSTS	15:9	Number of processed data blocks: 0x00… “unbounded” burst accesses 0x01 to 0x7E … number of words to transfer	

Note:

A single data block is 24 bits width for both, the sampling memory and the registers.

Burst Mode Operation

After the start condition the 32 bits burst mode command is sent from the SPI master on DI. At the same time, the status register GSR0 (four 1_B bits + four status bits) followed by 24 padding bits set to 0_B is shifted out on DO. After the command sequence is done, the register/FIFO data is shifted out to the SPI master on DO. In burst write mode, the register data to be written is shifted in from the SPI master (application processor e.g.).

Burst Mode Read Sequence:

In the read sequence, the SPI master reads from the device.

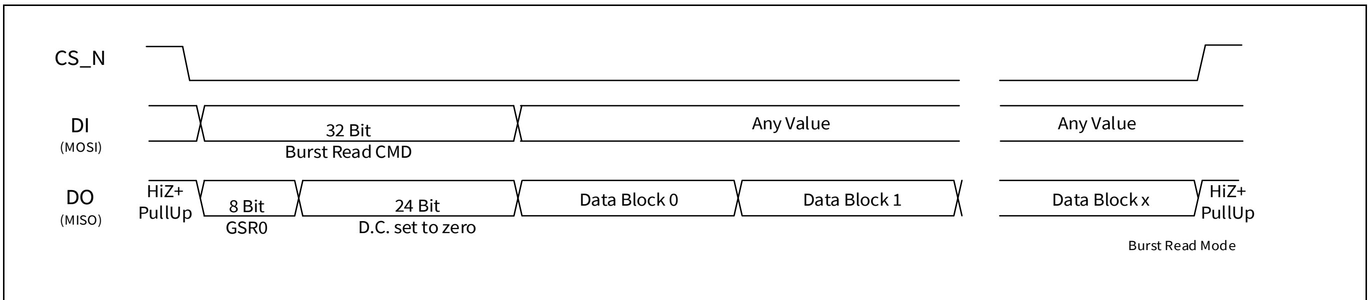


Figure 59 Burst mode read sequence

Burst Mode Write Sequence:

In the burst write mode, the SPI master writes to the device.

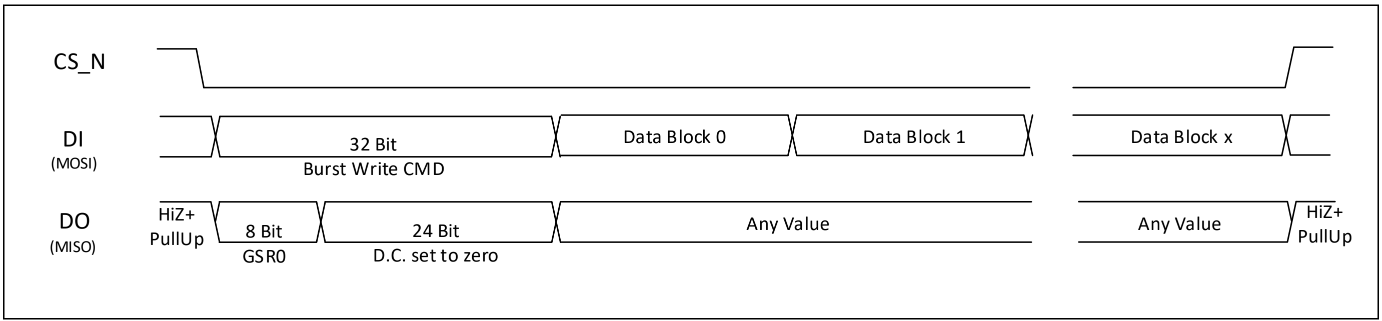


Figure 60 Burst mode write sequence

Sampling Data Arrangements in Data Blocks

The data from the FIFO are streamed out during the burst read request, starting from the FIFO address zero. The 1st ADC is the ADC channel with the lowest channel number. As far as the sampling memory is organized in 24 bits and up to four ADC channels are selectable through the ADC channel selection bits (CSx: BBCH_SEL, see section 4.10) the data blocks are arranged as follows.

In case a single ADC is selected, the data blocks are shown in Figure 61.

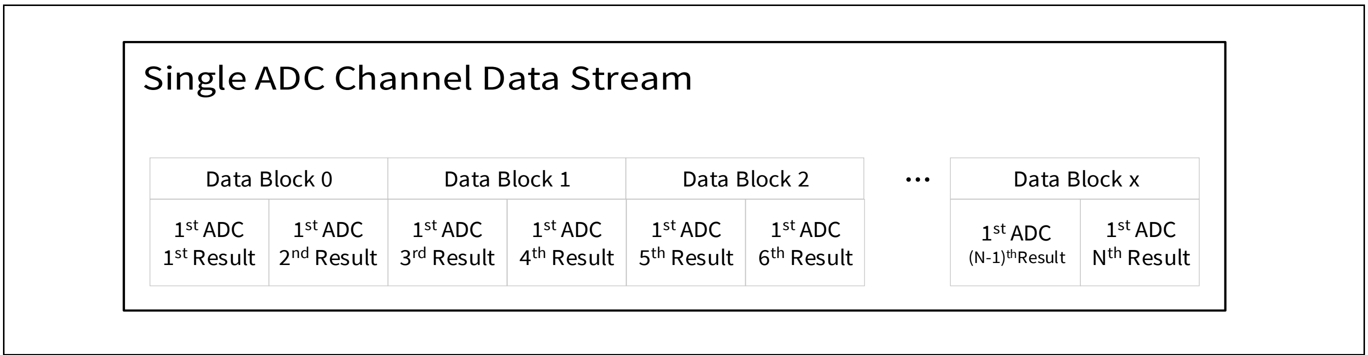


Figure 61 Single ADC channel selected

In case two ADCs are selected, the data blocks are arranged as shown in Figure 62.

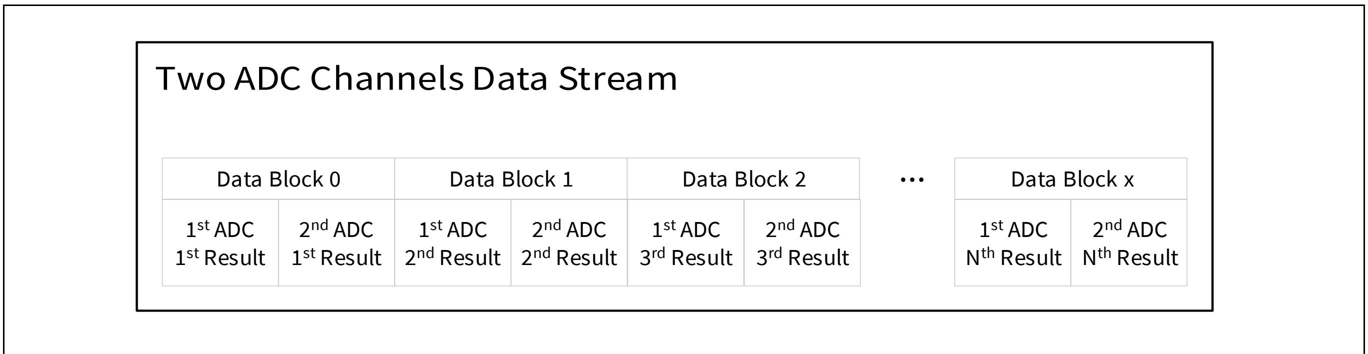


Figure 62 Two ADC channels selected

In case three ADCs are selected, the data blocks are arranged as shown in Figure 63.

Three ADC Channels Data Stream

Data Block 0		Data Block 1		Data Block 2		…	Data Block x	
1st ADC 1st Result	2nd ADC 1st Result	3rd ADC 1st Result	1st ADC 2nd Result	2nd ADC 2nd Result	3rd ADC 2nd Result		…th ADC Nth Result	…th ADC Nth Result

Figure 63 Three ADC channels selected

In case four ADCs are selected, the data blocks are arranged as shown in Figure 64.

Four ADC Channels Data Stream

Data Block 0		Data Block 1		…	Data Block x	
1st ADC 1st Result	2nd ADC 1st Result	3rd ADC 1st Result	4th ADC 1st Result		…th ADC Nth Result	…th ADC Nth Result

Figure 64 Four ADC channels selected

Example: Burst Mode Read Sampling Memory Sequence

The following burst mode command is sent from the host to initialize the burst mode to read from the FIFO an undefined number of sampling data:

BMCMD_RS = (ADDR = 0x7F, RW = 0x01, SADDR = 0x62, RWB = 0x0, NBURSTS = 0)

REMARK:

For each burst read request to the sampling memory, the sampling-memory address pointer is reset to the initial value. So that memory can be read out from the beginning until the application processor stops burst reading.

Example: Burst Mode Read Registers Sequence

The following burst mode command is sent from the host to initialize the burst mode to read out 10 registers starting from register address 3:

BMCMD_RR10 = (ADDR = 0x7F, RW = 0x01, SADDR = 0x3, RWB = 0x0, NBURSTS =10)

5.8 SPI Error Detection

SPI BURST_ERR and CLK_NUM_ERR (see also Table 45) will be cleared after these resets:

- SW reset
- HW reset

SPI BURST_ERR and CLK_NUM_ERR are reported in the global status bits of the next SPI transaction and latched as sticky bits in the FSTAT register.

In order to understand if the captured sample data are corrupted, the host can evaluate the bit field CLK_NUM_ERR and SPI BURST_ERR as reported inTable 57.

Table 57 SPI BURST_ERR and CLK_NUM_ERR Definitions

Length Range	Transaction	SPI BURST_ERR	CLK_NUM_ERR	Behavior on read/write
0	Null command	0_B	0_B	Ignored
1-31	Short length error in single	0_B	1_B	Command ignored
>32	Long length error in single	0_B	1_B	Extra bits ignored
1-31	Short length error in SPI burst header	0_B	1_B	Command ignored
1-7	Short length error in QSPI burst header	0_B	1_B	Command ignored
<24xN	Missing whole data word in bounded burst	1_B	0_B	Available data words used
>24xN	Extra whole data word in bounded burst	1_B	0	Extra data word(s) ignored
%24>0	Misaligned bit-count for bounded burst	1_B	1_B	Extra bits ignored
%24>0	Misaligned bit-count for infinite burst	0_B	1_B	Partial data word may be discarded

Note:

- *Ignored write transaction means that no register (or memory) content is affected by the partial write command, or incomplete data word.*

- *Ignored read transaction means that the returned data is invalid, and for the FIFO no words are removed by the partial read command, or incomplete data word.*

- *Discarded read transaction means that the data is already read from the FIFO but only partially transferred; subsequent read pops next word from FIFO.*

- *Data from the FIFO may be discarded after a length error in the infinite burst (NBURST=0) occurs. The FIFO read has to happen, since at that stage the data is required to be shifted out, but if not all bits are shifted out the FIFO is already read and the partial data word may be discarded.*

5.9 Quad SPI Mode

SPI will be set by default to a general compatible mode: suitable up to 25MHz

To address the quadSPI the chip will provide 4 bidirectional signal pins (SPI_DIO[0..3])

DualSPI mode is not supported

Quad SPI

	ADDR		WAIT		Data												
DIO 0	C4	C0			D4	D0	D4	D0	D4	D0	D4	D0	D4	D0	D4	D0	
DIO 1	C5	C1			D5	D1	D5	D1	D5	D1	D5	D1	D5	D1	D5	D1	…
DIO 2	C6	C2			D6	D2	D6	D2	D6	D2	D6	D2	D6	D2	D6	D2	
DIO 3	C7	C3			D7	D3	D7	D3	D7	D3	D7	D3	D7	D3	D7	D3	

Figure 65 QSPI Protocol implementation (read mode only)

Only 1 command is supported:

- Command = same as read address (either registers or FIFO). An address ≥ 0xC0 is not allowed.
- During burst read, the provided address will be incremented internally, the following data are taken from the address related location (<0x62 read from register, afterwards read from FIFO)

QSPI can be

- burst read of registers (>= 2 wt. cycles)
- burst read of FIFO (>= 2 wt. cycle)
- burst read over 0x62 border (>= 2 wt cycle)

5.10 Hardware Reset Sequence

After power up, the chip is not in a default reset condition and requires a dedicated HW reset as described below. Only after the HW reset also other reset sequences can be triggered via SPI (e.g. SW, FIFO and FSM- reset). For such SPI triggered resets an external OSC_CLK (see Table 2) needs to be applied, while the HW reset does not require any external OSC_CLK.

HW Reset Sequence: While CS_N is = '1_B' DIO3 must perform a $1_B \rightarrow 0_B \rightarrow 1_B$ transition

The behavior is presented in Figure 66 with:

T_CS_BRES = 100 ns

T_RES = 100 ns

T_CS_ARES = 100 ns

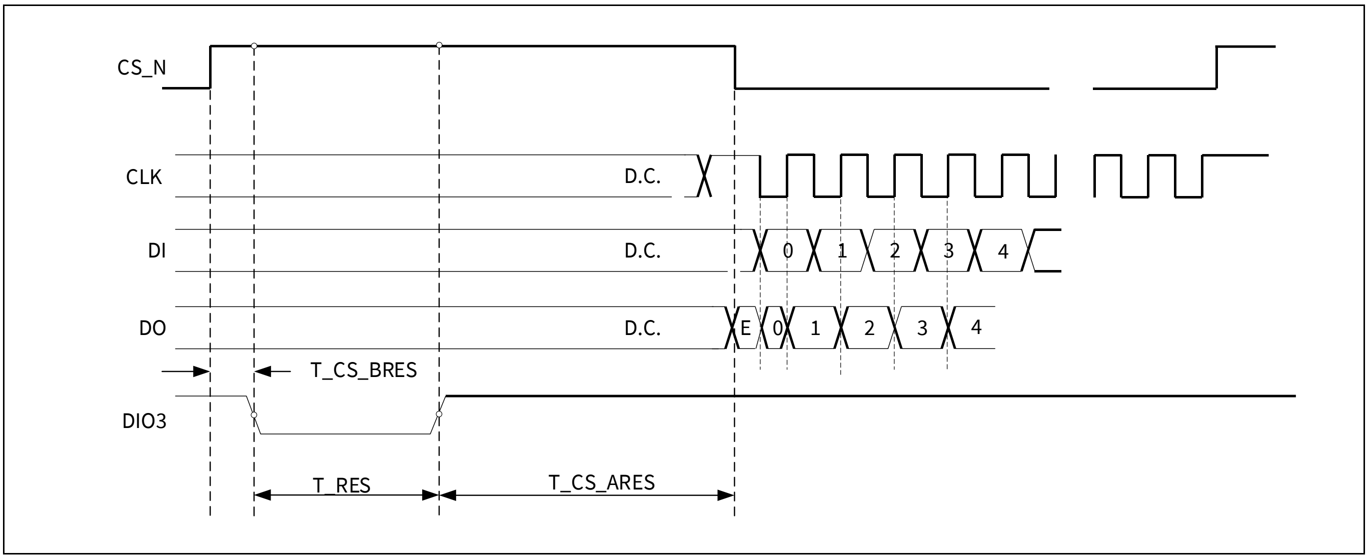


Figure 66 **Hardware reset Sequence**

5.11 Software Triggered Resets

Besides the hard reset, three reset sequences are supported and can be triggered in the ISO register (see also 4.2). They are defined according to the following hierarchy:

Soft reset → FIFO reset → FSM reset

- **Software Reset**
  - Resets all registers to default state
  - Resets all internal counters (shape, frame e.g.)
  - Perform FIFO reset
  - Performs FSM reset
  - A delay of 100 ns after the SW_RESET is needed before the next SPI command is sent

- **FIFO Reset**
  - Reset the read and write pointers of the FIFO
  - Array content will not be reset, but cannot be read out
  - FIFO empty is signaled, filling status = 0
  - Resets register FSTAT
  - Performs an implicit FSM reset

- **FSM Reset**
  - Resets FSM to deep sleep mode
  - Resets FSM internal counters for channel/shape set and timers
  - Resets STAT0 and STAT1 register
  - Reset PLL ramp start signal
  - Reset PA_ON
  - Terminates frame (shape and frame counters incremented although maybe not complete)

6 PLL Domain Functional Specification

The PLL is designed to generate high performance frequency chirps in the range of 58 GHz to 62 GHz. The modulation is performed inside the PLL bandwidth (in-band-modulation) with an analog charge pump based fractional-N RF-PLL architecture. It furthermore features a shape generator with high flexibility to allow different ramp shapes and duration times. The loop requires a low noise reference clock with a nominal frequency of 80 MHz.

6.1 PLL Interfaces and Clock Distribution:

Figure 67 shows the interfaces to the PLL and the distribution of the 80 MHz reference clock.

6.2 Reference Clock Distribution

The external 80 MHz reference clock signal is provided via a short, low jitter path directly to the input of the PLL analog part. From there the clock is distributed to the reference clock buffer of the PLL and also via another path to the STS, which is the defined interface between the PLL analog and the digital part. These paths are independent from each other since the clock provided through the STS to the output of the PLL macro ("osc_clk2dig") serves as the clock for the main FSM. It must be available even when the PLL is put into power down. Therefore the usage of internally generated supplies of the PLL is avoided. The main FSM clock can be gated via a dedicated register bit called PACR1.OSCCLKEN (see section 4.6) which quiets the clock path already at its beginning.

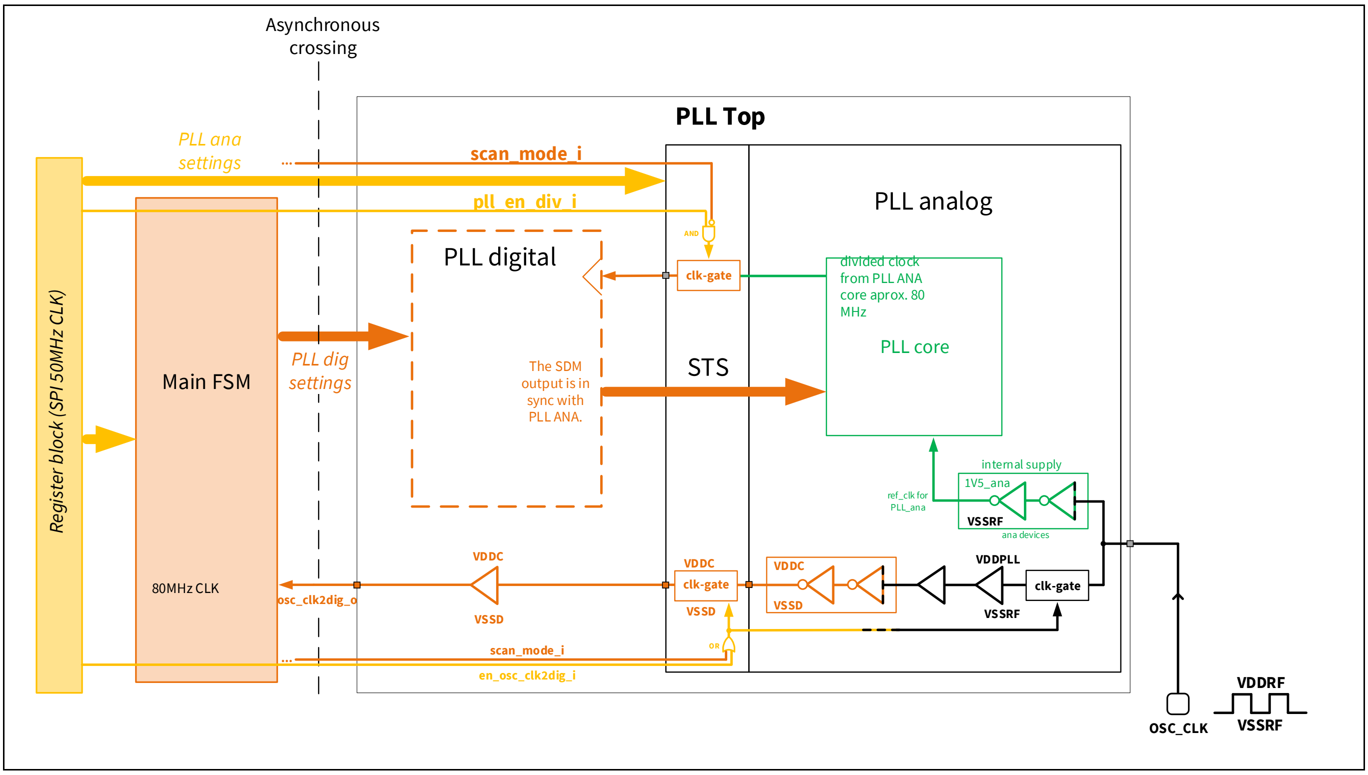


Figure 67 PLL and 80 MHz clock interface to the main FSM

6.2.1 Interfaces to the PLL

Most static settings and control signals dedicated to the analog part of the PLL are treated as asynchronous signals and are passed from the register bank to the STS of the PLL. This applies to digital signals that are not timing critical. Ramp generation parameters provided from the main FSM to the digital part of the PLL are registered inside the PLL digital. The start signal of the ramp also acts as a synchronization signal of the ramp parameters. This is required since the PLL digital runs on the divided clock of the PLL which ensures a known and synchronous timing relation between the sigma-delta bit stream and the analog part of the PLL that realizes the ramping behavior. The divided clock is only available if the PLL macro and the VCO are activated. Other control signals from PLL digital to the analog part are kept asynchronous. In order to close the PLL loop the analog part of the PLL core has interfaces to the RF-macro where the VCO and a part of the divider chain are located.

6.3 PLL Parameters and Specification

Table 58 summarizes the target parameters of the PLL-based frequency generator.

Table 58 PLL Specifications, VDDPLL=1.71 to 1.89 V, VDDLF=2.5 to 3.63V, Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition/Note
Parameter			Min	Typ	Max		
Reference Clock							
Reference Frequency	f_{ref}	MHz	75	80	85	6.3.1	$f_{ref} = f_{SYS\_CLK}$ See 2.2 78 MHz not allowed
Rise and Fall Time of Reference Clock	$t_{rs, fs, clk}$	ns			6	6.3.2	1.8 V CMOS clock
PLL Chirp Parameters							
Output Frequency Range	f_{RF}	GHz	58		62	6.3.4	Range depends on the VDDLF value
Continuous FM-Chirp Bandwidth	BW	GHz	0		4	6.3.5	PLL tuning range
VDDLF Range	VDDLF	V	2.5		3.63	6.3.6	4 GHz modulation BW requires at least VDDLF= 3.3V
Chirp slope	Slope	MHz/µs			400	6.3.7	
Frequency Ramp Linearity Error	Error	%			1	6.3.8	For 2 GHz BW minimum See 6.3.1, Figure 13, Table 15
Frequency Ramp Settling Time (fast chirp feature active)	$t_{PLL, settle}$	µs		5		6.3.9	See 6.3.2
PLL Phase Noise Single Sideband	$PN_{PLL,100kHz}$	dBc/Hz		-80	-75	6.3.10	@100kHz offset

6.3.1 Frequency Ramp Linearity Definition:

Frequency ramp linearity error is defined to be <1% of the FM-chirp bandwidth. The linearity error is calculated as the deviation from an “ideal” frequency ramp. The specification needs to be fulfilled after the frequency ramp settling time (see also section 3.3). The assumed worst-case FM-chirp bandwidth for linearity evaluations is 2 GHz.

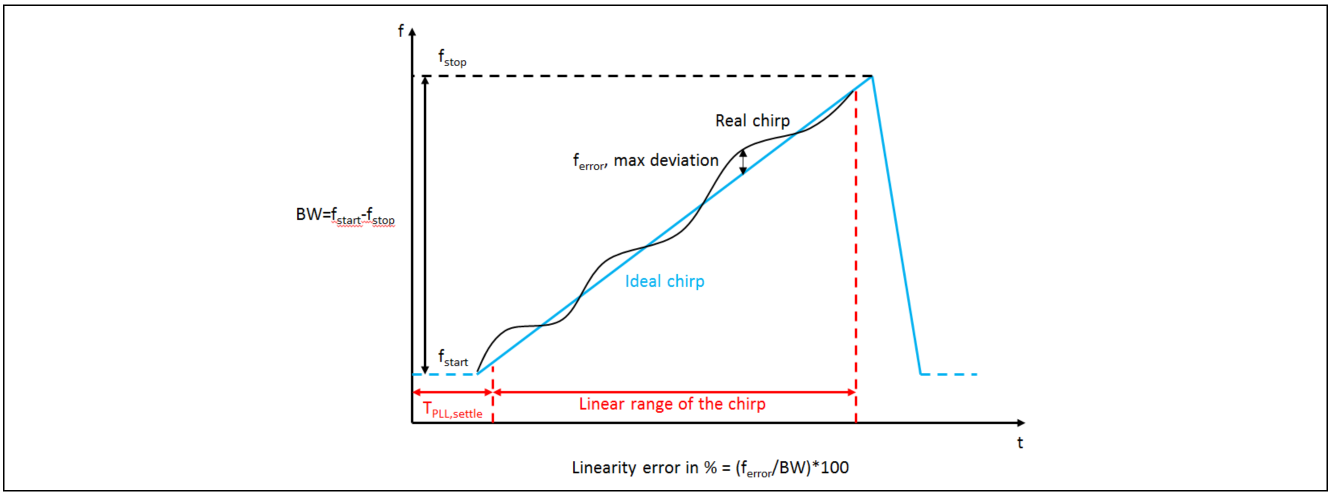


Figure 68 Frequency linearity definition

The max frequency error expected, assuming 2 GHz minimum BW and a max deviation of 1%, will be 20 MHz.

6.3.2 Frequency Ramp Settling Time

It is the time required by the PLL to damp undershoot and overshoot in case of saw-tooth shapes. A qualitative view is shown in Figure 69. See section 3.3 for a more detailed definition of the timings.

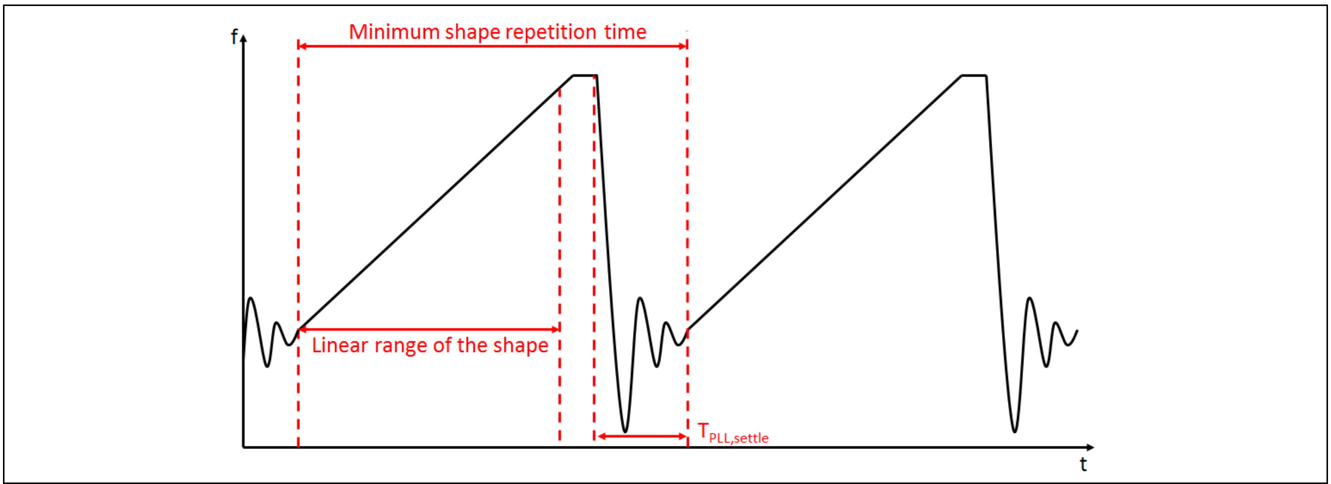


Figure 69 Chirp settling time

7 Analog-RF Domain Functional Specification

In the analog functional specification all analog components like RF frontend (RF FE), baseband amplifiers, and filters are described in more details.

The register definitions for the components are in section 0.

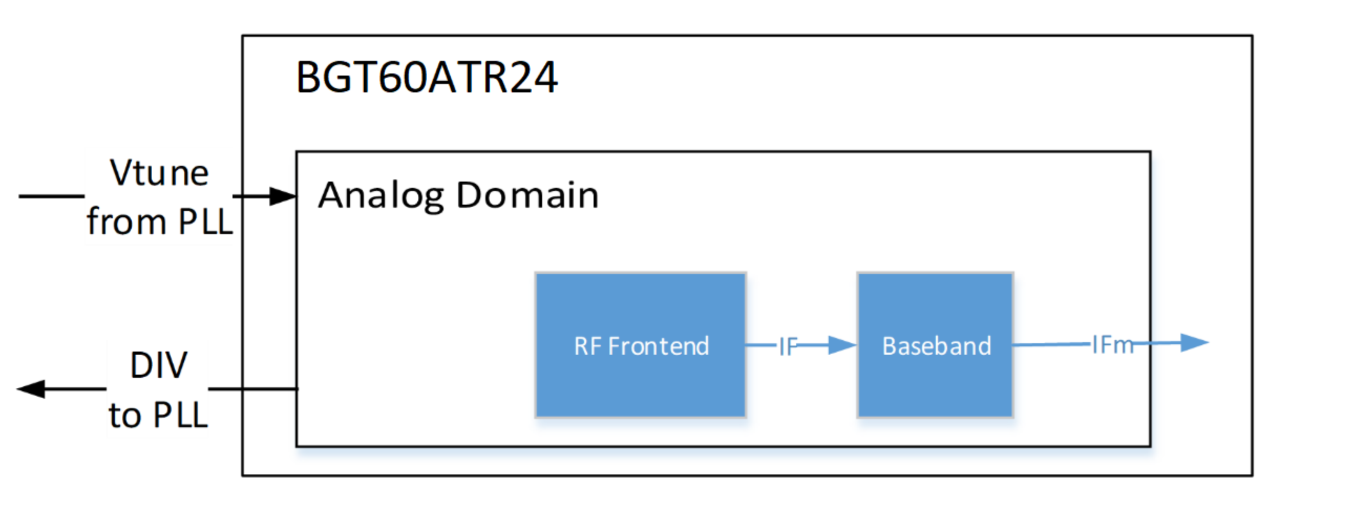


Figure 70 Analog domain simplified block diagram

7.1 RF Frontend (RF FE)

In the RF frontend, all features to enable the radar functionality are implemented.

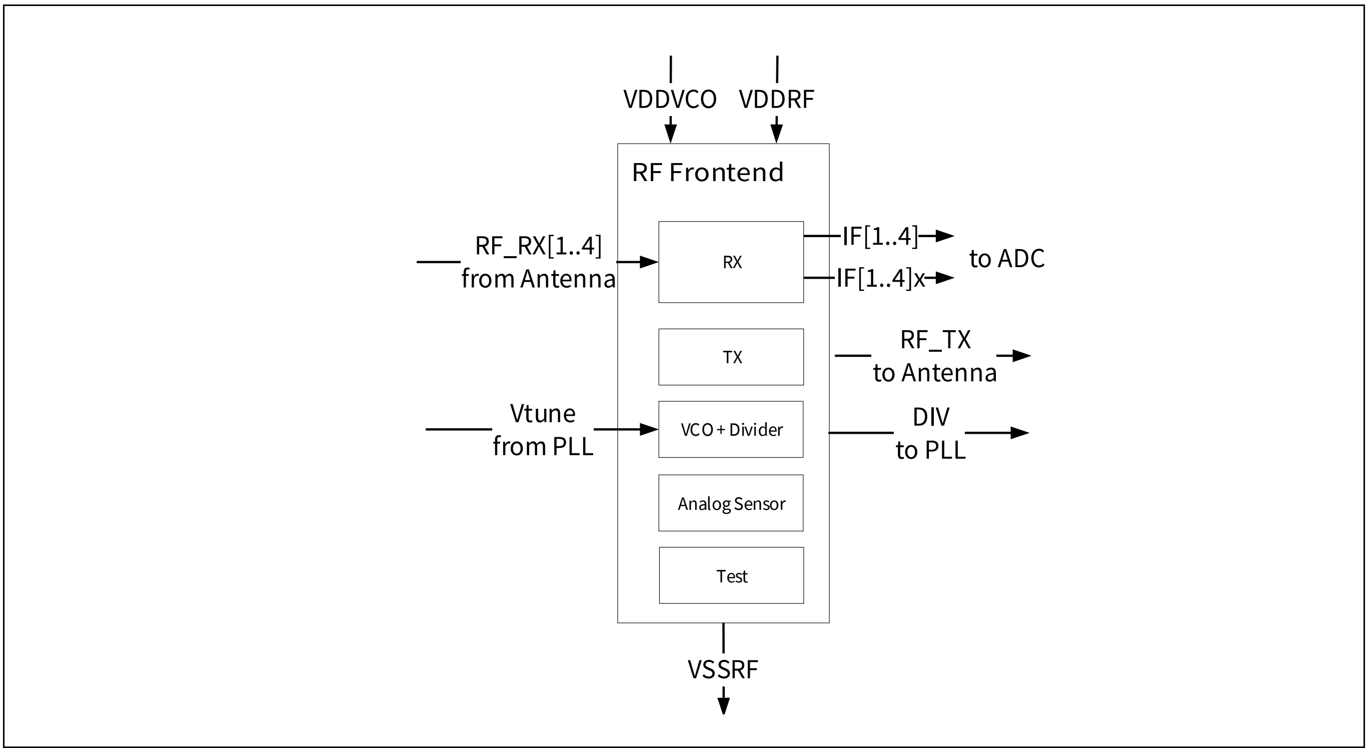


Figure 71 Simplified block diagram of BGT60ATR24C transceiver frontend

7.1.1 On-Chip Analog Sensor Output

The analog sensor outputs are connected to the SADC. See section 4.9 for the SADC input configuration. See also section 4.9 for enable pins definition.

7.1.2 RF FE Specifications

In the table below the target specifications for the RF frontend measured at die PAD interface.

Table 59 **RF FE Specifications,** min and max values cover the specified frequency range, f_{RF}= 58.0 to 62.0 GHz. Temperature range, Tb= -40 to +105°C, and voltage supply range, VDDRF= 1.71 to 1.89 V (unless otherwise specified)

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Frequency Range	f_{RF}	GHz	58.0		62.0	7.1.1	
Transmitter (for both TX channels)							
Transmit Output Power	P_{TX}	dBm	1.5	4.0	6.5	7.1.2	Conductive Power
Output Power Variation over Temperature	P_{TX_Temp}	dB	-1.8		+0.7	7.1.3	For Tx DAC set to #31
Transmitter Power Control Dynamic Range	P_{TXD}	dB		15		7.1.4	
DAC Resolution Transmitter Power Control	P_{TXC}	Bits		5		7.1.5	By design
Phase difference TX1 – TX2	$\Delta\varphi_{TX1-TX2}$	deg		180		7.1.6	By design
Receiver (for all four RX channels)							
Receiver Conversion Gain[2)]	CG_{RX}	dB	10.5	13	15.5	7.1.7	Including loss of package transition
Conversion Gain Variation Over Temperature	CG_{RX_Temp}	dB	-1.8		+0.7	7.1.8	Including the complete baseband chain
Receiver Single Sideband Noise Figure @ 100kHz offset	$NFssb_{RX}$	dB		13	16	7.1.9	Including loss of package transition
Receiver 1-dB Compression Point	$P\text{-}1dB_{RX}$	dBm	-10	-4		7.1.10	Including loss of package transition
Channel-to-Channel RX Isolation[3)]	Iso_{RX}	dBc	25		40	7.1.11	@300kHz VCO to RF offset in baseband, amplitude relative to reference channel
LO feedthrough at the RX port[3)]	$LOfeed_{RX}$	dBm	-30	-40	-50	7.1.12	
TX-to-RX Isolation[3)]	Iso_{TXRX}	dB	30	45		7.1.13	TX DAC state 31, one TX active
RX channel-to-channel phase difference	$\Delta\varphi_{RXm-RXn}$	deg		0 180		7.1.14	By design $\Delta\varphi_{RX1-RX2}$, $\Delta\varphi_{RX3-RX4}$

							$\Delta\varphi_{RX1-RX3}$, $\Delta\varphi_{RX1-RX4}$, $\Delta\varphi_{RX2-RX3}$, $\Delta\varphi_{RX2-RX4}$
Sensors							
Temperature Sensor Range	T_b	°C	-40		105	7.1.15	
Chip Backside Temperature (Temp) Vs Temperature Sensor Readout (Tsense) Relation	Temp Tsense	°C V		$Temp = \frac{Tsense - a}{b}$		7.1.16	
Temperature Sensor Offset (a)	a	V	0.784	0.7989	0.816	7.1.17	
Temperature Sensor Slope (b)	b	V/K		0.00297		7.1.18	
Output Power at Chip Pad Vs TX Peak Detector Readout Relation	Pout PPD_PA[4]	dBm V		$Pout = t_1 * \ln\left(\frac{PPD\_PA + y_0}{A_1}\right)$ y_0 = 0.04455 V A_1 = 0.18855 V t_1 = 11.35808 dBm		7.1.19	PPD_PA selected at SADC input
TX Peak Detector Accuracy	PPD_PAacc	dB	-2		+2	7.1.20	Over f_{RF}
TX Peak Detector Dynamic Range	PPD_PA_{DR}	dBm	-10		+10	7.1.21	Min. 8 bits SADC

[2]: power to voltage gain;

[3]: on Evalboard

Output power can be evaluated by sampling the level of the peak detector level at the output of the TX power amplifier. This signal has to be compared to a reference to de-embed thermal drift of the sensor. Therefore, both signals on channel SADC:CH3 (pd_out) and SADC:CH4 (pd_outx) are sampled by the SADC in two consecutive steps. PPD_PA= pd_out - pd_outx… See section 4.9.

Note: The 80 MHz spur clock signal could affect the SADC the readout (+/- 10mW). In order to have a more stable read out for the sensors, 16 avg for each sensor measurement are recommended.

7.2 Analog Baseband: Amplifiers and Filters

The baseband amplifiers and filters adjust the IF signals to fulfill the system requirements. They set the signal levels to drive full scale the ADC inputs without clipping.

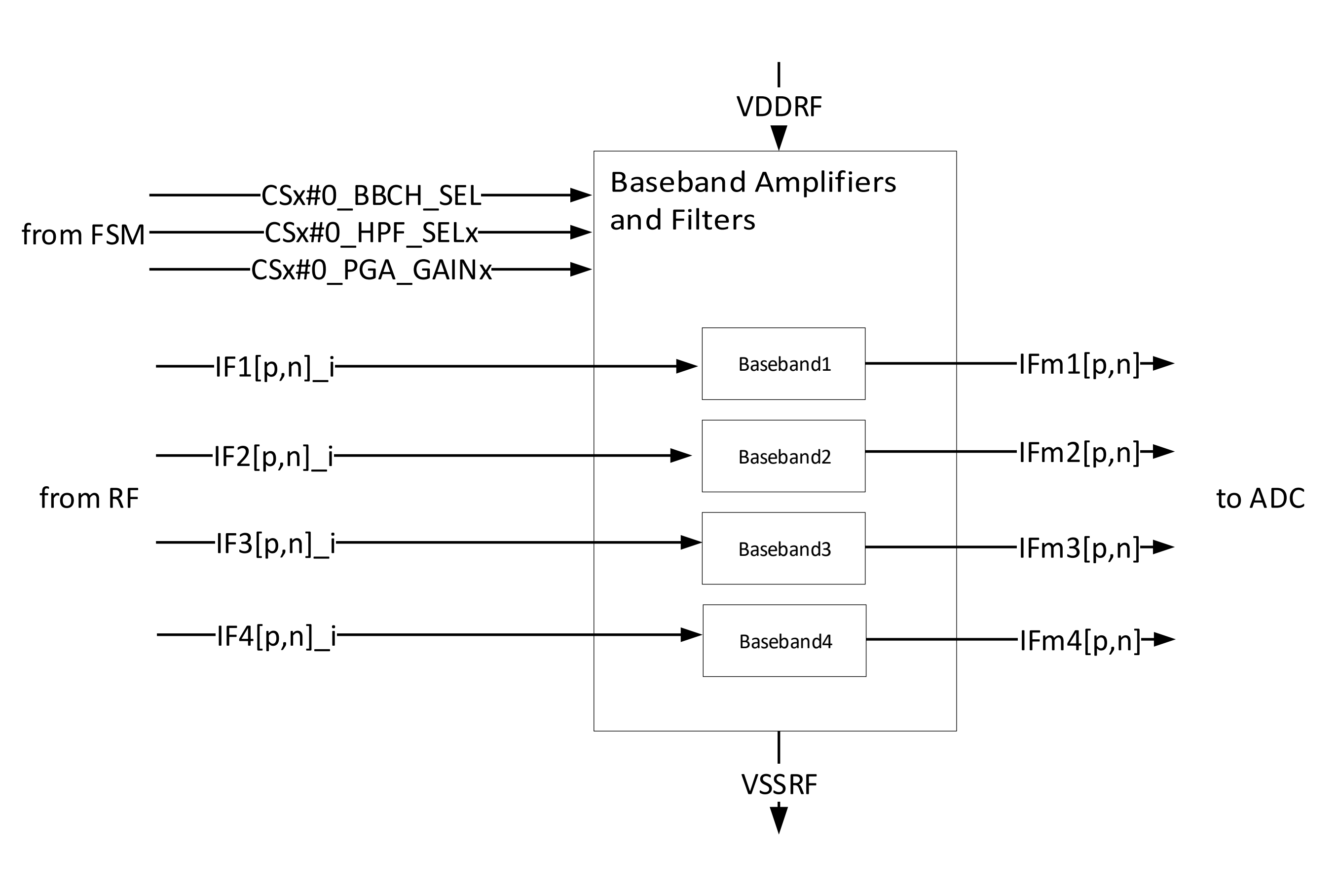


Figure 72 Baseband amplifiers and filters block diagram

7.2.1 Baseband Characteristics

The baseband block consists of four channels. Each channel consists of a high pass filter (HPF), a variable gain amplifier (VGA), and anti-aliasing filter (AAF) plus a driver for the ADC (see Figure 74).

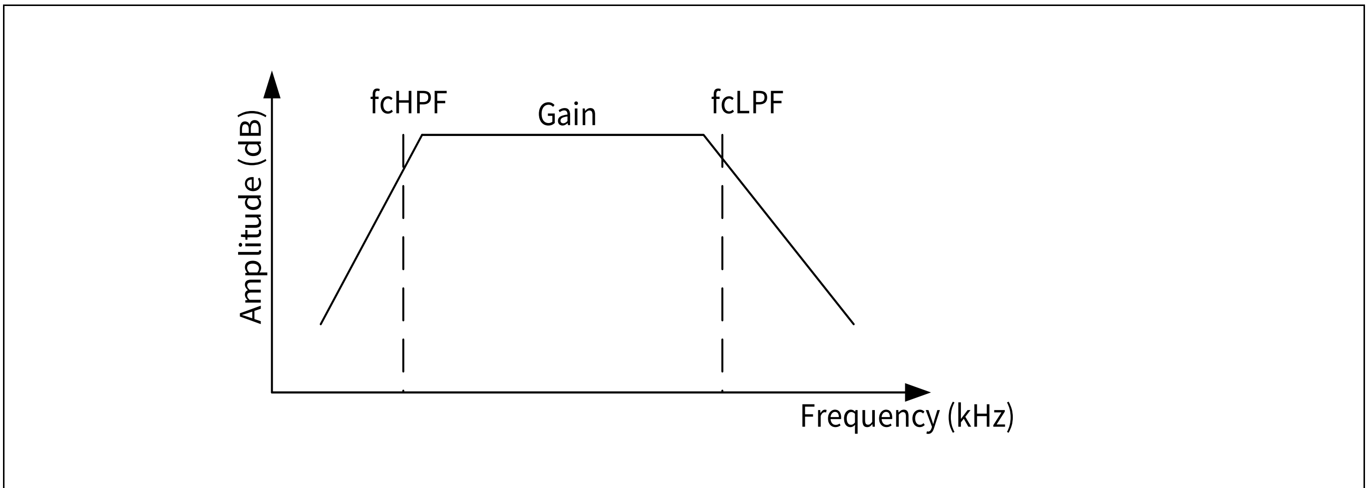


Figure 73 Baseband characteristic

The high pass filter is used in order to remove the DC-offset at the output of the RX mixer and also suppress the reflected signal from close in unwanted targets (radome, e.g.).

7.2.2 Baseband Requirements

The high pass filter can be tuned to accommodate different fcHPF according to different modulation parameters. As presented in Table 60 four different settings are possible.

Given the expected power levels the radar system will deal with, the HPF should not degrade the linearity of the system.

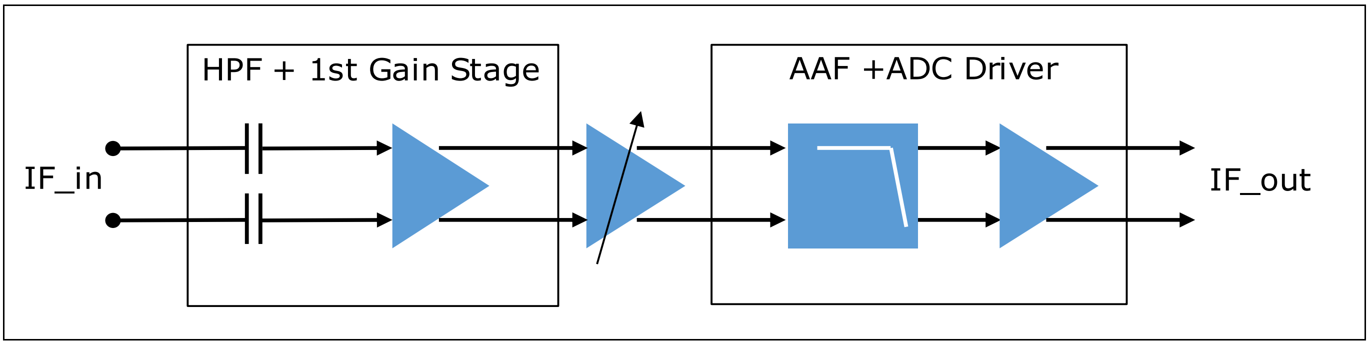


Figure 74 Baseband simplified block diagram, one for each channel

After the AC-coupling, the IF signals are amplified by the first amplifier stage. The first stage shows a selectable voltage gain of 18 or 30dB. The gain can be adjusted in the VGA in 6 steps of 5dB each up to a maximum gain of 30dB. The VGA is followed by a two stages, four poles antialiasing filter. The signal is then applied to an ADC driver amplifier, which has a gain of 1. Overall the baseband chain can be set to a maximum gain of 60dB.

The specific parameters of the baseband chain are summarized in Table 60, 0, and Table 62.

Table 60 High Pass Filter Selection. VDDRF= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	**Unit**	**Value**			**Number**	**Description**
Parameter		Min	Typ	Max		
Fc_HPF_0	kHz	12	20	28	7.2.1	HPF 3 dB cutoff frequency
Fc_HPF_1	kHz	32	40	48	7.2.2	HPF 3 dB cutoff frequency
Fc_HPF_2	kHz	63	70	93	7.2.3	HPF 3 dB cutoff frequency
Fc_HPF_3	kHz	65	80	95	7.2.4	HPF 3 dB cutoff frequency

Table 61 Baseband Gain Stages, VDDRF= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	**Unit**	**Value**			**Number**	**Description**
Parameter		Min	Typ	Max		
1st Gain Stage	dB		18/30		7.2.5	Selectable, by design
VGA	dB		30		7.2.6	6 steps
VGA Step Size	dB	4	5	6	7.2.7	

Table 62 Antialiasing Filter Specification, VDDRF= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	**Unit**	**Value**			**Number**	**Description**
Parameter		Min	Typ	Max		
fcLPF	kHz	450	500	650	7.2.8	3 dB cutoff frequency
LPF_Order			2nd		7.2.9	Four poles, by design
LPF_Flatness	dB		1		7.2.10	In band flatness, guaranteed by design

8 MADC Domain Functional Specification

The multichannel ADC (MADC) block consists of four differential SAR ADCs. The four ADCs are capturing the four differentials IF output signals from the baseband and convert them into a digital representation of the same. The one 1.5 V supply (VDDC) is internally generated by a dedicated LDO (see Figure 5). This block is enabled by bit MADC_EN in Table 30, parameters are set in 4.3. Each channel of the MADC can be enabled/disabled together with the respective baseband channel by the bits BBCH_SEL in Table 30. To simplify the dataflow to the memory the ADC channels to be used can be selected via the BBCH_SEL in Table 30. See also APU and APD in Table 37 and paragraph 5.2.

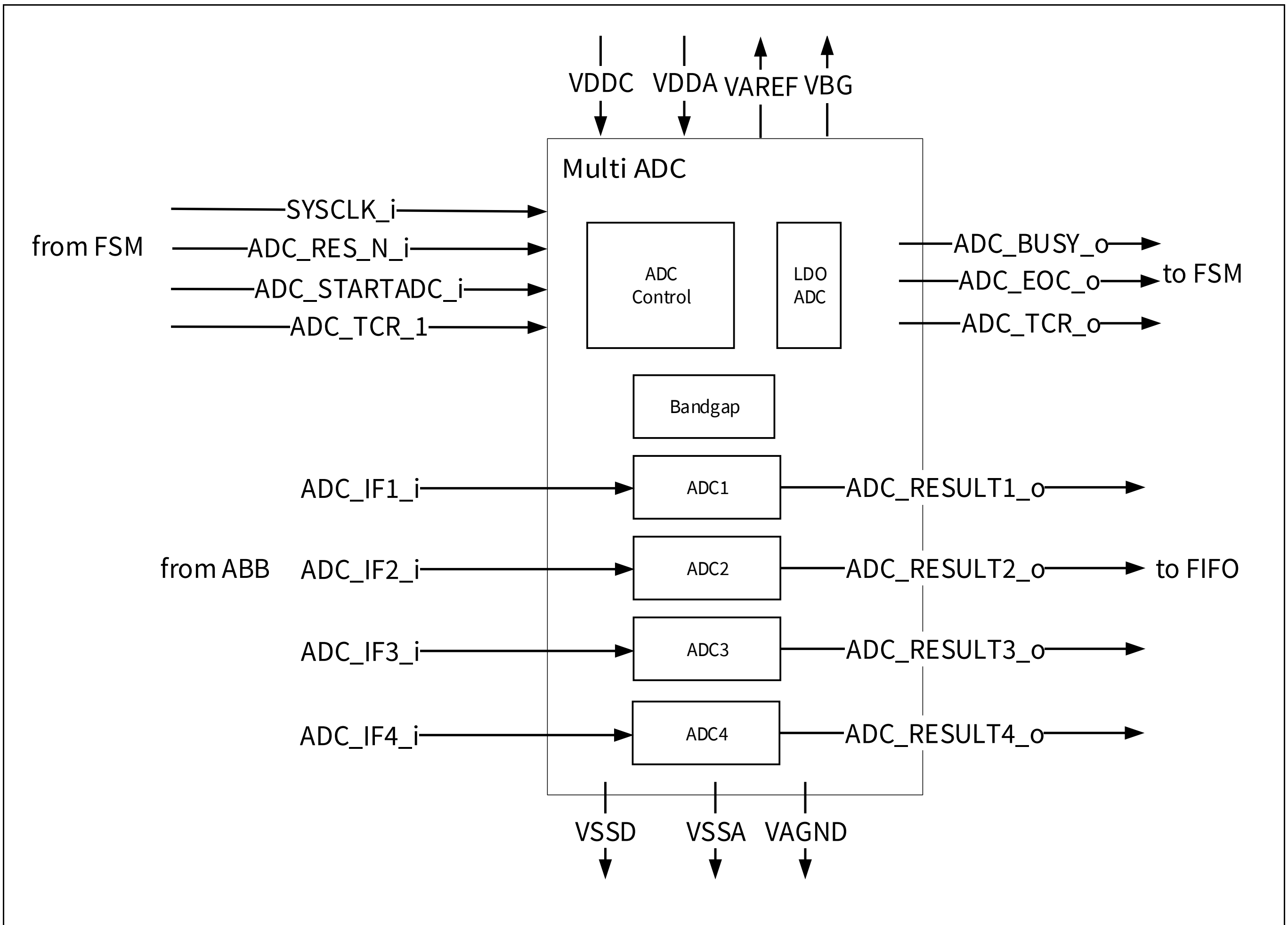


Figure 75 MADC block diagram

8.1 MADC Supply Voltage Requirements

The voltage supply to the ADC domain is provided on pin VDDA and the output of the internal ADC reference voltage is provided on pin VAREF. In order to filter out the voltage ripples due to switching effects a low ESR bypass capacitor with a value of C_{b2} = 470 nF should be used on the PCB.

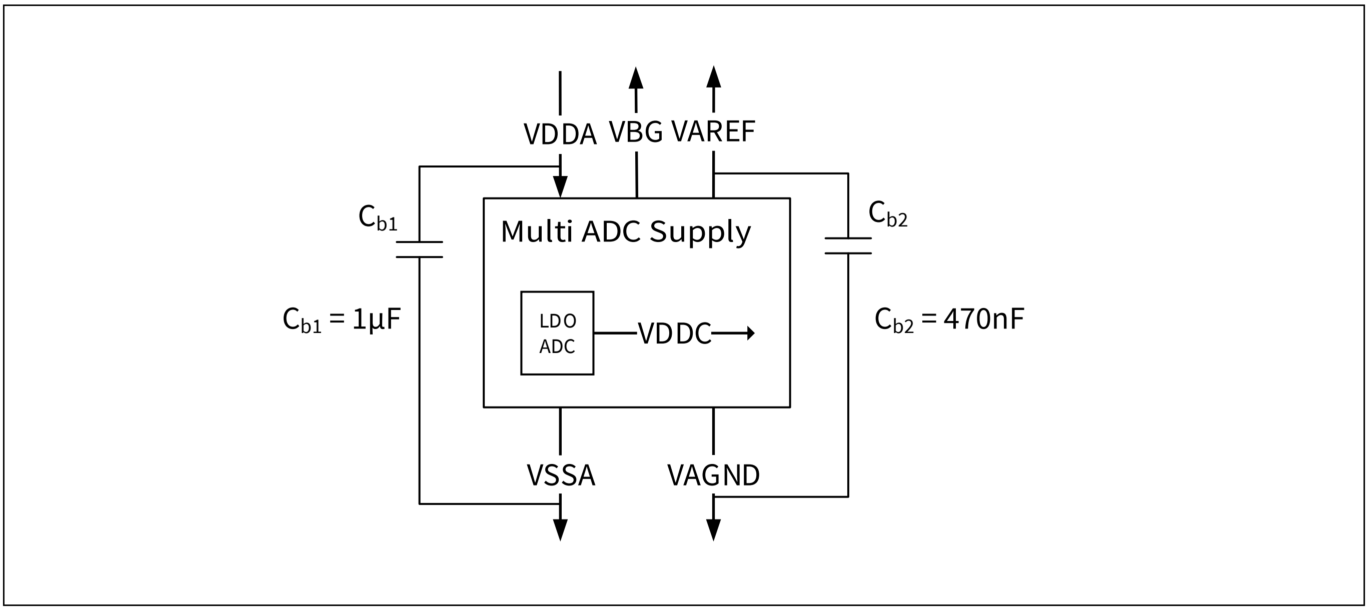


Figure 76 MADC input pin requirements

Both ground connection pins VSSA and VAGND share the same analog ground connection on PCB. The bypass capacitors should be mounted as close as possible to that pins.

Table 63 MADC Voltage Reference, VDDA= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		
Positive reference voltage with respect to VAGND, generated internally	VREFP	V	1.14	1.2	1.26	8.1.1	
Negative analog reference voltage	VAGND	V	0		0.1	8.1.2	Refers to board design ground plane

8.2 MADC Specifications

Table 64 below specifies the ADC parameters. The numbers include one over-conversion. All parameters are only valid with executed startup calibration. No parameter is targeted for production test.

Note:

$f_{ADC\_CLK} = f_{SYS\_CLK}$

REMARK:

If the ADC starts sampling before the bandgap is powered up (BG_EN in Table 32), the results will show some gain errors. To avoid this, follow the bandgap power up timing presented in section 8.4.

Table 64 MADC Specifications, VDDA= 1.71 to 1.89 V, Tb= -40 to +105°C [1)]

Spec	Symbol	Unit	Value			Number	Condition
Parameter			Min	Typ	Max		

Table 64 MADC Specifications, VDDA= 1.71 to 1.89 V, Tb= -40 to +105°C [1)]

Spec	Symbol	Unit	Value			Number	Condition
Resolution				12		8.2.1	With default settings and tracking conversion Table 67
Signal to noise ratio	SNR	dBFS	55	64		8.2.2	@ -6dB FS
Spurious free dynamic range	SFDR	dBFS	58	69		8.2.3	@ -6dB FS @ 600kHz
Inter modulation product	IM3	dBFS	62	69		8.2.4	@ -12dB FS each input tone @ 600kHz max f @ 50KHz Δf
Bandwidth input buffer	BW	kHz	600			8.2.5	1st order Filter in input Buffer
Conversion time – excluding sample time	Nconv	Counts of clk		24		8.2.6	including one tracking conversion, sampling time not included
Sampling time	T_s	Counts of clk	8			8.2.7	@ 80 MHz clk
Wake up time – bandgap and BG reference Buffer	T_{WUBGB}	us	300	600	1000	8.2.8	
Wake up time – ADC	T_{WUADC}	Counts of clk		660		8.2.9	without startup calibration
Startup calibration time[2,3)]	T_{SUCAL}	Counts of clk	3361	6049	16801	8.2.10	ADC0: DSCAL= 0_B Typical conditions: ADC0: STC=1_b ADC0: MSB_CTRL= 1_b
Setup time common mode input voltage	T_{VCM}	µs			1	8.2.11	
Power supply Rejection Ration on VDDS	PSRR	dB	20			8.2.12	

1) *Parameters guaranteed by design*
2) *T_{SUCAL}= (1792 * 2^ (ADC0:STC) + 896*ADC0:MSB_CTRL + 1569) * 1/f_{SYS_CLK}*
3) *Overall wake up time when calibration time is enabled = $T_{WUADC} + T_{SUCAL}$*

8.3 MADC Timing Diagrams

The interface is fully synchronized to the main clock. Figure 77 shows the 12 bits conversion timing in case of one tracking and no oversampling. Thus, the maximum speed of the ADC is set to 2.5 MSps at 80 MHz clock input. Figure 77 shows the SAR ADC timing.

Important: all configuration signals must be stable during a running conversion (between start_adc and one cycle before eoc).

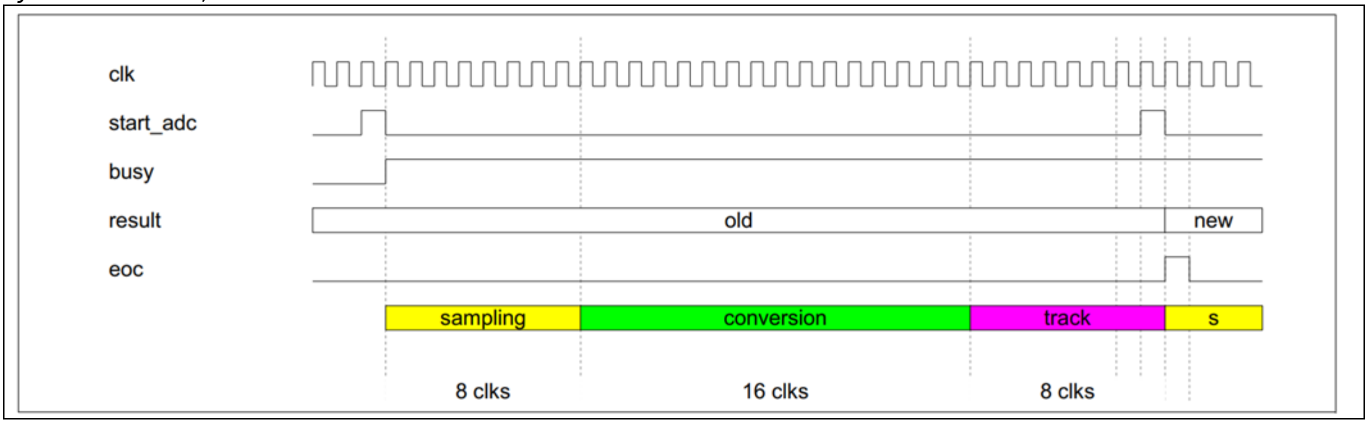


Figure 77 SAR ADC conversion timing diagram, 12 bit

8.4 MADC Startup Sequence

The following figure shows the startup sequence for the complete ADC.

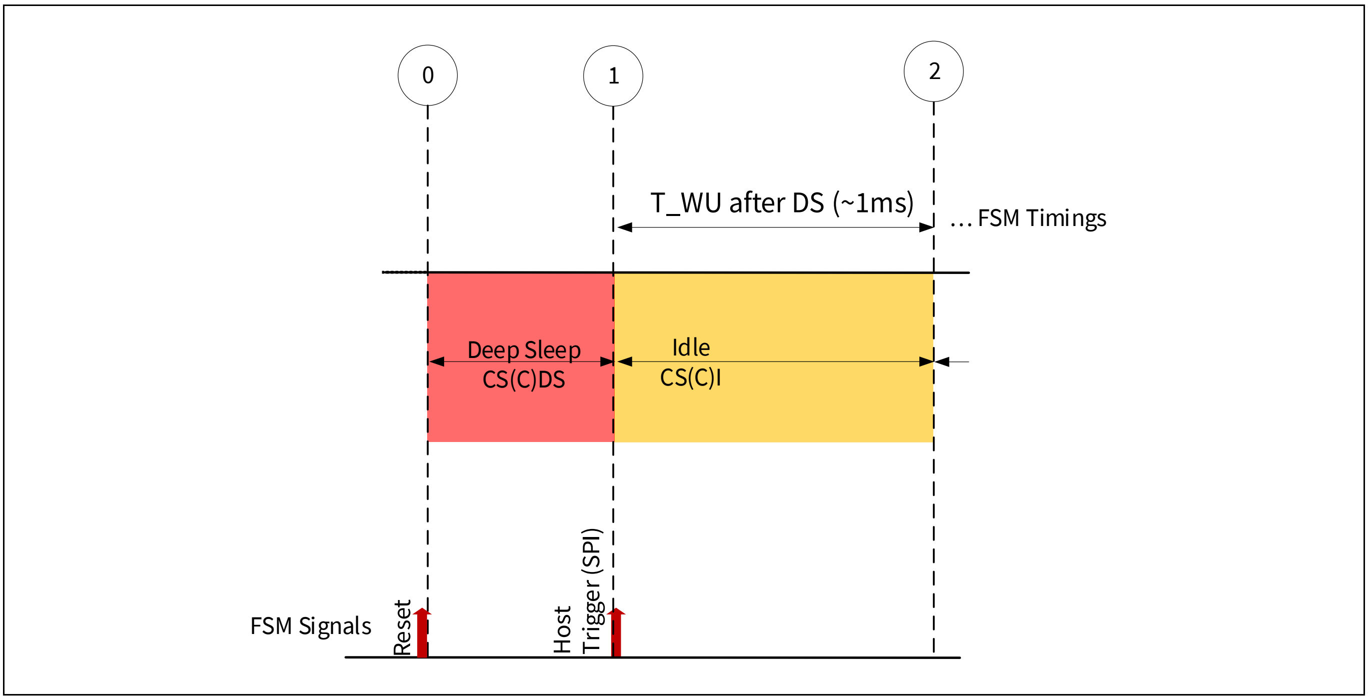


Figure 78 MADC start-up timing constraints

After a reset and trigger from the host, the FSM will move from the deep sleep mode into the idle mode. Here T_{WKUP} represents the overall time required by the bandgap to settle and it is the longest time required in the settling of the ADC.

The following Table 65 shows the start-up timing constraints:

Table 65 MADC Timing Constraints, VDDA= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	**Symbol**	**Unit**	**Value**			**Number**	**Condition**
Parameter			Min	Typ	Max		
Wake up time	T_{WUADC}	µs		8.25		8.4.1	@80 MHz
Setup time common mode input voltage	T_{VCM}	µs			1	8.4.2	
Wake-up time for bandgap and bandgap reference buffer	T_WU	µs	300		1000	8.4.3	

8.5 MADC Conversion Rate

The ADC clock input is f_{ADC_CLK}= f_{SYS_CLK}= 80 MHz and is derived from the system clock.

A conversion can include three different phases:

- Sampling
- Conversion
- Tracking

8.5.1 Sampling

During the first phase, the analog input voltage is sampled onto the input capacitor. The duration is controlled using the ADC0_STC bits. The following Table 66 shows the link between the register value ADC0_STC the clock periods STC_NUM and the sampling time.

Table 66 ADC0:STC Value Table (see section 4.3)

	Sampling clock periods	Sampling time in ns (f_{ADC_CLK}= 80 MHz)
ADC0:STC	**STC_NUM**	t_{sample}
0_D	4	50
1_D (default)	8	100
2_D	16	200
3_D	32	400

The sampling time is calculated as: N_{sample} = STC_NUM

8.5.2 Conversion

The charge from the sampling capacitor is redistributed to 13 + 2 capacitors. To identify the LSB bits of the result, 13 clock cycles are needed.

To identify the MSB bit of the result, one or two clock cycles are used, depending on register setting ADC0_MSB_CTRL:

- In case of MSB_CTRL is set to 0_B, just a single (1) clock cycle is used
- In case of MSB_CTRL is set to 1_B, two (2) clock cycles are used

The redistribution time is calculated as:

$$N_{conv}= (13 + 2 + \text{ADC0: MSB\_CTL})$$

8.5.3 Tracking

In this mode, the ADC performs a single sample conversion followed by several tracking conversions, depending on the setting of bits ADC0: TRACK_CFG:

Table 67 ADC0: TRACK_CFG Value Table

ADC0: TRACK_CFG	Additional conversions **TRACK_CFG_NUM**	Remarks
0_D	0	
1_D	1	Default
2_D	3	
3_D	7	

The duration of one tracking conversion is:

$$N_{track} = 8$$

The duration of all tracking conversions for a single result is then:

$$N_{track\_all} = 8 \text{ x } TRACK\_CFG\_NUM$$

8.5.4 ADC Conversion Rate

Based on what is defined in 8.5.1, 8.5.2 and 8.5.3 the following cycles are defined for a single conversion:

$$N_{ADC\_CONV} = N_{samp} + N_{conv} + N_{track\_all}$$

with N_{samp} the number of sampling, N_{conv} conversion and N_{track} tracking cycles, respectively.

All ADCs are synchronized to f_{SYS_CLK}.

8.5.5 ADC Sampling Rate

The ADC sampling rate is controlled by the ADC0: ADC_DIV value (see Table 22). The sampling rate of the ADC is given then by $f_{ADC\_SAMP} = f_{ADC\_CLK} / ADC\_DIV$. ADC0: ADC_DIV value needs to be greater than the number of clock cycles needed by a single ADC conversion as described in 8.5.4.

The sampling rate of the ADC is:

$$f_{ADC\_SAMP} = f_{ADC\_CLK} / ADC\_DIV$$

$$\text{with } ADC\_DIV > N_{ADC\_CONV}$$

Table 68 ADC Sampling Rate, VDDA= 1.71 to 1.89 V, Tb= -40 to +105°C

Spec	**Symbol**	**Unit**	**Value**			**Number**	**Condition**
Parameter			Min	Typ	Max		
ADC sampling rate	f_{ADC_SAMP}	MHz		2	4	8.5.1	
Effective number of bits resolution	ENOB	1		10.5		8.5.2	

9 SADC Domain Functional Specification

The Sensor ADC (SADC) is a single channel single-ended 8 bits SAR ADC.

The sensor ADC can be used to monitor the temperature output as well as the power detector outputs from the transmitter channels. Conversion data can be read out through the SADC register (see also section 4.24). The data can be added also to the header of MADC data frame in the FIFO (see also section 5.1). By default the SADC is set to read out the temperature sensor out (SADC_CTRL: SADC_CHSEL=0 in section 4.9). For additional settings please check section 4.9. See also Figure 79. The SADC can achieve a better resolution of 10 bits by means of oversampling (see section 9.2).

Due to the required conversion time, ADC data are not available during a shape but they would be available during next shape (there is a delay of one shape for these data).

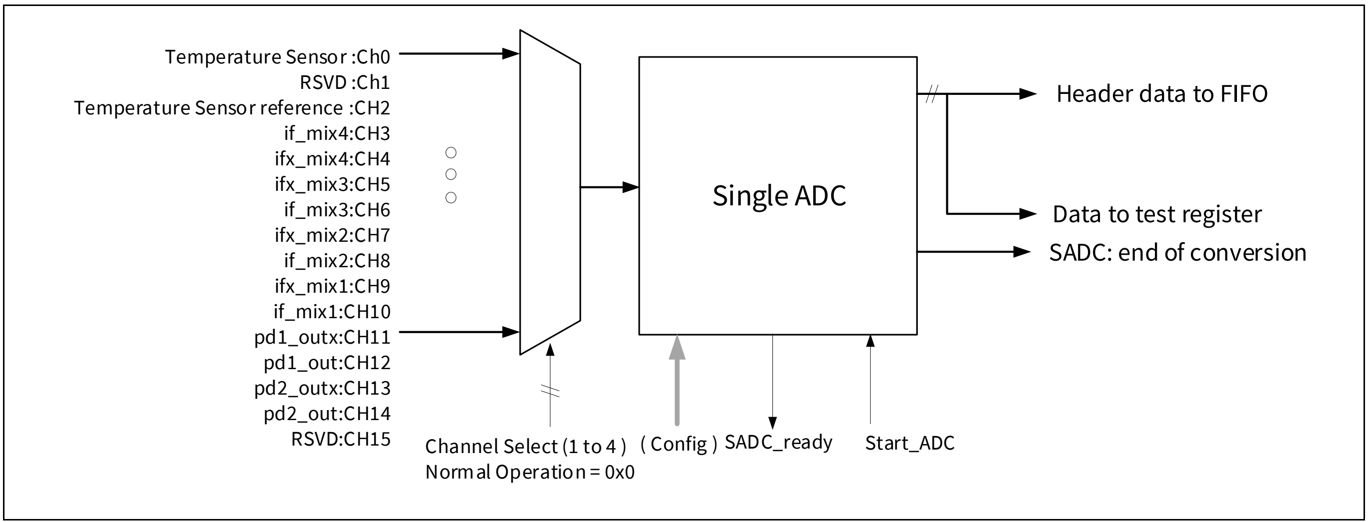


Figure 79 SADC Integration

9.1 SADC Functionality

Four main tasks are performed by the FSM to control the SADC:

- Enabling:
  - The SADC module is enabled through the CSCx register in any phase of the FSM state (see also 4.10)
- Initialization:
  - The host selects the channel in the channel register from SADC_CTRL control register (see also section 4.9)
- Triggering:
  - Each chirp-start during the active phase of shapes will trigger the SADC sampling/conversion
  - or by sending a SADC_START to SADC_CTRL register (see section 4.9)
- Results:
  - The conversion results are stored in the result register SADC_RESULTS register (see section 4.24) after the sampling and conversion is completed

9.2 SADC Conversion Formula

The SADC clock signal is running at 20 MHz and is derived from f_{ADC_CLK}= f_{SYS_CLK}= 80 MHz. The SADC startup time is 101 clock cycles without startup-calibration and 422 clock cycles with startup-calibration. If temperature or power supply conditions did not change dramatically, the startup-calibration can be avoided during frames.

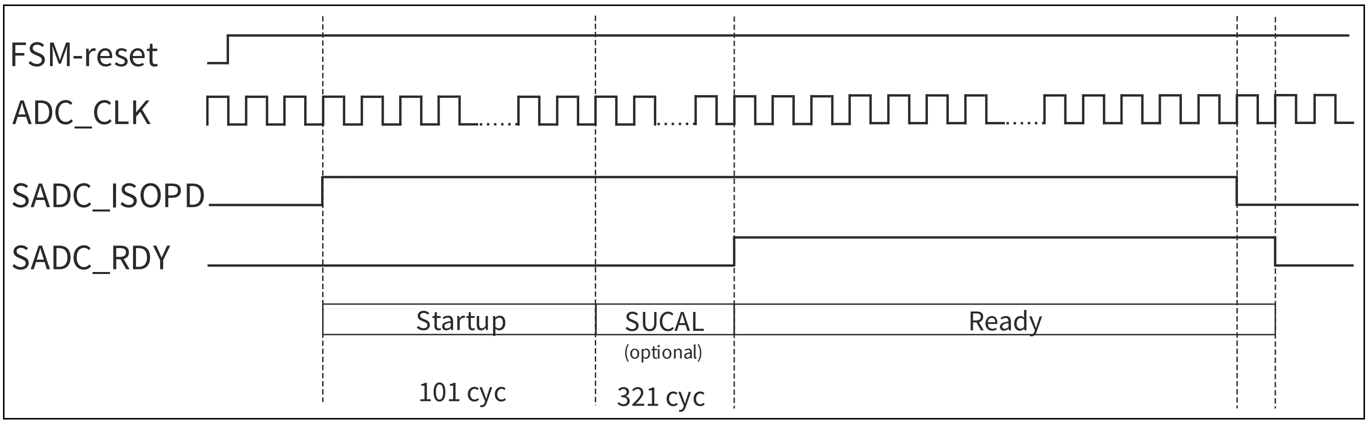


Figure 80 SADC startup timing

The conversion time N_{CONV_LEN} for a single analog to digital conversion into the result register SADC_RESULT (see section 4.24) is defined by the following relation:

$$N_{CONV\_LEN} = (N_{conv} + N_{sample\_dflt} + SESP \times N_{spread\_early\_samply}) \times OVS$$

Where:

N_{conv}= 13 clock cycles

N_{sample_dflt}= 16 clock cycles

$N_{spread\_early\_samply}$= 16 clock cycles

OVS … see SADC_CTRL: OVERS_CFG (see section 4.9)

SESP … see SADC_CTRL: SESP (see section 4.9).

The SADC conversion formula for 8 bits resolution is:

$$Dout_{8b} = ((2\text{^}8 \times V_{Ain}) / VREFP) \times G_{Ain} \text{ with an error of } \pm 0.1\%$$

Where:

V_{Ain} is the analog input to the SADC

G_{Ain} is the gain of the ADC module and can be set either to 1 or 0.75 (see section 4.9)

VREFP= 1.21V.

In order to achieve 10 bits resolution, the oversampling should be set to 32 (see section 4.9).

In order to measure correctly the power sensor output, see sections 7.1.2 and 4.9.

Note: Disabling the SADC
*To disable the SADC simply set in register CSCx (see section 0) SADC_ISOPD= '0_B' (**f_{SYS_CLK}** has to be still provided for at least one additional cycle for the command to take effect).*

10 Enhanced Functions

10.1 Chip ID Readout

Readout sequence:

1. Enable the EFUSE block by setting DFT0: EFUSE_EN = 1 with a single dedicated SPI write, while keeping all other fields in DFT0 with default values.
2. Initiate the sense operation by setting DFT0: EFUSE_SENSE = 1 and keeping DFT0: EFUSE_EN enabled
3. Wait for 2us or poll the register field DFT1: EFUSE_READY = 1.
4. Read out the device ID from CHIP ID #1 and CHIP ID #2.
5. Disable the EFUSE block DFT0: EFUSE_EN = 0.

10.2 Data Test Mode

A linear feedback shift register (LFSR) is built-in on chip. It will generate a pseudo random bit M-sequence that can be used to fill up the FIFO. This can be used to develop and test the complete pipeline from the FIFO on the BGT60ATR24C up to the Application Processor (AP) memory, including firmware and drivers, with a defined bit sequence.

The implemented LFSR is described by the following polynomial: $x^{12}+x^{11}+x^{10}+x^{4}+1$.

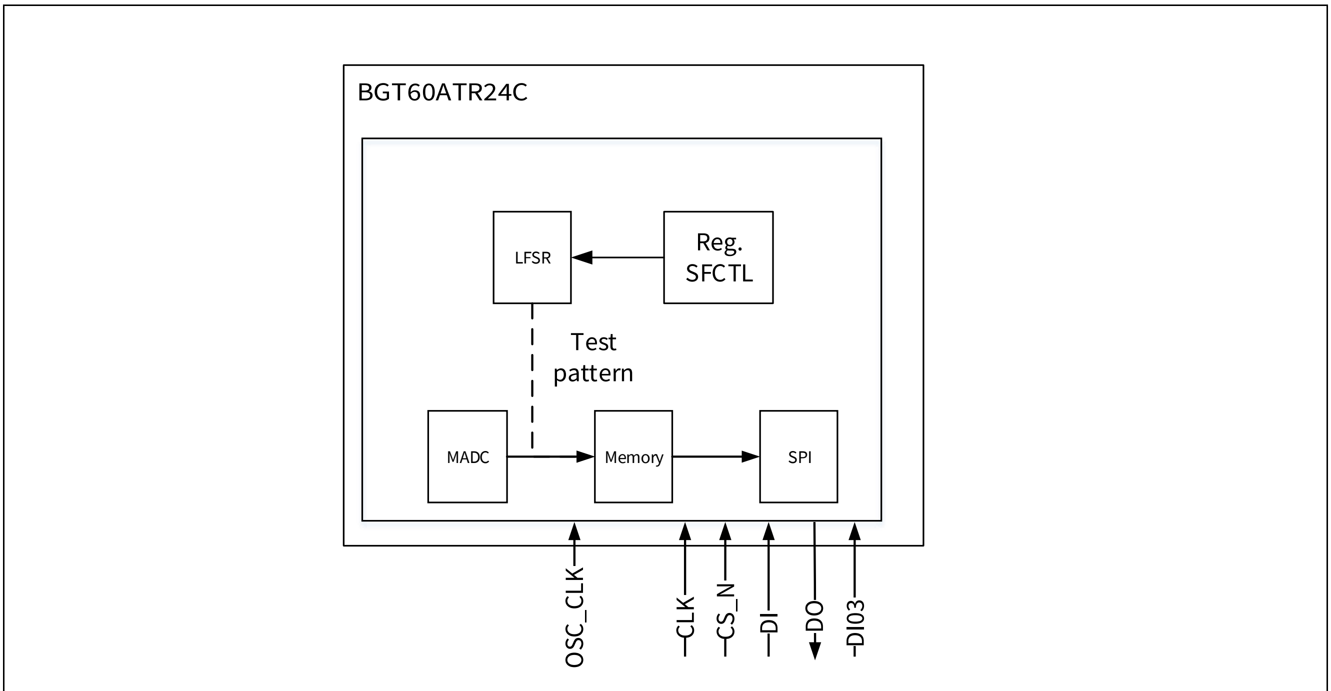


Figure 81 Digital pipeline simplified block diagram

The first ADC channel ADC_CH1 output data stream is bypassed by the data sequence coming from the LSFR generator.

The other channels can be disabled or used in normal operation.

- This test mode can be started with bit SFCTL: LFSR_EN= 1_B (see also 4.8):
- Activate test data instead of ADC data

- Initialization with MAIN: FSM_RESET= 1_B

10.3 CW Mode

In the continuous wave (CW) mode the device will be set to provide a constant output frequency. During CW mode no shapes are executed.

During the execution of this mode:

- Freq/timing parameters defined in shape registers are ignored
- PLL / RF / ADC runs with values programmed in PLL DFT0 (4.18) and CSU1 (4.10).
- All other CSx / shape settings are not handed over to functional blocks
- The values for REPS/REPC/REPT and frame relevant timings are used to shape a “virtual frame”
- Data from the FIFO can be read out following the structure of that “virtual frame”

Note:

For test purposes the “virtual frame” definition should be kept simple: 1 shape, 1 CS, e.g.

10.3.1 Enabling the CW mode

The CW mode should be preceded by either an HW or SW reset.

After this in order to enable the CW mode, the steps below should be followed:

- Enable the MAIN: CW_MODE= 1_B (see 4.2)
- Initialize the chip registers according to defined “virtual frame” (settings in 4.10 and 4.16)
- Enable the clock: PACR1: OSCCLKEN (see 4.6)
- Set frequency via PLLx: FSU setting from shape 1
- Set channel set for CSD/CSI/CSU1 (see4.11)
- set PLL DFT0: BYPRMPEN= 1_B (see 4.18)

By using the FRAME_START as trigger, the chip can be set in the different states of a shape as shown in Figure 82:

- TRIG#1: jump to 1 (DS -> IDLE)
- TRIG#2: jump to 2 (IDLE -> INIT0)
- TRIG#3: jump to 3 (INIT0 -> INIT1)
- TRIG#4: jump to 4
- TRIG#5: jump to 6
- TRIG#6: jump to 7
- Frequency update: at this stage the output frequency can be updated/programed (FSU) to any value and the current frequency will be updated immediately after PLL transition of DFT0: BYPRMPEN= 0_B -> 1_B.
- TRIG7: jump to 8
- At this stage the APU number of samples is generated by the ADC according to the ADC0 settings. In case if APU=0 no triggers are generated, manual triggering of MADC can be done via ADC0: TRIG_MADC. Once the APU number of samples is generated another automatic generation of samples can be done after FSM reset.
- TRIG8: jump to 10
- TRIG9: jump to 11
- TRIGx

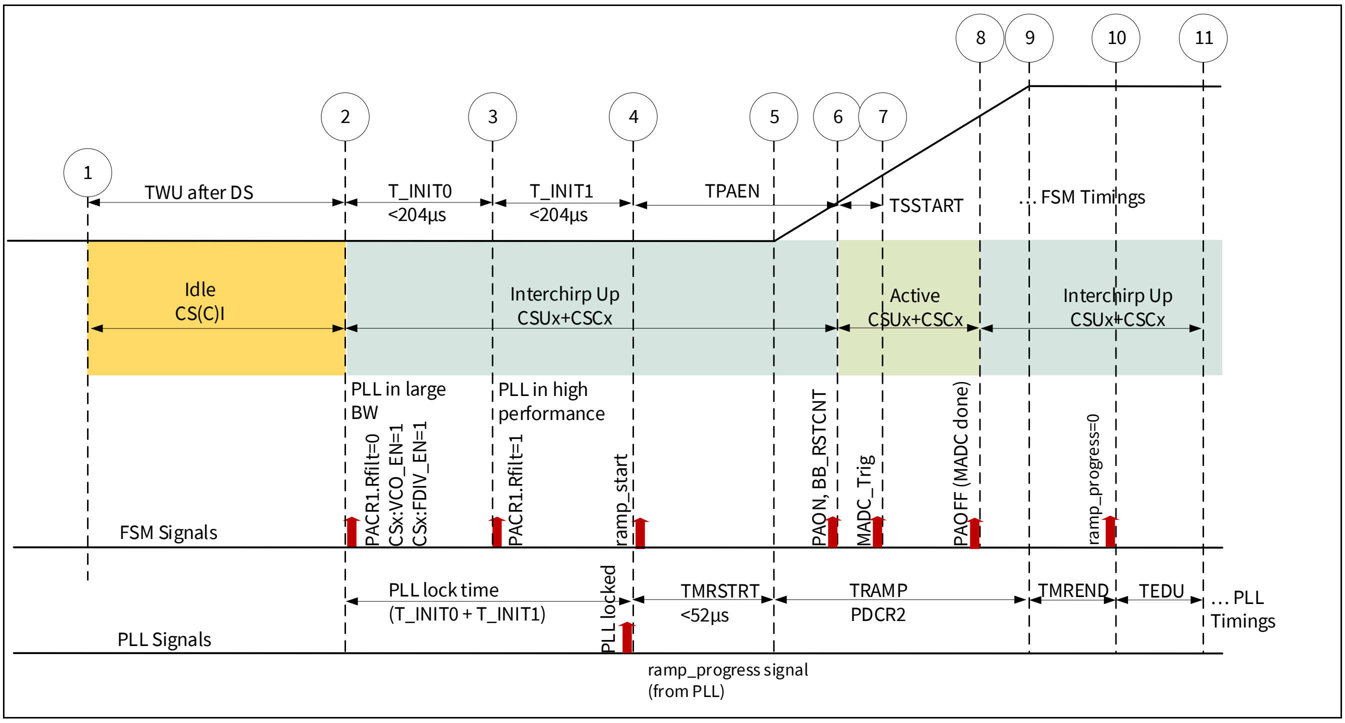


Figure 82 Steps that can be followed during a "virtual frame"

The FSM-reset will set back the FSM to initial state to start again with TRIG1.

This specific mode is intended also to test the power consumption of the chip during a specific sequence. It will offer the opportunity to break the expected shape that should be run during the radar (active) mode in static steps where the current consumption can be measured.

10.3.2 Baseband and ADC Test Mode

A test-tone generator can be used together with the CW mode. A test signal source derived from the OSC_CLK input at 80 MHz can be activated in the analog receiver chain; the same in each Rx chain. This test signal can be programmed in the register RFT0 (see section 4.19). The test tone can propagate through to each baseband chain by enabling a dedicated path. The MADC is triggered by the TRIG7 in Figure 82 and will sample the number of samples specified in the APU1 (see section 4.16). To run a new measurement an FSM-Reset is required.

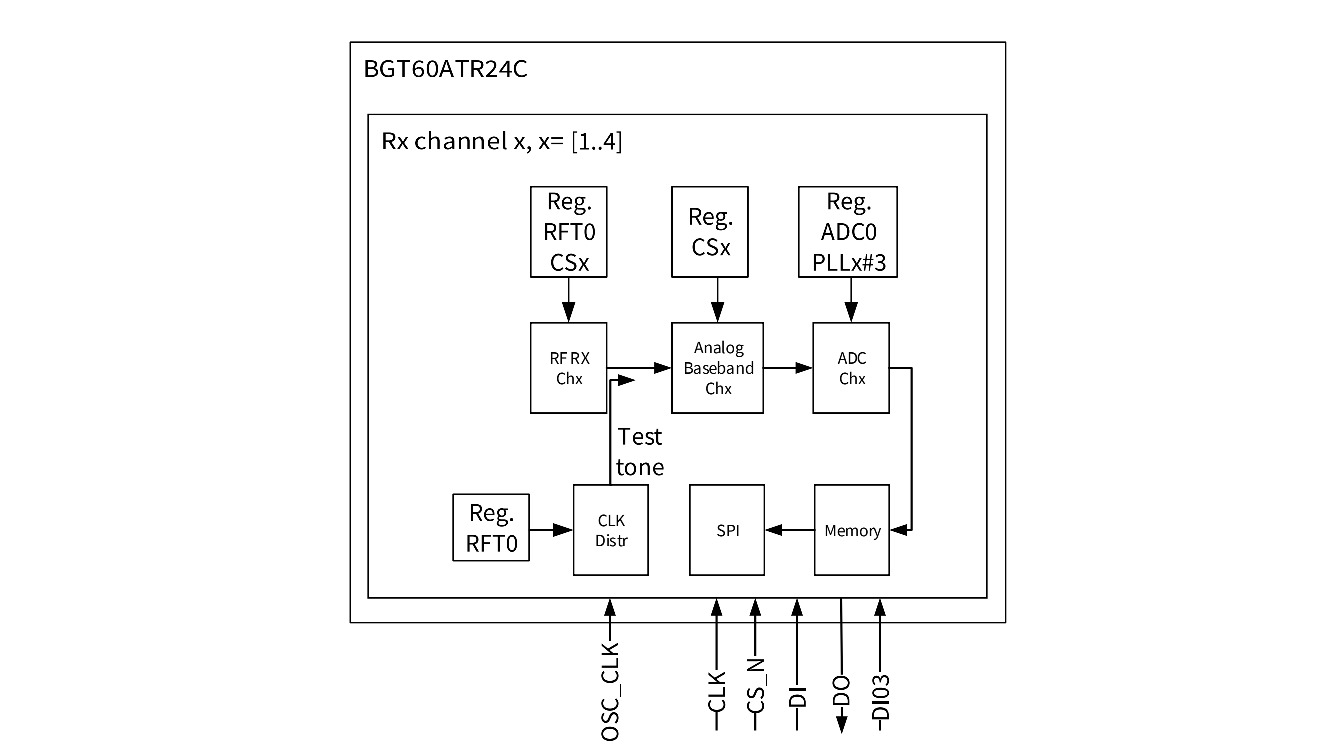


Figure 83 Baseband/ADC test block diagram

This feature represents a very convenient way to test and debug a complete system. The customer can program a dedicated frequency, set the baseband gain and cutoff filter of the HPF (0), set the ADC (see 4.3), and readout via SPI the sampled data into the application processor or microcontroller unit to verify if the complete baseband chain is working as expected.

In Figure 84 is reported one example of ADC readout when the baseband is fed with a test tone at 400kHz internally derived from the OSC_CLK input. Different readouts from different VGA settings are reported.

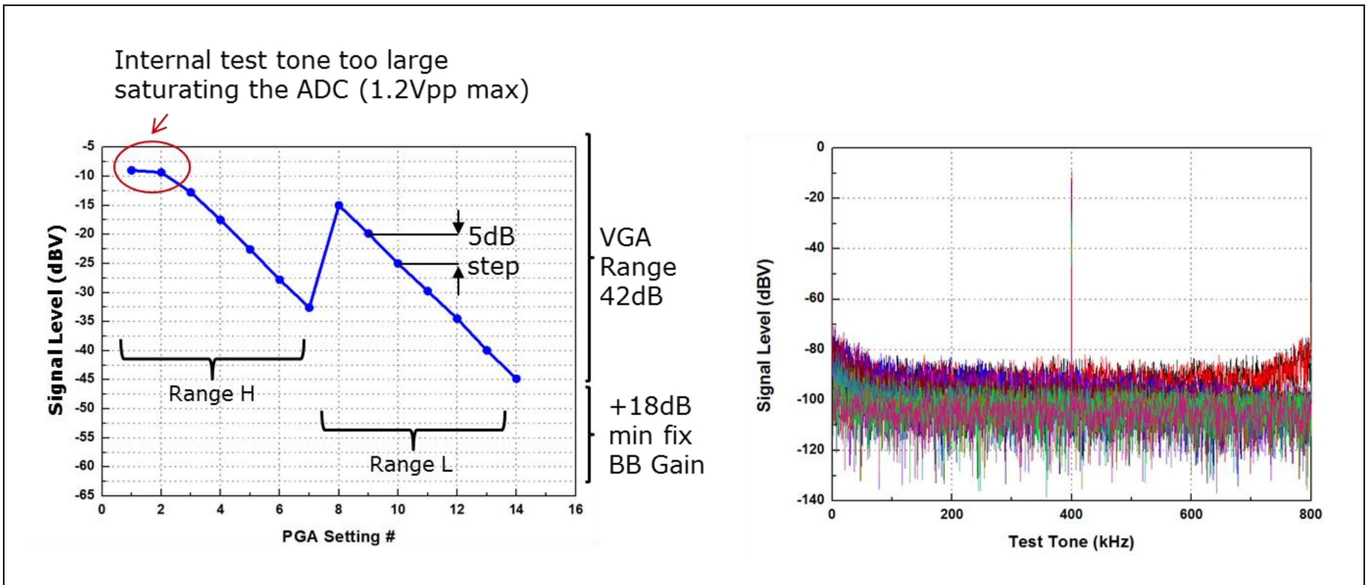


Figure 84 Example: ADC readout after FFT

10.4 IRQ Output

BGT60ATR24C provides one interrupt pin output (IRQ). In default mode, the IRQ signal is used to monitor the filling level of the FIFO as described below.

IRQ status definition:

- IRQ is high after:
  - CS_N goes high and FSTAT: FILL_STATUS >= SFCTL: FIFO_CREF (see also 4.8 and 4.25).
- IRQ is low (as a consequence of):
  - CS_N goes high and FSTAT: FILL_STATUS < SFCTL: FIFO_CREF (see also 4.8 and 4.25).
  - or CS_N is active low

The following figure shows the IRQ signal in case of FIFO-burst reads.

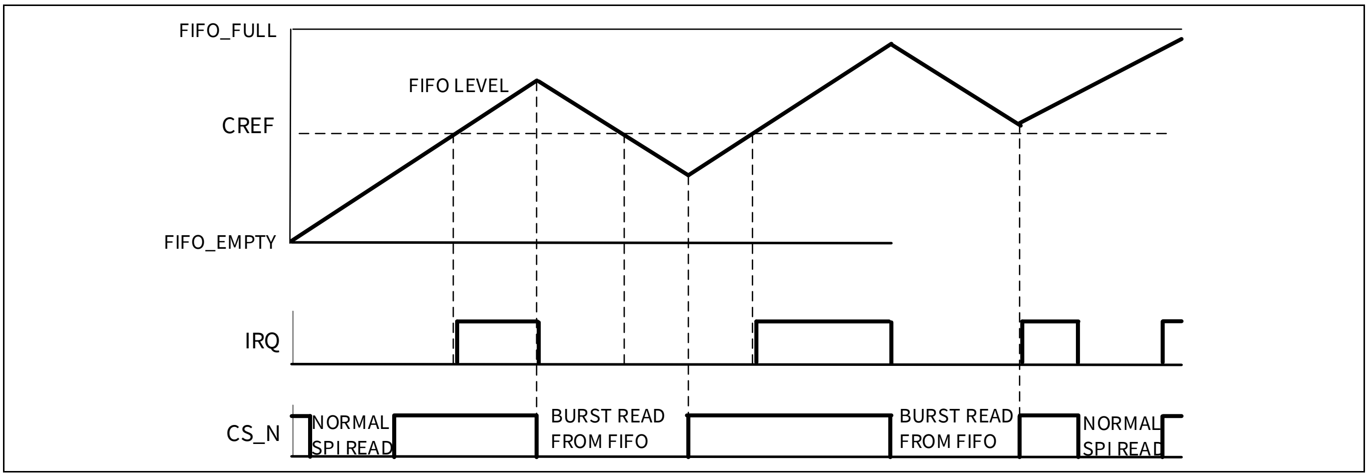
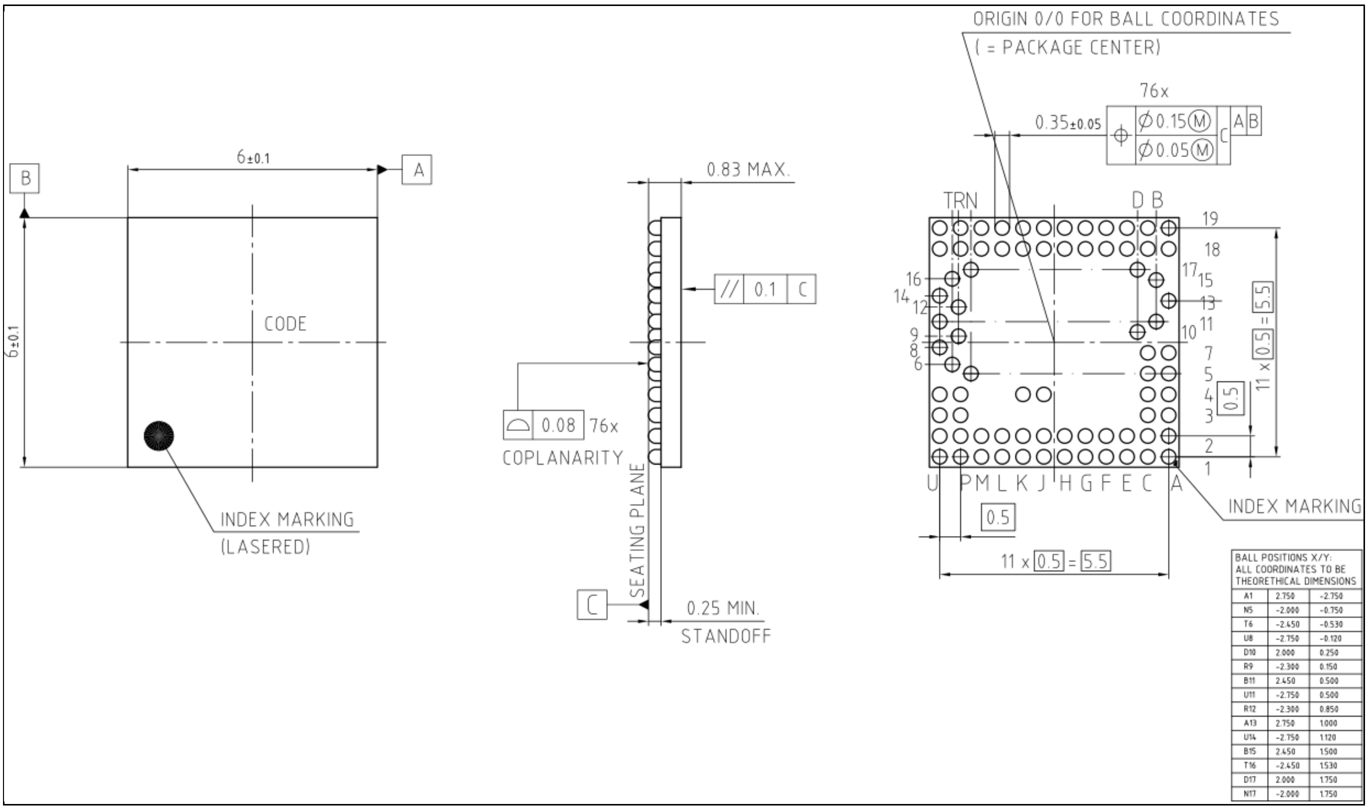


Figure 85 IRQ status behavior during radar mode with FSM capturing data

11 Package

The BGT60ATR24C chipset is housed in the PG-VFWLB-76-1 eWLP package with bump balls of 350µm diameter and a minimum standoff of 250 µm. According to IPC/JEDEC's J-STD, the moisture sensitivity level, MSL, is 3. The package size is (6.0 x 6.0 x 0.83) mm^3 with a general ball pitch of 500 µm except for the RF balls which are off-grid to support an RF package-to-PCB transition.



A1	2.750	-2.750
N5	-2.000	-0.750
T6	-2.450	-0.530
U8	-2.750	-0.120
D10	2.000	0.250
R9	-2.300	0.150
B11	2.450	0.500
U11	-2.750	0.500
R12	-2.300	0.850
A13	2.750	1.000
U14	-2.750	1.120
B15	2.450	1.500
T16	-2.450	1.530
D17	2.000	1.750
N17	-2.000	1.750

Figure 86 **Package Drawing**

Note: *Additional info about RF transition proposals, PCB layer stack-up definition, ground definition underneath the chip, and thermal behavior definition will be provided in an AN once evaluation board is completed.*

12 Abbreviations

Table 69 Abbreviations

Symbol	Description
AAF	Anti-aliasing filter
ADC	Analog to digital converter
AP	Application Processor
DAC	Digital to analog converter
ES	Engineering samples
EES	Early engineering samples
ESD	Electrostatic discharge
FMCW	Frequency modulated continuous wave
HBM	Human body model (related to ESD)
CDM	Charge device model (related to ESD)
HPF	High pass filter
IC	Integrated circuit
LPF	Low pass filter
MCU	Microcontroller Unit
PLL	Phase locked loop integrated circuit
RF	Radio Frequency
RSVD	Reserved
RX	Receiver
SPI	Serial peripheral interface
TX	Transmitter
LDO	Low dropout voltage regulator
RST	Reset or Default setting
MSB	Most significant bit
LSB	Least significant bit
VGA	Variable gain amplifier

13 Revision History

Major changes since the last revision.

Revision History: 2022-02-02, Revision 1.5	
Previous Revision: 2022-02-24, Revision 1.4	
Page	**Description of change**
77	Update of Table 52 and Table 53

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-03-02

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference