Final Datasheet of BGT24ATR22

BGT24ATR22
24 GHz radar sensor

Features

- 24 GHz radar transceiver MMIC
- 2 TX channels
- 2 RX channels
- Fully integrated low-phase-noise VCO
- Low noise figure NF_{SSB}: 13 dB @1 kHz
- Automatic frequency control
- Integrated analog base band amplifiers
- Automatic DC-offset compensation
- Integrated state machine with ultra-low power modes
- 12-bit ADC for dynamic range and detection performance
- Digital Radar Data Processing (DRDP) unit with integrated FFT
- Single-ended RF terminals
- Wide ambient temperature range: -40°C to +105°C
- VQFN-32 RoHS compliant, leadless package
- AEC-Q100 product validation

Potential applications

- Automotive Short Range Radar
- Smart trunk opener
- Hands-free trunk opener
- Motion detection
- Kick sensing

Product validation

Qualified for automotive applications with extended lifetime requirements.
Product validation according to AEC-Q100.

Description

BGT24ATR22 is a Silicon Germanium Monolithic Microwave Integrated Circuit for 24 GHz radar applications. It provides building blocks for analog signal generation and reception, operating in the frequency range from 24.0 GHz up to 24.25 GHz with 2 transmit channels and 2 receive channels. The analog base band and the ADC are integrated. The whole radar sensor is controlled by a finite state machine which is optimized for independent radar operation with ultra-low power consumption.

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1 Block diagram

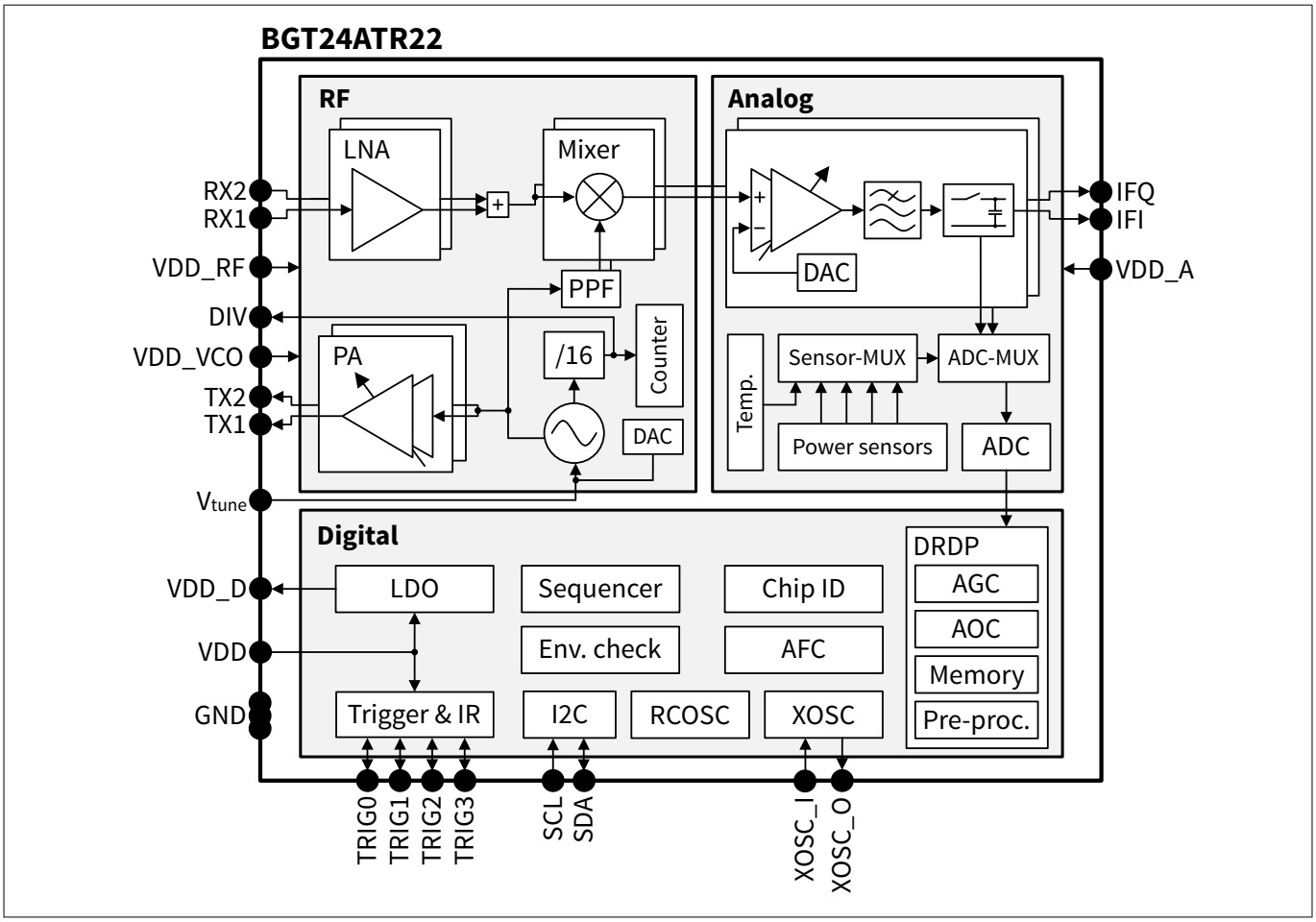

Figure 1 Block diagram of BGT24ATR22

1.1 General information

The BGT24ATR22 is a fully integrated radar transceiver operating from 24.0 GHz to 24.25 GHz. It is designed for ultra-low power Doppler radar applications and features 2 transmit channels, 2 receive channels, a fundamental *voltage controlled oscillator (VCO)*, an integrated *analog base band (ABB)* with offset compensation for *intermediate frequency (IF)* signal conditioning, *analog-to-digital converter (ADC)*, and a digital *finite state machine (FSM)* for power efficient control of the individual submodules. Furthermore, the radar transceiver has integrated radar data preprocessing.

The BGT24ATR22 has been designed using Infineon's automotive qualified 130 nm SiGe-BiCMOS *radio frequency (RF)* technology, and is housed in a compact leadless VQFN32 package package which can be processed in standard *surface mount technology (SMT)* flow.

Figure 1 shows the block diagram of the BGT24ATR22. A detailed functional description can be found in its User Manual. In the following, an overview of the submodules and their interactions is given.

1.2 RF section

The BGT24ATR22 has an integrated VCO as well as an integrated *digital-to-analog converter (DAC)* to control the VCO's tuning voltage. Via an external pin, a capacitor must be added to improve the noise performance of the VCO. For monitoring purposes, the *monolithic microwave integrated circuit (MMIC)* contains a frequency divider

output. This internal frequency divider is used by the digital *hardware (HW)* to implement an *automatic frequency control (AFC)* loop, which adjusts the tuning voltage to the desired operating frequency.

The BGT24ATR22 contains 2 transmit channels whose output power can be adjusted independently with a 6-bit tuning word within a range of more than 20 dB. The operation of the 2 transmit channels is intended to be interleaved so that only a single transmit channel is active at any time.

The MMIC features 2 receive channels. Each channel has its own *low noise amplifier (LNA)*. Their outputs are combined and therefore, the intended operating principle of the receiver is interleaving the receiver channels, similar to the transmit channels. The *polyphase filter (PPF)* generates a quadrature signal of the internal VCO signal that is used in the quadrature mixer to down-convert the combined receive signal.

1.3 Analog section

The BGT24ATR22 has two fully integrated ABB channels: one for the I-channel (in-phase channel) and one for the Q-channel (quadrature channel). Each ABB channel consists of:

- a compensation DAC, which cancels the mixer output's *direct current (DC)* offset voltage
- a *variable gain amplifier (VGA)* with an adjustable gain between 3 and 384
- an *anti-aliasing filter (AAF)* with 4 different cut-off frequencies, and
- a sample and hold circuitry.

With an analog multiplexer, the user can choose whether to connect the I-channel, the Q-channel or a sensor channel to the single internal ADC. The sensor channel has a second multiplexer which enables the user to choose what sensor data, such as temperature or RF power, to convert.

The ADC is a 12-bit *successive approximation register (SAR)* ADC with a maximum conversion rate of 2 MS/s when operated with a system clock of 40 MHz. The ADC contains a tracking feature as well as an oversampling feature to improve the *signal-to-noise ratio (SNR)* of the conversion.

1.4 Digital section

The BGT24ATR22 contains a *low-dropout voltage regulator (LDO)*, which generates the internal digital supply voltage of 1.5V for the digital section. For correct operation, a buffer capacitor of at least 10 µF must be placed as close as possible to the VDD_D pin of the package. The external digital interface voltage of the digital pins is equal to the supply input voltage of the LDO.

The clock for the digital domain can have the following sources:

- the quartz oscillator with an external quartz connected to XOSC_I and XOSC_O or an external clock at XOSC_I
- the external pin TRIG0, and
- the tunable internal RC oscillator.

  It is recommended to use RC-oscillator as system-clock, and to use quartz oscillator only for AFC, whenever stable clock is needed, since the quartz oscillator has higher power-consumption. The XOSC_I (1.5V level) or TRIG0 (1.8-3.3V level) can be used in case a stable clock is available from an external source and quartz oscillator can be saved. The frequency range of X-oscillator is 20 to 40 MHz. For the RC oscillator, the frequency range is 10 to 20 MHz.

The digital interface of the BGT24ATR22 is an *inter-integrated circuit (I2C)* with a maximum data rate of 400 kbit/s.

1 Block diagram

The digital HW contains the following building blocks:

- a sequencer, which controls the data acquisition of radar frames fully independently
- the AFC, which stabilizes that the RF frequency around a configured frequency
- an environment check, which verifies if the supply voltage or the temperature are within a defined range since the last frequency calibration to avoid out-of-band emissions, and
- digital radar data processing, which stores and pre-processes the radar data and sensor data.

2 Pin description

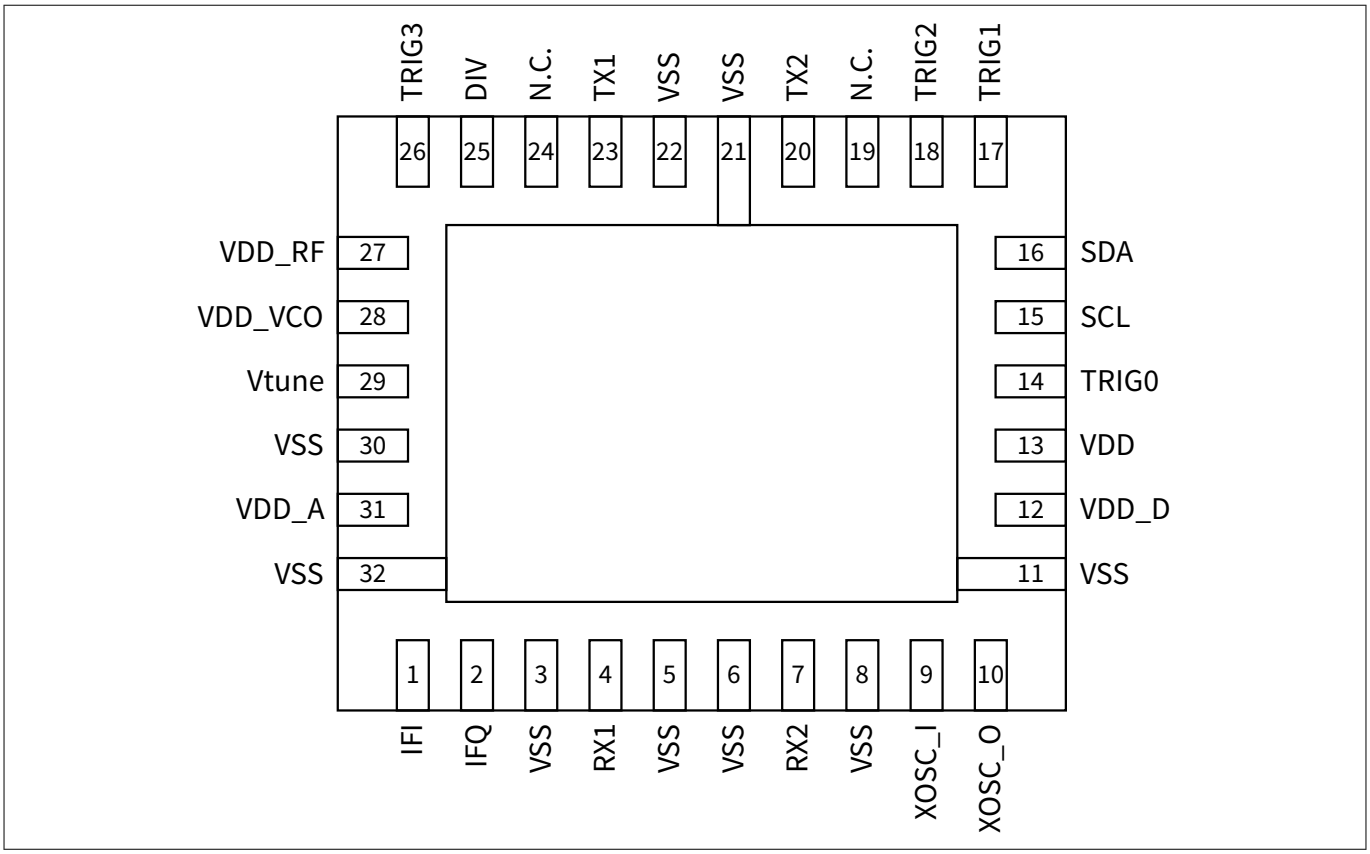

Figure 2 Pin diagram of BGT24ATR22 (top view)

Abbreviations

- AI: analog input
- AIO: analog input output
- AO: analog output
- DI: digital input
- DIO: digital input output
- DO: digital output
- GND: ground
- PWR: power supply
- N.C.: not connected

Table 1 Pin definitions and functions

Pin nr.	Name	Pin type	Function
1	IFI	AO	DFT not recommend to be used by customers
2	IFQ	AO	DFT not recommend to be used by customers
3	VSS	GND	Ground
4	RX1	AI	RX1 RF input signal
5	VSS	N.C.	not connected, to be grounded in application

(table continues...)

2 Pin description

Table 1 (continued) Pin definitions and functions

Pin nr.	Name	Pin type	Function
6	VSS	N.C.	not connected, to be grounded in application
7	RX2	AI	RX2 RF input signal
8	VSS	GND	Ground
9	XOSC_I	DI	External reference clock input - quartz
10	XOSC_O	DO	External reference clock output
11	VSS	GND	Ground
12	VDD_D	AO	Pin for filtering the internally generated 1.5 V
13	VDD	PWR	Supply voltage for LDO and trigger pins
14	TRIG0	DIO	External trigger pin 0
15	SCL	DI	Serial clock (I2C clock) pin
16	SDA	DIO	Serial data (I2C data) pin
17	TRIG1	DIO	External trigger pin 1
18	TRIG2	DIO	External trigger pin 2
19	N.C.	N.C.	not connected, to be left open in application
20	TX2	AO	TX2 RF output signal
21	VSS	GND	Ground
22	VSS	N.C.	not connected, to be grounded in application
23	TX1	AO	TX1 RF output signal
24	N.C.	N.C.	not connected, to be left open in application
25	DIV	AO	Frequency divider output
26	TRIG3	DIO	External trigger pin 3
27	VDD_RF	PWR	Supply voltage for the RF domain
28	VDD_VCO	PWR	Supply voltage for the VCO domain
29	Vtune	PWR	VCO tuning voltage
30	VSS	N.C.	not connected, to be grounded in application
31	VDD_A	PWR	Supply voltage for the analog domain
32	VSS	GND	Ground
33	Exposed pad	GND	Ground

3 General product characteristics

***Attention**: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit*

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_c = -40°C to 105°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Maximum supply voltage digital	VDD_{MR}	-0.3	-	+3.6	V		3.1.1
Maximum supply voltage analog	VDD_A_{MR} VDD_RF_{MR} VDD_VCO_{MR}	-0.3	-	+2.1	V		3.1.2
Digital input voltage	$V_{IN,D}$	-0.3	-	VDD + 0.3	V		3.1.3
Analog input voltages	$V_{IN,A}$	-0.3	-	VDD_A + 0.3	V		3.1.4
	$V_{IN,RF}$			VDD_RF + 0.3			3.1.5
	$V_{IN,VCO}$			VDD_VCO + 0.3			3.1.6
DC voltage at RX RF pins	$V_{DC,RX}$	-0.3	-	+0.3	V		3.1.7
DC voltage at TX RF pins	$V_{DC,TX}$	-0.3	-	VDD_RF + 0.3	V		3.1.8
Tune voltage	V_{TUNE}	-0.3	-	VDD_VCO + 0.3	V		3.1.9
Digital output current	I_{OUT}	-	-	-	mA		
Output current at IFI or IFQ	I_{IF}	-	-	tbd	mA		
RF input power	$P_{RF,MR}$	-	-	0	dBm		3.1.10
Maximum silicon bulk temperature	$T_{Si,MR}$	-40	-	+125	°C		3.1.11
Storage temperature	T_{stg}	-40	-	+150	°C		3.1.12

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Supply voltage LDO and digital interface	*VDD*	1.71	3.3	3.465	V	Supply condition, relevant tests performed within this range	3.2.1
Supply voltage digital	*VDD_D*	1.41	1.5	1.59	V	Chip internally generated.	3.2.2
Supply voltages analog	*VDD_A*	1.71	1.8	1.89	V		3.2.3
	VDD_RF	1.71	1.8	1.89	V		3.2.4
	VDD_VCO	1.71	1.8	1.89	V		3.2.5
Supply current analog in continuous wave mode	$I_{A,CW}$	-	105	140	mA	typical RX1/TX1- or RX2/TX2-pair in CW radar mode	3.2.6
Averaged supply current total in pulsed mode	$I_{T,P}$		150	1850	uA	PRT=160us, t_frame=100ms, SYSCLK=RC_OSC @15MHz, CLK_DIV=16, $P_{out,max}$, RF on time 10us; AFC in tracking mode, 2x heating pulse, 1x sampling pulse (for PC0/PC1)	3.2.7
			1.5	10	mA	PRT=160us, t_frame=1ms, SYSCLK=RC_OSC @15MHz, $P_{out,max}$, RF on time 10us; AFC off, 2x heating pulse, 1x sampling pulse (for PC0/PC1)	3.2.8
Supply noise analog	$V_{N,EFF}$	-	-	25	uVrms	BW = 10 Hz to 100 kHz	3.2.9
Operational temperature range	T_B	-40	-	105	°C	At package exposed pad. Ambient temperature not below -40°C	3.2.10
Operating frequency range	f_{RF}	24.0	-	24.25	GHz		3.2.11

(table continues...)

Table 3 (continued) Functional range

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Thermal resistance of package	$R_{th,P}$	-	2.6	-	K/W		3.2.12

3.3 ESD integrity

Table 4 ESD integrity

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
ESD according to *human body model (HBM)* Q100-002	$V_{ESD,HBM}$	-2000	-	+2000	V	All pins	3.3.1
ESD according to *charge device model (CDM)* Q100-011	$V_{ESD,CDM}$	-500	-	+500	V	All pins	3.3.2
ESD according to CDM Q100-011-corner pins	$V_{ESC,CDMCP}$	-750	-	+750	V	Corner pins	3.3.3

4 Electrical characteristics

4.1 VCO electrical characteristics

Table 5 VCO electrical characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Operating frequency range	Refer to 3.2.11						
Tuning voltage range	V_{tune}	0	-	1.89	V	External tune voltage	4.1.1
		0.35	-	1.45	V	Internal tuning voltage; guaranteed range	4.1.2
Tuning sensitivity	S_{VCO}	950	-	2100	MHz/V	within 24.0 GHz to 24.25 GHz	4.1.3
Temperature drift	$\Delta f/\Delta T$	-12	-5	-	MHz/K	0.3V<V_{tune}<1.5V	4.1.4
VCO tuning DAC resolution	$R_{VCO,DAC}$	-	10	-	bits		4.1.5
Operating current at *VDD_VCO* supply	I_{VCO}	25	33	40	mA		4.1.5
single-sideband (SSB) phase noise	*PN*	-	-88	-80	dBc/Hz	At 100 kHz offset	4.1.6
Harmonic signals	P_{harm}	-	-	-30	dBm	For second harmonic	4.1.7
Nonharmonic signals	P_{spur}	-	-	-45	dBm	carrier offset > ±1 MHz, in CW mode (sequencer off)	4.1.8
VCO pushing	$\Delta f/\Delta VDD\_VCO$	-	180	350	MHz/V	Static abs. integral value measured with internal V_{tune} and interpolated between VDD_VCO, min and -max	4.1.9
VCO static pulling vs. load	Δf_{sp}	-5	-	5	MHz	TX output load max. *voltage standing wave ratio (VSWR)* 2:1	

(table continues...)

Table 5 (continued) VCO electrical characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
VCO pulling by TX channel selection	$\Delta f_{p,TX}$	-5	-	5	MHz	Static measurement	4.1.10
VCO pulling by divider enable/ disable	$\Delta f_{p,DIV}$	-5	-	5	MHz		4.1.12
Tuning port input resistance	R_{Vtune}	100	-	-	kΩ		4.1.13
Tuning port leakage current	I_{Vtune}	-200	-	500	nA		4.1.14
Tuning port input capacitance	C_{Vtune}	-	-	10	pF		4.1.15

With the operation of the internal DAC controlled by the state machine, the user may not need to know all details of the Vtune port. Therefore, the parameters for the Vtune port marked internal (red font). If they are considered useful, just remove the internal tag.

4.2 TX section

Table 6 Transmitter characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Operating current at *VDD_RF* supply	I_{TX}	-	18	23	mA	Single channel active with maximum output power	4.2.1
RF output power	P_{OUT}	-5	0	3	dBm	Max. output power setting of a single TX channel	4.2.1
Output power leakage	$P_{TX,leak}$	-	-	-33	dBm	For TX off	4.2.2
Output power adjustable range	G_{adj}	30	-	-	dB	6-bit control, 45uA TX bias offset current	4.2.3
Output power adjustable step size	$L_{st,out}$	-	-	1.5	dB	For highest 20 dB of RF output power, 45uA TX bias offset current	4.2.4
Channel to channel TX output power variation	ΔP_{TX}	-1.5	-	1.5	dB	At maximum output power	4.2.5

(table continues...)

Table 6 (continued) Transmitter characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Output power variation over temperature	$P_{T,flat}$	-2.5	-	2.5	dB	At maximum output power	4.2.6
TX channel isolation	$ISO_{TX,TX}$	23	30	-	dB	S-parameter measurement	4.2.7
TX to RX isolation	$ISO_{TX,RX}$	30	-	-	dB		
TX load impedance	Z_{TX}	-	50	-	Ω	Single ended, chip impedance changes with output power; at outer edge of compensation structure	4.2.8
TX to IF isolation	$X_{TX,RX,max}$	30	35	-	dB	TX at full output power, resultant vector of quadrature I & Q DC vectors is calculated and mapped to an RX RF-input power value caused by TX leakage	4.2.9
TX VGA DAC resolution	$R_{TX,DAC}$	-	6	-	bits		4.2.10

4.3 Frequency divider and counter section

Table 7 Frequency divider characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
VCO dividing factor	D_{DIV}	-	16	-			4.3.1
Divider analog output power level	P_{DIV}	-10	-	-	dBm		4.3.2
Divider analog output load impedance	Z_{DIV}	-	50	-	Ω		4.3.3
Operating current at *VDD_RF* supply	I_{DIV}	25	33	40	mA		4.3.4

(table continues...)

Table 7 (continued) Frequency divider characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Frequency counter input frequency	$f_{count,max}$	-	-	1.875	GHz		4.3.5
Frequency counter output frequency	f_{DIV}	-	-	58.6	MHz		4.3.6

4.4 RX section

Table 8 Receiver characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Operating frequency range	Refer to 3.2.11						
Voltage conversion gain	G_V	8	14	19	dB	Only for the downconverter	4.4.1
SSB noise figure	NF_{SSB100}	-	20	-	dB	SSB at 100 Hz of the downconverter	4.4.2
SSB noise figure	NF_{SSB1k}	-	14	-	dB	SSB at 1 kHz of the downconverter	4.4.3
SSB noise figure	$NF_{SSB100k}$	-	13	-	dB	SSB at 100 kHz of the downconverter	4.4.4
Input 1 dB compression point	IP_{1dB}	-16	-11.5	-	dBm	Only for the downconverter	4.4.5
Operating current at *VDD_RF* supply	I_{RX}	15	25	35	mA		
RF isolation between RX channels	$IF_{RF,RX}$	23	30	-	dB	S-parameter measurement	4.4.6
Leakage of local oscillator to RF input ports	$L_{LO,RFin}$	-	-	-30	dBm	TX in off mode	4.4.7
Input impedance	Z_{RX}	-	50	-	Ω	Single ended; at outer edge of compensation structure	4.4.8

(table continues...)

Table 8 (continued) Receiver characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Input return loss RF	RL_{RF}	10	15	-	dB	For active and inactive LNA; measured on Infineon GSG reference board	4.4.9
Voltage conversion gain variation	ΔG_{RX}	-2.5	-	2.5	dB	Channel to channel	4.4.10
RX channel phase variation	$\Delta\theta_{SSB100k}$	-5	-	5	deg	Channel to channel and over temperature as well as supply voltage	4.4.11
Quadrature amplitude imbalance	ε_A	-1.5	-	1.5	dB		4.4.12
Quadrature phase imbalance	ε_P	-15	-	15	deg		4.4.13
ABB nominal gain	$G_{V,ABB}$	3	-	384	-	The ABB is DC-coupled to the mixer output. 8 gain configurations	4.4.14
ABB gain step	$\Delta G_{V,ABB}$	1.8	2	2.2	-	Factor between successive settings	4.4.15
Overall SSB noise figure	$NF_{SSB100,ABB}$	tbd	tbd	tbd	dB	Overall SSB NF at 100 Hz of downconverter and ABB, when ABB Gain "tbd"	-
Overall SSB noise figure	$NF_{SSB1k,ABB}$	tbd	tbd	tbd	dB	Overall SSB NF at 1 kHz of downconverter and ABB, when ABB Gain "tbd"	-

(table continues...)

Table 8 (continued) Receiver characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
RMS noise	$N_{RMS,ABB}$	-	3	-	LSB	$P_{out,max}$, ABB gain=48, ABB BW 100 kHz; PRT=500us, t_frame=64ms, nr of samples=64, fVCO=24.2GHz, ADC_CONF 0x5C49, measured at Infineon reference board - all RF ports are termnated;	4.4.16
Mixer offset compensation DAC voltage range	$V_{Off,DAC}$	±180	±200	-	mV		4.4.17
AAF cut-off frequency	f_{AAF}	60	100	140	kHz	RXABB_CONF = 3	4.4.18
		120	200	280	kHz	RXABB_CONF = 2	4.4.19
		600	1000	1400	kHz	RXABB_CONF = 1	4.4.20
		1560	2600	3640	kHz	RXABB_CONF = 0	4.4.21
Mixer output frequency range	$f_{mix,out,max}$	-	1600	-	MHz	-3 dB bandwidth	
Mixer output impedance	$Z_{mix,out}$	-	280	-	Ω		
Mixer offset compensation DAC resolution	$R_{AOC,DAC}$	-	9	-	bits		4.4.22
IF DC offset drift	$D_{DC,OFFSET}$	-	value	tbd	LSB	Not measured yet!!!	

4.5 Analog-to-digital converter

The integrated ADC is a differential SAR ADC. It contains a tracking feature and an oversampling feature to improve its performance. A detailed functional description can be found in the User Manual.

4 Electrical characteristics

Table 9 ADC characteristics

T_c = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Resolution	R_{ADC}	-	12	-	bits	With tracking conversion or oversampling (11 bit physical implementation)	4.5.1
ADC clock frequency	$f_{ADC,CLK}$	10	40	80	MHz	$f_{ADC,CLK} = f_{SYS,CLK}$	4.5.2
Average operating current at digital supply *VDD_D*	$I_{ADC,D}$	-	0.7	-	mA		4.5.
Average operating current at analog supply *VDD_RF*	$I_{ADC,A}$	-	0.6	-	mA		4.5.
Signal-to-noise ratio	*SNR*	55	64	-	dB	At -6 dB FS	4.5.
Spurious free dynamic range	*SFDR*	58	69	-	dB	At -6 dB FS and 600 kHz	4.5.
Inter modulation product	*IM3*	62	69	-	dB	At -12 dB FS, 600 kHz max. frequency, and 50 kHz spacing	4.5.
Single conversion time	N_{conv}	8	25	57	clock cycles		4.5.
Sampling time	T_s	4	8	32	clock cycles		4.5.3
Start-up calibration time	T_{SUCAL}	3361	6049	16801	clock cycles		4.5.4
Wake-up time	T_{WUADC}	-	662	-	clock cycles	Without start-up calibration. If start-up calibration is activated, overall wake-up time is $T_{SUCAL}+T_{WUADC}$	4.5.5
Power supply rejection ratio	*PSRR*	20	-	-	dB		4.5.0

4.6 Quartz oscillator characteristics

Table 10 Quartz oscillator characteristics

T_C = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Quartz oscillator operating frequency	f_{XTAL}	20	-	40	MHz		4.6.1
Quartz oscillator operating current at *VDD_D* supply	I_{XTAL}	-	75	135	µA		4.6.
Quartz oscillator external load capacitance	$C_{XTAL,load}$	-	12	-	pF	according to the requirements of the selected crystal, refer to User Manual	4.6.2
Quartz oscillator settling time	$t_{XTAL,settle}$	-	185	-	µs	typ. value with a 38.4MHz crystal (ESR typical 20Ω)	4.6.3
Quartz oscillator phase noise	PN_{XTAL}	-	-	-146	dBc/Hz		4.6.5

4.7 RC oscillator characteristics

Table 11 RC oscillator characteristics

T_C = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
RC oscillator operating frequency	f_{RCOSC}	10	-	20	MHz		4.7.1
RC oscillator operating current at *VDD_D* supply	I_{RCOSC}	tbd	-	tbd	µA		4.7.
RC oscillator settling time	$t_{RCOSC,settle}$	-	5	-	µs		4.7.2
RC oscillator operating frequency temperature sensitivity	S_{RCOSC}	tbd	tbd	tbd	kHz/K	typical value with trim setting 15	4.7.4

4.8 Digital IO pins and I2C interface

Table 12 Digital IO and I2C characteristics

T_C = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
LOW level input voltage	$V_{IN(L)}$	0	-	0.25 * VDD	V		4.8.1
HIGH level input voltage	$V_{IN(H)}$	0.7 * VDD	-	VDD + 0.3	V	Not exceeding 3.465 V	4.8.2
I2C standard speed data rate	$f_{I2C,std}$	-	100	-	kbit/s	I2C clock derived from system clock between 8 MHz and 20 MHz	4.8.3
I2C fast speed data rate	$f_{I2C,fast}$	-	400	-	kbit/s	I2C clock derived from system clock between 12.5 MHz and 20 MHz	4.8.4

The integrated I2C slave interface supports slow and fast speed with a 7-bit I2C address. It does not support the optional features of the I2C protocol, like clock stretching, 10-bit slave address, general call, or software reset.

A detailed description of the protocol used to access registers can be found in the User Manual of the BGT24ATR22.

4.9 Temperature sensor

Table 13 Temperature sensor

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Temperature range	T	-40	-	+105	°C		4.9.1
ADC readout code	$V_{TEMP,OUT}$	-	2040	-	LSB	At 105°C	4.9.2
Sensitivity	$S_{TEMP,SENSE}$	-	8.8	-	LSB/K		4.9.3
Accuracy	$T_{SENS,ACC}$	-5	-	+5	K	At 105°C by considering temperature calibration value via calculation formula	4.9.4

4.10 TX output level sensor

Table 14 TX output level sensor characteristics

T_C = -40°C to 105°C, supply voltage LDO 1.71 V to 3.465 V, all analog supply voltages 1.71 V to 1.89 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24.0 GHz to 24.25 GHz.

Parameter	Symbol	Value			Unit	Condition	Number
		Min.	Typ.	Max.			
Transmitter output level sensitivity	S_{sense}	1.29	-	2	dBV/dBm		4.10.1
Dynamic range of output level sensor	ΔP_{sense}	-	30	-	dB		4.10.2

Matthias Brandl: As the measurement happens with the internal ADC, would not it be better to have a formula how to convert ADC values to power. - The same applies to the temperature sensor.

Matthias Brandl: I would like to remove this chapter and put the formula in the user manual.

5 Package outline

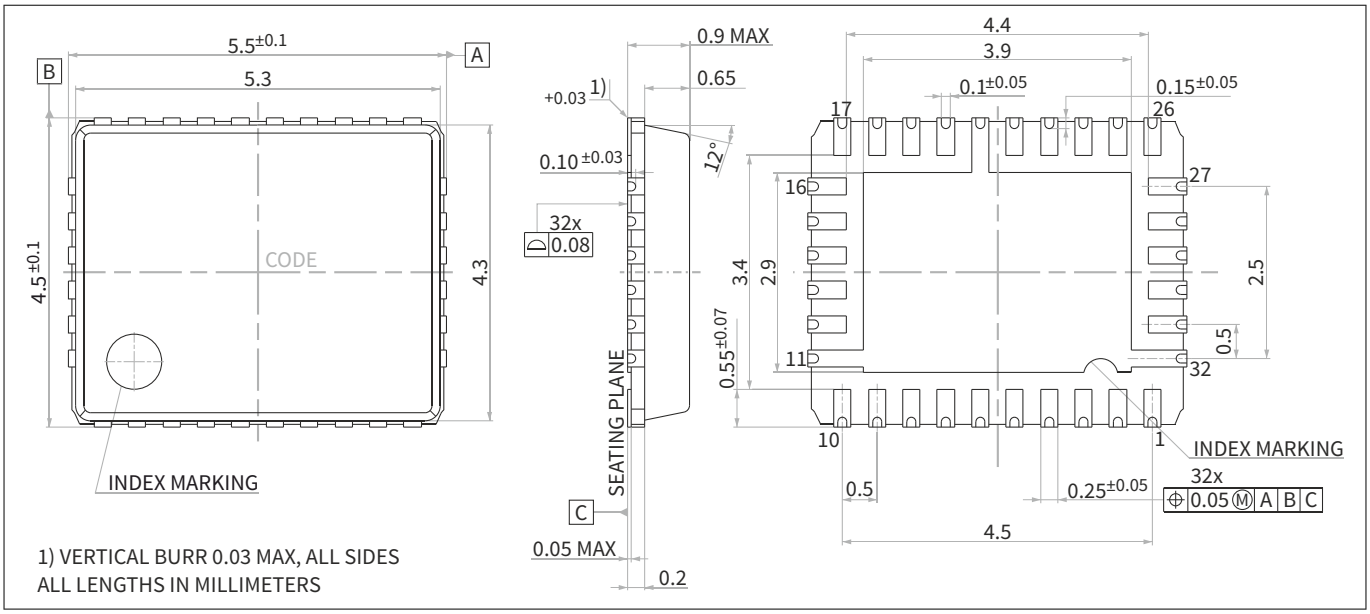

Figure 3 Package outline with top, side, and bottom view of VQFN-32-9.

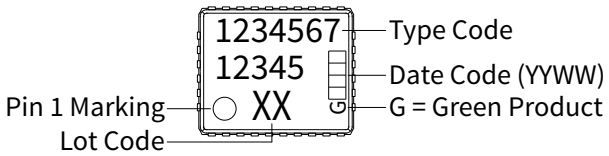

Figure 4 Marking layout of VQFN-32-9.

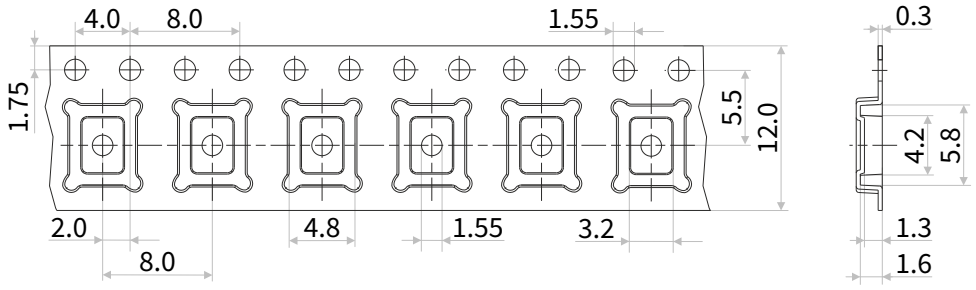

Figure 5 Tape of VQFN-32-9.

Glossary

AAF

anti-aliasing filter (AAF)

A filter used before a signal sampler to restrict the bandwidth of a signal to satisfy the Nyquist–Shannon sampling theorem over the band of interest.

ABB

analog base band (ABB)

A signal that has a near-zero frequency range, this is, a spectral magnitude that is nonzero only for frequencies in the vicinity of the origin and negligible elsewhere.

ADC

analog-to-digital converter (ADC)

A device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

AFC

automatic frequency control (AFC)

A method or circuit to automatically keep a resonant circuit tuned to a set frequency.

CDM

charge device model (CDM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge.

DAC

digital-to-analog converter (DAC)

A device that converts digital data into an analog signal (typically voltage).

DC

direct current (DC)

A form of power supply in which the flow of electric charge is only in one direction.

DRDP

digital radar data processing (DRDP)

The radar submodule that handle data storage and radar data preprocessing.

FSM

finite state machine (FSM)

An abstract machine that can be in exactly one of a finite number of states at any given time.

HBM

human body model (HBM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge based on a human body.

HW

hardware (HW)

The collection of physical components that comprise a computer or any other electronic system.

Glossary

I2C

inter-integrated circuit (I2C)

A synchronous serial communication bus which is widely used for attaching lower-speed peripheral ICs to processors and microcontrollers.

IF

intermediate frequency (IF)

The frequency corresponding to the carrier frequency or another characteristic frequency of an input radio-frequency signal in a signal resulting from each frequency translation.

LDO

low-dropout voltage regulator (LDO)

A direct current linear voltage regulator that can regulate the output voltage even if the supply voltage is very close to the output voltage.

LNA

low noise amplifier (LNA)

An amplifier specially designed to introduce the minimum possible internal noise for a given gain and to obtain the maximum possible signal-to-noise ratio at the output.

MMIC

monolithic microwave integrated circuit (MMIC)

A type of integrated circuit device that operates at microwave frequencies (300 MHz to 300 GHz).

PPF

polyphase filter (PPF)

A filter which splits an input signal into a given number of equidistant sub-bands.

RF

radio frequency (RF)

A frequency of a periodic radio wave or of the corresponding electric oscillation.

SAR

successive approximation register (SAR)

A type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation using a binary search through all possible quantization levels.

SMT

surface mount technology (SMT)

A method in which the electrical components are mounted directly onto the surface of a printed circuit board.

SNR

signal-to-noise ratio (SNR)

A measure that compares the level of a desired signal to the level of background noise.

SSB

single-sideband (SSB)

One side of a carrier signal.

Glossary

VCO

voltage controlled oscillator (VCO)

An oscillator whose frequency is a function of the voltage of an input signal.

VGA

variable gain amplifier (VGA)

An electronic amplifier that varies its gain depending on a control voltage.

VSWR

voltage standing wave ratio (VSWR)

A measure of impedance matching of loads to the characteristic impedance of a transmission line.

Revision history

Document version	Date of release	Description of changes
V0.1	2023-11-30	Final datasheet first draft
V1.0	2024-03-13	Final datasheet first release

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