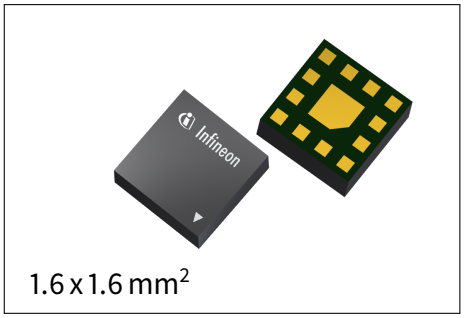
BGSX44MA12

4P4T Rx Switch with MIPI RFFE Interface

Features

- 4P4T Receive switch
- Low Insertion Loss and high port to port Isolation up to 3.8GHz
- Low current consumption
- MIPI RFFE 2.0 compliant control interface
- External USID select pin
- Ultra low profile leadless plastic package
- RoHS and WEEE compliant package



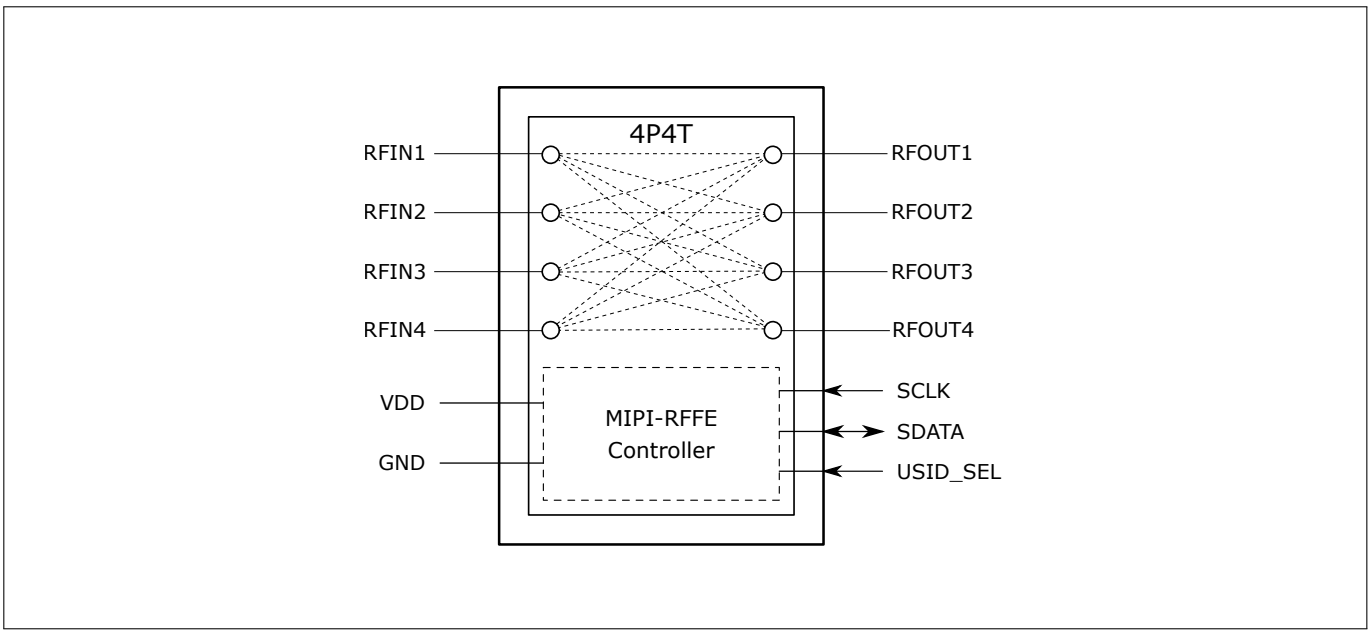
Application

Quadruple Receive Switch for Cellular Mobile devices. GSM/WCDMA/LTE Multimode Support including LTE Carrier Aggregation.

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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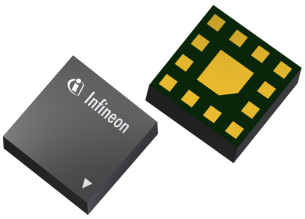
1 Features



- RF CMOS 4P4T Receive switch with high linearity
- Suitable for multi-mode LTE and WCDMA applications
- Ultra-low insertion loss and harmonics generation
- 0.1 to 3.8 GHz coverage
- High port-to-port-isolation
- Common VDD and MIPI supply for small package
- Integrated MIPI RFFE interface operating in 1.65 to 1.95 V voltage range
- External USID select pin
- Leadless and halogen free package ATSLP-12-12 with lateral size of 1.6 mm x 1.6 mm and thickness of 0.6 mm
- High EMI robustness
- RoHS and WEEE compliant package

2 Product Description

The BGSX44MA12 RF CMOS switch is specifically designed for LTE and WCDMA Receive path applications. This 4P4T offers low insertion loss and low harmonic generation.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.65 to 1.95 V. The BGSX44MA12 RF Switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 1.6 x 1.6 mm^2 and a maximum thickness of 0.6 mm.

Product Name	Marking	Package
BGSX44MA12	X4	ATSLP-12-12

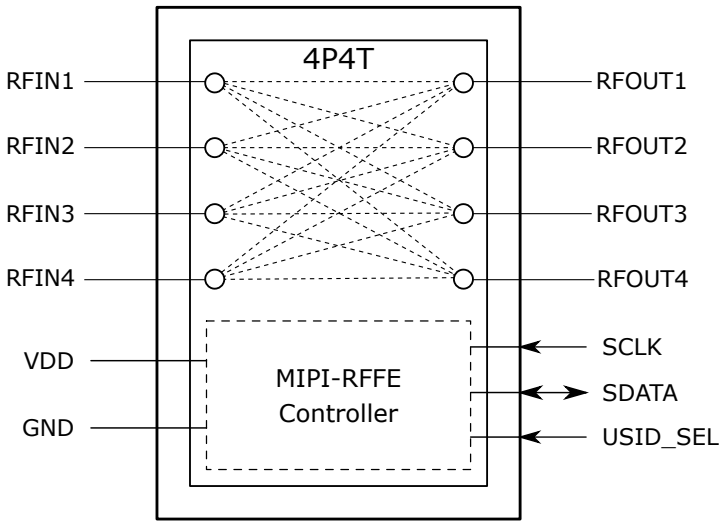


Figure 1: BGSX44MA12 Block Diagram

3 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	3.8	GHz	[1]
Chip & RFFE Supply voltage	V_{DD}	-0.5	–	2.2	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
RF input power at all RF ports	P_{RF}	–	–	28	dBm	CW
ESD capability, CDM[2]	V_{ESD_CDM}	–	–	Class C3		All pins
ESD capability, HBM[3]	V_{ESD_HBM}	–	–	Class 2		All pins
ESD capability, system level[4]	V_{ESD_RF}	-8	–	+8	kV	RF versus system GND, with 27 nH shunt inductor
		-6	–	+6	kV	RF versus system GND, with 56 nH shunt inductor

[1] There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[3] ANSI/ESDA/JEDEC JS-001 (R=1.5 kΩ, C=100 pF).
[4] IEC 61000-4-2 (R=330 Ω, C=150 pF), contact discharge.

Table 2: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
RFFE Control Voltage Levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{DD}+0.7 (max. 2.2)	V	–

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

4 Operation Ranges

Table 3: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip & RFFE Supply voltage[1)]	V_{DD}	1.65	1.8	1.95	V	–
Chip & RFFE supply current[2)]	I_{DD}	–	80	210	µA	–
Supply current in standby mode[2)]	I_{DD}	–	3.5	10	µA	Default or low-power mode
RFFE input high voltage[3)]	V_{IH}	0.7*V_{DD}	–	V_{DD}	V	–
RFFE input low voltage[3)]	V_{IL}	0	–	0.3*V_{DD}	V	–
RFFE output high voltage[3)]	V_{OH}	0.8*V_{DD}	–	V_{DD}	V	–
RFFE output low voltage[3)]	V_{OL}	0	–	0.2*V_{DD}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
Ambient temperature	T_A	-40	25	85	°C	–

[1)] Bypass capacitor 1nF - 10nF
[2)] T_A = −40 °C ... 85 °C, V_{DD} = 1.65 ... 1.95 V
[3)] SCLK and SDATA

Table 4: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power(50 Ω)	P_{RF}	–	–	25	dBm	–

5 RF Characteristics

Table 5: RF Characteristics[1] at T_A = −40 °C .. 85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 1.65V .. 1.95V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss at T_A = 25 °C, V_{DD}= 1.8V						
All RFIN/RFOUT ports	IL	–	0.45	0.55	dB	699 to 960MHz
except		–	0.60	0.70	dB	1710 to 2200MHz
RFIN1,2/RFOUT2		–	0.70	0.80	dB	2300 to 2700MHz
RFIN3,4/RFOUT4		–	0.80	1.00	dB	3400 to 3800MHz
RFIN1,2/RFOUT2 RFIN3,4/RFOUT4	IL	–	0.45	0.55	dB	699 to 960MHz
		–	0.60	0.80	dB	1710 to 2200MHz
		–	0.75	0.90	dB	2300 to 2700MHz
		–	0.90	1.20	dB	3400 to 3800MHz
Insertion Loss						
All RFIN/RFOUT ports	IL	–	0.45	0.60	dB	699 to 960MHz
except		–	0.60	0.80	dB	1710 to 2200MHz
RFIN1,2/RFOUT2		–	0.70	0.90	dB	2300 to 2700MHz
RFIN3,4/RFOUT4		–	0.90	1.10	dB	3400 to 3800MHz
RFIN1,2/RFOUT2 RFIN3,4/RFOUT4	IL	–	0.45	0.60	dB	699 to 960MHz
		–	0.60	0.85	dB	1710 to 2200MHz
		–	0.75	1.00	dB	2300 to 2700MHz
		–	1.00	1.30	dB	3400 to 3800MHz
Return Loss						
All RFIN/RFOUT ports	RL	19	23	–	dB	699 to 960MHz
		12	17	–	dB	1710 to 2200MHz
		11	15	–	dB	2300 to 2700MHz
		7.5	11	–	dB	3400 to 3800MHz
Isolation						
All RFIN/RFOUT ports	ISO	36	46	–	dB	699 to 960MHz
		31	40	–	dB	1710 to 2200MHz
		29	38	–	dB	2300 to 2700MHz
		25	36	–	dB	3400 to 3800MHz

[1] Measured on application board without any external matching components

Table 6: RF Characteristics[1] at T_A = −40 °C .. 85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 1.65V .. 1.95V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation up to 12.75 GHz						
All RFIN/RFOUT ports, H2	P_{Harm}	–	-105	-95	dBc	15 dBm, 50 Ω, CW Mode
All RFIN/RFOUT ports, H3	P_{Harm}	–	-95	-90	dBc	15 dBm, 50 Ω, CW Mode
Intermodulation Distortion in Rx Band						
2nd order input refered intercept point (all Ports)	IIP2	100	115	–	dBm	Tx = 20 dBm, Interferer = 0 dBm, 50Ω
3rd order input refered intercept point (all Ports)	IIP3	55	61	–	dBm	
Switching Time[2]						
MIPI to RF time	t_{INT}	–	2.5	4	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power up settling time	t_{PUP}	–	10	25	µs	After power down mode

[1] Measured on application board without any external matching components
[2] Do not change switch state during first 10µs of power-up

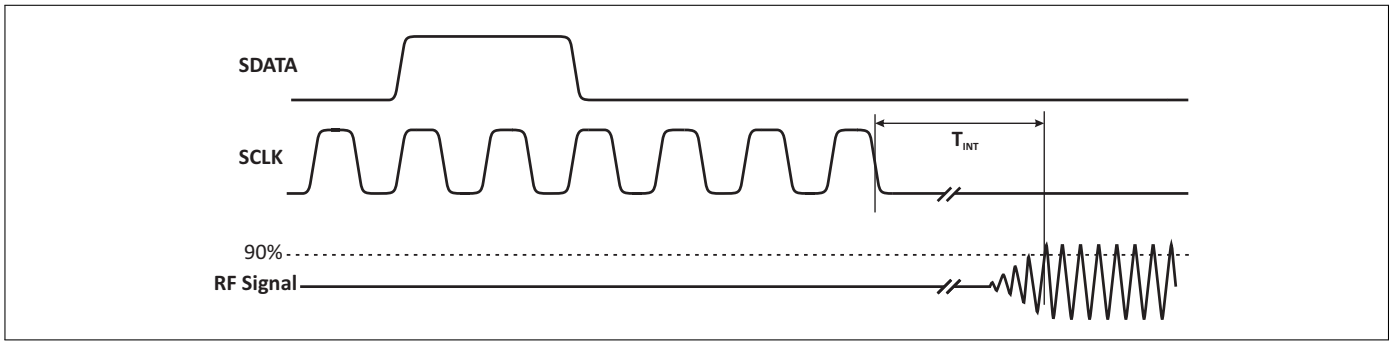


Figure 2: MIPI to RF Time

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 2.0 - 25. September 2014.

Table 7: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.0 standard	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences & extended register write with EXT_PRODUCT_ID
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VDD, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin for changing USID: USID_SEL=0 → 1010 USID_SEL=1 → 1011
USID selection via SDATA / SCLK swap feature	No	

Table 8: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 9: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x01	REGISTER_1	7:0	MODE_CTRL	RFIN 1 & 2 control	00000000	No	Trigger1	R/W
0x02	REGISTER_2	7:0	MODE_CTRL	RFIN 3 & 4 control	00000000	No	Trigger1	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11100110	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 7	No	No	R/W

Table 10: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	RESERVED	Extension to PRODUCT_ID register 0x1D	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Packaged switch revision ID	0000	No	No	R
		3:0	SUB_REVISION	Packaged switch sub-revision ID	0001			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

Table 11: Modes of Operation (Truth Table)

		REGISTER_1 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	RFIN1-RFOUT1 ISO	x	x	x	x	x	x	x	0
2	RFIN1-RFOUT1	x	x	x	x	x	x	x	1
3	RFIN1-RFOUT2 ISO	x	x	x	x	x	x	0	x
4	RFIN1-RFOUT2	x	x	x	x	x	x	1	x
5	RFIN1-RFOUT3 ISO	x	x	x	x	x	0	x	x
6	RFIN1-RFOUT3	x	x	x	x	x	1	x	x
7	RFIN1-RFOUT4 ISO	x	x	x	x	0	x	x	x
8	RFIN1-RFOUT4	x	x	x	x	1	x	x	x
9	RFIN2-RFOUT1 ISO	x	x	x	0	x	x	x	x
10	RFIN2-RFOUT1	x	x	x	1	x	x	x	x
11	RFIN2-RFOUT2 ISO	x	x	0	x	x	x	x	x
12	RFIN2-RFOUT2	x	x	1	x	x	x	x	x
13	RFIN2-RFOUT3 ISO	x	0	x	x	x	x	x	x
14	RFIN2-RFOUT3	x	1	x	x	x	x	x	x
15	RFIN2-RFOUT4 ISO	0	x	x	x	x	x	x	x
16	RFIN2-RFOUT4	1	x	x	x	x	x	x	x
		REGISTER_2 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	RFIN3-RFOUT1 ISO	x	x	x	x	x	x	x	0
2	RFIN3-RFOUT1	x	x	x	x	x	x	x	1
3	RFIN3-RFOUT2 ISO	x	x	x	x	x	x	0	x
4	RFIN3-RFOUT2	x	x	x	x	x	x	1	x
5	RFIN3-RFOUT3 ISO	x	x	x	x	x	0	x	x
6	RFIN3-RFOUT3	x	x	x	x	x	1	x	x
7	RFIN3-RFOUT4 ISO	x	x	x	x	0	x	x	x
8	RFIN3-RFOUT4	x	x	x	x	1	x	x	x
9	RFIN4-RFOUT1 ISO	x	x	x	0	x	x	x	x
10	RFIN4-RFOUT1	x	x	x	1	x	x	x	x
11	RFIN4-RFOUT2 ISO	x	x	0	x	x	x	x	x
12	RFIN4-RFOUT2	x	x	1	x	x	x	x	x
13	RFIN4-RFOUT3 ISO	x	0	x	x	x	x	x	x
14	RFIN4-RFOUT3	x	1	x	x	x	x	x	x
15	RFIN4-RFOUT4 ISO	0	x	x	x	x	x	x	x
16	RFIN4-RFOUT4	1	x	x	x	x	x	x	x

7 Application Information

Pin Configuration and Function

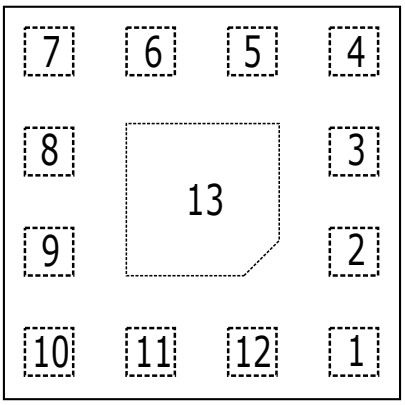


Figure 3: BGSX44MA12 Pin Configuration (top view)

Table 12: Pin Definition and Function

Pin No.	Name	Function
1	USID_SEL	MIPI USID select pin (to be connected to VDD or GND)
2	RFOUT3	RFout port 3
3	RFOUT4	RFout port 4
4	RFIN4	RFin port 4
5	RFIN3	RFin port 3
6	RFIN2	RFin port 2
7	RFIN1	RFin port 1
8	RFOUT2	RFout port 2
9	RFOUT1	RFout port 1
10	VDD	Common VDD & MIPI supply
11	SCLK	MIPI RFFE clock
12	SDATA	MIPI RFFE data
13	GND	Common ground

8 Package Information

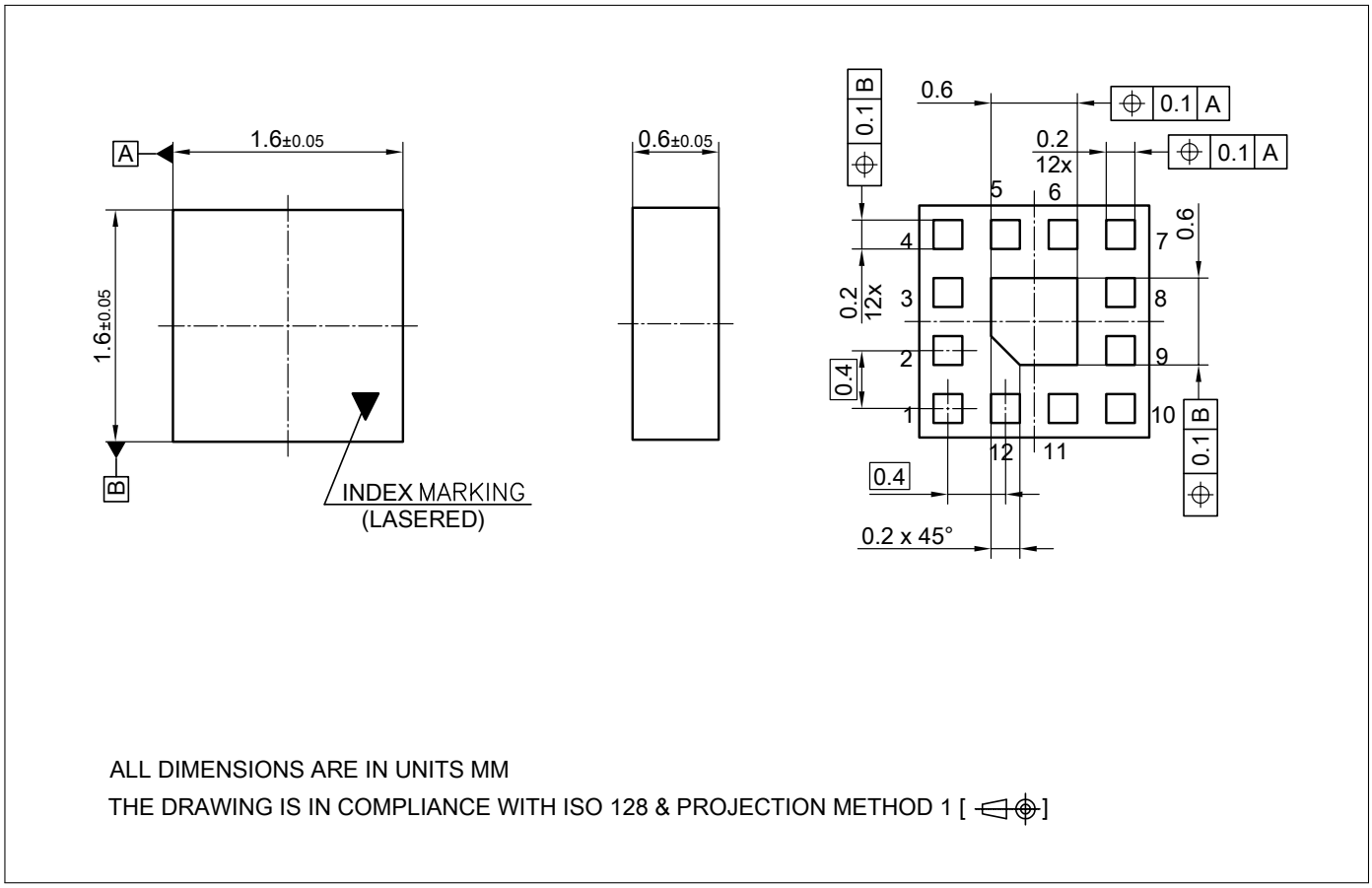


Figure 4: ATSLP-12-12 Package Outline (top, side and bottom views)

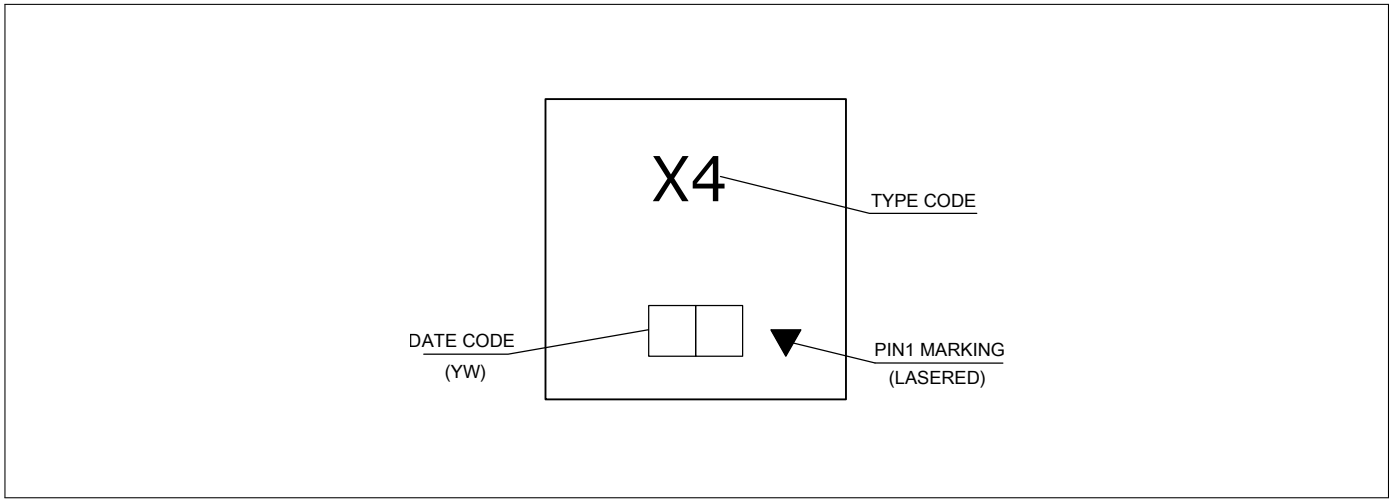


Figure 5: Marking Specification (top view)

Table 13: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 14: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

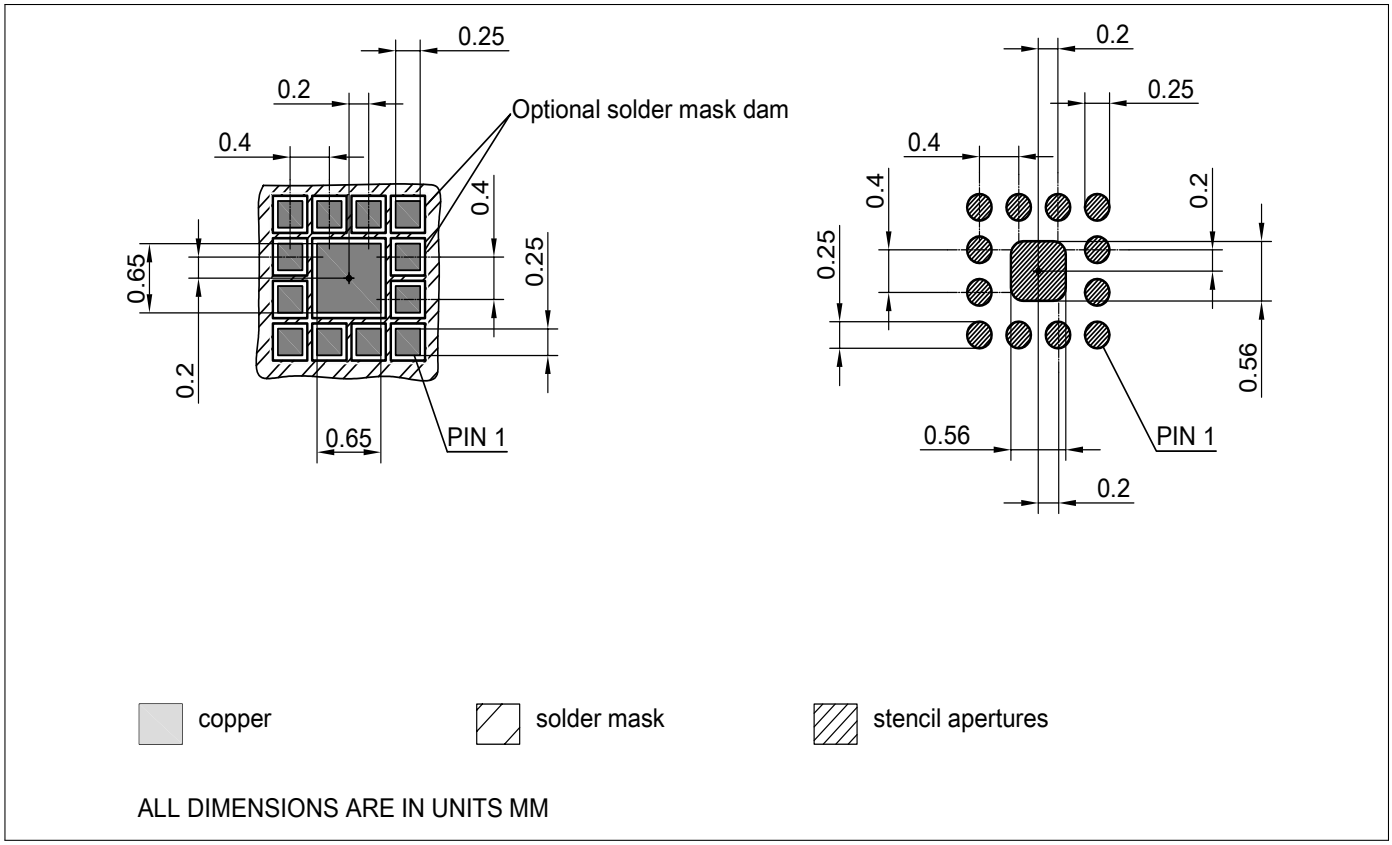


Figure 6: Footprint Recommendation

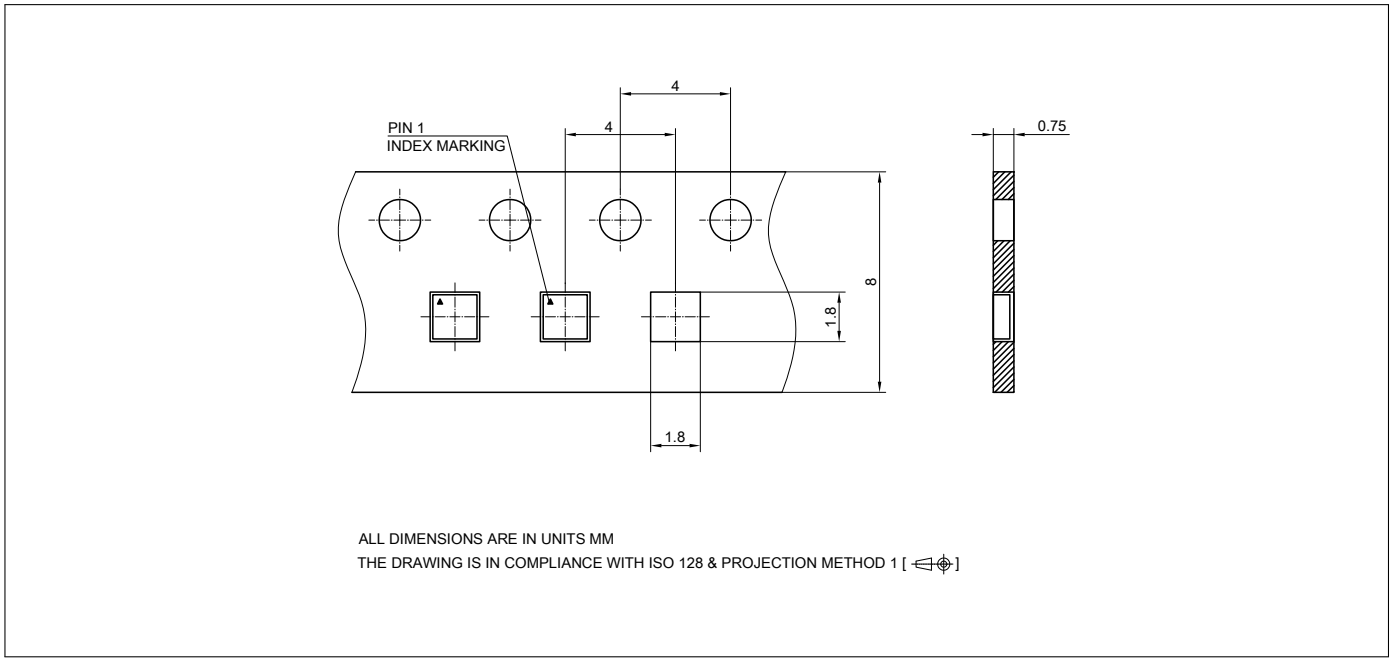


Figure 7: ATSLP-12-12 Carrier Tape

Revision History	
Revision v2.1 - 2018-04-26	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.2, 2018-05-28	
3	Maximum Ratings updated in Table 1

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