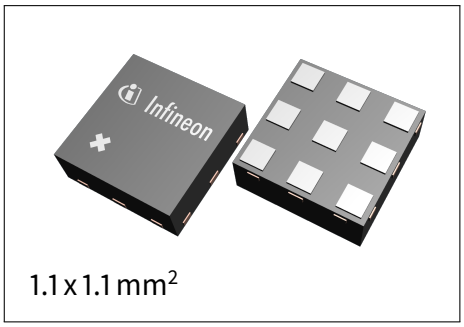
BGA9V1MN9

3.8 GHz Low Noise Amplifier with Gain Steps and MIPI Control

Features

- Operating frequencies: 3.3 - 4.2 GHz
- Insertion power gain: 21.0 dB
- Gain dynamic range: 24 dB
- Low noise figure: 0.75 dB
- Low current consumption: 5.8 mA
- Multi-state control: Gain- and Bypass-Modes
- Small TSNP leadless package



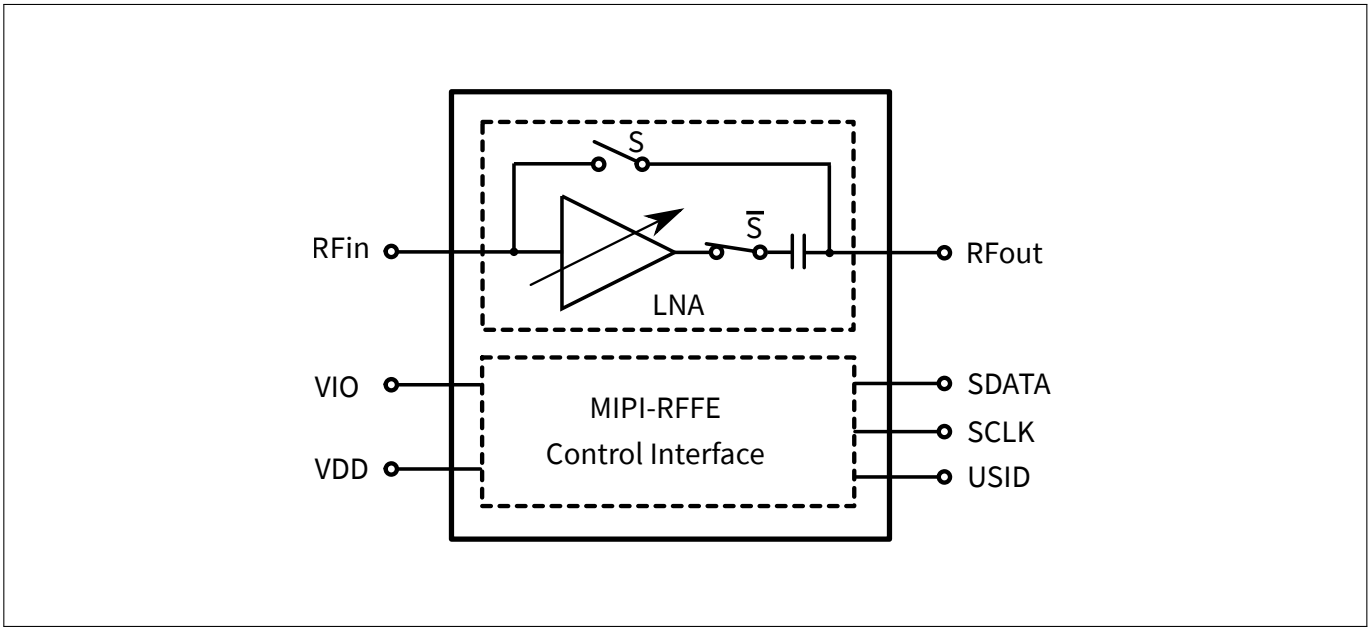
Potential Applications

The BGA9V1MN9 is designed for 4G and 5G applications covering 3GPP Bands between 3.3 and 4.2 GHz (Bands B42, B43, n77 and n78). Thanks to a high gain and an ultra-low Noise Figure performance of the LNA frontend losses can be compensated and the data rate can be significantly improved. The MIPI interface provides a comprehensive control over multiple gain steps and bias modes to increase the overall system dynamic range.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block Diagram



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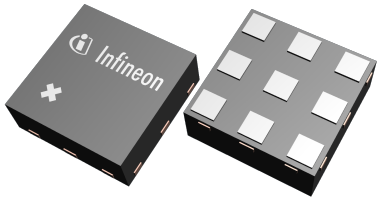
1 Features



- Power gain: 21.0 dB
- Low noise figure: 0.75 dB
- Low current consumption: 5.8 mA
- Frequency range from 3.3 to 4.2 GHz
- Supply voltage: 1.1 to 2.0 V
- Integrated MIPI RFFE interface operating in 1.65 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- USID select pin
- Small form factor 1.1 mm x 1.1 mm
- High EMI robustness
- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

2 Product Description

The BGA9V1MN9 is a low noise amplifier for LTE and 5G which covers a wide frequency range from 3.3 GHz to 4.2 GHz. The LNA provides up to 21.0 dB gain and 0.75 dB noise figure at a current consumption of 5.8 mA in the application configuration described in Chapter 7. With the Gain Step feature the gain and linearity can be adjusted to increase the system dynamic range and to accommodate to changing interference scenarios. The BGA9V1MN9 supports ultra-low bypass current of 2 µA and 1.2 V operating voltage to reduce power consumption. It operates from 1.1 V to 2.0 V supply voltage over temperature. The compact 9 pin TSNP-9 package with the dimension of 1.1 x 1.1 mm helps to save space on the PCB.

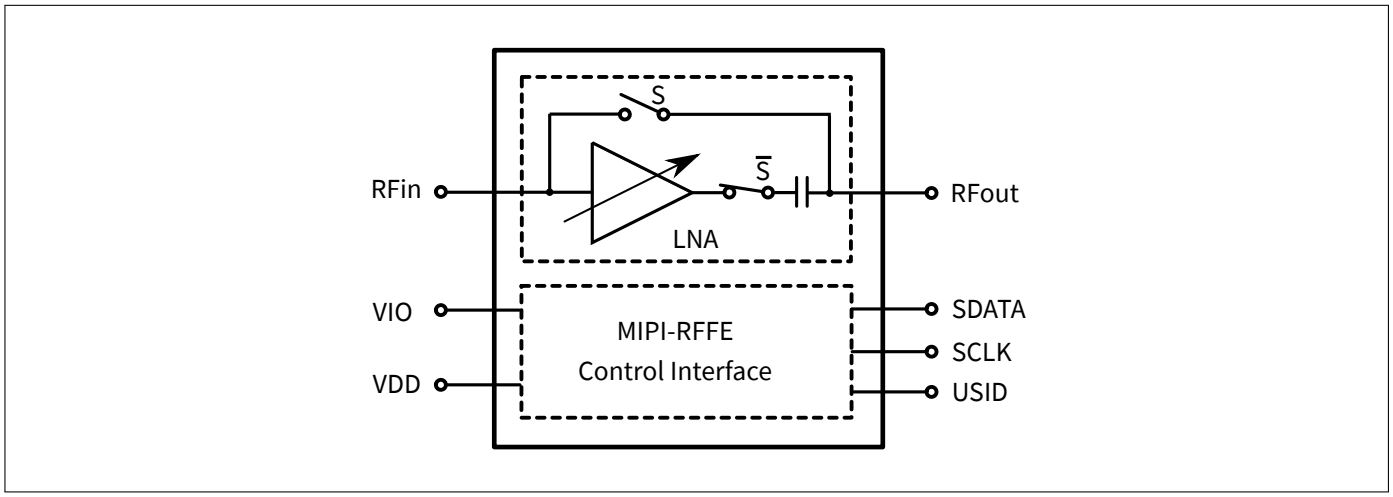


Figure 1: BGA9V1MN9 Block diagram

Product Name	Marking	Package
BGA9V1MN9	V	TSNP-9-6

3 Maximum Ratings

Table 1: Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage VDD	V_{DD}	-0.5	–	2.2	V	[1]
Voltage at RFin	V_{AI}	0	–	0	V	–
Voltage at RFout	V_{AO}	0	–	0	V	–
Current into pin VDD	I_{DD}	–	–	22	mA	–
RF input power	P_{IN}	–	–	25	dBm	–
Total power dissipation	P_{tot}	–	–	50	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-30	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
ESD robustness, HBM	V_{ESD_HBM}	-1000	–	1000	V	[2]
ESD robustness, CDM	V_{ESD_CDM}	-1000	–	1000	V	[3]
RFFE Supply Voltage	V_{IO}	-0.5	–	2.2	V	–
RFFE Supply Voltage Levels	V_{SCLK}, V_{SDATA}, V_{USID}	-0.7	–	V_{IO} + 0.7 (max. 2.2)	V	–

[1] All voltages refer to GND-Nodes unless otherwise noted
[2] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

4 DC Characteristics

Table 3: DC Characteristics at T_A = 25 °C

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	1.1	1.8	2.0	V	–
Supply Current	I_{DD}	4.3	5.8	7.3	mA	G0/G1 mode in Bias6
		2.7	3.7	4.7	mA	G2-G5 mode in Bias2
		–	2	4	µA	Bypass mode (all bias)
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[2]	V_{IH}	0.7 * V_{IO}	–	V_{IO}	V	Logical "1"
RFFE input low voltage[2]	V_{IL}	0	–	0.3 * V_{IO}	V	Logical "0"
RFFE output high voltage[3]	V_{OH}	0.8 * V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[3]	V_{OL}	0	–	0.2 * V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	3	–	µA	Idle State

[1] Based on the application described in Chapter 7
[2] SCLK, SDATA and USID
[3] SDATA

5 RF Characteristics

Table 4: RF Characteristics in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, f = 3.3– 4.2 GHz, performance guaranteed in bias modes as in Table 3

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain f = 3800 MHz	$1/\lvert S_{21}\rvert^2$	19.5	21.0	22.5	dB	G0
		16.5	18.0	19.5	dB	G1
		13.4	14.9	16.4	dB	G2
		10.4	11.9	13.4	dB	G3
		7.0	8.5	10.0	dB	G4
		-4.2	-2.7	-1.2	dB	G5
		-4.0	-3.0	-2.0	dB	G6
Noise Figure f = 3800 MHz	NF	–	0.75	1.3	dB	G0
		–	0.8	1.4	dB	G1
		–	1.0	1.6	dB	G2
		–	1.15	1.7	dB	G3
		–	1.4	2.0	dB	G4
		–	11.0	12.0	dB	G5
		–	3.0	4.0	dB	G6

Continued on next page

Table 4: RF Characteristics – Continued from previous page

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Return Loss[1] f = 3800 MHz	RL_{in}	5	8	–	dB	G0
		4	7	–	dB	G1
		8	12	–	dB	G2
		7	11	–	dB	G3
		7	11	–	dB	G4
		10	14	–	dB	G5
		9	13	–	dB	G6
Output Return Loss f = 3800 MHz	RL_{out}	10	24	–	dB	G0
		10	20	–	dB	G1
		10	33	–	dB	G2
		10	17	–	dB	G3
		8	12	–	dB	G4
		10	20	–	dB	G5
		7	10	–	dB	G6
Reverse Isolation f = 3800 MHz	$1/\lvert S_{12}\rvert^2$	30	35	–	dB	G0
		31	36	–	dB	G1
		26	31	–	dB	G2
		28	33	–	dB	G3
		30	35	–	dB	G4
		27	32	–	dB	G5
		2.0	3.0	–	dB	G6
Inband input 1dB-compression point f = 3800 MHz	IP_{1dB}	-22	-18	–	dBm	G0
		-21	-17	–	dBm	G1
		-12	-16	–	dBm	G2
		-12	-16	–	dBm	G3
		-12	-16	–	dBm	G4
		-3	+1	–	dBm	G5
		+3	+7	–	dBm	G6
Inband input 3rd-order intercept point[2]	$IIP3$	-12	-7	–	dBm	G0
		-12	-7	–	dBm	G1
		-9	-4	–	dBm	G2
		-9	-4	–	dBm	G3
		-9	-4	–	dBm	G4
		+5	+11	–	dBm	G5
		+18	+23	–	dBm	G6
Gain step phase error after compensation[3] f = 3800 MHz		-5	–	5	°	–

Continued on next page

[1] Can be tuned by using additional external matching components
[2] Input power = −30 dBm for each tone for modes G0-G5 / −15 dBm for mode G6, f_1 = 3800 MHz, $f_2 = f_1 + 1$ MHz
[3] Considers part to part variation after compensation in Base Band with constant value

Table 4: RF Characteristics – Continued from previous page

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain dependent phase offset *f* = 3800 MHz		–	0	–	°	G0/G1 (reference phase)
		–	-14.0	–	°	G2/G3/G4
		–	-45.5	–	°	G5
		–	152.5	–	°	G6
Stability	*k*	> 1	–	–		*f* = 20 MHz - 10 GHz
MIPI to RF time	t_{PUP}	–	–	1	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2

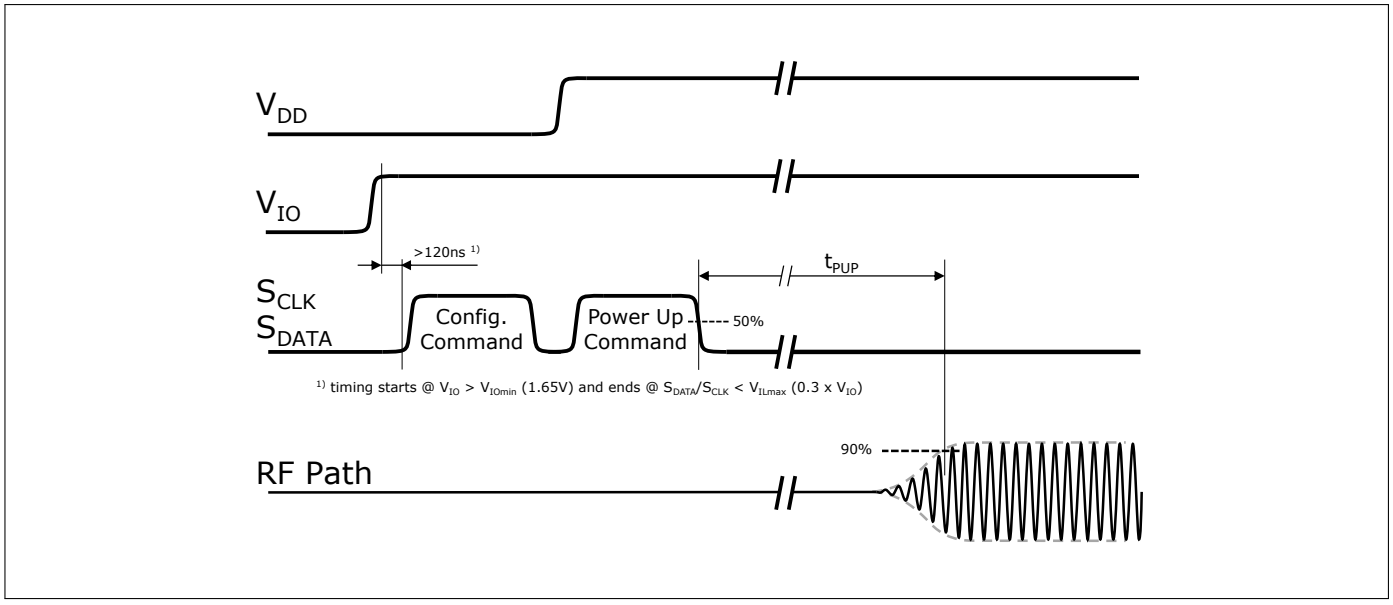


Figure 2: MIPI to RF time

6 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017' as well as the 'Qualcomm RFFE Vendor specification 80-N7876-1 Rev. W'.

Table 5: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_Sel pin	Yes	See Tab. 10
USID selection via SDATA / SCLK swap feature	Yes	See Tab. 10

Table 6: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 7: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x01	REGISTER_1	7:0	MODE_CTRL	LNA control	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE) 1: Low Power Mode (LOW POWER)	1	Yes	No	R/W MW
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE) 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		2	TRIGGER_2	0: No action (data held in shadow REG) 1: Data transferred to active REG	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
		0	TRIGGER_0	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	01010100	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001			R
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 10	No	No	R/W

Table 8: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID		00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0000	No	No	R
		3:0	SUB_REVISION		0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Programs the drive strength of the SDATA driver in readback modes. 0x0: 10pF 0x1: 20pF 0x2: 30pF 0x3: 40pF 0x4: 50pF (default) 0x5: 60pF 0x6: 80pF 0x7: 80pF	0x4			
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data masked (held in shadow REG)	0	No	No	R/W MW
				1: Data not masked (ready for transfer to active REG)				
		6	TRIGGER_MASK_9	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		5	TRIGGER_MASK_8	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_7	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_6	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_MASK_5	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		1	TRIGGER_MASK_4	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		0	TRIGGER_MASK_3	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				

Table 9: Register Mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action (data held in shadow REG)	0	Yes	No	R/W MW
				1: Data transferred to active REG				
		6	TRIGGER_9	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		5	TRIGGER_8	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		4	TRIGGER_7	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		3	TRIGGER_6	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		2	TRIGGER_5	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		1	TRIGGER_4	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_3	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				

Table 10: USID States

USID pin	SDATA/SCLK	USID
0	Nominal	0b1000
1	Nominal	0b1001
0	Swap	0b1010
1	Swap	0b1011

Table 11: Gain Modes of Operation (Truth Table, Register_1)

		REGISTER_1 Bits							
State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
1	OFF	0	x	x	x	x	x	x	x
2	Gain G0	1	0	0	1	x	x	x	x
3	Gain G1	1	0	1	0	x	x	x	x
4	Gain G2	1	0	1	1	x	x	x	x
5	Gain G3	1	1	0	0	x	x	x	x
6	Gain G4	1	1	0	1	x	x	x	x
7	Gain G5	1	1	1	0	x	x	x	x
8	Gain G6 (Bypass)	1	1	1	1	x	x	x	x

Table 12: Bias settings (Truth Table, Register_1)

		REGISTER_1 Bits							
State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
9	Bias0 (2.5 mA)	1	x	x	x	0	0	0	0
10	Bias1 (3.1 mA)	1	x	x	x	0	0	0	1
11	Bias2 (3.7 mA)[1]	1	x	x	x	0	0	1	0
12	Bias3 (4.2 mA)	1	x	x	x	0	0	1	1
13	Bias4 (4.7 mA)	1	x	x	x	0	1	0	0
14	Bias5 (5.2 mA)	1	x	x	x	0	1	0	1
15	Bias6 (5.8 mA)[2]	1	x	x	x	0	1	1	0
16	Bias7 (6.3 mA)	1	x	x	x	0	1	1	1
17	Bias8 (6.8 mA)	1	x	x	x	1	0	0	0
18	Bias9 (7.3 mA)	1	x	x	x	1	0	0	1
19	Bias10 (7.8 mA)	1	x	x	x	1	0	1	0

[1]Target bias mode for Gain modes G2-G5
[2]Target bias mode for Gain modes G0-G1

7 Application Information

Pin Configuration and Function

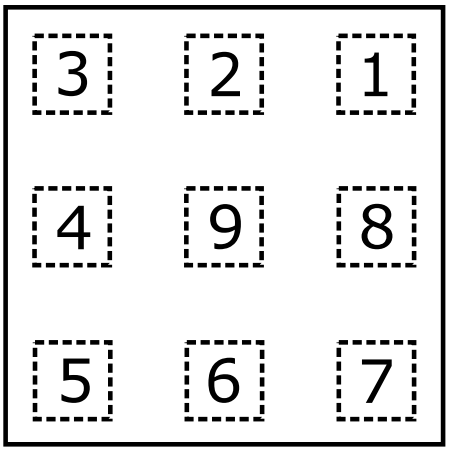


Figure 3: BGA9V1MN9 Pin Configuration (top view)

Table 13: Pin Definition and Function

Pin No.	Name	Function
1	AO	LNA output
2	GND	Ground
3	AI	LNA input
4	USID	USID select pin
5	VIO	MIPI RFFE supply
6	SCLK	MIPI RFFE clock
7	SDATA	MIPI RFFE data
8	VDD	Power supply
9	GND	Ground

Application Board Configuration

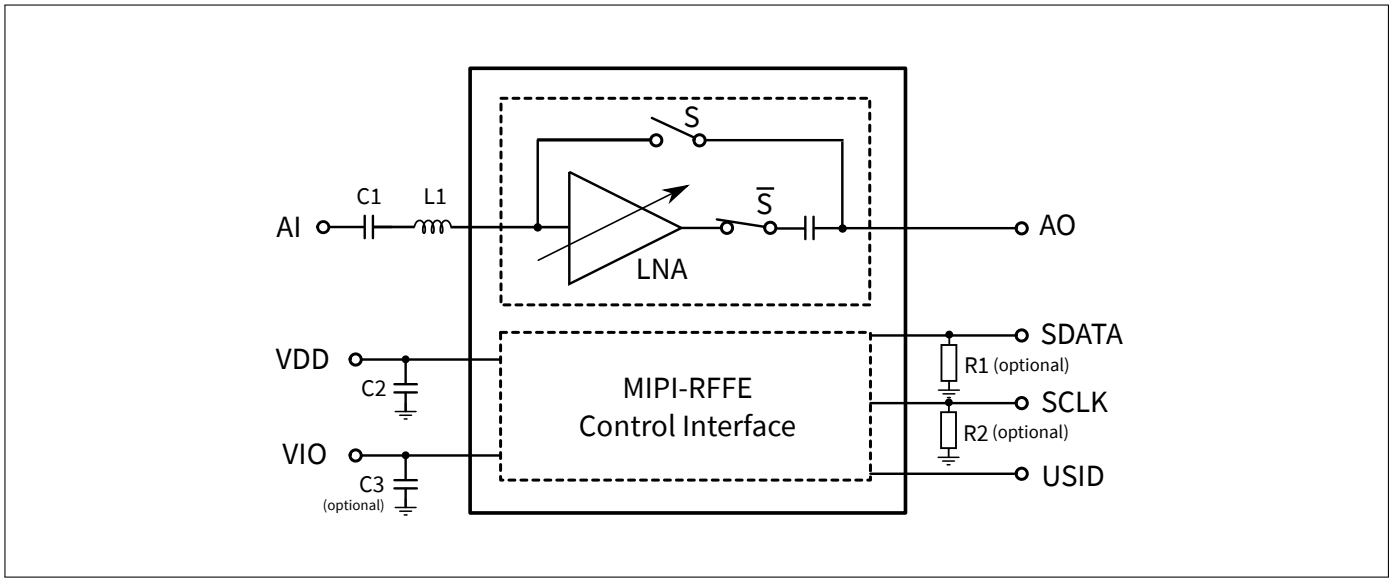


Figure 4: BGA9V1MN9 Application Schematic

Table 14: Bill of Materials Table

Name	Value	Package	Manufacturer	Function
C1	22 pF	0201	Various	DC block
C2	10 nF	0201	Various	RF bypass[1]
C3 (optional)	10 nF	0201	Various	RF bypass[1]
L1	2.7 nH	0201	muRata LQP type	Input matching
R1 (optional)	100 kΩ	0201	Various	Pull-down resistor[2]
R2 (optional)	100 kΩ	0201	Various	Pull-down resistor[2]
N1	BGA9V1MN9	TSNP-9-6	Infineon	Variable gainstep LNA

[1] RF bypass recommended to mitigate power supply noise.
[2] External pulldown may be required if master doesn't provide proper pulldown before first SSC.

8 Package Information

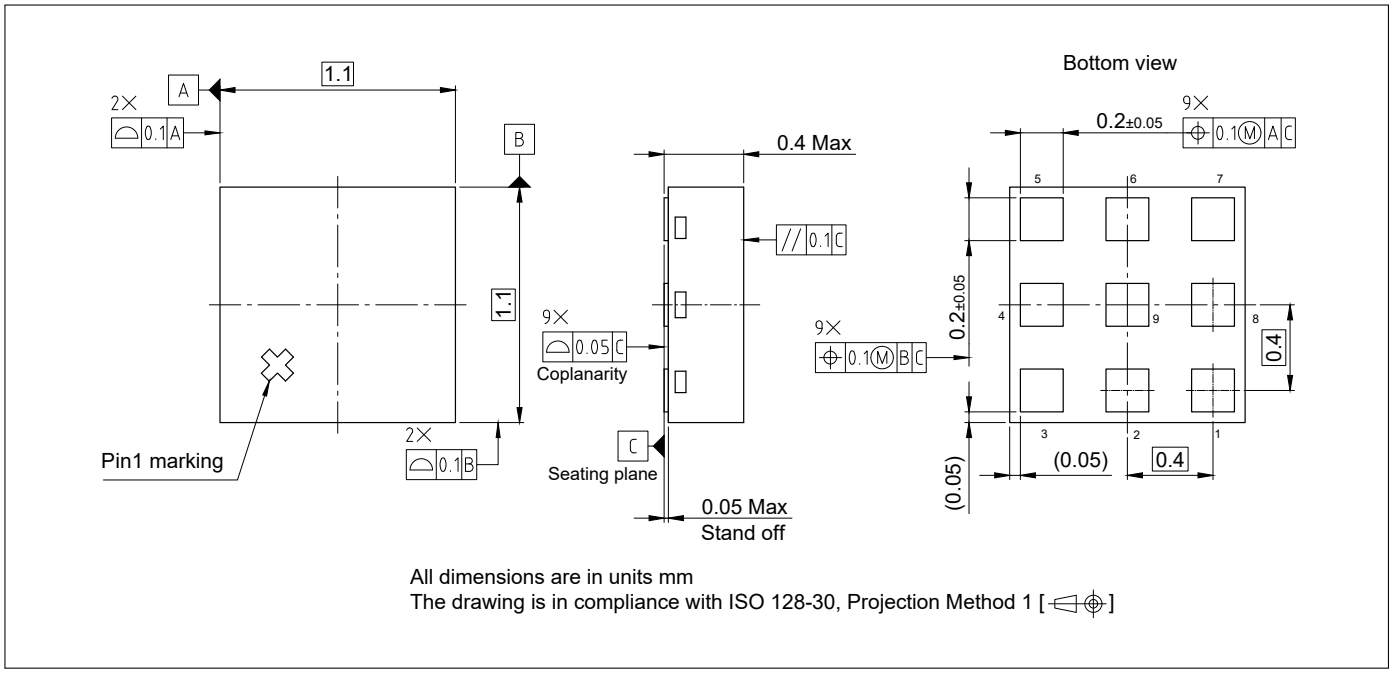


Figure 5: TSNP-9-6 Package Outline (top, side and bottom views)

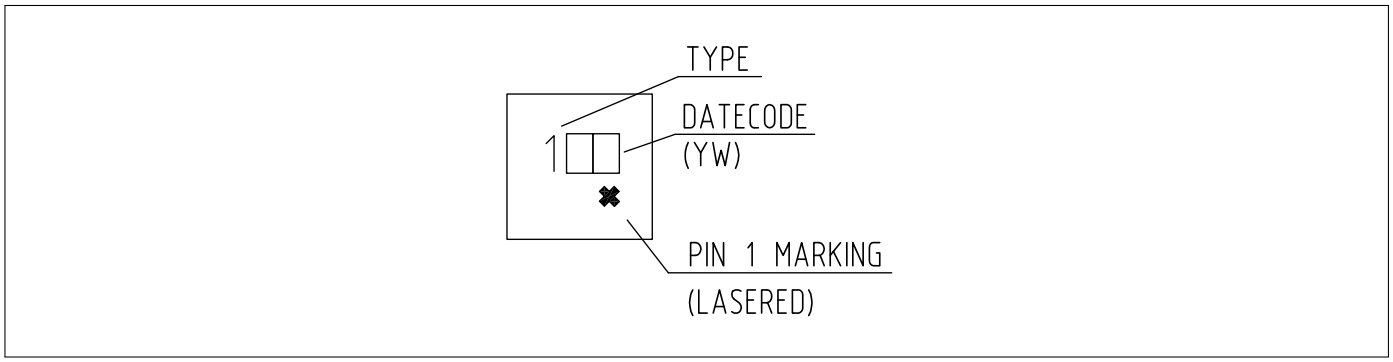


Figure 6: Marking Specification (top view)

Table 15: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 16: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

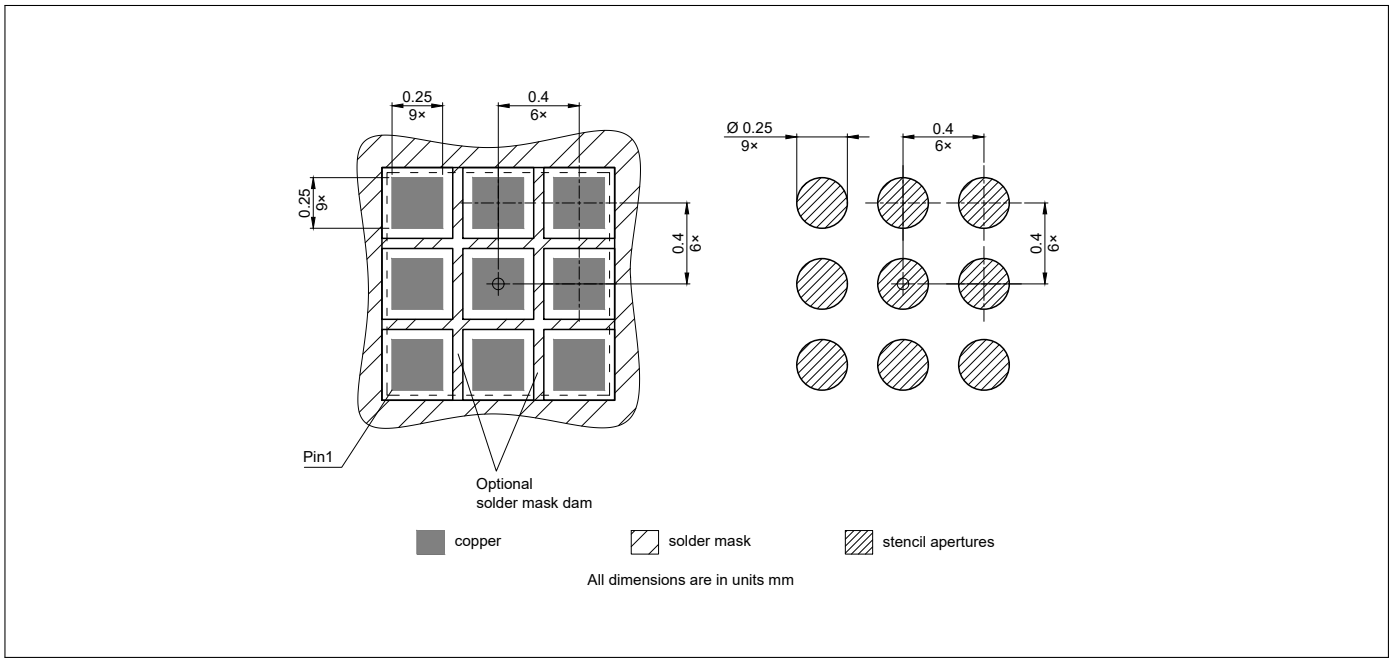


Figure 7: TSNP-9-6 Footprint Recommendation

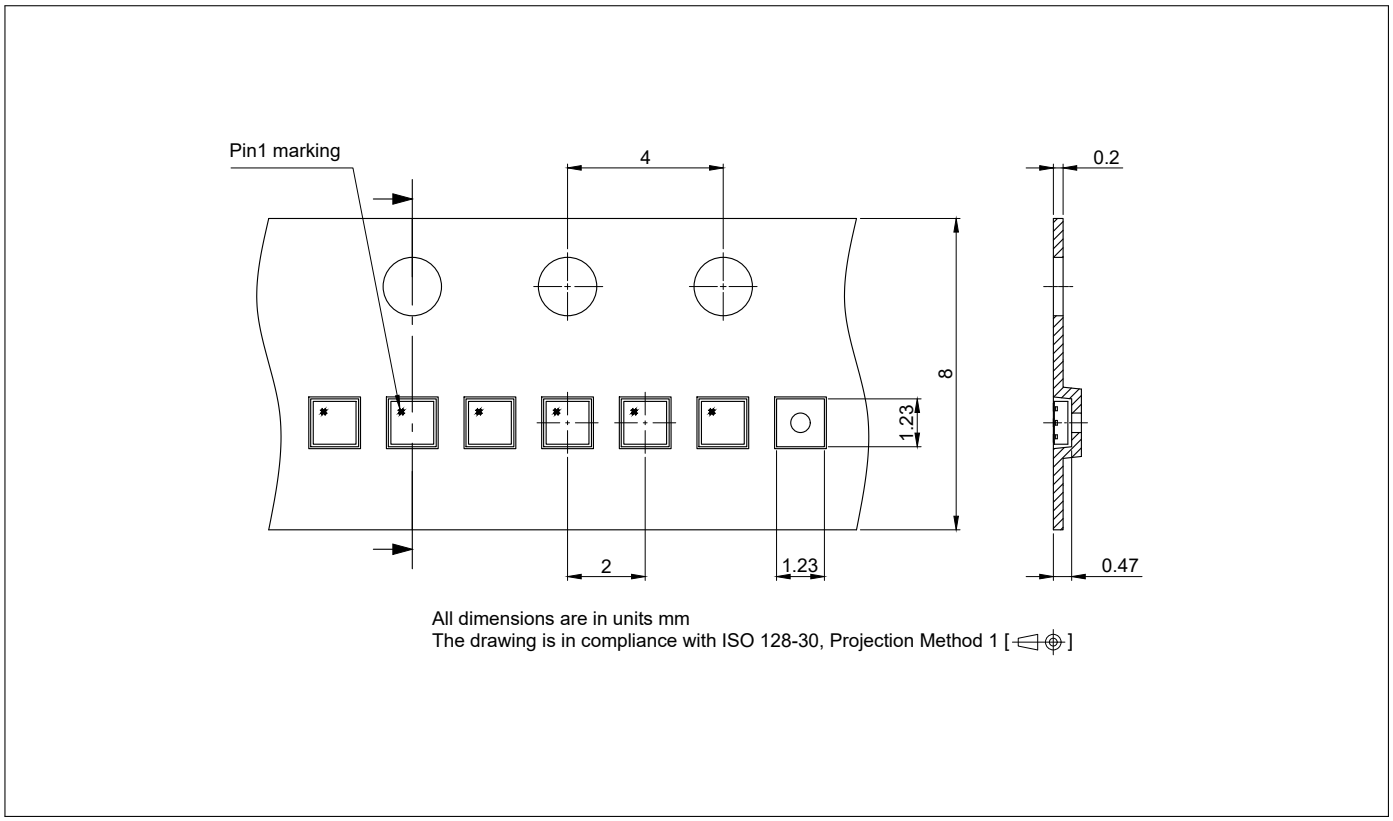


Figure 8: TSNP-9-6 Carrier Tape

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.0, 2021-04-28	
all	Initial version of final datasheet

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