# XDPL8221 CSV file parameter description for 100 W reference design

## XDP™ digital power

## Ordering code: REF-XDPL8221-U100W

## About this document

### Scope and purpose

This document describes the parameters defined in the CSV file for the XDPL8221 digital controller.

### Intended audience

This document is intended for anyone who intends to design a high-performance dual-stage Power Factor Correction (PFC) + flyback AC/DC-DC converter for LED lighting based on the XDPL8221 digital controller.

## Table of contents

# 1 Introduction

This application note describes the available parameters and their use for the XDPL8221, which is a configurable digital platform product. It can be configured to meet a wide range of application requirements. This is enabled by changing the application-related parameters. These are constants used by the application firmware, which is programmed in the IC controller and can be adapted to the respective LED-driver requirements on the different boards. The parameters are defined in the CSV file provided by Infineon. The procedure for changing the parameters is done through the .dp Vision tool.

*Note: The predefined parameters used in this description are intended for the 100 W universal-input reference board.*

# 2 Parameter handling/recommendations

After finishing calculations of the hardware components according to the design guide (see **[4]**), the user must determine the configuration of the XDPL8221. This is achieved by entering the hardware configuration and the customer's requirements into the .dp Vision tool. Based on this data, the .dp Vision tool will automatically calculate all relevant parameters. The tool allows the user to test the ICs with the parameters and finally to burn the parameters into the ICs.

A complete list of available parameters in the XDPL8221 can be found in the XDPL8221 datasheet (see **[1]**). Detailed information on using the .dp Vision tool is available in the application note for the XDPL8221 reference design (see **[2]**) and in the .dp Vision User Guide (see **[3]**).

The following sub-sections describe a few examples of how to set up an XDPL8221 configuration file.

## 2.1 Design parameters

The parameters are defined with default values in the CSV file. This is provided by Infineon and is available to be downloaded from http://www.infineon.com/cms/en/product/promopages/digital-power. After opening an existing configuration CSV file through the .dp Vision tool, it is necessary to enter the appropriate values calculated in the XDPL8221 system design simulation tool. Available parameters are presented in the following sub-sections.

*Note: .dp Vision will check the plausibility of the parameter values input by the user. If any value violates the limits, the value will turn red and a warning will appear. The limits may also depend on other user inputs.*

### 2.1.1 GUI limits for basic mode

The Graphical User Interface (GUI) limits define the limits of the output set-points for the usage of the GUI (for the end customer to program different specific parameters of LED drivers) as follows:

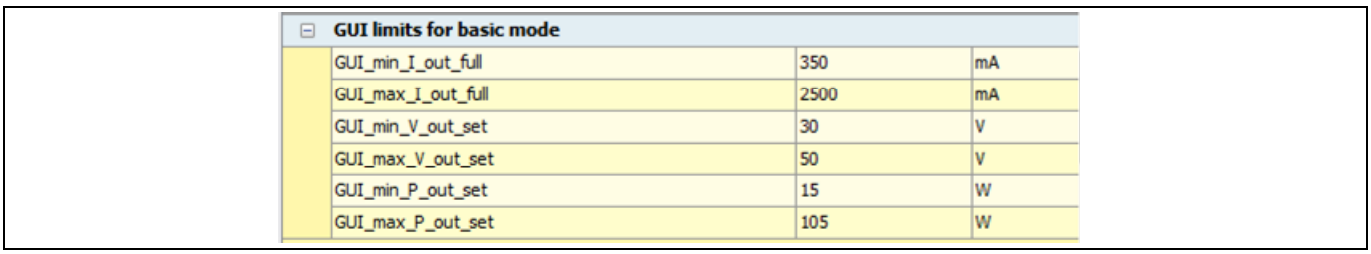



**Figure 1 Limits for the output set-points**

The parameters are described in **Table 1**.

**Table 1 Value limits for the output set-points**

| Parameter | Description | Unit |
|---|---|---|
| GUI_min_I_out_full | The minimum non-dimmed output current set-point for the GUI | mA |
| GUI_max_I_out_full | The maximum non-dimmed output current set-point for the GUI | mA |
| GUI_min_V_out_set | The minimum output voltage set-point for the GUI | V |
| GUI_max_V_out_set | The maximum output voltage set-point for the GUI | V |
| GUI_min_P_out_set | The minimum output power set-point for the GUI | W |
| GUI_max_P_out_set | The maximum output power set-point for the GUI | W |

## 2.1.2 Output set-points

The most prominent feature of the XDPL8221 is that the controller can regulate the output in Constant Current (CC), Constant Voltage (CV) and Limited Power (LP) modes. To configure the CC, CV and LP modes, three parameters are necessary, as shown in Figure 2.

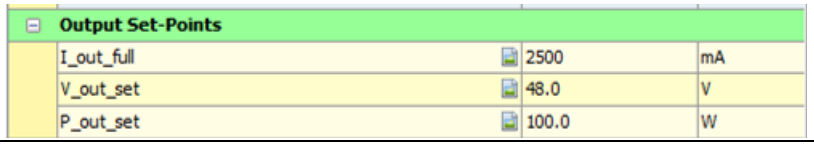



**Figure 2 Output set-point parameters**

The parameters are described in **Table 2** and the corresponding **Figure 3**.

**Table 2 Output set-point parameters**

| Parameter | Description | Unit |
|---|---|---|
| I_out_full | In CC mode: non-dimmed (100 percent) regulated output current value<br>In CV and LP modes: maximum output current value | mA |
| V_out_set | In CV mode: regulated output voltage value<br>In CC and LP modes: maximum output voltage value | V |
| P_out_set | Maximum limited output power value | W |

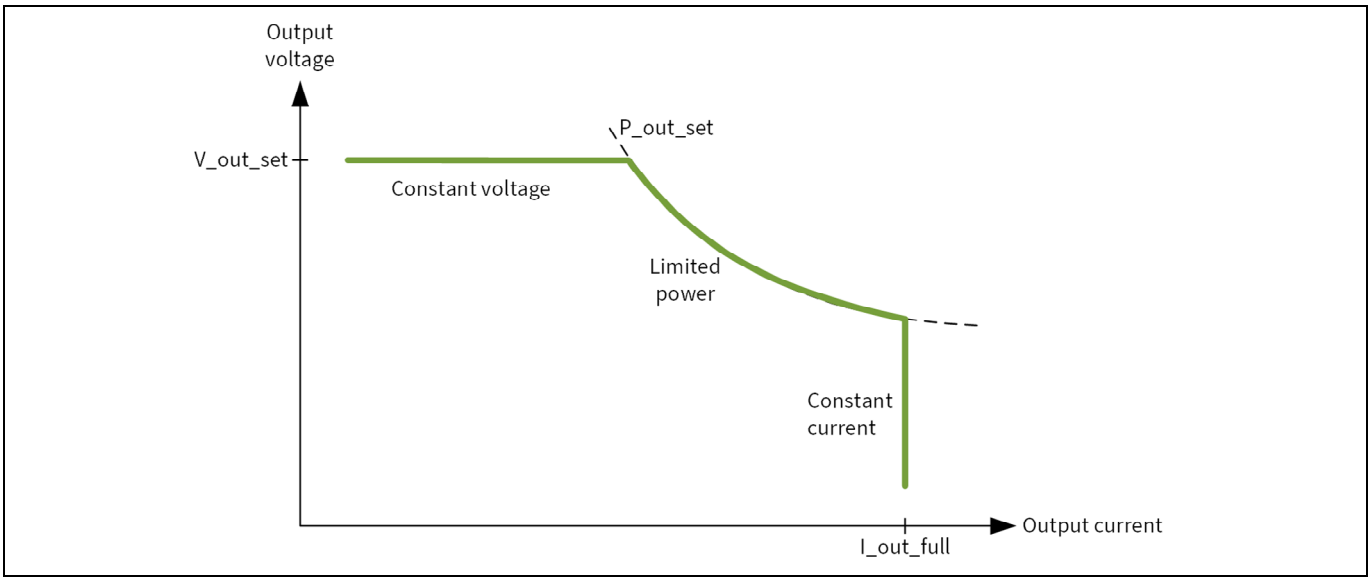



**Figure 3 XDPL8221 CC/CV/LP mode**

### 2.1.3 Hardware configuration

Hardware configurations represent the core board component values that are assembled on the respective application board. The parameters should be entered in the fields as shown.

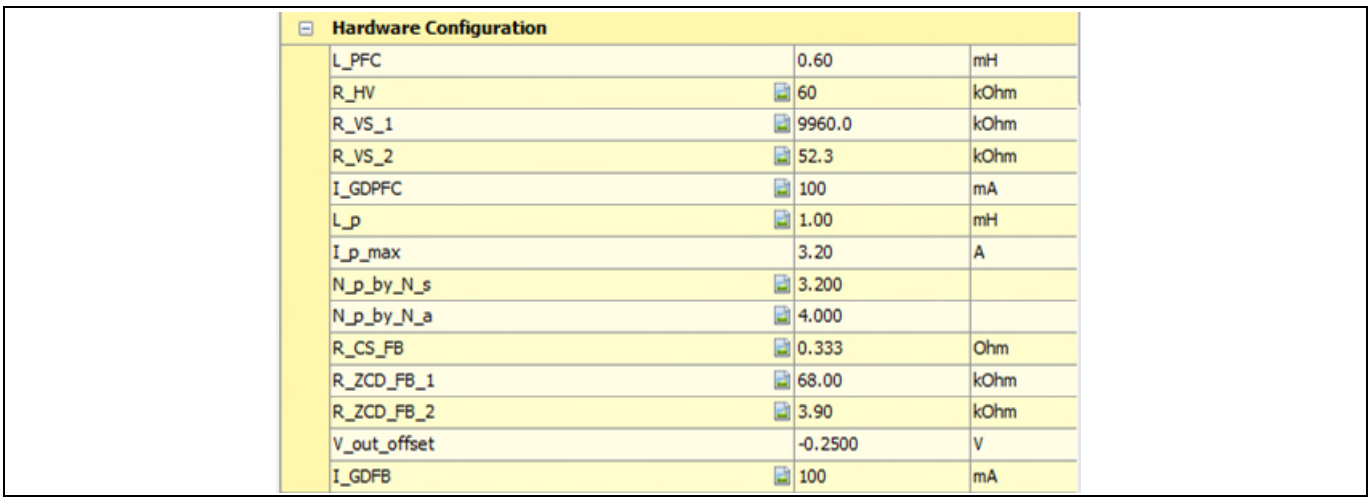



**Figure 4 Hardware configuration parameters**

The parameters are described in **Table 3** and **Figure 5**.

**Table 3 Hardware configuration parameters**

| Parameter | Description | Unit |
|---|---|---|
| L_PFC | PFC choke inductance | mH |
| R_HV | HV resistor value for start-up cell current limitation and AC/DC input voltage sensing | kΩ |
| R_VS_1 | PFC bus voltage sense divider upper resistor value | kΩ |
| R_VS_2 | PFC bus voltage sense divider lower resistor value | kΩ |
| I_GDPFC | PFC gate driver output current when turning on | mA |
| L_p | Flyback transformer primary inductance | mH |
| I_p_max | Flyback maximum primary peak current value | A |
| N_p/N_s | Flyback transformer turns ratio of primary to secondary windings | – |
| N_p/N_a | Flyback transformer turns ratio of primary to auxiliary windings | – |
| R_CS_FB | Flyback Current Sense (CS) resistor value | Ω |
| R_ZCD_FB_1 | Flyback Zero Crossing Detection (ZCD) divider upper resistor value | kΩ |
| R_ZCD_FB_2 | Flyback ZCD divider lower resistor value | kΩ |
| V_out_offset | Output voltage offset to compensate for the voltage drop of the transformer winding and the ZCD resistor's divider tolerance | V |
| I_GDFB | Flyback gate driver output current when turning on | mA |

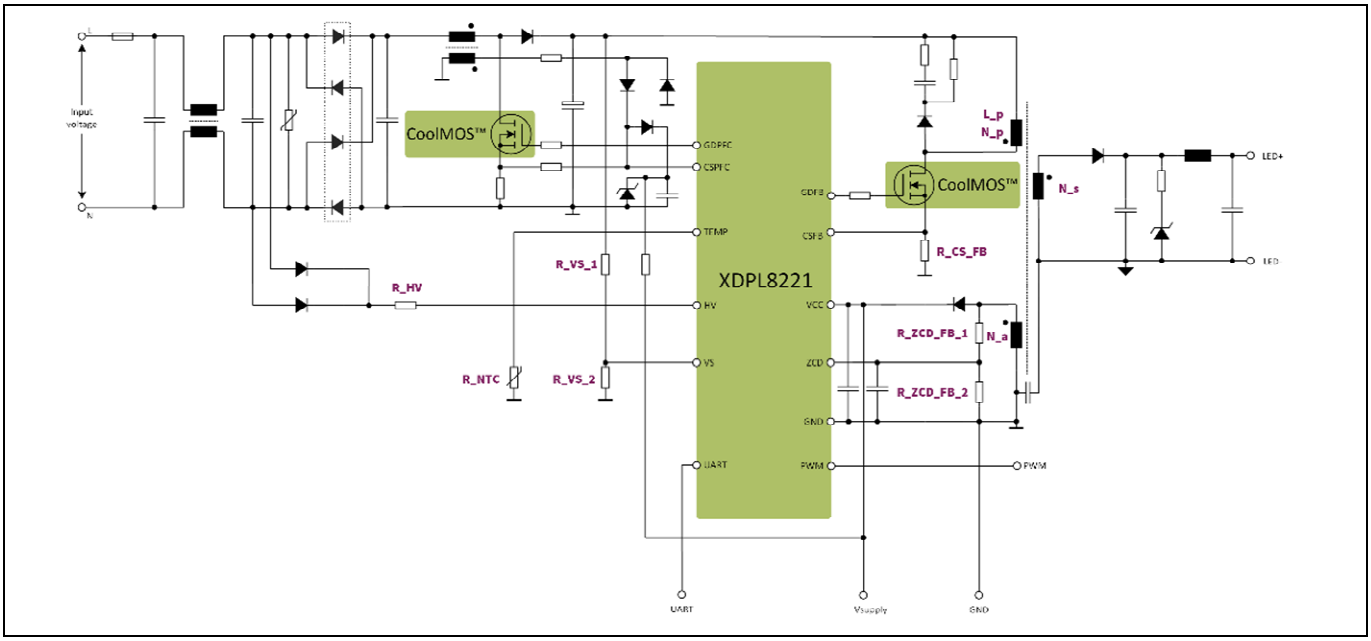



**Figure 5 XDPL8221 typical application schematic**

## 2.1.4 PFC protection

Customers must define PFC protection parameters individually according to their own application requirements in order to protect the PFC core components on the application board.

| PFC Protections | | |
|---|---|---|
| Reaction_V_bus_OVP2 | Auto-Restart | |
| V_bus_OVP1 | 485.0 | V |
| t_start_max_PFC | 400 | ms |
| Reaction_Vin_OV | Auto-Restart | |
| V_in_OV | 320 | Vrms |
| V_in_UV | 71 | Vrms |
| V_in_start_hyst | 12 | Vrms |
| Reaction_PFC_OCP2 | Latch-Mode | |
| V_CS_OCP1_PFC | 0.750 | V |

**Figure 6 PFC protection parameters**

The parameters are described in **Table 4** with the corresponding **Figure 7**.

**Table 4 PFC protection parameters**

| Parameter | Description | Unit |
|---|---|---|
| Reaction_V_bus_OVP2 | Controller reaction to the bus over-voltage level 2 detection:<br>“Fast-Auto-Restart Mode”: controller will be in fast auto-restart mode.<br>“Auto-Restart Mode”: controller will be in auto-restart mode<br>“Latch-Mode”: controller will be in latch mode | – |
| V_bus_OVP1 | Bus over-voltage detection level 1 threshold value.<br>PFC will stop switching if the detection threshold is reached continuously for the defined blanking time (384 µs). Flyback will continue switching. | V |

| Parameter | Description | Unit |
|---|---|---|
| t_start_max_PFC | Maximum PFC soft-start time at start-up.<br>If the defined bus voltage V_bus_steady_entry_UV (see **Table 9**) is not reached within this time, the controller will enter auto-restart mode. | ms |
| Reaction_Vin_OV | Controller reaction to the input over-voltage detection:<br>“Auto-Restart Mode”: controller will be in auto-restart mode<br>“Latch-Mode”: controller will be in latch mode | – |
| V_in_OV | Input over-voltage detection threshold value | V |
| V_in_UV | Input under-voltage detection threshold value | V |
| V_in_start_hyst | Voltage hysteresis between brown-out and brown-in threshold | V |
| Reaction_PFC_OCP2 | Controller reaction to PFC over-current level 2 detection:<br>“Auto-Restart Mode”: controller will be in auto-restart mode<br>“Latch-Mode”: controller will be in latch mode | – |
| V_CS_OCP1_PFC | Maximum voltage at the PFC CS resistor to trigger over-current protection level 1 | V |

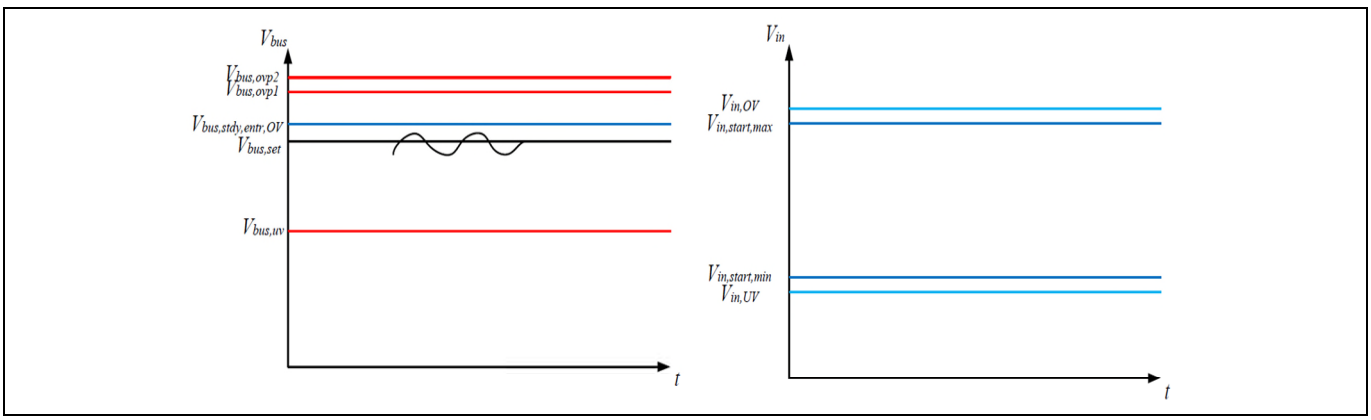
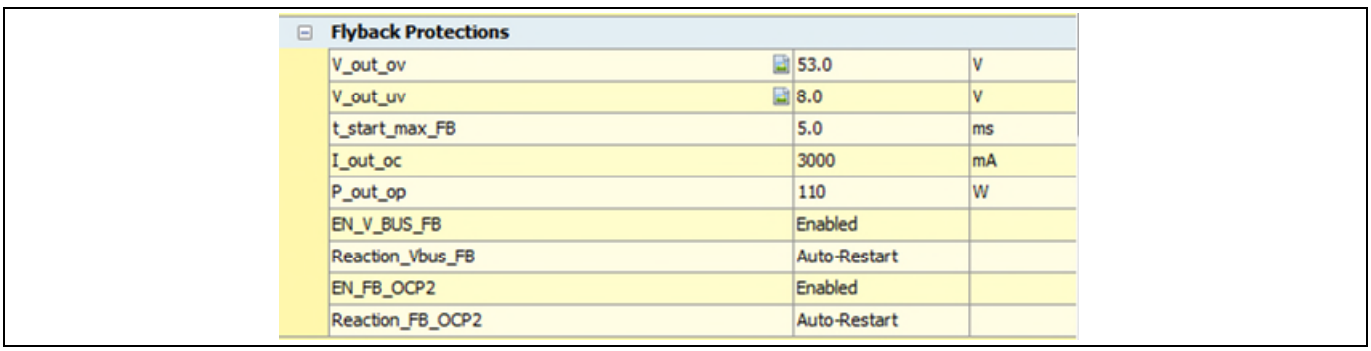



**Figure 7 PFC protection description**

## 2.1.5 Flyback protection

Flyback protection parameters must be defined individually for specific application requirements in order to protect the core flyback components on the application board.



| Flyback Protections | | |
|---|---|---|
| V_out_ov | 53.0 | V |
| V_out_uv | 8.0 | V |
| t_start_max_FB | 5.0 | ms |
| I_out_oc | 3000 | mA |
| P_out_op | 110 | W |
| EN_V_BUS_FB | Enabled | |
| Reaction_Vbus_FB | Auto-Restart | |
| EN_FB_OCP2 | Enabled | |
| Reaction_FB_OCP2 | Auto-Restart | |

**Figure 8 Flyback protection parameters**

The flyback protection parameters are described in **Table 5** with the corresponding **Figure 9**.

**Table 5 Flyback protection parameters**

| Parameter | Description | Unit |
|---|---|---|
| V_out_ov | Output over-voltage detection threshold.<br>If the output over-voltage detection threshold is reached for the blanking time, the controller will enter auto-restart mode. | V |
| V_out_uv | Output under-voltage detection threshold.<br>If the output under-voltage detection threshold is reached for the blanking time, the controller will enter auto-restart mode. | V |
| t_start_max_FB | Maximum flyback start-up time in order to detect an output short at start-up | ms |
| I_out_OC | Output over-current detection threshold value.<br>If the output over-current detection threshold is reached for the blanking time, the controller will enter auto-restart mode. | A |
| P_out_OP | Output over-power detection threshold value.<br>If the output over-power detection threshold is reached for the blanking time, the controller will enter auto-restart mode. | W |
| EN_V_BUS_FB | To enable the bus voltage plausibility check through the flyback stage:<br>Enabled: bus voltage check by flyback feature is enabled<br>Disabled: bus voltage check by flyback feature is disabled | - |
| Reaction_Vbus_FB | Controller reaction to the bus voltage plausibility check error:<br>“Auto-Restart”: controller will enter auto-restart mode<br>“Latch-Mode”: controller will enter latch mode | - |
| EN_FB_OCP2 | To enable the flyback over-current protection level 2 detection:<br>Enabled: over-current protection level 2 is enabled<br>Disabled: over-current protection level 2 is disabled | - |
| Reaction_FB_OCP2 | Controller reaction to the flyback over-current protection level 2 detection:<br>“Auto-Restart”: controller will enter auto-restart mode<br>“Latch-Mode”: controller will enter latch mode | - |

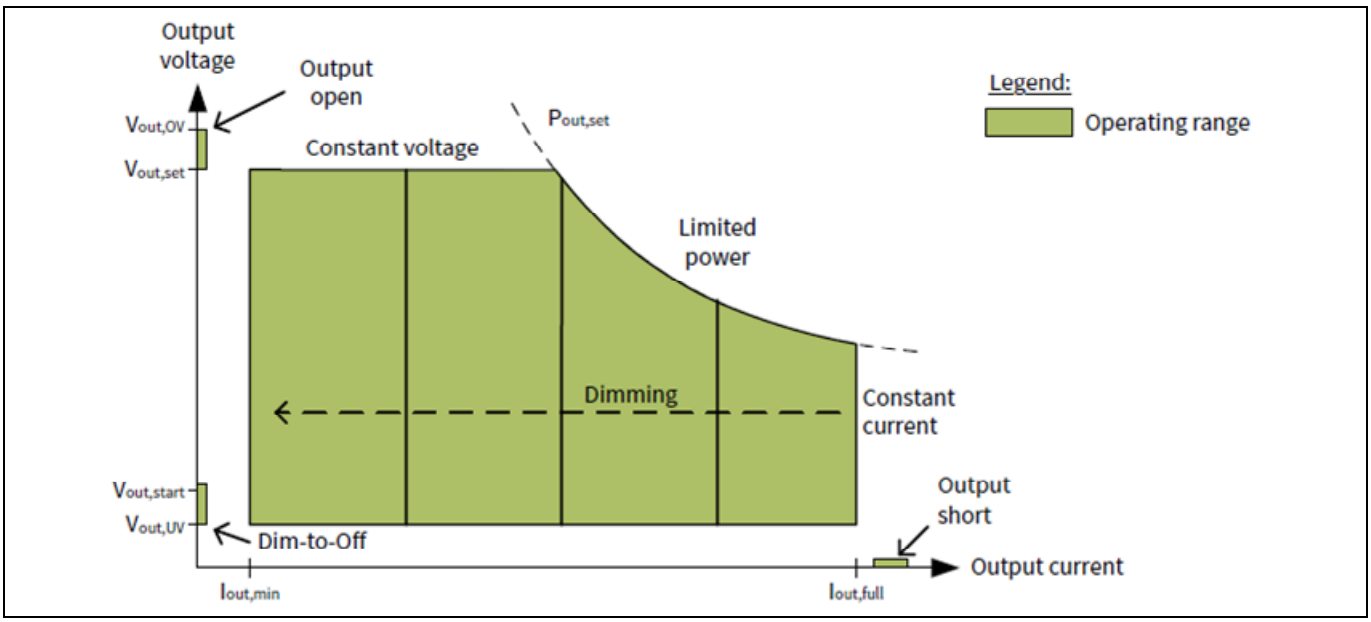



**Figure 9 Flyback protection description**

## 2.1.6 Adaptive temperature protection

This section allows the user to set the values and reactions for temperature protection. It is necessary to enter temperature threshold values that define the device's behavior regarding operating temperature conditions. In addition to the conventional over-temperature protection, the XDPL8221 also features an external advanced adaptive temperature protection.

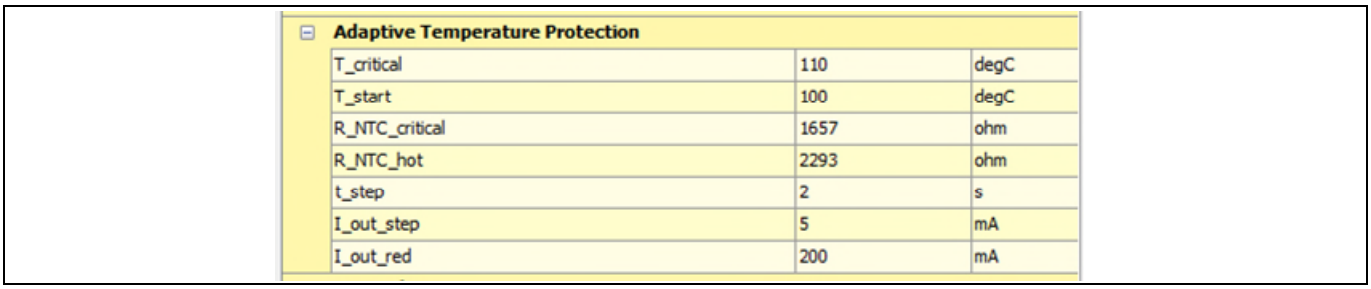



**Figure 10 Adaptive temperature protection parameters**

The parameters are described in **Table 6**, **Figure 11** and **Figure 12**.

**Table 6 Adaptive temperature protection parameters**

| Parameter | Description | Unit |
|---|---|---|
| T_critical | Defines the internal over-temperature protection threshold. If the internal temperature reaches this threshold, the internal over-temperature protection is activated and the controller will react with a defined protection mode. | °C |
| T_start | Defines the internal recovery temperature threshold. After the internal over-temperature protection is triggered, when the internal temperature drops back to this threshold, the controller will return to normal operation. | °C |
| R_NTC_critical | Defines the external NTC resistor value threshold. If the connected external NTC resistor value reaches this threshold, the external temperature protection is activated and the controller will react with a defined protection mode. | Ω |
| R_NTC_hot | Defines the external NTC resistor value threshold. If the connected external NTC resistor value reaches this threshold, the adaptive temperature protection is activated with thermal management reaction. | Ω |
| t_step | Thermal management: time step for each output current change | s |
| I_out_step | Thermal management: output current step change | A |
| I_out_red | Thermal management: lowest output current value that can be reached while reducing current | A |

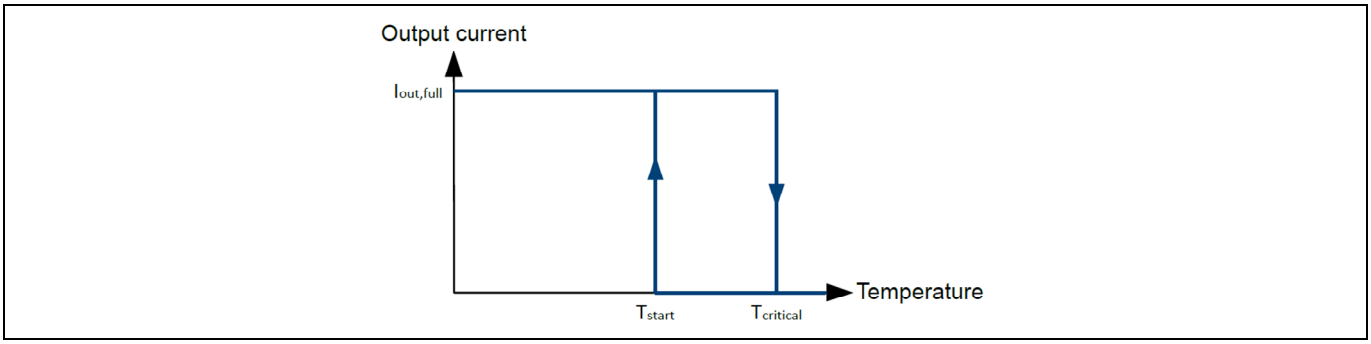



**Figure 11 Over-temperature protection parameters description**

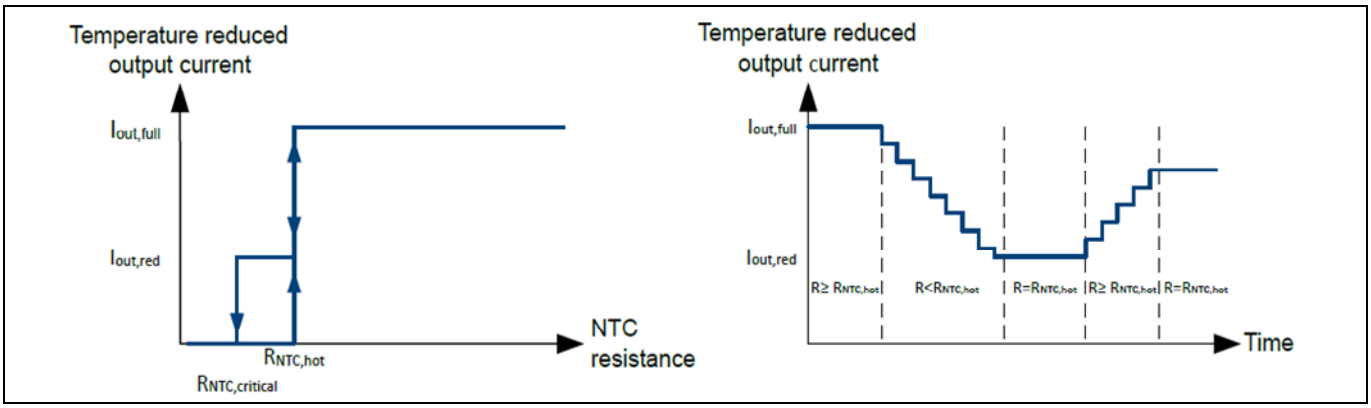



**Figure 12 Adaptive temperature protection parameters description**

## 2.1.7 General protection

General protection parameters set the different global protection features.

| General Protections | | |
|---|---|---|
| EN_VCC_Undervoltage | Disabled | |
| VCC_ov | 24.8 | V |
| VCC_uv | 9.6 | V |
| t_AR | 1.00 | s |
| t_AR_fast | 0.400 | s |
| N_AR_max | 10 | |
| Debug_Mode | Disabled | |

**Figure 13 General protection parameters**

The parameters are described in **Table 7** and **Figure 14**.

**Table 7 General protection parameters**

| Parameter | Description | Unit |
|---|---|---|
| EN_VCC_Undervoltage | To enable the $V_{CC}$ under-voltage protection. The controller will enter auto-restart mode if the threshold VCC_UV is reached.<br>Enabled: the $V_{CC}$ under-voltage protection feature is enabled.<br>Disabled: the $V_{CC}$ under-voltage protection feature is disabled. | – |
| VCC_ov | $V_{CC}$ over-voltage threshold | V |
| VCC_uv | $V_{CC}$ under-voltage threshold | V |
| t_AR | Auto-restart time defines the duration in the controller protection mode auto-restart.<br>It starts at the moment the controller stops operation until the next restart. | s |
| t_AR_fast | Fast auto-restart time defines the duration in the controller protection mode fast auto-restart.<br>It starts at the moment the controller stops operation until the next restart. | s |
| N_AR_max | Maximum number of restarts in case of any limited number of restarts for any protection. After this number of restarts, the controller will latch. | – |

| Parameter | Description | Unit |
|---|---|---|
| Debug_Mode | Debug mode switches all protections to stop mode.<br>“Disabled”: controller will enter corresponding defined mode in case of protection.<br>“Enabled”: Controller will enter stop mode in case of any protection. | – |

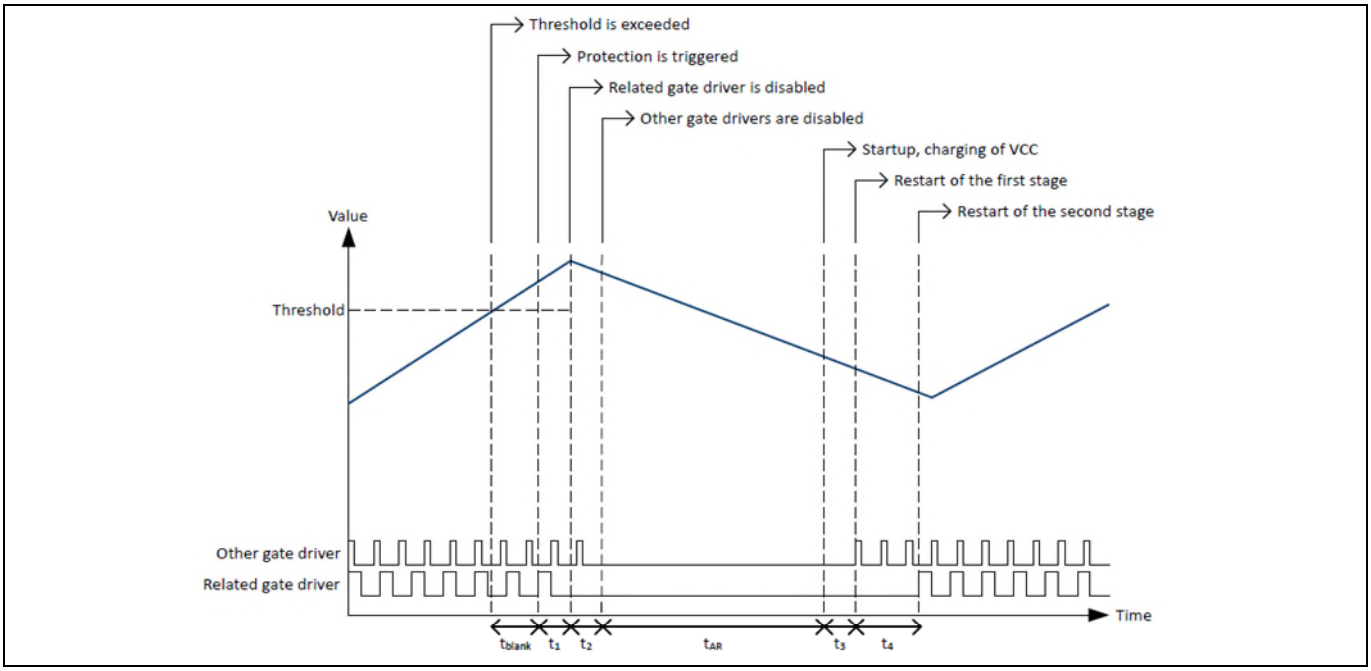



**Figure 14 General protection parameters description**

## 2.1.8 Start-up and shut-down

The parameters in this section define the start-up and end conditions for both the PFC and FB stages.

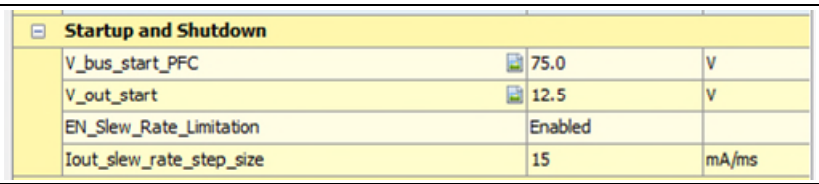



**Figure 15 Start-up and shut-down parameters**

The parameters are described in **Table 8** and **Figure 16**.

**Table 8 Start-up and shut-down parameters**

| Parameter | Description | Unit |
|---|---|---|
| V_bus_start_PFC | Bus voltage threshold value. The PFC soft-start is executed when the bus voltage is higher than this threshold. | V |
| V_out_start | Output voltage threshold value. After the output voltage reaches this threshold, control loop is activated and start-up is finished. | V |

| Parameter | Description | Unit |
|---|---|---|
| En_Slew_Rate_Limitation | To enable the slew rate limitation for flyback output current:<br>Enabled: the slew rate limitation is enabled<br>Disabled: the slew rate limitation is disabled | – |
| Iout_slew_rate_step_size | Limit for the rising slew rate of the output current | mA/ms |

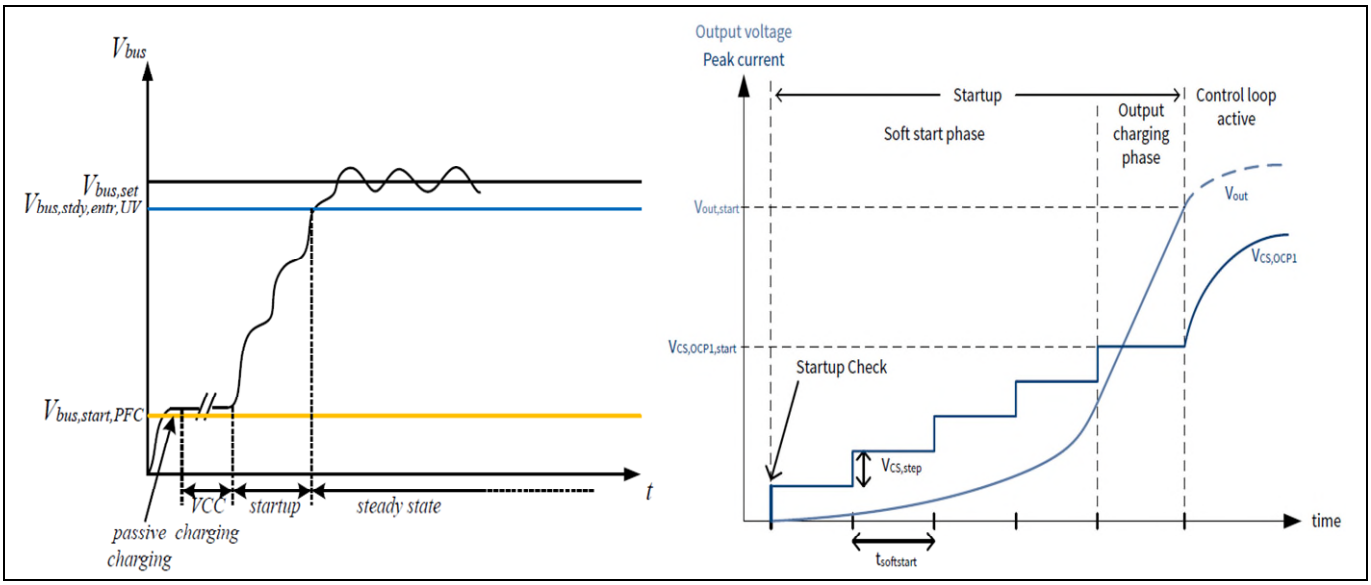
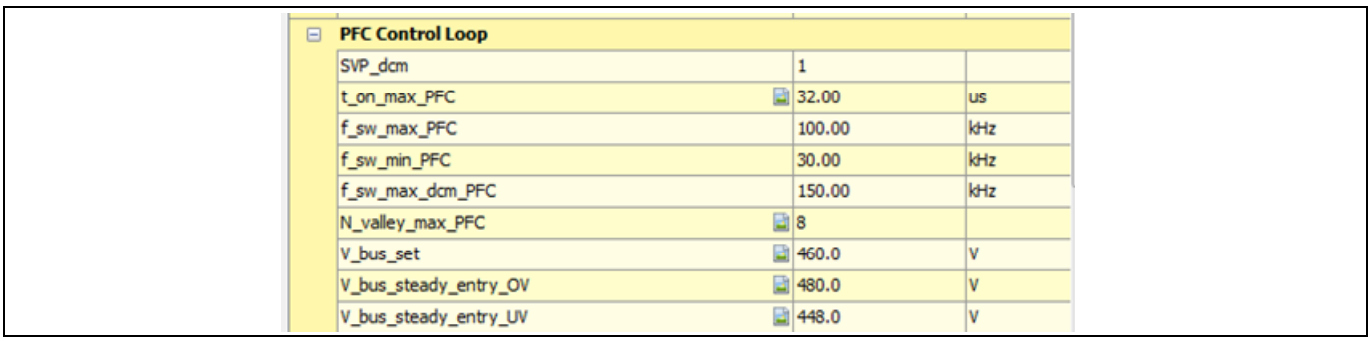



**Figure 16 Start-up and shut-down parameters description**

## 2.1.9 PFC control loop

PFC control loop parameters determine PFC behavior in operation.



| PFC Control Loop | | |
|---|---|---|
| SVP_dcm | 1 | |
| t_on_max_PFC | 32.00 | us |
| f_sw_max_PFC | 100.00 | kHz |
| f_sw_min_PFC | 30.00 | kHz |
| f_sw_max_dcm_PFC | 150.00 | kHz |
| N_valley_max_PFC | 8 | |
| V_bus_set | 460.0 | V |
| V_bus_steady_entry_OV | 480.0 | V |
| V_bus_steady_entry_UV | 448.0 | V |

**Figure 17 PFC control loop parameters**

The parameters are described in **Table 9** and **Figure 18**.

**Table 9 PFC control loop parameters**

| Parameter | Description | Unit |
|---|---|---|
| SVP_dcm | PFC regulator proportional gain in DCM | – |
| t_on_max_PFC | PFC maximum on-time limit | µs |
| f_sw_max_PFC | PFC maximum switching frequency | kHz |
| f_sw_min_PFC | PFC minimum switching frequency | kHz |

| Parameter | Description | Unit |
|---|---|---|
| f_sw_max_dcm_PFC | PFC maximum switching frequency in DCM | kHz |
| N_valley_max_PFC | The maximum possible PFC switching valley | – |
| V_bus_set | Bus voltage set-point | V |
| V_bus_steady_entry_OV | Bus voltage steady-state entry over-voltage threshold:<br>After the bus OVP1 protection is triggered, normal PFC operation is resumed when bus voltage falls below this threshold. | V |
| V_bus_steady_entry_UV | Bus voltage steady-state entry under-voltage threshold:<br>Once this threshold is reached, PFC soft-start is finished and the steady-state PFC operation starts. | V |

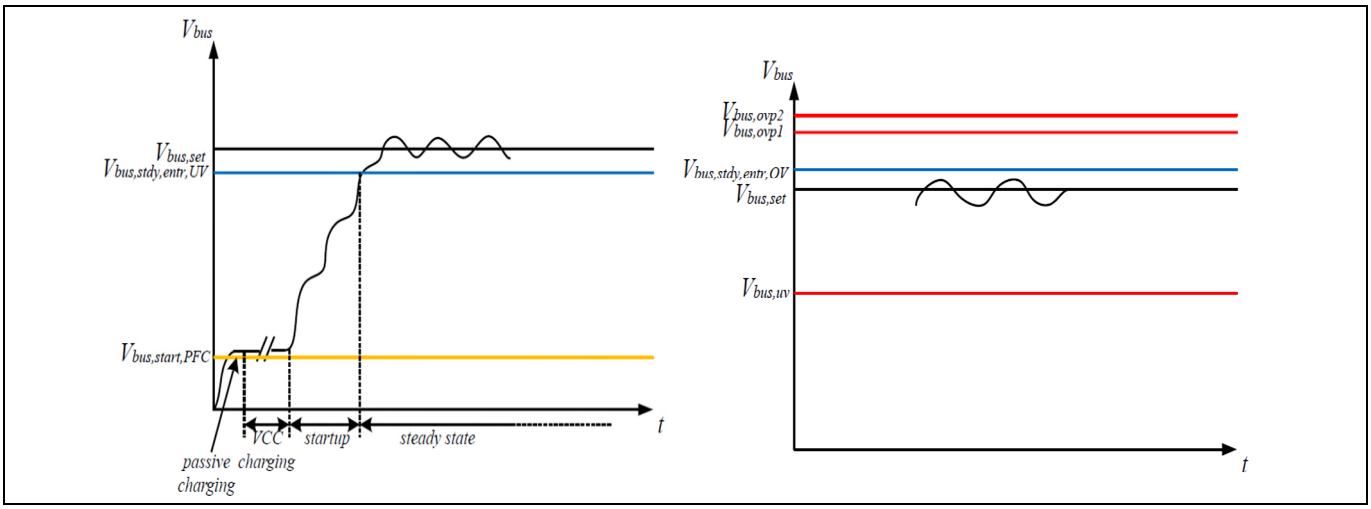
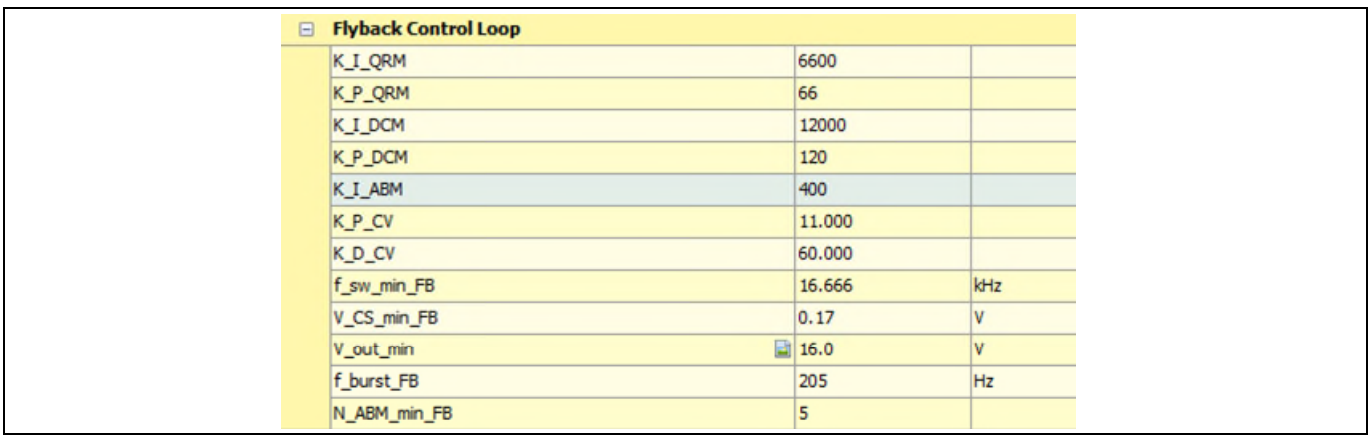



**Figure 18 PFC control loop parameters description**

## 2.1.10 Flyback control loop

Flyback control loop parameters determine the flyback behavior.



| Flyback Control Loop | | |
|---|---|---|
| K_I_QRM | 6600 | |
| K_P_QRM | 66 | |
| K_I_DCM | 12000 | |
| K_P_DCM | 120 | |
| K_I_ABM | 400 | |
| K_P_CV | 11.000 | |
| K_D_CV | 60.000 | |
| f_sw_min_FB | 16.666 | kHz |
| V_CS_min_FB | 0.17 | V |
| V_out_min | 16.0 | V |
| f_burst_FB | 205 | Hz |
| N_ABM_min_FB | 5 | |

**Figure 19 Flyback control loop parameters**

The parameters are described in **Table 10** and **Figure 20**.

**Table 10 Flyback control loop parameters**

| Parameter | Description | Unit |
|---|---|---|
| K_I_QRM | Integral gain of the control loop in QRM. Typically, a good value is 100*K_P_QRM. | – |
| K_P_QRM | Proportional gain of the control loop in QRM | – |
| K_I_DCM | Integral gain of the control loop in DCM. Typically, a good value is 100*K_P_DCM. | – |
| K_P_DCM | Proportional gain of the control loop in DCM | – |
| K_I_ABM | Integral gain of the control loop in ABM | – |
| K_P_CV | Proportional gain for CV mode | – |
| K_D_CV | Derivative gain for CV mode | – |
| f_sw_min_FB | Minimum switching frequency of flyback converter | kHz |
| V_CS_min_FB | Minimum primary peak current converted to voltage at the shunt resistor. Decrease to achieve lower output current (a wider dimming range). Increase in case of instabilities due to ringing at the CSFB pin. | V |
| V_out_min | Minimum output voltage | V |
| f_burst_FB | Burst frequency in Active Burst Mode (ABM) | Hz |
| N_ABM_min_FB | Minimum number of pulses in the ABM | – |

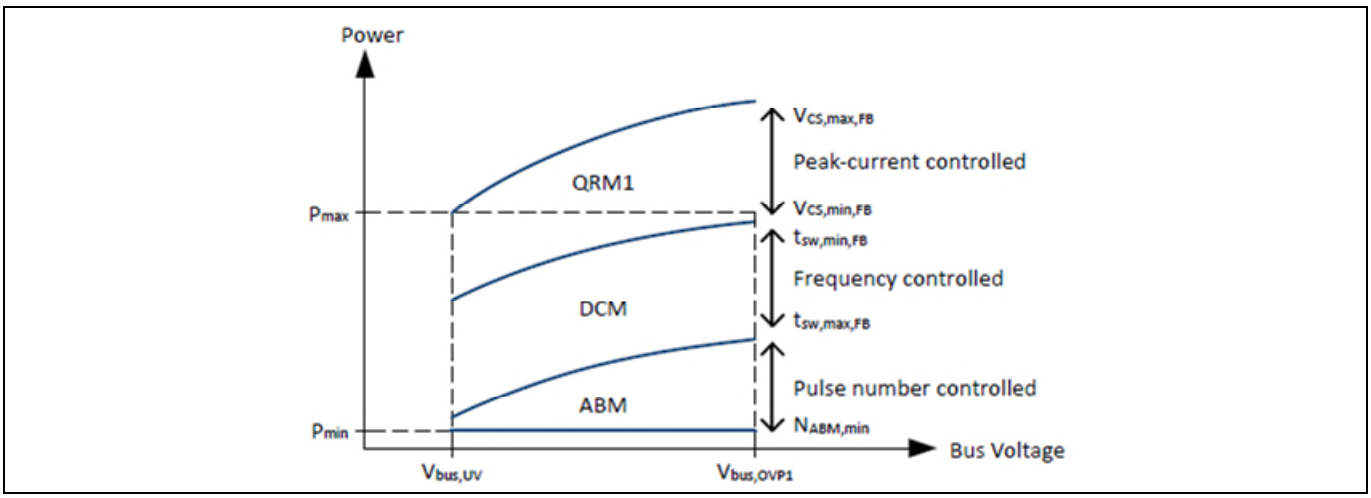



**Figure 20 Flyback control loop parameters description**

## 2.1.11 Dimming

This section enables users to define parameters related to the dimming function. The digital controller XDPL8221 will set the analog output current level according to the measured PWM duty cycle at the PWM pin.

The human eye is subject to the logarithm of light power (Weber-Fechner law). As a consequence, the quadratic dimming curve on the right of **Figure 22** creates a dimming experience comparable to the human eye. It is therefore recommended to use this in combination with, for example, 0 to 10 V wall dimmers. The linear curve on the left of **Figure 22** can also be selected if the dimming voltage is provided by an external source (e.g. a microcontroller for DALI).

For applications in which no hard wall switch is available to turn off the light completely, the XDPL8221 provides a dim-to-off feature. If enabled, the XDPL8221 will turn off the output current if a duty cycle lower than D_DIM_off is sensed. The output current will be turned on again if the dimming voltage exceeds D_DIM_min again.

### Parameter handling/recommendations

In most applications, the dimmer is supplied by the other separated isolated output of the LED driver (e.g. a current-sink dimmer). This requires maintaining a minimum output voltage to provide power to the dimmer. The XDPL8221 includes a feature that can maintain the output voltage at a programmable level $V_{out,start}$ while the driver is in the dim-to-off state. The driver will recharge the output to this voltage level every ms.

*Note: The dim-to-off feature with maintenance of output voltage requires an active bleeder circuit.*

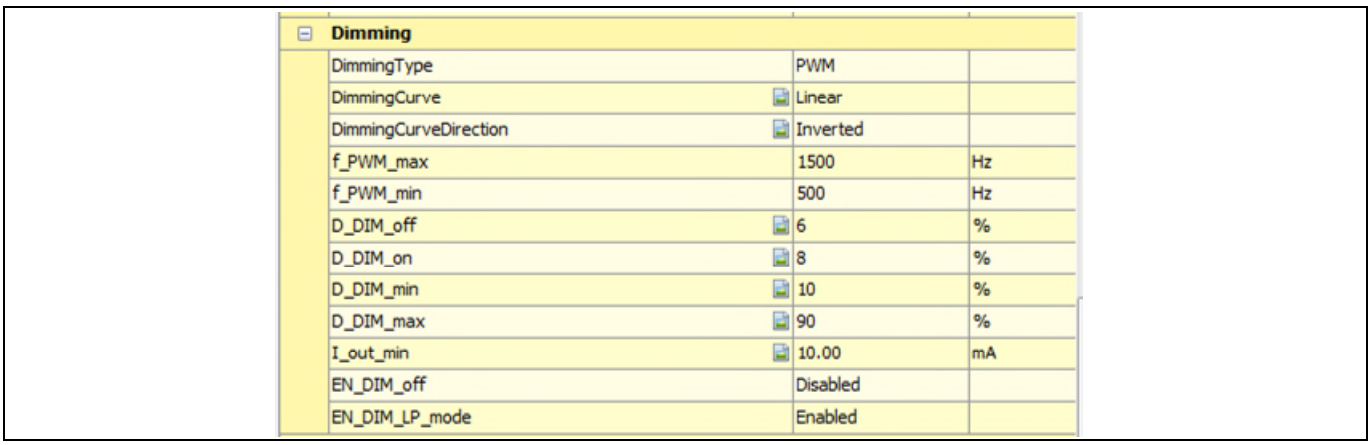



**Figure 21 Dimming parameters**

The parameters are described in **Table 11** and **Figure 22**.

**Table 11 Dimming parameters**

| Parameter | Description | Unit |
|---|---|---|
| Dimming type | Dimming determined by:<br>“PWM”: PWM dimming is enabled<br>“UART”: UART dimming is enabled | – |
| Dimming curve | Dimming curve shape:<br>“Linear”<br>“Eye-Adapted” | – |
| Dimming curve direction | Direction of the dimming curve:<br>“Normal”<br>“Inverted” | – |
| f_PWM_max | Maximum frequency of the dimming PWM signal | Hz |
| f_PWM_min | Minimum frequency of the dimming PWM signal | Hz |
| D_DIM_off | Threshold for the PWM dimming duty cycle:<br>If this threshold is reached, the XDPL8221 will enter dim-to-off mode. | % |
| D_DIM_on | Threshold for the PWM dimming duty cycle:<br>If the XDPL8221 is in the dim-to-off mode and this threshold is reached, XDPL8221 will wake up and output the minimum output current. | % |
| D_DIM_min | Threshold for the PWM dimming duty cycle that maps to the minimum current | % |
| D_DIM_max | Threshold for the PWM dimming duty cycle that maps to the full current defined in the output set-points section | % |

| Parameter | Description | Unit |
|---|---|---|
| I_out_min | Minimum output current in dimmed mode | mA |
| EN_DIM_off | To enable the dim-to-off feature:<br>Enabled: the dim-to-off feature is enabled<br>Disabled: the dim-to-off feature is disabled | – |
| EN_DIM_LP_mode | Enable dimming of limited power mode:<br>The limited maximum possible current value in the limited power mode will be mapped to the D_DIM_max | – |

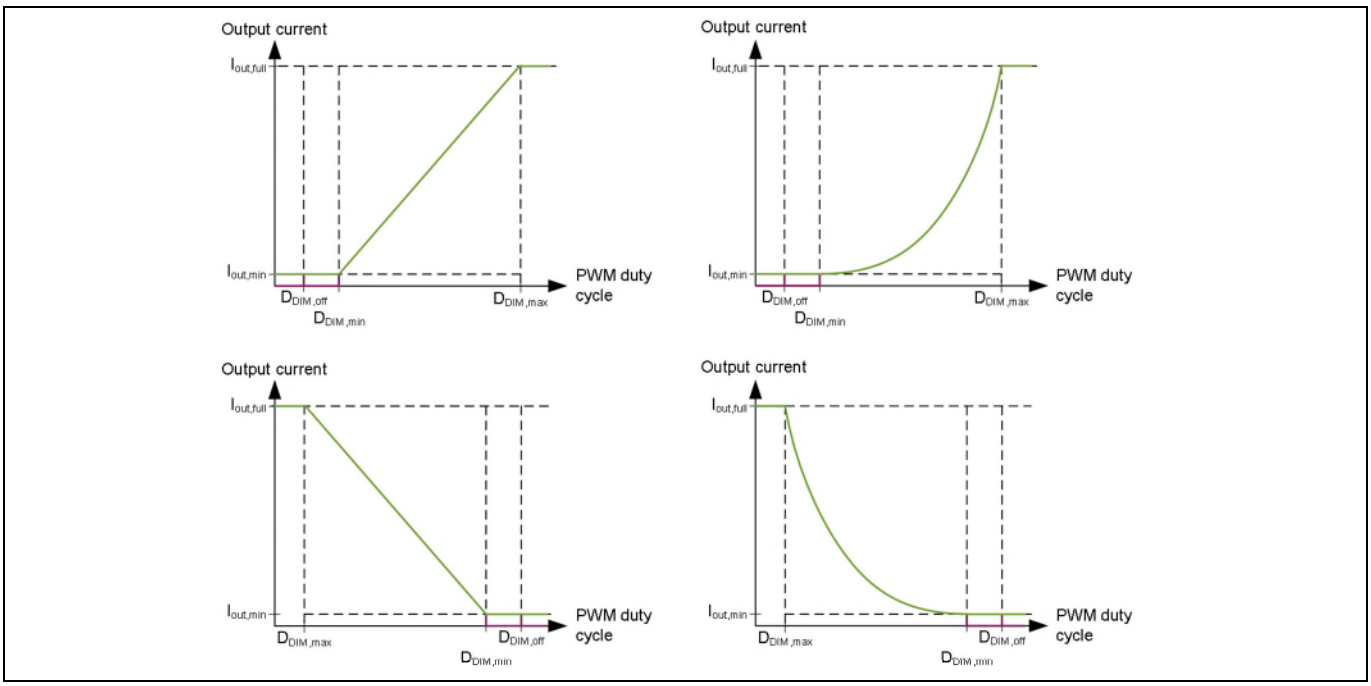



**Figure 22 Dimming parameters description**

## 2.1.12 UART communication interface

This section defines the parameters of the UART communication interface.

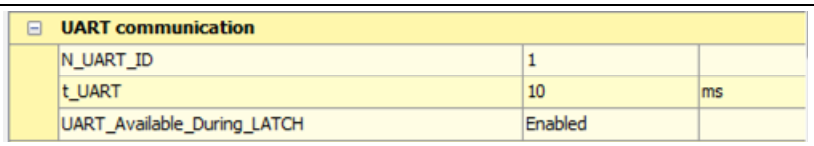



**Figure 23 UART communication interface parameters**

The parameters of UART communication interface are described in **Table 12**.

**Table 12 UART communication interface parameters**

| Parameter | Description | Unit |
|---|---|---|
| N_UART_ID | The unique UART ID of the XDPL8221 for addressing | – |
| t_UART | UART time-out:<br>After the XDPL8221 is woken up from sleep mode (e.g. auto-restart, | ms |

| Parameter | Description | Unit |
|---|---|---|
| | latch, dim-to-off) through the UART command SYNC successfully, further UART communication must be finished within this defined value, or the controller will go back to sleep mode. | |
| UART_Available_During _LATCH | Enable UART communication when the XDPL8221 is in latch mode | – |

### 2.1.13 Fine-tuning parameters

The fine-tuning parameters compensate for the parasitic elements of the hardware that affect the accuracy of the system. They enable better performance of the target application. For more information about how to calculate these parameters, please refer to the XDPL8221 design guide for the 100 W reference board.

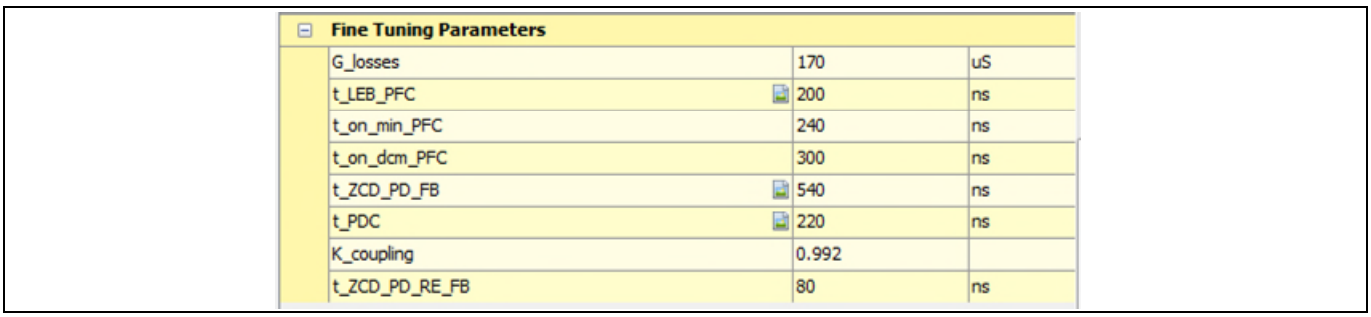



**Figure 24 Fine-tuning parameters**

The fine tuning parameters are described in **Table 13** and **Figure 25**.

**Table 13 Fine-tuning parameters**

| Parameter | Description | Unit |
|---|---|---|
| G_losses | Conductivity of lumped loss at the flyback output, which compensates for the power transfer loss from the primary to the secondary side for the accuracy of the primary-side regulation | µs |
| t_LEB_PFC | PFC converter:<br>CS leading-edge blanking | ns |
| t_on_min_PFC | Minimum on-time limit for the PFC regulator | ns |
| t_on_dcm_PFC | PFC regulator on-time for DCM entry | ns |
| t_ZCD_PD_FB | Flyback converter:<br>Delay of the zero-crossing signal. Tune this parameter to achieve switching of the flyback at the valley of the auxiliary voltage. This value influences the accuracy of the output current. | ns |
| t_PDC | Flyback converter:<br>Propagation delay compensation. Tune this parameter to eliminate any output current regulation error due to a variation of bus voltage. | ns |
| K_coupling | Flyback converter:<br>Transformer coupling coefficient. Tune this parameter to eliminate any offset error between measured output current and the values set in this GUI. | – |
| t_ZCD_PD_RE_FB | Flyback converter: | ns |

| Parameter | Description | Unit |
|---|---|---|
| | Rising-edge delay of the zero-crossing signal. Tune this parameter to optimize the output current accuracy with respect to output voltage regulation. | |

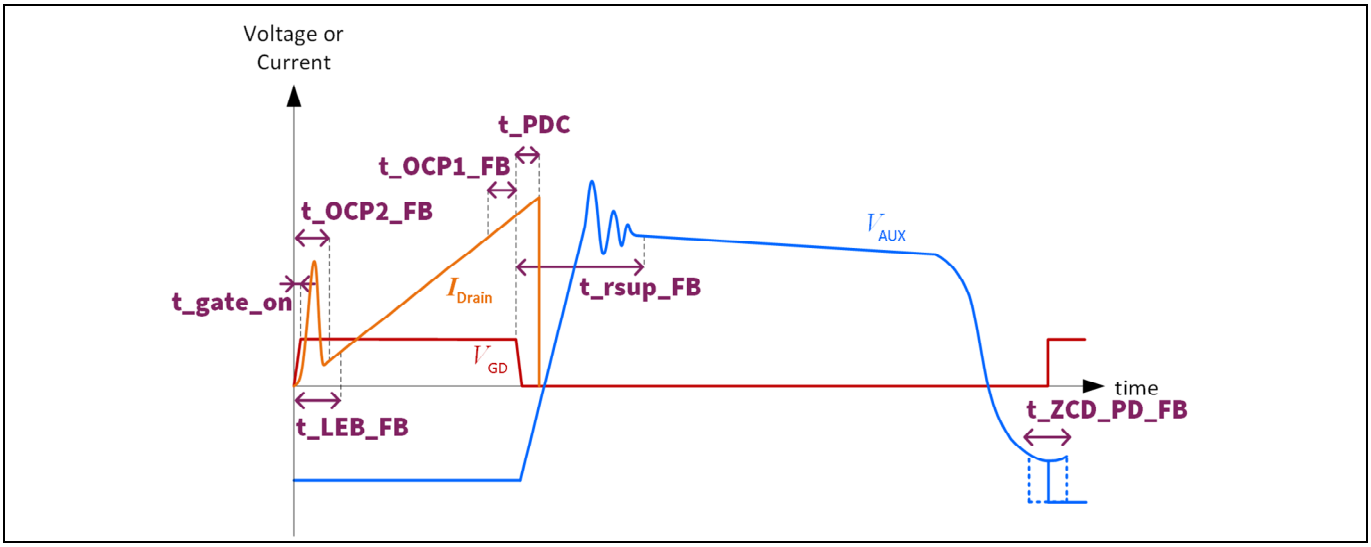



**Figure 25 Fine-tuning parameters description**

# 3 Default parameter values for XDPL8221 100 W reference board

The following table gives the default parameter values for the 100 W reference board.

**Table 14 Default parameter values for 100 W reference board**

| Parameter | Value | Unit |
|---|---|---|
| **GUI limits** | | |
| GUI_min_I_out_full | 350 | mA |
| GUI_max_I_out_full | 2500 | mA |
| GUI_min_V_out_set | 30 | V |
| GUI_max_V_out_set | 50 | V |
| GUI_min_P_out_set | 15 | W |
| GUI_max_P_out_set | 100 | W |
| **Output set-points** | | |
| I_out_full | 2500 | mA |
| V_out_set | 48 | V |
| P_out_set | 100 | W |
| **Hardware configuration** | | |
| L_PFC | 0.6 | mH |
| R_HV | 60 | kΩ |
| R_VS_1 | 9960 | kΩ |
| R_VS_2 | 52.3 | kΩ |
| I_GDPFC | 100 | mA |
| Lp | 1 | mH |
| I_p_max | 3.2 | A |
| N_p/N_s | 3.2 | – |
| N_p/N_a | 4.0 | – |
| R_CS_FB | 0.333 | Ω |
| R_ZCD_FB_1 | 68 | kΩ |
| R_ZCD_FB_2 | 3.9 | kΩ |
| V_out_offset | -0.25 | V |
| I_GDFB | 100 | mA |
| **PFC protection** | | |
| Reaction_V_bus_OVP2 | Auto-restart | – |
| V_bus_OVP1 | 485 | V |
| t_start_max_PFC | 400 | ms |
| Reaction_Vin_OV | Auto-restart | – |
| V_in_OV | 320 | Vrms |

**Default parameter values for XDPL8221 100 W reference board**

| Parameter | Value | Unit |
|---|---|---|
| V_in_UV | 71 | Vrms |
| V_in_start_hyst | 12 | Vrms |
| Reaction_PFC_OCP2 | Latch mode | – |
| V_CS_OCP1_PFC | 0.75 | V |
| **Flyback protection** | | |
| V_out_OV | 53 | V |
| V_out_UV | 8 | V |
| t_start_max_FB | 5 | ms |
| I_out_OC | 3000 | mA |
| P_out_OP | 110 | W |
| EN_V_BUS_FB | Enabled | – |
| Reaction_VBus_FB | Auto-restart | – |
| EN_FB_OCP2 | Enabled | – |
| Reaction_FB_OCP2 | Auto-restart | – |
| **Adaptive temperature protection** | | |
| T_critical | 110 | °C |
| T_start | 100 | °C |
| R_NTC_critical | 1657 | Ω |
| R_NTC_hot | 2293 | Ω |
| t_step | 2 | s |
| I_out_step | 5 | mA |
| I_out_red | 200 | mA |
| **General protection** | | |
| EN_VCC_Undervoltage | Disabled | – |
| VCC_OV | 24.8 | V |
| VCC_UV | 9.6 | V |
| t_AR | 1 | s |
| t_AR_fast | 0.4 | s |
| N_AR_max | 10 | – |
| Debug_Mode | Disabled | – |
| **Start-up and shut-down** | | |
| V_bus_start_PFC | 75 | V |
| V_out_start | 12.5 | V |
| EN_slew_rate_limitation | Enabled | – |
| Iout_slew_rate_sleep_size | 15 | mA/ms |

**Default parameter values for XDPL8221 100 W reference board**

| Parameter | Value | Unit |
|---|---|---|
| **PFC control loop** | | |
| SVP_dcm | 1 | – |
| t_on_max_PFC | 32 | us |
| f_sw_max_PFC | 100 | kHz |
| f_sw_min_PFC | 30 | kHz |
| f_sw_max_dcm_PFC | 150 | kHz |
| N_valley_max_PFC | 8 | – |
| V_bus_set | 460 | V |
| V_bus_steady_entry_OV | 480 | V |
| V_bus_steady_entry_UV | 448 | V |
| **Flyback control loop** | | |
| K_I_QRM | 6600 | – |
| K_P_QRM | 66 | – |
| K_I_DCM | 12000 | – |
| K_P_DCM | 120 | – |
| K_I_ABM | 400 | – |
| K_P_CV | 11000 | – |
| K_D_CV | 60000 | – |
| f_sw_min_FB | 16.666 | kHz |
| V_CS_min_FB | 0.17 | V |
| V_out_min | 16 | V |
| f_burst_FB | 205 | Hz |
| N_ABM_min_FB | 5 | – |
| **Dimming** | | |
| DimmingType | PWM | – |
| DimmingCurve | Linear | – |
| DimmingCurveDirection | Inverted | – |
| f_PWM_max | 1500 | Hz |
| f_PWM_min | 500 | Hz |
| D_DIM_off | 6 | % |
| D_DIM_on | 8 | % |
| D_DIM_min | 10 | % |
| D_DIM_max | 90 | % |
| I_out_min | 10 | mA |
| EN_DIM_off | Disabled | – |
| En_DIM_LP_Mode | Enabled | – |

**Default parameter values for XDPL8221 100 W reference board**

| Parameter | Value | Unit |
|---|---|---|
| **UART communication interface** | | |
| N_UART_ID | 1 | – |
| t_UART | 10 | ms |
| UART_Available_During _LATCH | Enabled | – |

| **Fine-tuning parameters** | | |
|---|---|---|
| G_losses | 170 | µs |
| t_LEB_PFC | 200 | ns |
| t_on_min_PFC | 240 | ns |
| t_on_dcm_PFC | 300 | ns |
| t_ZCD_PD_FB | 540 | ns |
| t_PDC | 220 | ns |
| K_coupling | 0.992 | – |
| t_ZCD_PD_RE_FB | 80 | ns |

# 4 References

[1] XDPL8221 Datasheet

[2] XDPL8221 100 W Reference Board Description

[3] .dp Vision Basic Mode User Manual

[4] XDPL8221 Design Guide

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 1.1 | 2023-03-10 | Editorial changes |
| 1.0 | 2018-10-12 | Initial version |
| | | |

**Trademarks**
All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2023-03-10**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



**Do you have a question about this document?**

**Email:** erratum@infineon.com

**Document reference**
**AN_201711_PL39_006**

**IMPORTANT NOTICE**

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:
REFXDPL8221U100WTOBO1