600 W Half Bridge LLC Evaluation Board with 600 V CoolMOS™ C7

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Application Note

About this document

Scope and purpose

The present 600 W Evaluation Board is a great example of a full Infineon solution, including high voltage and low voltage power devices, controllers and drivers in order to demonstrate the most flexible and effective way to design the High Voltage DC/DC stage of a Server PSU fulfilling the 80Plus® Titanium Standard.

Furthermore the reader will get additional information how the 600 V CoolMOS™ C7 behaves in this LLC board and what benefits will be achieved.

Intended audience

This document is intended for design engineers who want to improve their high voltage power conversion applications.

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1 Introduction

The opportunity to significantly reduce the size of power converters by increasing the switching frequency created by the MOSFET technology has recently focused topology development and optimization on the reduction of switching losses of the semiconductor devices, which are perceived as the major obstacle to maximizing the switching frequency of PWM converters.

This has triggered studies on the resonant power conversion, which allows minimizing the switching losses through the achievement of zero-voltage (ZVS) or zero-current (ZCS) switching behavior.

An important example of resonant power conversion is provided by the LLC topology, which is able to address the requirements of high efficiency and power density through the achievement of a true Zero Voltage Switching. Last but not least, its bill of material is significantly reduced compared to the other very popular soft switching topology, the phase shift Full Bridge. These arguments bring the LLC resonant converter more and more in usage in the server/telecom market.

This document will describe an analog controlled 600 W Half Bridge (HB) LLC converter designed using Infineon products. Order information for ISAR: **EVAL_600W_12V_LLC_C7**

2 HB LLC Converter Design Considerations

In the present chapter the most relevant design decisions are explained and documented with related calculations.

2.1 Principle of operation

The principle schematic of a Half Bridge LLC converter is shown in the Figure 1. C_r, L_r and L_m represent the so called “resonant tank”: together with the main transformer they are the key components in the LLC design. The primary Half Bridge and the secondary synchronous rectification are the other two stages to be defined.

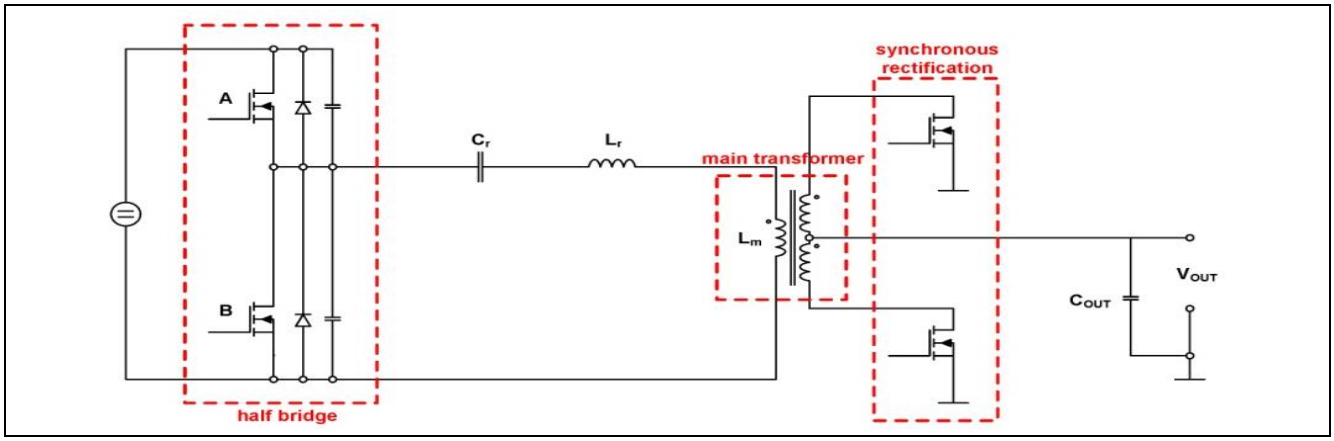

Figure 1 Principle schematic of a Half Bridge LLC converter

The LLC is a resonant converter that means it operates with frequency modulation, instead of the Pulse Width Modulation (PWM), traditional approach to power conversion.
Starting point in a resonant converter design is the definition of an energy transfer function, which can be seen as a voltage gain function, so a mathematical relationship between input and output voltages of the converter. Trying to get this function in an “exact” way involves several nonlinear circuital behaviors governed by complex equations. However, under the assumption that the LLC operates in the vicinity of the series resonant frequency important simplifications can be introduced.
In fact, under this assumption, the current circulating in the resonant tank can be considered purely sinusoidal, ignoring all higher order harmonics: this is the so called First Harmonic Approximation Method (FHA), which is the most common approach to the design of a LLC converter.
In the FHA the voltage gain is calculated with reference to the following equivalent resonant circuit, shown in Figure 2.

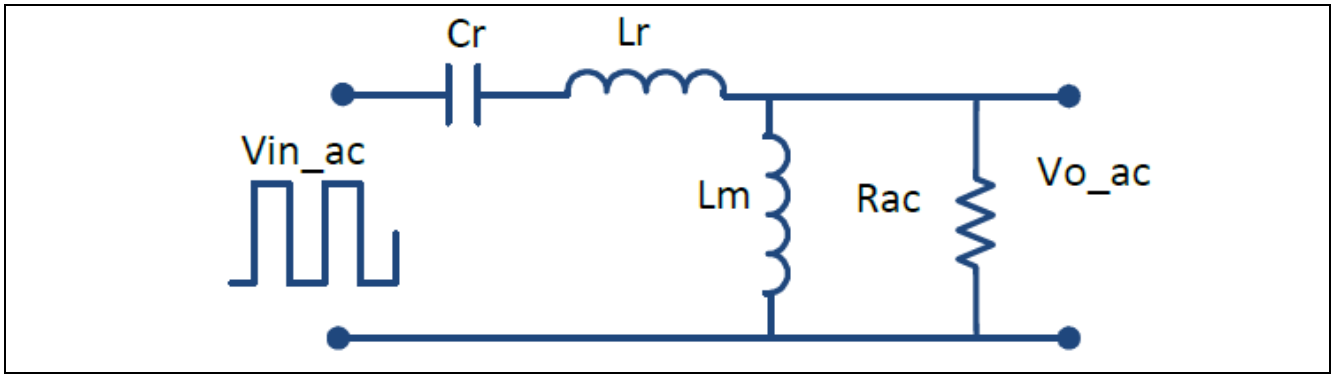

Figure 2 First Harmonic Approximation equivalent resonant circuit

The mathematical expression of the gain K is:

$$K(Q,m,Fx)=\left|\frac{Vo\_ac(s)}{Vin\_ac(s)}\right|=\frac{Fx^2(m-1)}{\sqrt{(m\cdot Fx^2-1)^2+Fx^2\cdot(Fx^2-1)^2\cdot(m-1)^2\cdot Q^2}} \quad (1)$$

where:

$$m=\frac{Lr+Lm}{Lr};\qquad fr=\frac{1}{\sqrt{Lr\cdot Cr}};\qquad Fx=\frac{fs}{fr};\qquad Rac=\frac{8}{\pi^2}\cdot\frac{Np^2}{Ns^2}\cdot Ro;\qquad Q=\frac{\sqrt{Lr/Cr}}{Rac}; \quad (2)$$

So the resonant tank gain K can be plotted in function of the normalized switching frequency f_x for different values of the Quality factor Q and any single value of the inductance factor m.
In this chapter it will be shown a design procedure for the selection of the main LLC parameters, with the goal to achieve the best performance while fulfilling input and output regulation requirements.
At same time, Zero Voltage Switching operation of the primary Half Bridge MOSFETs must be ensured, in order to get full benefits out of the soft switching behavior, especially at light load.

2.2 Input design data

In Table 1 an overview of the major design parameter is displayed.

Table 1 Design parameters

Description	Minimum	Nominal	Maximum
Input Voltage	350 V_{DC}	380 V_{DC}	410 V_{DC}
Output Voltage	11.9 V_{DC}	12 V_{DC}	12.1 V_{DC}
Output Power			600 W
Efficiency at 50% P_{max}	97.5%		
Switching Frequency	90 kHz	150 kHz	250 kHz
Dynamic Output Voltage regulation (0-90% Load step)			Max. overshoot = 0.1 V Max. undershoot= 0.3 V
V_{out_ripple}			150 mV_{pk-pk}

From the table above, the first important design parameters can be derived:

Main transformer turn ratio

$$n=\frac{Np}{Ns}=\frac{Vin\_nom}{2\cdot Vout\_nom}\approx 16 \quad (3)$$

Minimum needed Gain

$$K_{min}(Q,m,Fx)=\frac{n\cdot Vo\_min}{Vin\_max/2}\approx 0.95 \quad (4)$$

Maximum needed Gain

$$K_{max}(Q,m,Fx)=\frac{n\cdot Vo\_max}{Vin\_min/2}\approx 1.08 \quad (5)$$

2.3 Selection of the inductance factor m

The inductance factor (Equation 2) has an important impact on the converter operation. Lower values of m achieve higher boost gain and narrower range of the frequency modulation, that means more flexible control and regulation, which is valuable in applications with very wide input voltage range.
On the other hand, this means also smaller values of L_m which leads into significantly high magnetizing current circulating in the primary side: this current doesn't contribute to the power transferred, but mainly generates conduction losses on the primary side.
In other words, there is a trade-off between flexible regulation and overall efficiency requirements, especially at light load.
In the case of our demo board, main goal is to achieve high efficiency, so relatively high m is selected, also because the input range is relatively narrow and in any case we rely in the bulk capacitor in case of specific hold up time requirement at the complete AC/DC SMPS level - so in our case m≈12.

2.4 Gain curve

The resulting gain curves, Figure 3, for loads between 10% and 100% P_{max} are in the following plot:

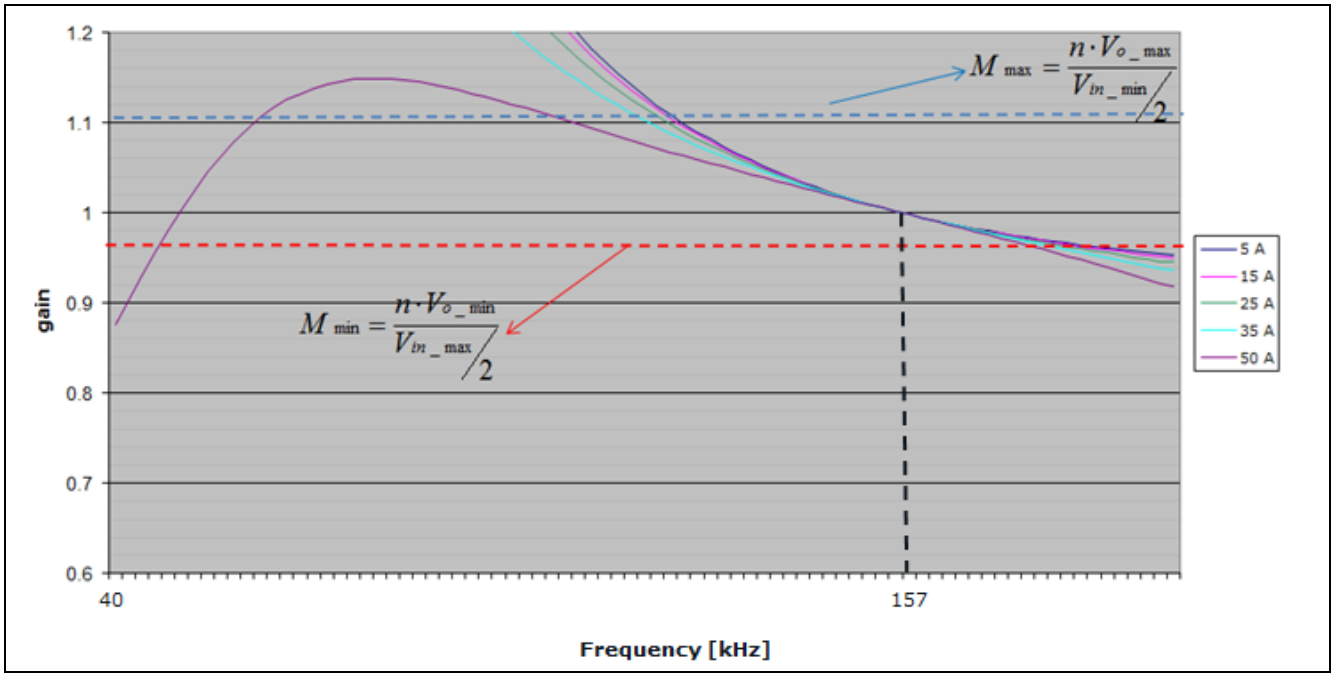

Figure 3 Gain curve

Both the M_{min} and M_{max} limits cross all the gain curves of our LLC converter: that means the regulation is fully achieved in the specified ranges.

2.5 Resonant components calculation

Combining equations (1) and (2), we get a system where the unknown are L_r, C_r and L_m.
Solving it, the following values are set for the LLC converter:

$$n = \frac{Np}{Ns} = \frac{V_{in\_nom}}{2 \cdot V_{out\_nom}} \approx 16 \Rightarrow Np = 16; Ns = 1 \quad (6)$$

$$m = \frac{Lr + Lm}{Lr} \approx 12 \Rightarrow Lm = 195\mu H; Lr = 17\mu H \quad (7)$$

$$Cr = 66nF \quad (8)$$

$$fr = \frac{1}{2\pi \cdot \sqrt{Lr \cdot Cr}} \approx 150KHz \quad (9)$$

2.6 The ZVS behavior: energy and time considerations

The ZVS calculations involve two kind of analysis, the one in the energy domain and the other in the time domain. The goal is to have enough energy in the resonant tank able to discharge the output capacitance of the primary MOSFET, but also an appropriate dead time between the turn-off of each device and the corresponding turn-on of the one at the other side of the Half Bridge.
$C_{o(er)}$ is the C_{oss} energy related component of the used High Voltage MOSFET, in our case IPP60R180C7.
Q_{oss} is the charge stored in C_{oss} at $V_{in(nom)}$=380 V_{DC}

2.6.1 Energy related equations

$$\mathrm{Im}ag\_\min = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot Vo}{2\pi \cdot fsw\_\max \cdot Lm} = 0.672A \quad (10)$$

$$En_{res\_\min} = \frac{1}{2} \cdot (Lm + Lr) \cdot I^2_{mag\_\min} = 95.1\mu J \quad (11)$$

$$En_{cap\_\max} = \frac{1}{2} \cdot (2Co(er)) \cdot V^2_{DS\_\max} \approx 9\mu J \quad (12)$$

$$\Rightarrow En_{res\_\min} > En_{cap\_\max} \quad (13)$$

2.6.2 Time related equations

It can be demonstrated that:

$$tdead = \frac{tecs}{2} + \frac{2 \cdot Qoss@\mathrm{Vin\_nom}}{\mathrm{Im},pk} = \frac{tecs}{2} + \frac{2 \cdot Co(tr)@\mathrm{Vin\_nom} * \mathrm{Vin\_nom}}{\mathrm{Im},pk} \quad (14)$$

where t_{dead} is the dead time set between the conduction time of the two HB devices and t_{ecs} is the time when the channel of each MOSFET is still in conduction after turning it off (linear mode operation), which is function of device parameters like $V_{gs(th)}$, $R_{g(tot)}$ and C_{gs}/C_{gd}.
Using that equation, together with the min and max values of the magnetizing current:

$$\mathrm{Im}ag\_\min = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot Vo}{2\pi \cdot fsw\_\max \cdot Lm} = 0.672\ A \quad (10)$$

$$\mathrm{Im}ag\_\max = \frac{2\cdot\sqrt{2}}{\pi}\cdot\frac{n\cdot Vo}{2\pi\cdot fsw\_\min\cdot Lm} = 1.66\,A \tag{11}$$

$$tdead,\min = \frac{tecs}{2} + \frac{2\cdot Qoss,@400V}{\mathrm{Im},ag,\max} \approx 130\,ns \tag{14}$$

$$tdead,\max = \frac{tecs}{2} + \frac{2\cdot Qoss,@400V}{\mathrm{Im}ag,\min} \approx 311\,ns \tag{15}$$

2.7 The main transformer design

As explained more in details in the chapter 2.6 of the present document, the target efficiency of this design is fixed by the 80PLUS® Titanium Standard; that means fixing certain minimum requirements for the High Voltage DC/DC stage at 10%, 20%, 50%, 100% load conditions.
The most critical condition for the main transformer is the full load, mainly due to thermal reasons. The selection of the core size and material is done according to this condition along with the power density (thus switching frequency) target and the available airflow.
Keeping a margin in the design, the minimum efficiency requirement at full load is fixed for the Half Bridge LLC converter to 97%, which means our goal is to keep the total dissipated power in that condition below 18 W.
In order to guarantee a balanced spread of power and heating, a good rule in the design of the LLC Converter is to keep the total power dissipated on the main transformer below 1/6 of the total dissipated power, which means the max allowed power on it shall be below 3 W. This is our first important design input.
The max operating temperature is 55°C, as in typical server applications. Due to transformer safety insulation approvals, the max operating temperature of the transformer must be lower than 110°C, thereof:

$$\Delta T_{trafo\_MAX} = (110-55)°C = 55°C \tag{16}$$

From (16) and (17) the max thermal resistance of the core shape can be easily derived:

$$R_{th\_trafo\_MAX} = \frac{\Delta T_{trafo\_MAX}}{P_{trafo\_MAX}} = \frac{55}{3}\,°C/W = 18.3\,°C/W \tag{17}$$

So our selected core shape must have thermal resistance lower than 18.3°C/W.
This requirement can be fulfilled with different choices: the preferred will allow maximizing the ratio between available winding area and effective volume, of course compatibly with the eq. (18).
Also considering the power density target (in the range of 20 W/inch^3), the most suitable selection is PQ 35/35, shown in Figure 4.
The related coil form shows a minimum winding area of 1.58 cm^2 and a thermal resistance of 16.5°C/W, thus able to dissipate up to 3.33 W by keeping the ΔT_{MAX} <55°C.
Once verified that the thermal equations are fulfilled, we can proceed with the design of the primary and secondary windings and the core material selection, with some important goals:

- Fitting the geometry/overall dimensions of the core
- Fulfilling the condition (16)
- Try to split as much equally as possible the losses between core and windings: ideally “fifty-fifty” should be achieved at full load, but any percentage close to it would be acceptable.

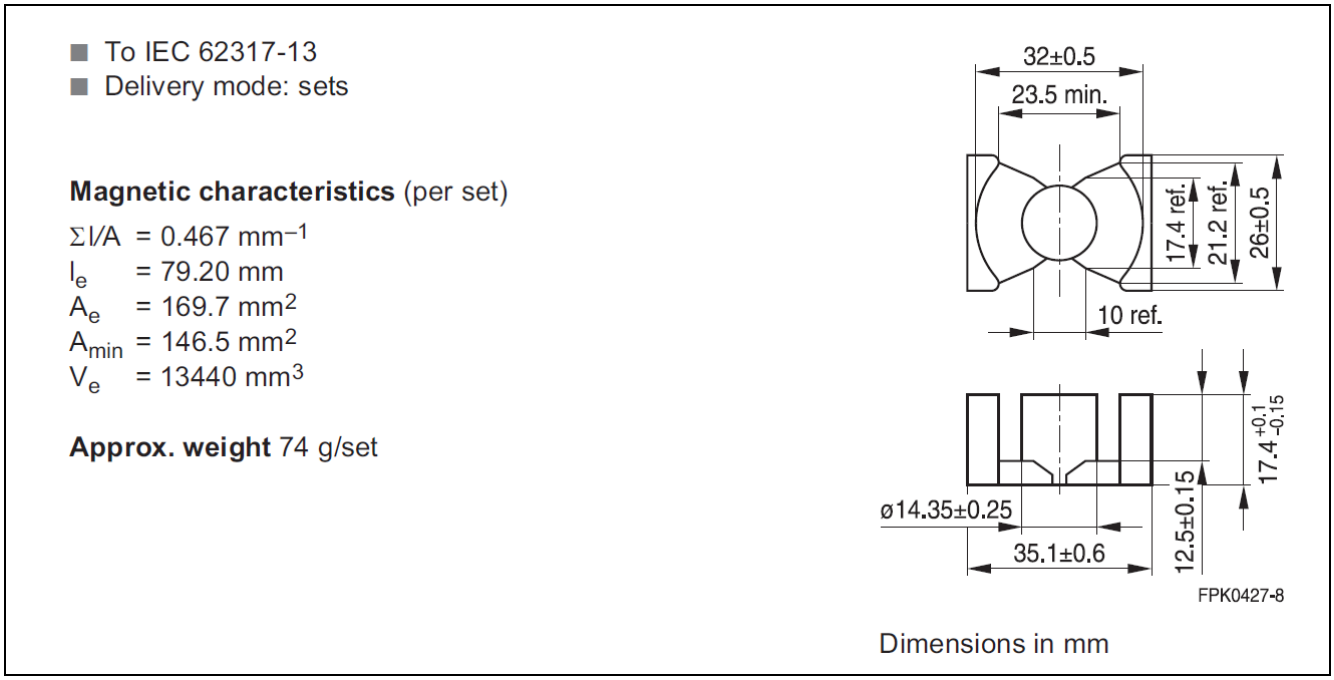

Figure 4 TDK-Epcos PQ35/35 core

The selected core material is the ferrite TDK PC95, showing a very interesting plot of Core Losses (PCV) vs. Flux Density vs. frequency (see Figure 5 below):
The final structure of the main transformer is reported in Figure 6 below. This has been developed in cooperation with the partner company Kaschke Components GmbH, Göttingen – Germany.
So the primary is realized in a “sandwich” technique using 16 turns of 4 layers of litz wire 45 strands 0.1 mm diam. This allows minimizing the AC losses due to skin and proximity effect. The secondary is done with copper band 20x0.5 mm.

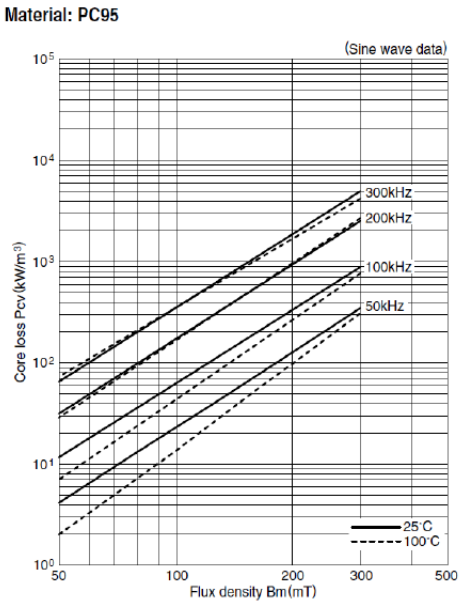

Figure 5 Ferrite core material TDK PC95

HB LLC Converter Design Considerations

With this choice, at full load condition the total copper losses will be (primary + secondary, DC+AC components) are 1.1 W, the core losses are 1.8 W, so overall:

$$P_{trafo} = P_{copper} + P_{core} = 2.9W < P_{trafo\_MAX} \quad (18)$$

In other words, the equation (18) fulfils the thermal equation (17).

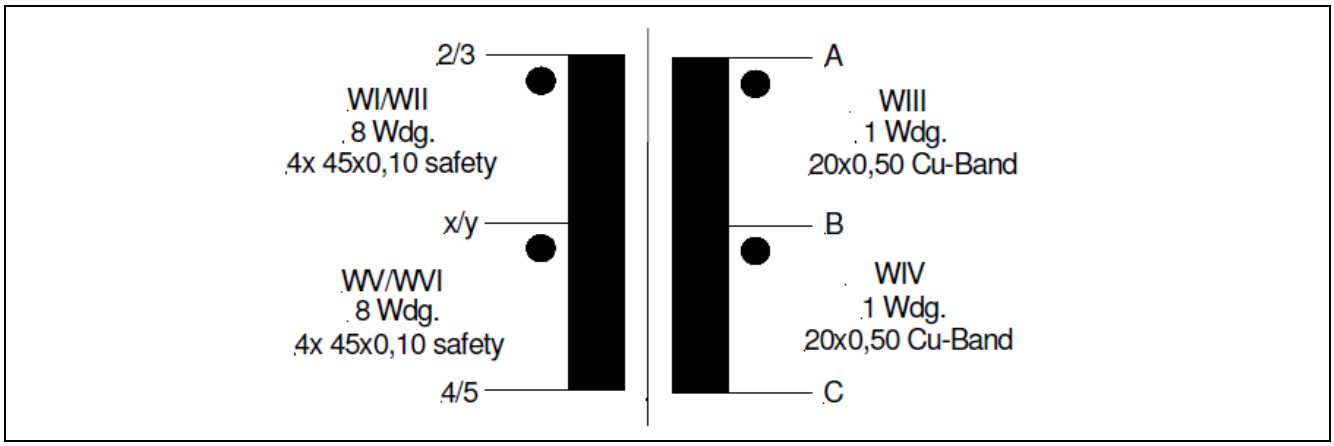

Figure 6 Winding structure of the PQ 35/35 LLC transformer (Kaschke Components GmbH)

An important transformer parameter involved in the LLC design is the primary or magnetizing inductance L_m, which, according to eq. (7) must be 195 µH. This value is obtained with distributed air-gap on the side legs of the PQ core: this construction is preferred since it minimizes the effect of the so called “fringing flux” which generates additional losses in the windings close to the inner limb.

2.8 The resonant choke design

In LLC designs with stringent power density requirements, the resonant choke is typically embedded in the transformer, in the sense that the leakage inductance is utilized according this purpose. This technique has the big advantage to save space and the cost of an additional magnetic component, but also some drawbacks, like the not easy controllability of the L_r value in mass production.
In the case of the present design, it has been decided to use an external L_r.This is due to the fact that the demo board is intended to be primarily used for test and benchmarking and therefore high power density is not in the main focus: having the resonant inductance externally allows to change the resonant tank in a more flexible way.
According to equation (7), the overall value of L_r shall be 17 µH, including the contribution of the transformer leakage inductance + the external resonant choke.

The external resonant choke is realized using a RM-12 core and a winding construction illustrated in Figure 7 below and implemented by the partner company Kaschke Components GmbH, Göttingen - Germany.

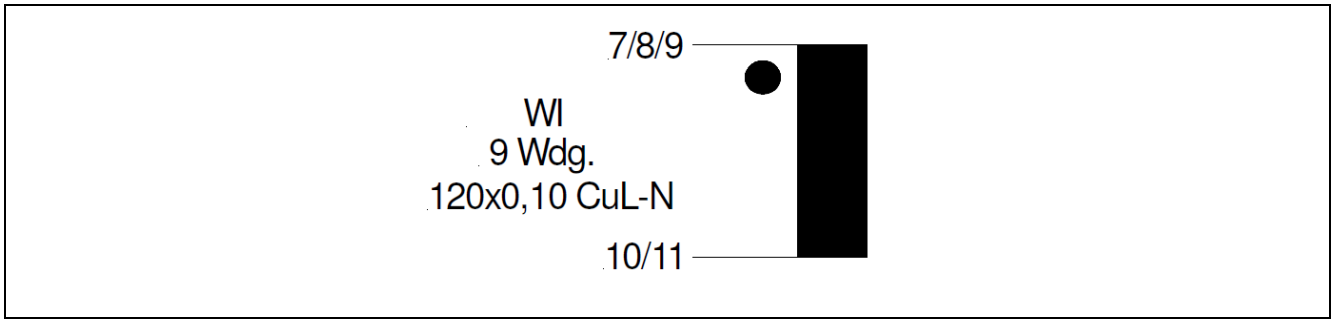

Figure 7 Winding structure of the RM 12 resonant choke (Kaschke Components GmbH)

HB LLC Converter Design Considerations

2.9 The Synchronous Rectification Stage

In applications that target high efficiency both at low and high loads –such as 80PLUS® Titanium- while often requiring high power densities, it is critical to select for the Synchronous Rectification Stage MOSFETs that combine multiple key characteristics.
First of all, these Sync Rec MOSFETs should exhibit very low $R_{DS(on)}$. Indeed, due to the low voltages observed on the secondary side of server power supplies, large currents flow through the Sync Rec MOSFETs. Moreover, compared with hard switching topologies such as ZVS PS FB (Zero Voltage Switching Phase-Shifted Full Bridge), using LLC topology leads not only to increased peak currents for the Sync Rec MOSFETs, but also higher root-mean-square currents I_{RMS}.

Since the conduction losses $P_{cond,SR}$ of each Sync Rec MOSFET are defined by:

$$P_{cond\_SR} = R_{DS,on} \cdot (I_{RMS})^2 \tag{19}$$

These losses can only be mitigated through the use of a part with very low $R_{DS(on)}$.

Secondly, it is critical for these Sync Rec MOSFETs to exhibit low gate charges Q_g:

At lower loads, the switching losses of the Sync Rec MOSFETs predominate over the already mentioned conduction losses. In the case of LLC topology, the main contributor of these switching losses is related to Q_g.
Most of the time, a driving voltage of 12 V is applied to Sync Rec MOSFETs. Although 12 V is not necessary the optimized driving voltage for Sync Rec MOSFETs (more on this below), this driving voltage is very popular in server PSUs because it is readily available: there is no need to derive it from another voltage rail. Therefore, we decided to follow this trend for this demo board by driving the Sync Rec MOSFETs with 12 V.
This requirement for low Q_g puts extra-strain on MOSFET manufacturers, especially considering that Sync Rec MOSFETs need to exhibit at the same time a very low $R_{DS(on)}$. Such a feat was however possible for Infineon thanks to the new Infineon OptiMOS™ 40 V generation, whose gate charges have been significantly reduced in comparison with the previous generation.

Thirdly, the paralleled Sync Rec MOSFETs should turn on almost simultaneously.
This can be achieved thanks to a tightening of the threshold voltage $V_{GS(th)}$ range. In the case new OptiMOS™ 40 V generation, its datasheet guarantees a very narrow $V_{GS(th)}$ range, with min and max values equal to 1.2 V and 2.0 V respectively.

Finally, the MOSFET package is critical for a variety of reasons.
The package should exhibit low parasitic inductances in order to confine its contribution to the V_{DS} overshoot to a strict minimum. This is even more critical in server applications using LLC topology, due to the limited headroom for the V_{DS} overshoot between the transformer secondary voltage (25 V) and the 90% derating (36 V_{max}) or even 80% derating (32 V_{max}) applied to the V_{DS} of the Sync Rec MOSFETs;
Moreover, due to the conflicting requirements for high power density and high current capability, the package should combine a minimum footprint with good power dissipation.

Because of the high current densities arising at the source pins, which can lead to electro-migration and thereafter destruction of the Sync Rec MOSFETs, the package should provide an enlarged source connection. While the first two sub-items are tackled by standard SuperSO8 packages, it is the addition of source fused leads implemented in the new Infineon OptiMOS™ 40 V generation that reduces the high current densities above mentioned.

3 Board description

3.1 General overview

Figure 1 is the top view, bottom view and the assembly of 600W Half Bridge LLC evaluation board. Key components are: **(1)** heat sink with the assembly of primary side switches IPP60R180C7 **(2)** Resonant capacitor **(3)** LLC analog controller ICE2HS01G **(4)** Resonant inductor **(5)** Main DC-DC transformer **(6)** PCB assembly of the auxiliary circuit with bias QR Flyback controller ICE2QR2280Z **(7)** Heat sink assembly for cooling the synchronous rectifier **(8)** Output capacitor **(9)** Output inductor **(10)** Half Bridge MOSFET gate driver 2EDL05N06PF and **(11)** Synchronous rectifier OptiMOS™ BSC010N04LS **(12)** Advanced dual-channel Gate Drive 2EDN7524F.

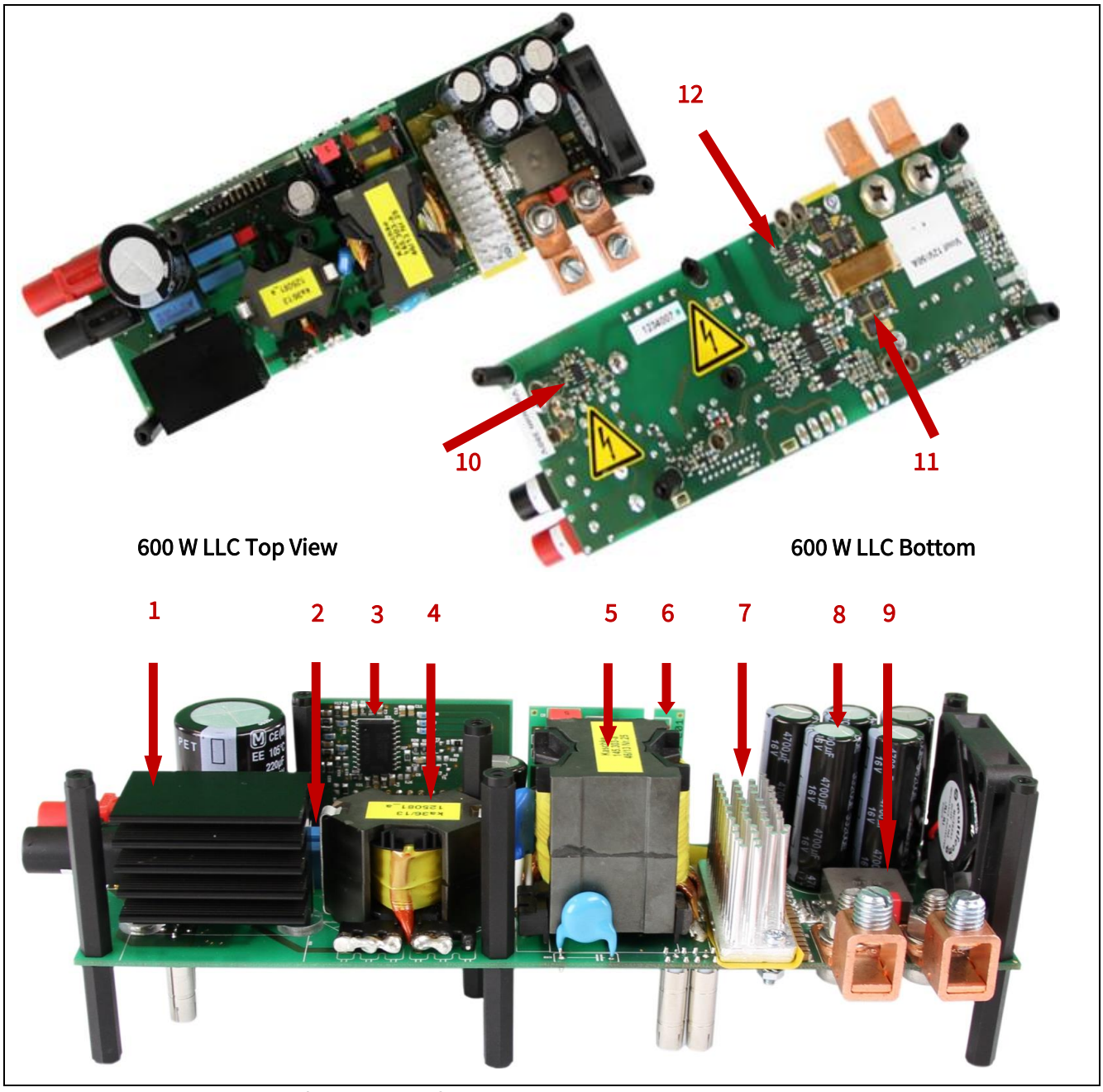

Figure 8 IFX 600W LLC Evaluation Board

3.2 Infineon BOM

This HB LLC 600 W demonstration board is a full Infineon solution, meeting the highest efficiency standard 80PLUS® Titanium using the following parts:

3.2.1 Primary HV MOSFETs CoolMOS™ IPP60R180C7

The 600 V CoolMOS™ C7 is the next step of Silicon improvement based on the 650 V CoolMOS™ C7. It stays with the strategy to increased switching performance in order to enable highest efficiency in any kind of target applications as for boost topologies like PFC's (power factor correction) and high voltage DC/DC stages like LLC's (DC/DC stage with resonant tank in order to maintain zero voltage switching). Although the 600 V CoolMOS™ offers very fast switching, it also kept the ease of use level (how easy to control the switch) of the 650 V C7 "parent technology". Therefore the 600 V CoolMOS™ C7 is optimized device for highest efficiency SMPS (switched mode power supply). The 600 V C7 represents the new standard of SJ MOSFET.

In LLC application, converter is in resonant operation with guaranteed ZVS even at a very light load condition. Switching loss caused by E_{oss} during turn-on can be considered negligible in this topology. With this consideration, CoolMOS™ C7 family of parts offers superior price/performance ratio with low FOMs (R_{on}*Q_g and R_{on}*Q_{OSS}), which means that MOSFET switching transitions can happen in a shorter dead time period. This will result to a lower turn-off losses pushing further the efficiency. The following are the additional features and benefits of CoolMOS™ C7 making it suitable and advantageous for resonant switching topologies like LLC:

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120 V/ns
- Increased efficiency due to Best-in-Class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$ *Q_g
- Best-in-class $R_{DS(on)}$/package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

3.2.2 LLC analog controller ICE2HS01G

ICE2HS01G is Infineon's 2nd generation HalfBridge LLC controller designed especially for high efficiency Half Bridge or FullBridge LLC resonant converter with synchronous rectification (SR) control for the secondary side. With its new driving techniques, the synchronous rectification can be realized for LLC converter operated with secondary switching current in both CCM and DCM conditions. No special synchronous rectification controller IC is needed at the secondary side. The maximum switching frequency is supported up to 1 MHz. Apart from the patented SR driving techniques, this IC provides very flexible design and integrates full protection functions as well. It is adjustable for maximum/minimum switching frequency, soft-start time, frequency, dead time between primary switches, turn-on and turn-off delay for secondary SR MOSFETs. The integrated protections include input voltage brownout, primary three-levels over current, secondary over load protection and no-load regulation. It also includes a burst mode function which offers an operation with low quiescent current maintaining high efficiency at low output load while keeping output ripple voltage low.

3.2.3 Half Bridge Gate Drive 2EDL05N06PF

2EDL05N06PF is one of the drivers from Infineon's 2EDL EiceDRIVER™ Compact 600V Half Bridge gate driver IC family with monolithic integrated low-ohmic and ultrafast bootstrap diode. Its level-shift SOI technology supports higher efficiency and smaller form factors of applications. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions. The two independent

Board description

drivers outputs are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic which are optimised either for IGBT or MOSFET. 2EDL05N06PF (DSO-8) and 2EDL05N06PJ (DSO-14) are driver ICs with undervoltage-lockout for MOSFETs. These two parts are recommended for server/telecom, low-voltage drives, e-bike, battery charger and Half Bridge based switch mode power supply topologies.

- Individual control circuits for both outputs
- Filtered detection of under voltage supply
- All inputs clamped by diodes
- Off line gate clamping function
- Asymmetric undervoltage lockout thresholds for high side and low side
- Insensitivity of the bridge output to negative transient voltages up to -50 V given by SOI-technology
- Ultra fast bootstrap diode

3.2.4 Advanced dual-channel Gate Drive 2EDN7524F

The Fast Dual Channel 5 A Low-Side Gate Driver is an advanced dual-channel driver optimized for driving both Standard and Superjunction MOSFETs, as well as GaN Power devices, in all applications in which they are commonly used. The input signals are TTL compatible (CMOS 3.3 V) with an input voltage range from 3 V to +20 V. The ability to operate with -10 V_{DC} at the input pins protects the device against ground bounce conditions. Each of the two outputs is able to sink and source a 5 A current utilizing a true rail-to-rail stage, that ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail respectively. Very low channel to channel delay matching, typ. 1 ns, enables the double source and sink capability of 10 A, by paralleling both channels. Different logic input/output configurations guarantee high flexibility in all applications; e.g. with two paralleled switches in a boost configuration (see Figure below). The gate driver is available in the three package options: A standard PG-DSO-8, a thin PG-WSON-8-1 and PG-TSSOP-8-1 (minimized DSO 8 package).

Main Features

- Industry-Standard Pinout
- Two Independent Low-Side Gate Drivers
- 5 A Peak Sink/Source Output Driver at V_{DD} = 12 V
- -10 V_{DC} Negative Input Capability against GND-Bouncing
- Enhanced operating robustness due to High Reverse Current Capability
- True Low-Impedance Rail-To-Rail Output (0.7 Ω and 0.55 Ω)
- Very Low Propagation Delay (19 ns)
- Typ. 1 ns Channel to Channel Delay Matching
- Wide Input and Output Voltage Range up to 20 V
- Active Low Output Driver even on Low Power or Disabled Driver
- High Flexibility through Different Logic Input Configurations (LVTTL and CMOS 3.3 V)
- PG-DSO-8, PG-WSON-8-1 and PG-TSSOP-8-1 Package
- Extended Operation from -40 °C to 150 °C (Junction Temperature)
- Particularly Well-Suited for Driving Standard, Superjunction MOSFETs, IGBTs or GaN Power Devices

Board description

Typical Applications

- SMPS
- DC/DC Converters
- Motor Control
- Solar Power, Industrial Applications

3.2.5 Bias QR Flyback controller ICE2QR2280Z

ICE2QRxxxx is a second generation quasi-resonant PWM CoolSET™ with power MOSFET and startup cell in a single package optimized for off-line power supply applications such as LCD TV, notebook adapter and auxiliary/housekeeping converter in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system average efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption at standby mode operation and low output voltage ripple. The numerous protection functions give a full protection of the power supply system in failure situation. Main features of ICE2QR2280Z which make it suitable as an auxiliary converter of this LLC demonstration board are:

- High voltage (650 V/800 V) avalanche rugged CoolMOS™ with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback Point Correction with digitalized sensing and control circuits
- V_{CC} undervoltage and overvoltage protection with Autorestart mode
- Over Load /open loop Protection with Autorestart mode
- Built-in Over temperature protection with Autorestart mode
- Adjustable output overvoltage protection with Latch mode
- Short-winding protection with Latch mode
- Maximum on time limitation
- Maximum switching period limitation

3.2.6 Synchronous Rectification MOSFETs OptiMOS™ BSC010N04LS

For the synchronous rectification stage the selected device is BSC010N04LS, from the latest OptiMOS™ 40 V family. SR is in fact naturally the best choice in high efficiency designs of low output voltage and high output current LLC, as in our case. In applications that target high efficiency both at light and heavy loads – such as 80PLUS® Titanium- while often requiring high power densities, it is critical to select SR MOSFETs that combine following key characteristics:

- Very low $R_{DS(on)}$: BSC010N04LS provides the industry's first 1mΩ 40 V product in SuperSO8 package.
- Low gate charge Q_g, which is important in order to minimize driving losses, with benefits on light load efficiency
- Very tight $V_{GS(th)}$ range: in fact, in case of paralleling this allows the MOSFETs to turn-on almost simultaneously. Selected OptiMOS™ offer very close min and max of $V_{GS(th)}$, respectively 1.2 and 2 V.

Board description

- Monolithically integrated Schottky like diode, in order to minimize the conduction losses on it.
- Package; BSC010N04LS in SuperSO8 with source fused leads is able to address all the typical crucial requirements for a suitable SR MOSFET package:
  - Minimizing parasitic inductances
  - Combining compact footprint with good power dissipation
  - Enlarged source connection in order to minimize electro-migration occurrence.

3.3 Board schematic

3.3.1 Mainboard schematic

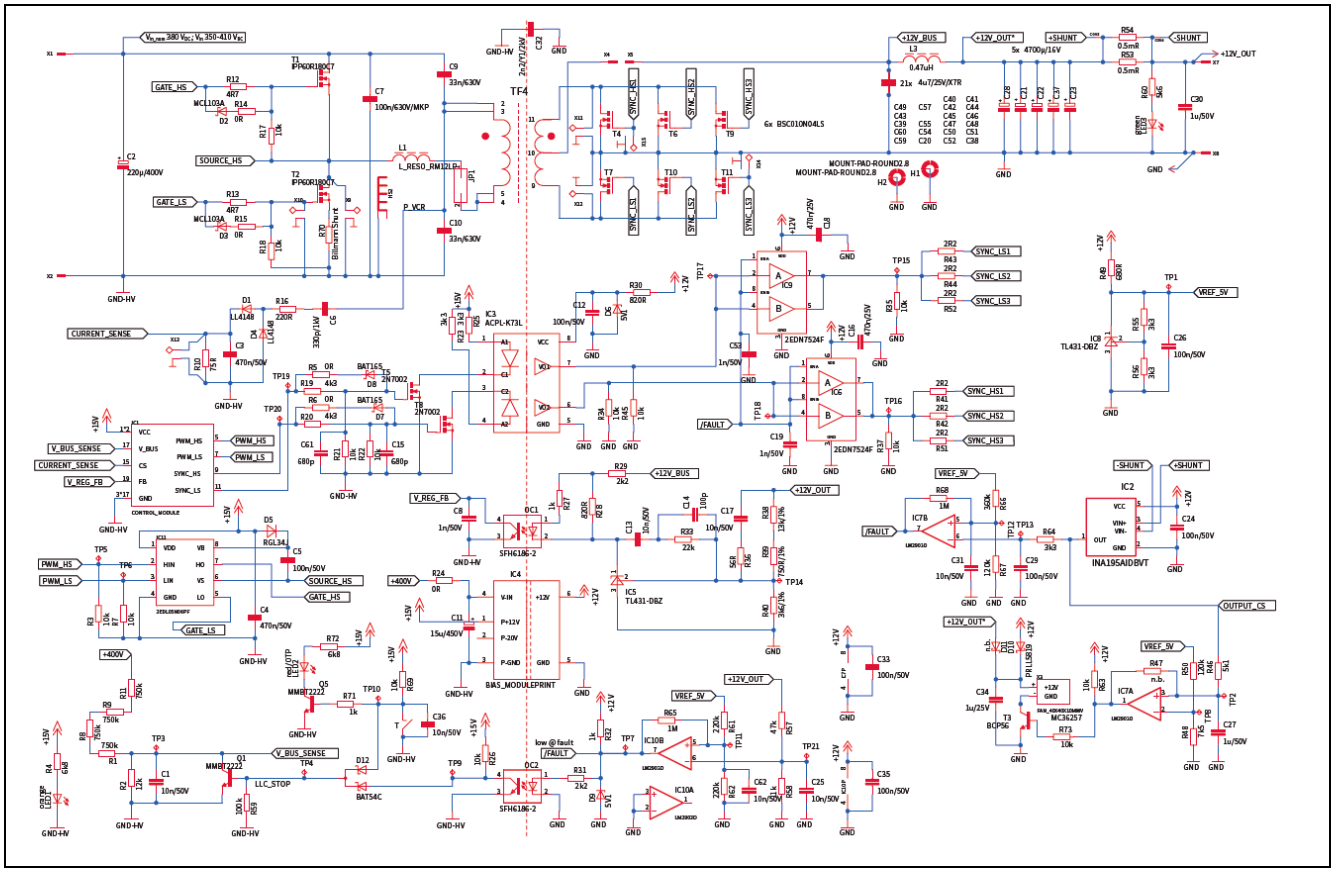

Figure 9 Mainboard schematic

3.3.2 Control board schematic

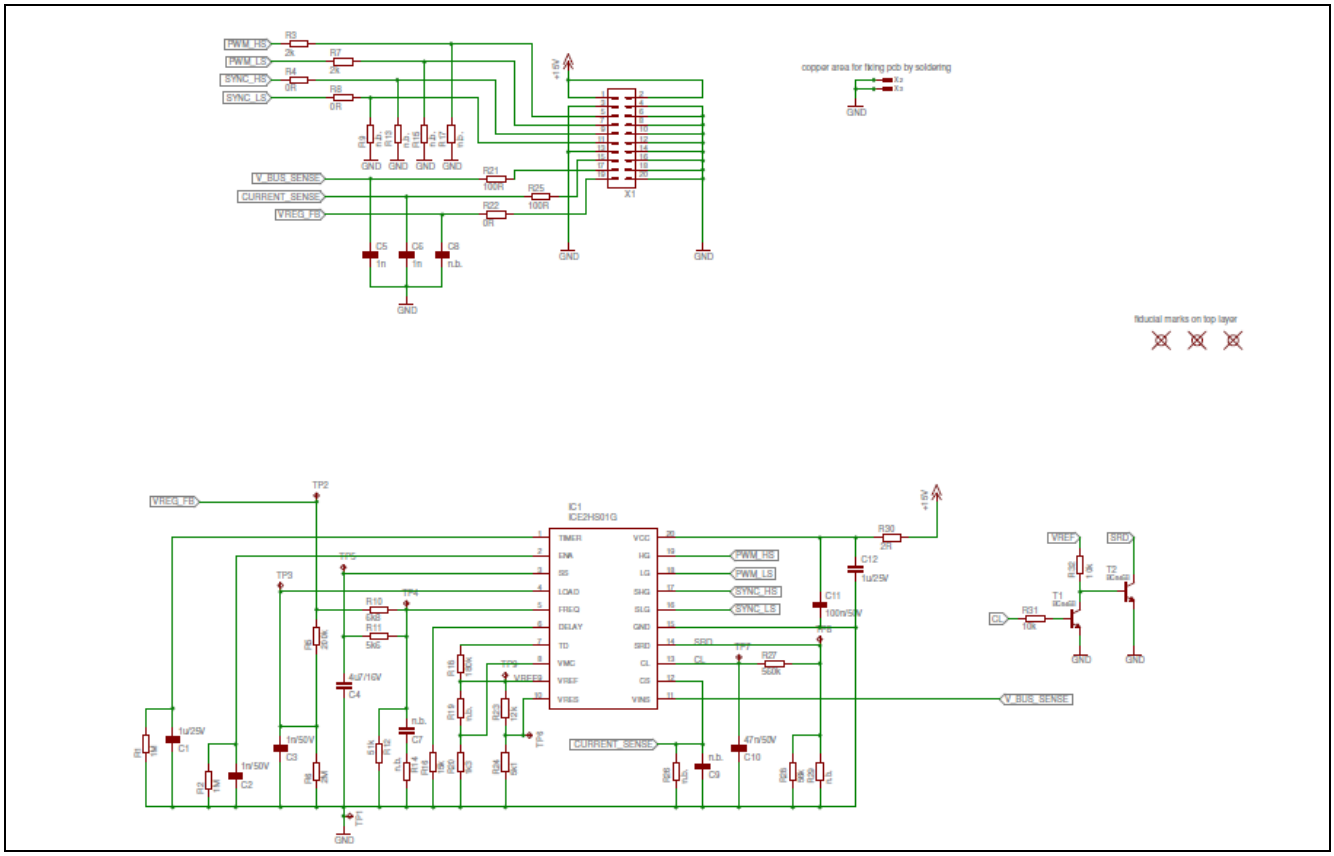

Figure 10 Control board schematic

3.3.3 Biasboard schematic

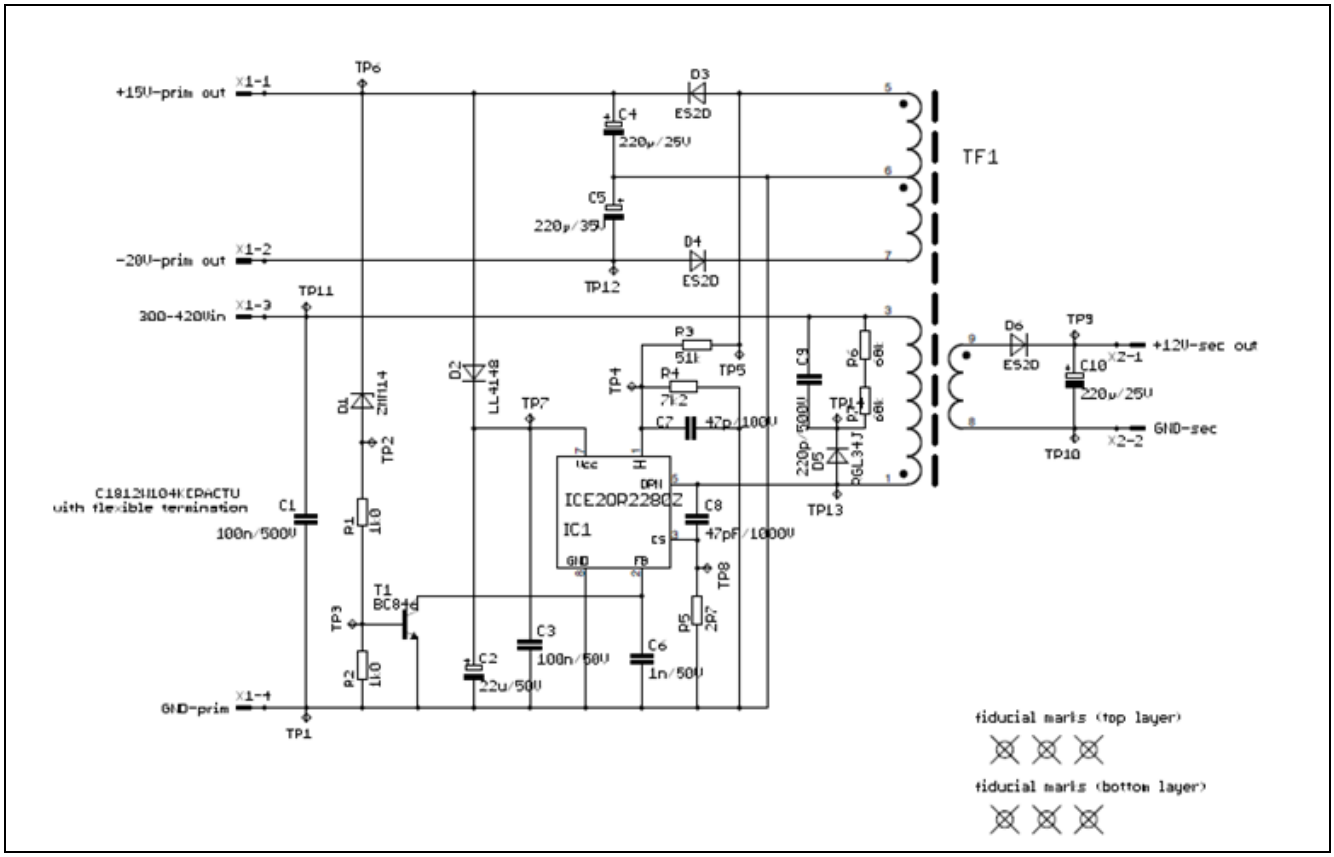

Figure 11 Biasboard schematic

Board description

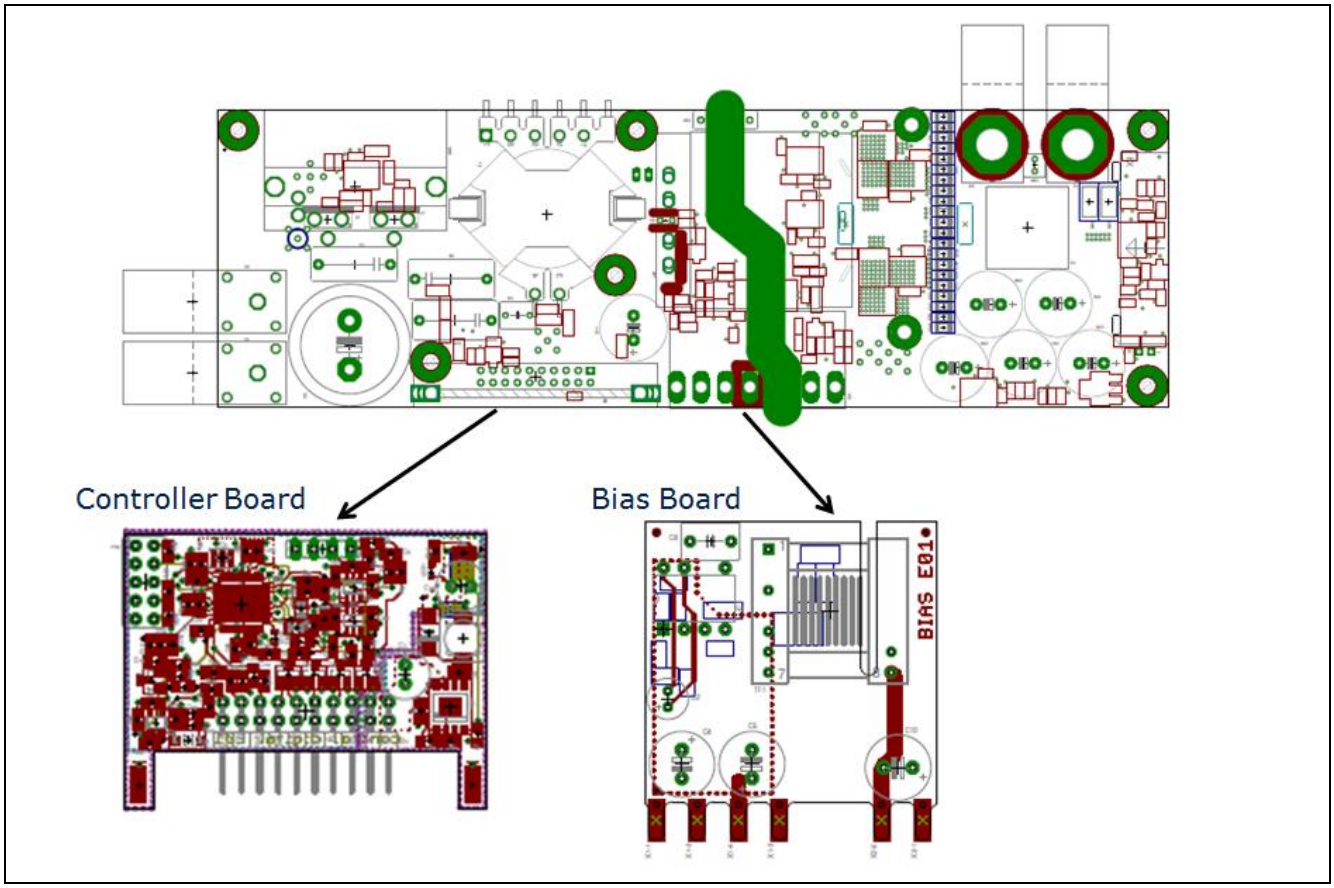

Figure 12 Mainboard PCB with Control – and Bias Board

4 Typical characteristics with 600 V CoolMOS™ C7

4.1 Critical LLC operation - hard commutation

In LLC converter, hard commutation of the body diode normally only occurs during the start-up, burst mode, overload and short circuit condition. These conditions can be minimized if not avoided in the design using an analog controller with proper selection of resonant components and properly setting of the minimum and maximum operating frequency. Hard commutation happens in LLC during the commutation period of the body diode. During this time, resonant inductor current is flowing through body diode of the MOSFET creating ZVS condition upon this MOSFET's turn-on. When the current is not able to change its direction prior to the turn-on of the other MOSFET, more charges will remain in the P-N junction of that MOSFET. When the other MOSFET turns on, a large shoot-through current will flow due to the reverse-recovery current of the body diode. This results to a high reverse recovery peak current I_{RRM} and high reverse recovery dv/dt which sometimes could result to a MOSFET breakdown.

In this 600 W LLC analog controlled demonstration board, only the burst mode condition has the tendency of undergoing hard commutation. In Figure 13, hard commutation at burst mode is minimal that IPP60R180C7 was able to withstand without any problem.

Figure 13 Hard commutation during burst mode operation, V_{DS_pk} , $V_{GS\_max/min}$ and I_{RMM}

Typical characteristics with 600 V CoolMOS™ C7

The voltage spike on the gate V_{GS} and drain V_{DS} can be influenced by varying both turn-on and turn-off gate resistors up to 10 ohm without affecting the efficiency, thanks to the switching behavior of the C7 technology.
Thanks to the very carefully design and control loop on this 600 W Analog LLC Demonstration board, there is neither during start-up nor for short-circuit condition any hard commutation observed.

4.2 Full ZVS area

Nearly full ZVS is achieved on the entire output load range as shown in Figure 14.

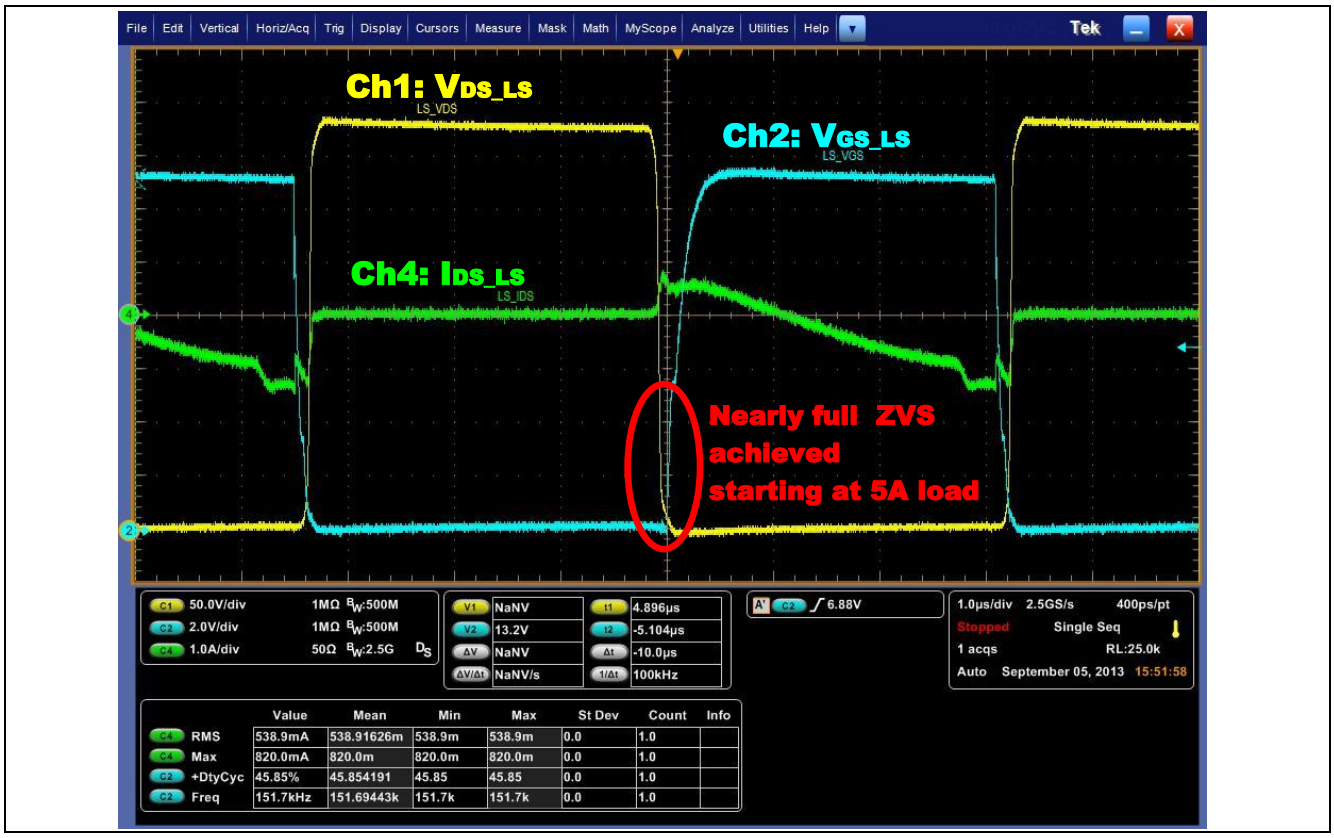

Figure 14 Nearly Full Zero Voltage Switching (ZVS) starting at 5 A load

4.3 Burstmode operation

At no load or a very light load condition, LLC controller provides frequency approaching to its maximum setting. In this condition, in order to still achieve full ZVS, magnetizing current should be high enough to discharge the output capacitances. Due to magnetizing current limitation, switching loss especially turn-off loss is relatively high if the devices will continue to switch at the highest frequency. In order to overcome this phenomenon, burst mode function is enabled and implemented. This results to an effective lower switching losses and driving losses because of the low burst frequency. Additionally, this helps to achieve regulation even at no load condition. In Figure 15 one can see the waveform of Burst Mode Operation at no-load and/or very light load condition

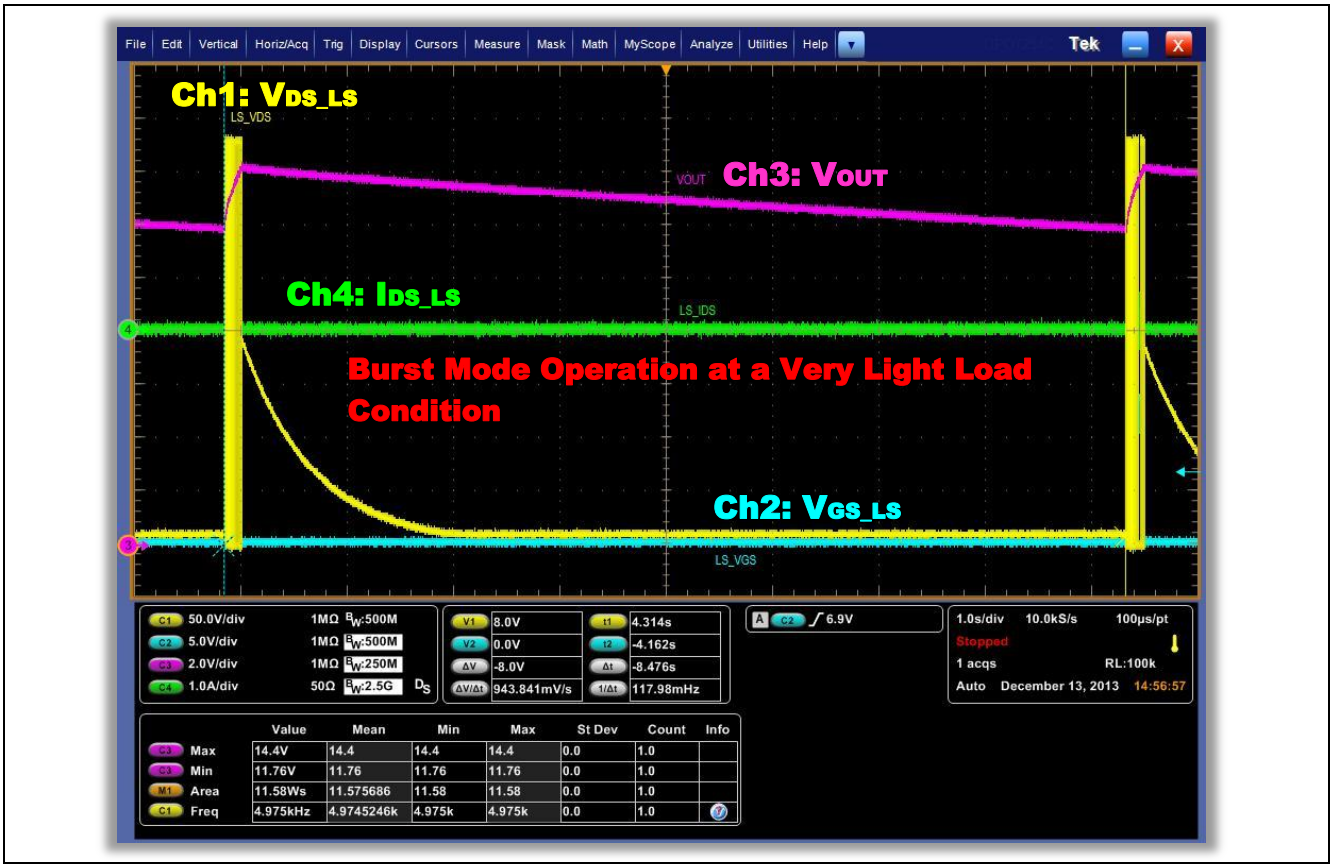

Figure 15 Burst Mode Operation at no-load and/or very light load condition

4.4 Efficiency

4.4.1 Titanium Efficiency

Figure 16 shows the efficiency comparison of this 600 W LLC evaluation board in relation to the Titanium Efficiency Standard. At the most important efficiency point (50% load), this LLC board offers 0.3 % efficiency benefit compared to the Titanium Efficiency Line.

Typical characteristics with 600 V CoolMOS™ C7

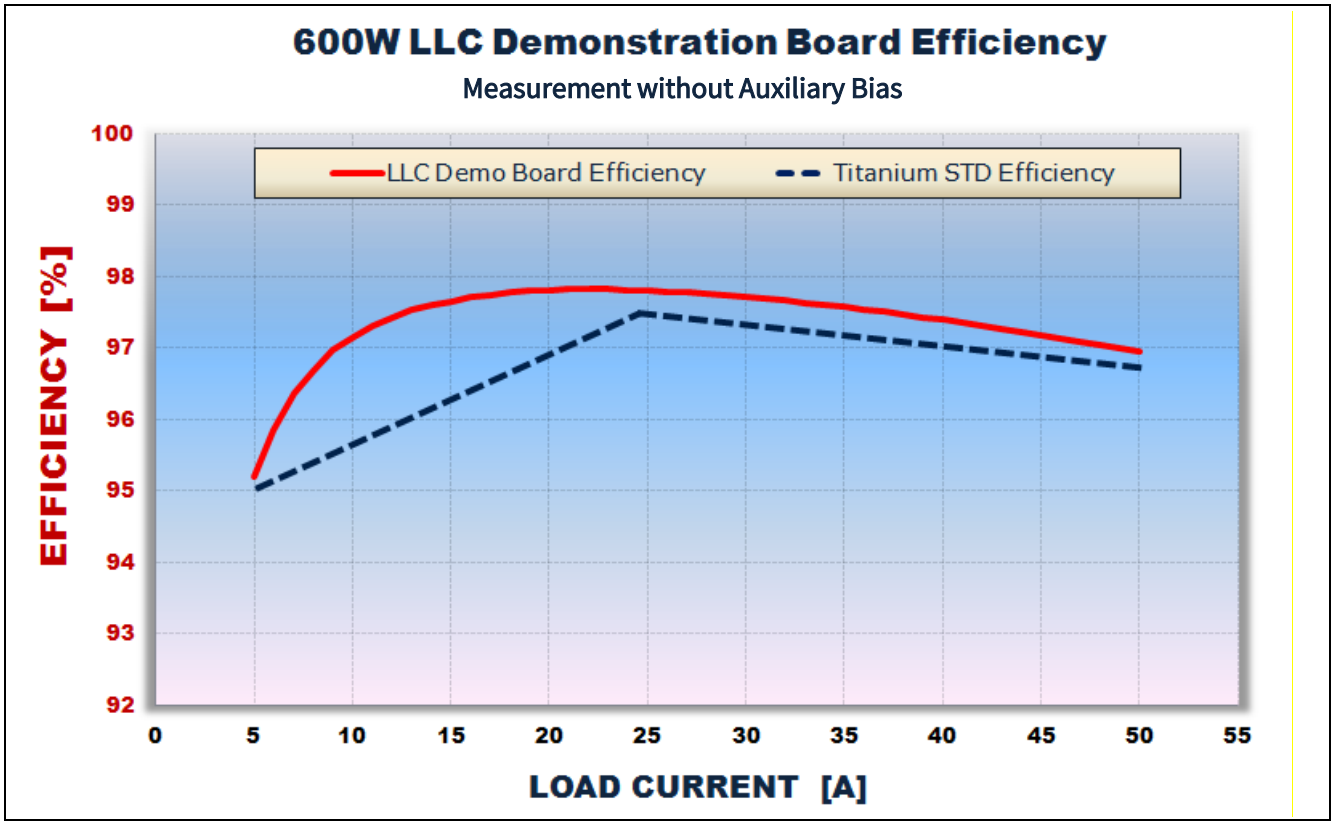

Figure 16 IFX 600 W LLC Demonstration Board Efficiency vs Titanium STD Efficiency

4.4.2 Efficiency comparison in resonant LLC Half Bridge

Figure 17 shows the efficiency comparison in a 600 W LLC circuit, V_{in}=380 V, V_o=12 V, running at resonant frequency f_o=157 kHz. The 0.1 % improvement across the load range is mostly related to the low turn off losses and the low C_{oss} dissipation, since other switching losses are minimal when operating at the resonant frequency. Furthermore, it's expected to gain more efficiency benefit when operating above the resonant frequency, where turn off losses start to engage.

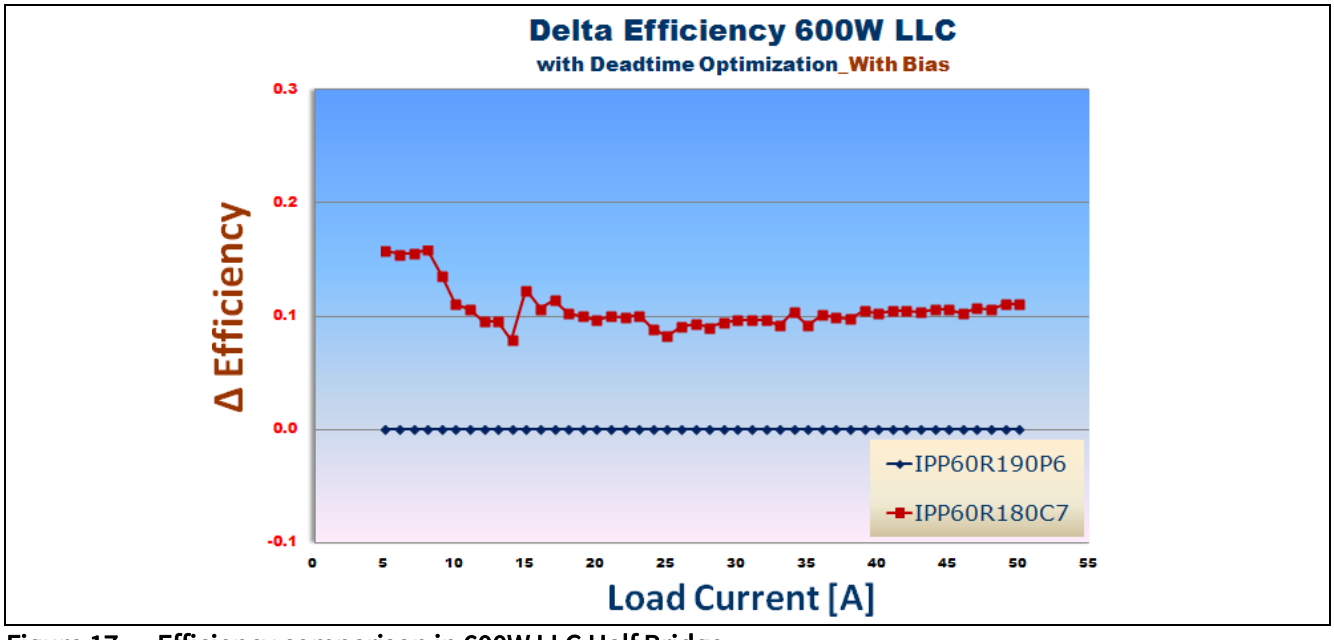

Figure 17 Efficiency comparison in 600W LLC Half Bridge

5 Test/powerup procedure

Table 2 Test/Powerup procedure

Test	Test procedure	Condition
1. Auxiliary Circuit Turn-On	Apply 30 V_{DC} on the input.	V_{in}: ~30 V_{DC}
		Orange LED will light up
2. LLC Converter Turn-On	Apply 350 V_{DC}. Converter will give Vout =12 V_{DC}.	V_{in}: 350 V_{DC}
		V_{out}:12 V
3. Operational switching frequency	Using voltage probe, monitor switching frequency at following test conditions:	V_{in}:380 V_{DC}
		V_{out}:12 V
	@5 A Output Load 10%Load - ~ 155 kHz*	**I_{out}: 5 A**
	@25 A Output Load 50%Load - ~ 142 kHz*	**I_{out}: 25 A**
	@50 A Output Load 100%Load - ~ 132 kHz*	**I_{out}: 50 A**
	*(*measure freq. at "Pri_LS_VGS"-connector)*	
	[* +/-10 kHz]	
4. Fan enable	Switch the load from 50 A to 5 A. Increase the output load current from 11-14 A, fan should turn on.	V_{in} =380 V_{DC}
		I_{out}= 5 A
		ÞFan is off
		V_{in} =380 V_{DC}
		I_{out}= 11-14 A
		ÞFan is on
5. Switch off Input Start-up at No load	Switch off the Input	V_{in}= 0 V_{DC}
		I_{out}= 0 A
	Switch at 380 V_{DC} on **no load output**. Operation should be in burst mode.	V_{in} =380 V_{DC}
		I_{out} = 0 A
		V_{out} = 11,5 – 12,5
6. Switch off Input; Start-up at Full load	Switch off the Input	**V_{in}= 0 V_{DC}**
		I_{out}= 0A
	Apply 380 V_{DC} with full load @50 A output. V_{out} is in between 11.8 – 12.2 V_{DC}* *(*measure on the board-connector)*	V_{in} =380 V_{DC}
		V_{out}: 11,8 – 12,3 V_{DC}
		I_{out} = 50 A
7. Running No Load -> Output Short Circuit	Switch off load from 380 V_{DC} **50 A** to 380 V_{DC} **0 A**.	V_{in} =380 V_{DC}
	Short circuit the load using the short circuit function of the e-load. **Converter should latch.**	*(after short circuit)* **V_{out} = 0 V_{DC}**
		I_{out} = 0 A

Test/powerup procedure

Test	Test procedure	Condition
8. Switch off Input & remove short circuit	Switch off the Input.	**V_{in}= 0 V_{DC}**
9. Running Full Load -> Over Current Protection	Remove short circuit function on the load.	I_{out}= 0 A
	Apply 380 V_{DC} 50 A with full load output. Increase the current on the output 1 A each step until the converter goes into protection starting from 50 A. OCP occurs between 55 A and 62 A.	V_{in} =380 V_{DC}
		I_{out} = 50 A
		OCP = between 55 A – 62 A
10. Running Full Load -> Output Short Circuit	Apply 380 V_{DC} 50 A with full load output. Short circuit the load using the short circuit functions of the load. Converter should latch.	I_{out}= 0 A
		V_{in} =380 V_{DC}
		I_{out} = 50 A
		(after short circuit) **V_{out}=0 V_{DC}**
11. Switch off Input; Start- Up -> Output Short Circuit	Switch off the Input.	V_{in}= 0 V_{DC}
		I_{out}= 0 A
	Apply 380 V_{DC} with output load short circuit. *Converter should be in hiccup/latch mode.*	V_{in} =380 V_{DC}
		I_{out} = short circuit
		V_{out} = 0 V short circuit (hiccup/latch)
12. Switch off Input & remove short circuit	Switch off the Input.	V_{in}= 0 V_{DC}
	Remove short circuit function on the load.	I_{out}= 0 A
13. Dynamic Loading	Apply 380 V_{DC}. Set the electronic load to dynamic loading mode with the following settings:	V_{in} =380 V_{DC}
	CCDH1: Iout 5 A	**I_{out} = 5 A…50 A** **V_{out} = 11,5 – 12,5 V_{DC}**
	CCDH2: Iout 50 A	
	Dwell time: 10 ms	
	Load slew rate: 1 A/µS	

6 Useful material and links

With the following links you can find more detailed information about the used devices from Infineon and the magnetic components.

- **Primary HV MOSFETs CoolMOS™ IPP60R180C7:**
  http://www.infineon.com/dgdl/Infineon-IPP60R180C7DS-v02_00-EN.pdf?fileId=5546d4624cb7f111014d483fe4ba707b

- **LLC Analog Controller ICE2HS01G**
  http://www.infineon.com/dgdl/ICE2HS01G_PDS_v2.1_20110524_Public.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a40a650012a458289712b4c

- **Advanced Dual-Channel Gate Drive 2EDN7524F**
  http://www.infineon.com/dgdl/Infineon-2EDN752x_2EDN852x-DS-v01_00-EN.pdf?fileId=5546d4624cb7f111014d672f9fbb5142

- **Bias QR Flyback Controller ICE2QR2280Z**
  http://www.infineon.com/dgdl/Datasheet_ICE2QR2280Z_v21_20110830.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a7fedfc012a8d8038e00473

- **SR MOSFETs OptiMOS™ BSC010N04LS**
  http://www.infineon.com/dgdl/BSC010N04LS_rev2.0.pdf?folderId=db3a304313b8b5a60113cee8763b02d7&fileId=db3a3043353fdc16013552c1c63647c4

- **Main Transformer and Resonant Choke Ferrite Cores**
  http://en.tdk.eu/blob/519704/download/2/ferrites-and-accessories-data-book-130501.pdf
- **Half Bridge Gate Drive 2EDL05N06PF**
  http://www.infineon.com/cms/en/product/power/gate-driver/eicedrivershigh-voltage-gate-driver-ics-and-boards/gate-driver-ic-eicedriver-compact/2EDL05N06PF/power/gate-driver/2EDL05N06PF/power/gate-driver/2EDL05N06PF/productType.html?productType=db3a30443e36c802013e3c260fb915fd

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[2] Francesco Di Domenico and others: “Design of 600 W HB LLC Demo Board using 600 V CoolMOS™ P6”, Infineon Technologies AN 2015

[3] Lawrence Lin, Gary Chang: “Consideration of Primary side MOSFET Selection for LLC topology”, Infineon Technologies AN 2014

[4] Anders Lind: “LLC Converter Design Note”, Infineon Technologies AN 2013-03

[5] Liu Jianwei, Li Dong: “Design Guide for LLC Converter with ICE2HS01G”, Infineon Technologies AN V1.0, July 2011

[6] F. Stückler, S. Abdel-Rahman, K. Siu: “600 V CoolMOS™ C7 Design Guide”, Infineon Technologies

8 List of abbreviations

Table 3 Abbreviation and symbols used

C_{GD}	internal gate drain capacitance $C_{GD}=C_{rss}$
C_{iss}	input capacitance $C_{iss}=C_{GS}+C_{GD}$
$C_{o(er)}$	effective output capacitance
C_r	resonant capacitance
di/dt	steepness of current slope at turn off / turn on
DUT	device under test
dv/dt	steepness of voltage slope at turn off / turn on
E_{off}	power loss during switch off
E_{on}	power loss during switch on
E_{oss}	stored energy in output capacitance (C_{oss}) at typ. V_{DS}=400V
FHA	First Harmonic Approximation Method
FOM	Figures of Merit
f_r	resonand frequency
I_D	drain current
I_{RMS}	effective root mean square current
I_{mag}	magnatizing current
$I_{m,pk}$	peak current
K	gain factor
L_r	resonant inductance
L_m	magnatizing inductance
m	voltage gain
N_p	primary winding
N_S	secondary winding
n	transformer turn ratio
MOSFET	metal oxide semiconductor field effect transistor
P_{cond_SR}	synchronos conduction losses
PFC	power factor correction
PNP	bipolar transistor type (pnp vs. npn)
Q_{OSS}	Charge stored in the C_{OSS}
Q	quality factor
R_{ac}	total equivalent resistor
$R_{DS(on)}$	drain-source on-state resistance
$R_{g,tot}$	total gate resistor
R_o	output resistor
R_{th}	thermal resistor
t_{dead}	dead time
t_{ecs}	early channel shut down time
V_{DS}	drain to source voltage, drain to source voltage
V_{gsth}	drain to source threshold voltage
V_{O_AC}	output voltage, alternating current
V_{In_AC}	input voltage, alternating current

List of abbreviations

V_{In_nom} ..... nominale input voltage
V_{out_nom} ..... nominale output
ZCS ..... zero current switching
ZVS ..... zero voltage switching

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release
Revision 1.1	Update on Layout and Structure
Revision 1.2	Update on Section 3.2.4

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