300 W PFC evaluation board with ICE3PCS01G CCM PFC controller

About this document

Scope and purpose

The evaluation board presented here is a 300 W power factor correction (PFC) circuit with 85 ~ 265 VAC universal input and output of 395 VDC rated voltage or 333 VDC in boost follower mode. The continuous conduction mode (CCM) PFC controller ICE3PCS01G is employed in this board to achieve the unity power factor.

This ICE3PCS01G is specially designed for applications of power supplies used in PC, server, LCD/PDP TV and Telecom, requesting high efficiency and power factor. The voltage loop compensation is integrated digitally for better dynamic response and less design effort. Appreciated for its high integrated design, ICE3PCS01G can achieve full requirements of the PFC application implemented in the 14-pin in DSO14 package. At the same time the number of peripheral components is minimized. The gate switching frequency is adjustable from 21 kHz to 100 kHz and able to synchronize with external switching frequency from 50 kHz to 100 kHz. In order to improve the power conversion efficiency further, the CoolMOS™ CP series and high voltage silicon carbide (SiC) schottky diode thinQ!TM are used into this boost type PFC circuit.

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1 Evaluation board

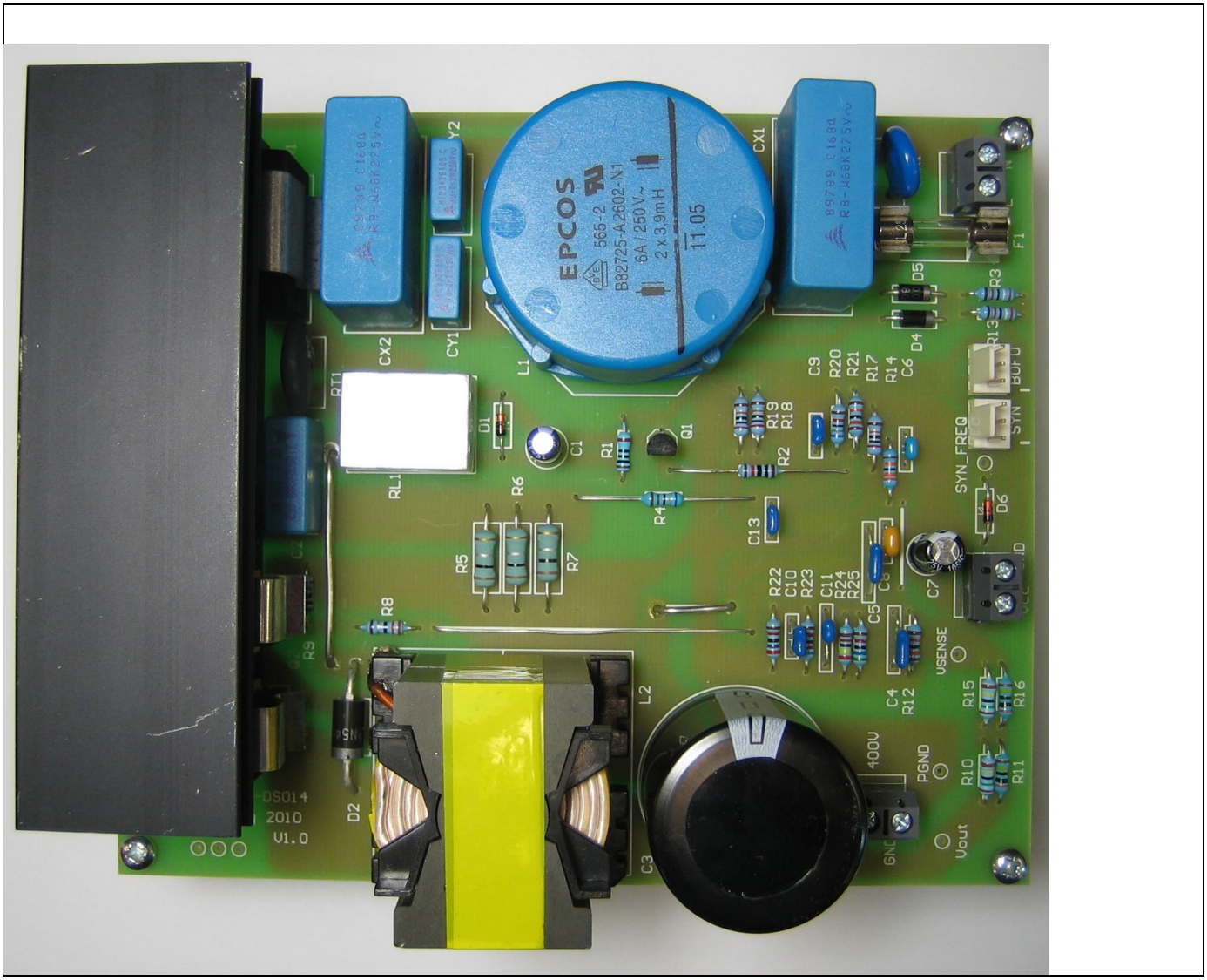


Figure 1 ICE3PCS01G Demo board

2 Technical specifications

Table 1 Technical specifications

Input voltage	85 VAC ~ 265 VAC
Input frequency	47Hz ~ 63 Hz
Output voltage and current	395 VDC, 0.75 A
Output power	~ 300 W
Average efficiency	> 96% at 115 VAC
Switching Frequency	21 kHz ~ 100 kHz

3 Circuit description

Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L1, X2- capacitors CX1/CX2 and Y1-capacitor CY1/CY2 are used to suppress common mode noise as well as differential mode noise. RT1 is placed in series to limit inrush current during each power on. A relay is mounted across the RT1 to short the resistor when VOUT is higher than 95% rated voltage.

Power Stage – Boost type PFC converter

After the bridge rectifier BR1, there is a boost type PFC converter consisting of L2, Q2, D3 and C3. The third generation CoolMOS™ IPP60R199P is used as the power switch Q2. BR1, Q2 and SiC Diode D3 share the same heat sink so that the system heat can be equably spread. Output capacitor C3 provides energy buffering to reduce the output voltage ripple (100Hz) to the acceptable level and meet the holdup time requirement.

PWM control of boost converter

The ICE3PCS01G is a 14-pins control IC for power factor correction converters. It is suitable for wide range line input applications from 85 to 265 VAC with overall efficiency above 96%. The IC supports converters in boost topology and it operates in continuous conduction mode (CCM) with average current control.

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM) resulting in a higher harmonics but still meeting the Class D requirement of IEC 1000-3-2.

The outer voltage loop controls the output bulk voltage, integrated digitally within the IC. Depending on the load condition, internal PI compensation output is converted to an appropriate DC voltage which controls the amplitude of the average input current.

The IC is equipped with various protection features to ensure safe operating condition for both the system and device.

4 Circuit operation

4.1 Soft startup

During power up when the V_{OUT} is less than 95% of the rated level, internal voltage loop output increases from initial voltage under the soft-start control. This results in a controlled linear increase of the input current from 0A thus reducing the current stress in the power components.

Once V_{OUT} has reached 95% of the rated level, the soft-start control is released to achieve good regulation and dynamic response and VB_OK pin outputs 5V indicating PFC output voltage in normal range.

4.2 Boost follower

The IC provides adjustable lower step of bulk voltage in case of low line input and light output power. The low line condition is determined when pin BOP voltage is less than 2.3 V. Pin BOFO is connected to PWM feedback voltage through a voltage divider, representing the output power. The light load condition is determined when pin BOFO voltage is less than 0.5 V. Once these two conditions are met in the same time, a 20 uA current source is flowing out of pin VSENSE so that the bulk voltage should be reduced to a lower level in order to keep the VSENSE voltage same as the internal reference 2.5 V.

The reduced bulk voltage can be designed by upper side resistance of voltage divider from pin VSENSE. Thus the low side resistance is designed by the voltage divider ratio from the reference

2.5 V to the rated bulk voltage. An internal 300 kΩ resistor will be paralleled with external low side resistor of BOFO pin to provide the adjustable hysteresis for entry/exit power when boost follower is activated.

The boost follower feature will be disabled internally during PFC soft-start in order to prevent bulk voltage oscillation due to the unstable PWM feedback voltage. This feature can also be disabled externally by pulling up pin BOFO higher than 0.5 V continuously.

4.3 Gate switching frequency

The switching frequency of the PFC converter can be set with an external resistor R_{FREQ} at pin FREQ with reference to pin SGND. The voltage at pin FREQ is typical 1V. The corresponding capacitor for the oscillator is integrated in the device and the R_{FREQ}/frequency is given in Figure 2. The recommended operating frequency range is from 21 kHz to 100 kHz. As an example, a R_{FREQ} of 68 kΩ at pin FREQ will set a switching frequency F_{SW} of 65 kHz typically.

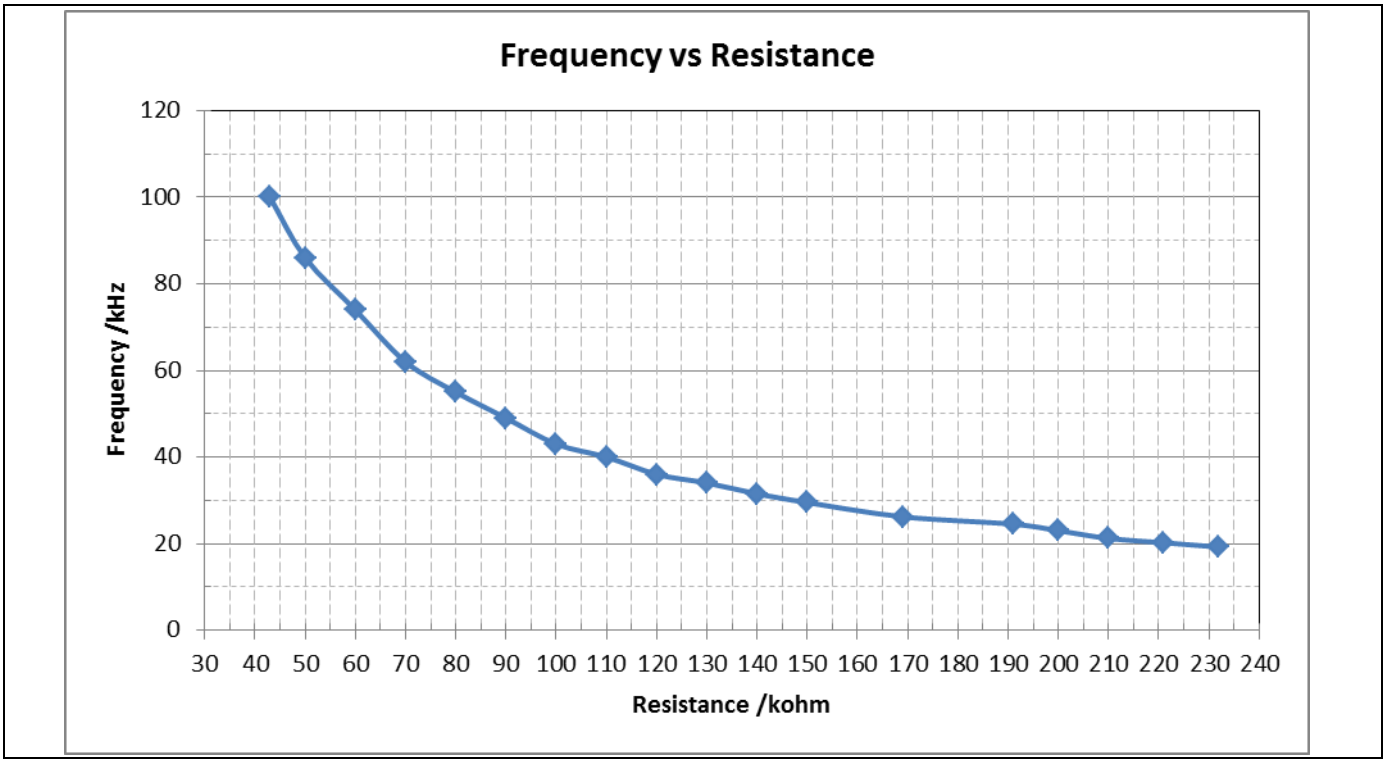


Figure 2 Frequency settings

The switching frequency can be synchronized to the external pulse signal after 6 external pulses delay once the voltage at the FREQ pin is higher than 2.5 V. The synchronization means two points. Firstly, the PFC switching frequency is tracking the external pulse signal frequency. Secondly, the falling edge of the PFC signal is triggered by the rising edge of the external pulse signal. The external R20 combined with R21 and the external diode, D6 can ensure FREQ pin voltage to be kept between 1.0 V (clamped internally) and 5 V (maximum pin voltage). If the external pulse signal has disappeared longer than 108 us (typical) the switching frequency will be synchronized to internal clock set by the external resistor R20.

4.4 Protection features

4.4.1 Input brown-out protection (BOP)

ICE3PCS01G provides a new BOP feature whereby it senses directly the input voltage for input brown-out condition via an external resistor/capacitor/diode network. This network provides a filtered value of V_{IN} which turns the IC on when the voltage at pin 9 (BOP) is more than 1.25 V. The IC enters into the fault mode when BOP goes below 1.0V. The hysteresis prevents the system to oscillate between normal and fault mode. Note also that the peak of V_{IN} needs to be at least 20% of the rated V_{OUT} in order to overcome open loop protection and power up system.

4.4.2 Open loop protection (OLP)

The open loop protection is available for this IC to safe-guard the output. Whenever voltage at pin VSENSE falls below 0.5 V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected). In this case, most of the blocks within the IC will be shutdown. It is implemented using a comparator with a threshold of 0.5 V.

4.4.3 First over-voltage protection (OVP1)

Whenever V_{OUT} exceeds the rated value by 8%, the first over-voltage protection OVP1 is active. This is implemented by sensing the voltage at pin VSENSE with respect to a reference voltage of 2.7V. A VSENSE voltage higher than 2.7 V will immediately block the gate signal. After bulk voltage falls below the rated value, gate drive resumes switching again.

4.4.4 Second over-voltage protection (OVP2)

The second OVP (OVP2) is provided in case that the first one fails due to the aging or incorrect resistors connected to the VSENSE pin. This is implemented by sensing the voltage at pin OVP with respect to a reference voltage of 2.5 V. When voltage at OVP pin is higher than 2.5 V, the IC will immediately turn off the gate, thereby preventing damage to bus capacitor.

When the bulk voltage drops out of the hysteresis, which is below 2.3 V the IC can be latched further or begin auto soft-start. These two protection modes are distinguished through detecting the external equivalent resistance connecting to VBTHL_EN pin after V_{CC} is higher than UVLO threshold. If the equivalent resistance is higher than 100kΩ the IC selects latch mode for second OVP, otherwise auto soft-start mode.

In normal operation the trigger level of OVP2 should be designed higher than OVP1. However in the condition of mains transient overshoot the bulk voltage may be pulled up to the peak value of mains that is higher than the threshold of OVP1 and OVP2. In this case the OVP1 and OVP2 are triggered in the same time the IC will shut down the gate drive until bulk voltage falls out of the two protection hysteresis, then resume the gate drive again

4.4.5 Peak current limit

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin ISENSE reaches -0.2 V. This voltage is amplified by a factor of -5 and connected to comparator with a reference voltage of 1.0 V. A deglitcher with 200 ns after the comparator improves noise immunity to the activation of this protection. In other words, the current sense resistor should be designed lower than -0.2 V PCL for normal operation.

4.4.6 IC supply under voltage lockout

When V_{CC} voltage is below the under voltage lockout threshold V_{CCUVLO}, typical 11 V, IC is off and the gate drive is internally pull low to maintain the off state. The current consumption is down to 1.4 mA only.

4.4.7 Bulk Voltage Monitor and Enable Function (VBTHL_EN)

The IC monitors the bulk voltage status through VSENSE pin and output a TTL signal to enable PWM IC or control inrush relay. During soft-start once the bulk voltage is higher than 95% rated value, pin VB_OK outputs a high level. The threshold to trigger the low level is decided by the pin VBTHL voltage adjustable externally.

When pin VBTHL is pulled down externally lower than 0.5 V most function blocks are turned off and the IC enters into standby mode for low power consumption. When the disable signal is released the IC recovers by soft-start.

5 Circuit diagram

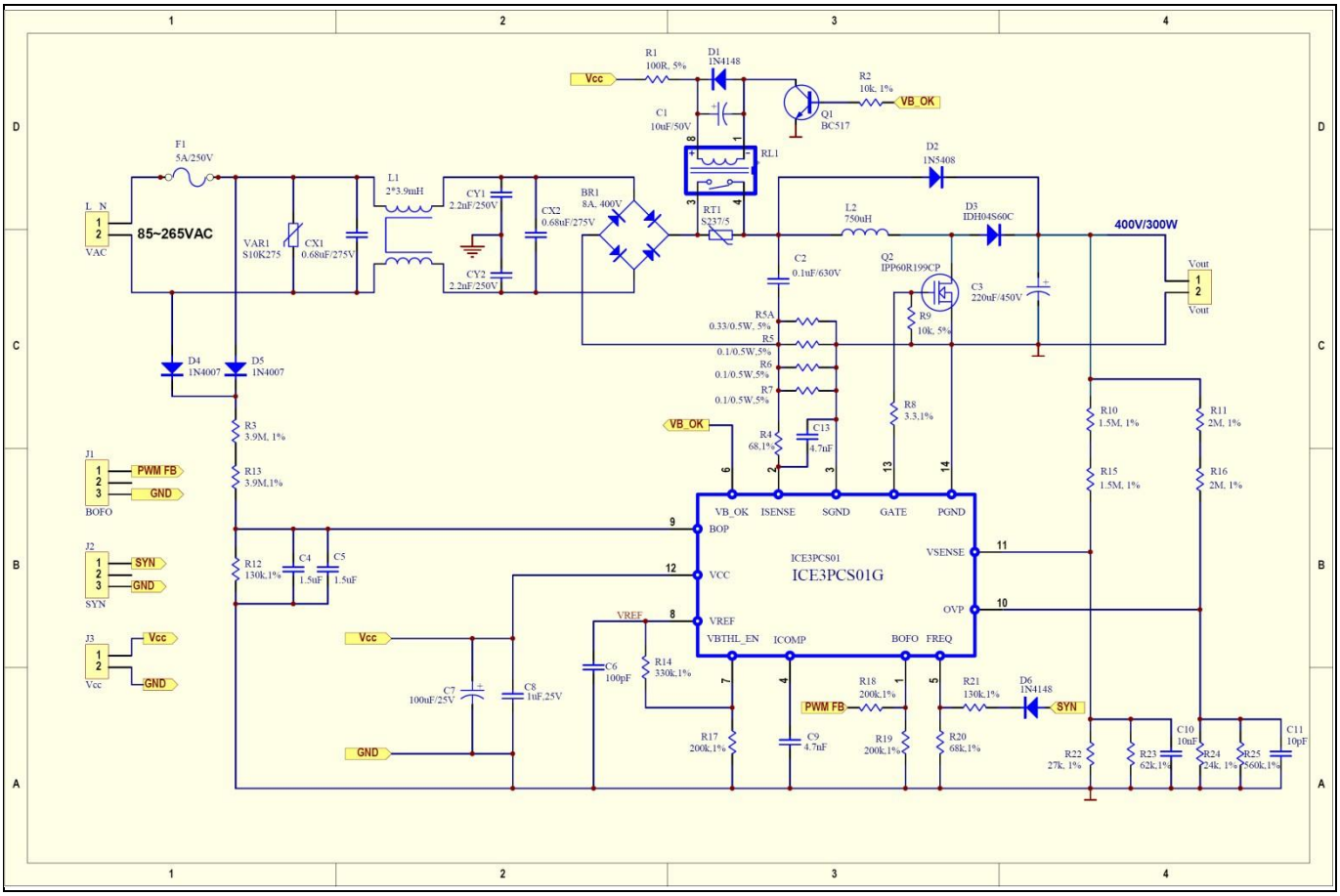


Figure 3 Schematic of 300 W PFC demo board

6 PCB layout

6.1 Top layer view

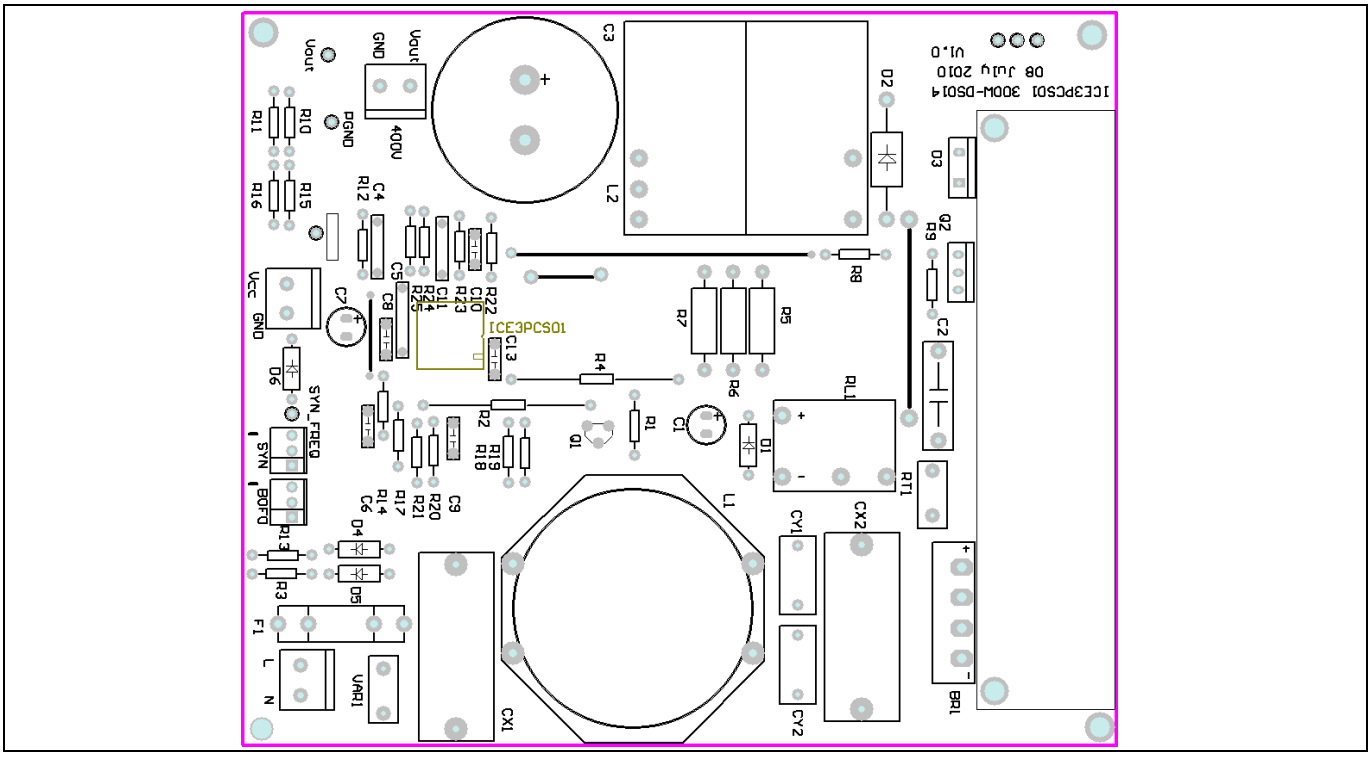


Figure 4 Top layer view

6.2 Bottom layer view

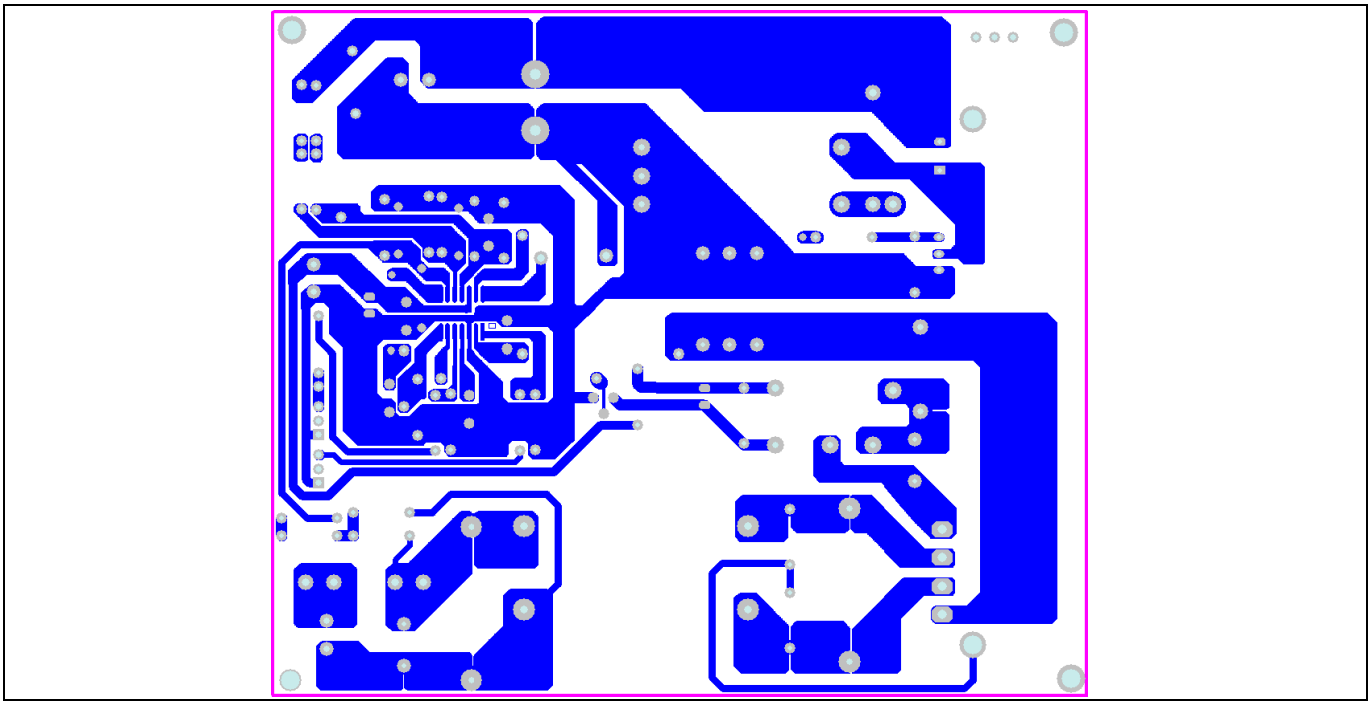


Figure 5 Bottom layer view

7 Component list

Designator	Part type	Description	Manufacturer/ Part No.
BR1	8A, 400V	Bridge Rectifier	Vishay / KBU8G
C1	10uF/50V	Electrolytic Cap	
C2	0.1uF/630V	Ceramic Cap	Epcos / B32652A6104J
C3	220uF/450V	Electrolytic Cap	Epcos / B43304C5227M
C4	1.5 uF/50V	Ceramic Cap	
C5	1.5 uF/50V	Ceramic Cap	
C6	100pF/50V	Ceramic Cap	
C7	100uF/25V	Electrolytic Cap	
C8	1uF/25V	Ceramic Cap	
C9	4.7nF/50V	Ceramic Cap	
C10	10nF/50V	Ceramic Cap	
C11	10pF/50V	Ceramic Cap	
C13	4.7nF/50V	Ceramic Cap	
CX1	0.68uF, X1, 275V	Ceramic Cap	Epcos / B32922C3474M
CX2	0.68uF, X1, 275V	Ceramic Cap	Epcos / B32922C3474M
CY1	2.2nF, Y2, 250V	Ceramic Cap	Epcos / B81123C1222M000
CY2	2.2nF, Y2, 250V	Ceramic Cap	Epcos / B81123C1222M000
D1	1N4148	Diode	
D2	1N5408	Diode	Vishay / 1N5408
D3	IDH04S60C	Diode	Infineon Technologies
D4	1N4007	Diode	Vishay / 1N4007
D5	1N4007	Diode	Vishay /1N4007
D6	1N4148	Diode	
F1	5A	Fuse	
IC1	ICE3PCS01G	DSO-14	Infineon Technologies
J1	Jumper	Connector (BOFO)	
J2	Jumper	Connector (SYNC)	
J3	Jumper	Connector (V_{CC})	
J4	Jumper	Connector (V_{IN})	
J5	Jumper	Connector (V_{OUT})	
L1	2*3.9mH	CM Choke	Epcos / B82725J2602N20
L2	750uH	PFC Choke	
Q1	BC517	NPN Transistor	
Q2	IPP60R199CP	Power MOSFET	Infineon Technologies
R1	100R/0.25W, 5%	Carbon Film Resistor	
R2	10k/0.25W, 1%	Carbon Film Resistor	
R3	3.9M/0.25W, 1%	Carbon Film Resistor	
R4	68/0.25W, 1%	Carbon Film Resistor	

Component list

R5A	0.33/0.5W, 5%	Metal Film Resistor	
R5	0.1/0.5W, 5%	Metal Film Resistor	
R6	0.1/0.5W, 5%	Metal Film Resistor	
R7	0.1/0.5W, 5%	Metal Film Resistor	
R8	3.3/0.25W, 1%	Carbon Film Resistor	
R9	10k/0.25W, 5%	Carbon Film Resistor	
R10	1.5M/0.25W, 1%	Carbon Film Resistor	
R11	2M/0.25W, 1%	Carbon Film Resistor	
R12	130k/0.25W, 1%	Carbon Film Resistor	

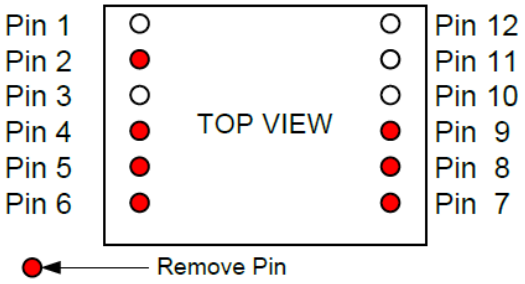
8 Boost Choke Layout

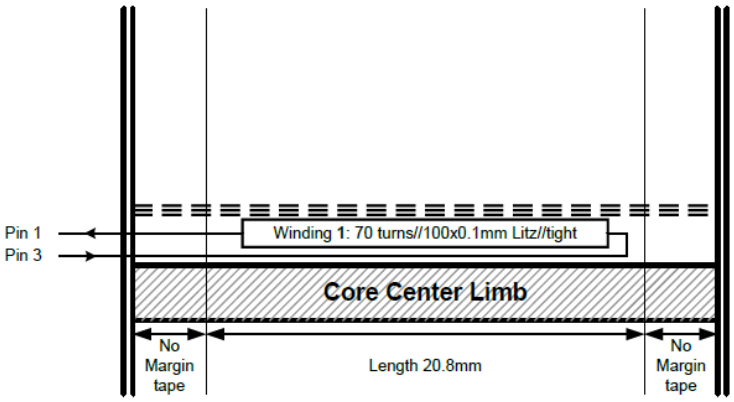
Core: PQ-core PQ3535 (TDK)

Material: PC95

Inductance: L=750uH

Windings	Start	End	Wire	Turns	Layers	Method
1	**1**	**3**	100x0.1mm Litz	70	4 or 5	Tight





9 Test report

All test condition are supply with Vcc = 20 V.

9.1 Load and line test

Input	V_{IN}	I_{IN}	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	Eff.	PF
85Vac	84.88	0.27	21.99	395.70	0.05	20.90	95.07	0.98
	84.75	0.50	42.25	395.70	0.10	40.43	95.69	0.99
	84.64	0.72	60.55	395.70	0.15	57.99	95.78	0.99
	84.46	0.98	82.66	395.70	0.20	79.16	95.76	1.00
	84.32	1.22	102.56	395.70	0.25	98.52	96.06	1.00
	83.99	1.83	153.71	395.70	0.37	147.67	96.07	1.00
	83.59	2.49	207.71	395.70	0.50	199.03	95.82	1.00
	83.29	3.10	257.86	395.70	0.62	246.26	95.50	1.00
	82.89	3.76	310.84	395.70	0.75	295.84	95.17	1.00
115Vac	114.84	0.21	21.95	395.70	0.05	20.90	95.19	0.93
	114.75	0.38	42.36	395.70	0.10	40.84	96.43	0.98
	114.67	0.53	59.97	395.70	0.15	57.98	96.68	0.99
	114.53	0.72	81.78	395.70	0.20	79.33	97.01	0.99
	114.43	0.89	101.66	395.70	0.25	98.51	96.90	1.00
	114.18	1.34	152.27	395.70	0.37	147.69	96.99	1.00
	113.90	1.81	205.23	395.70	0.50	198.99	96.96	1.00
	113.69	2.24	254.16	395.70	0.62	246.15	96.85	1.00
	113.36	2.70	305.67	395.70	0.75	295.73	96.75	1.00
230Vac	229.84	0.16	21.90	395.70	0.05	20.89	95.37	0.58
	229.79	0.23	42.15	395.70	0.10	40.85	96.92	0.80
	229.76	0.30	59.43	395.70	0.15	57.96	97.54	0.88
	229.69	0.38	81.17	395.70	0.20	79.35	97.75	0.92
	229.64	0.46	100.56	395.70	0.25	98.48	97.93	0.95
	229.52	0.67	150.32	395.70	0.37	147.66	98.23	0.97
	229.38	0.90	202.36	395.70	0.50	198.91	98.30	0.98
	229.27	1.10	250.09	395.70	0.62	245.99	98.36	0.99
	229.10	1.32	300.44	395.70	0.75	295.58	98.38	0.99
265Vac	264.87	0.17	21.85	395.70	0.05	20.87	95.55	0.48
	264.83	0.22	42.14	395.70	0.10	40.86	96.95	0.71
	264.80	0.28	59.52	395.70	0.15	57.96	97.38	0.81
	264.76	0.35	81.24	395.70	0.20	79.37	97.70	0.87
	264.69	0.42	100.58	395.70	0.25	98.46	97.89	0.92
	264.59	0.60	150.30	395.70	0.37	147.68	98.26	0.95
	264.47	0.78	202.05	395.70	0.50	198.90	98.44	0.97
	264.37	0.96	249.75	395.70	0.62	245.97	98.49	0.98
	264.22	1.15	299.93	395.70	0.75	295.54	98.54	0.99

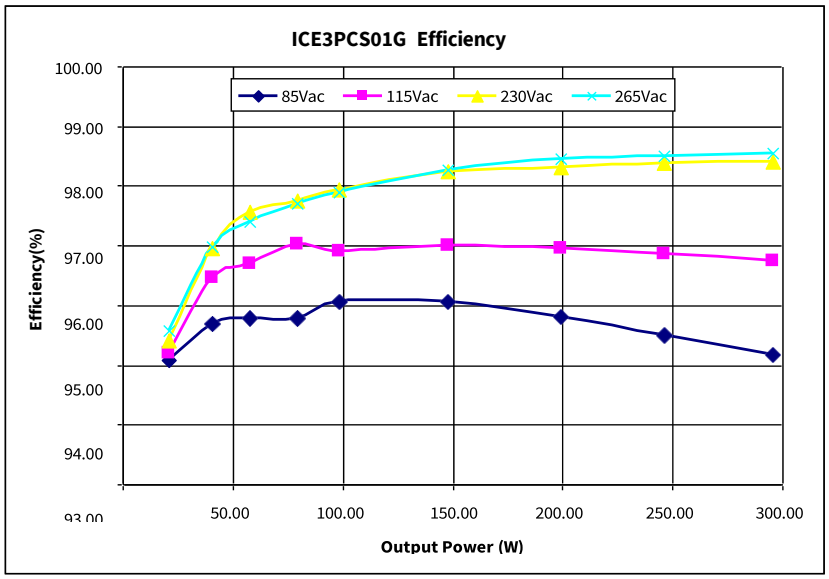


Figure 6 PFC stage efficiency

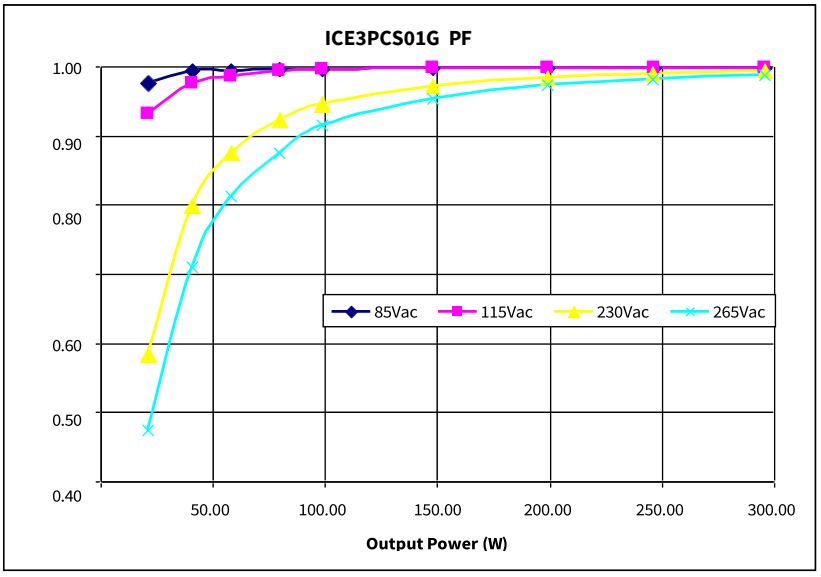


Figure 7 Power factor

9.2 Load and line test in boost follower mode

Input	V_{in}	I_{in}	P_{in}	V_{out}	I_{out}	P_{out}	Eff.	PF
85Vac	84.88	0.28	23.52	333.53	0.07	22.51	95.69	0.98
	84.79	0.47	39.38	333.53	0.11	38.09	96.72	0.99
	84.67	0.74	62.22	333.53	0.18	59.82	96.14	1.00
	84.57	0.96	80.87	333.53	0.23	77.83	96.25	1.00
	84.44	1.23	103.28	333.53	0.30	99.47	96.32	1.00
	84.15	1.85	155.70	333.53	0.45	149.83	96.23	1.00
	83.87	2.45	205.07	333.53	0.59	196.81	95.97	1.00
	83.55	3.13	260.78	333.53	0.75	249.27	95.59	1.00
	83.26	3.77	313.24	333.53	0.89	298.15	95.18	1.00

115Vac	114.84	0.22	23.50	333.53	0.07	22.50	95.75	0.94
	114.78	0.35	39.46	333.53	0.12	38.43	97.39	0.97
	114.69	0.54	61.59	333.53	0.18	59.80	97.09	0.99
	114.61	0.70	80.09	333.53	0.23	77.80	97.14	0.99
	114.52	0.90	102.44	333.53	0.30	99.47	97.10	1.00
	114.31	1.35	154.17	333.53	0.45	149.78	97.15	1.00
	114.11	1.78	202.70	333.53	0.59	196.77	97.07	1.00
	113.88	2.26	257.07	333.53	0.75	249.23	96.95	1.00
	113.67	2.71	307.99	333.53	0.89	297.98	96.75	1.00

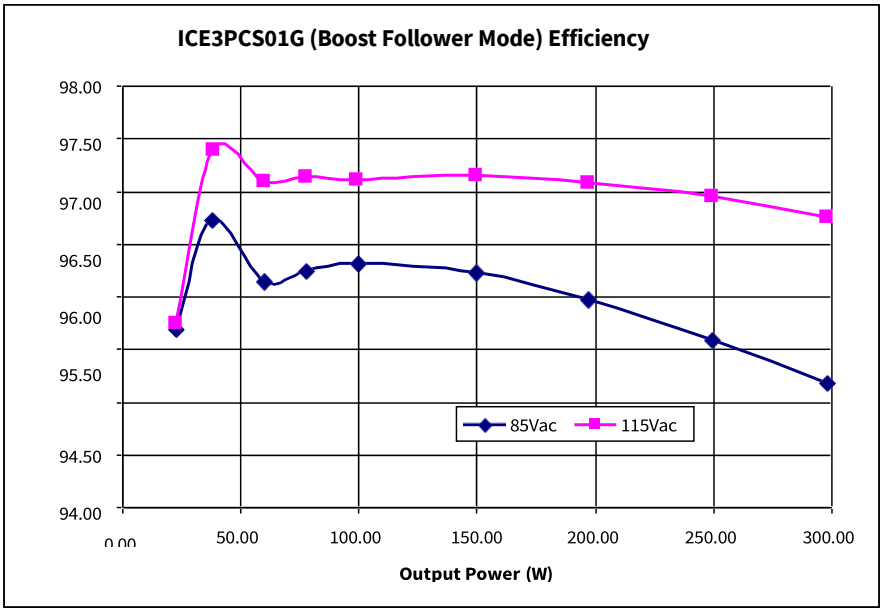


Figure 8 Power stage efficiency at boost follower mode

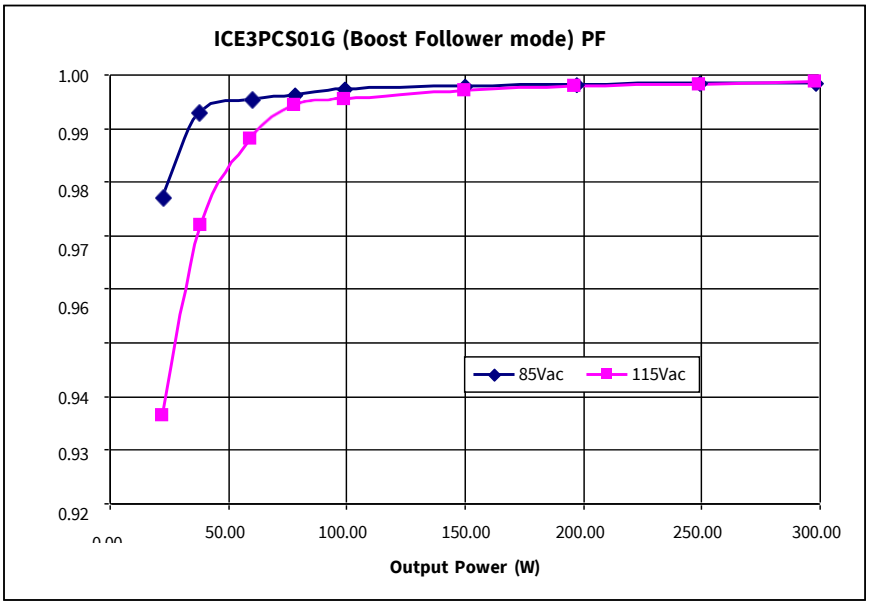


Figure 9 Power factor at boost follower mode

9.3 Harmonic test according to EN61000-3-2 Class D requirement

Test condition I: 85 VAC input, full load (300 W output).

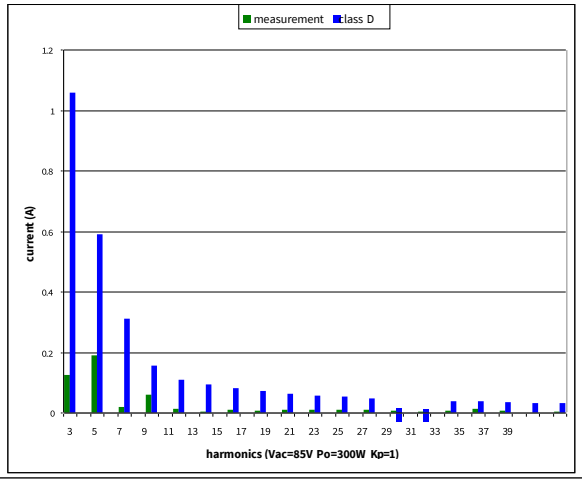


Figure 10 Harmonics in normal operation

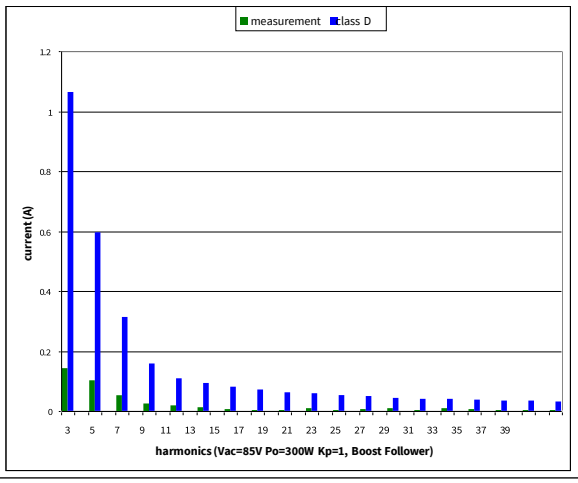


Figure 11 Harmonics in boost follower

Test condition II: 85 VAC input, 10% of full load (30 W output).

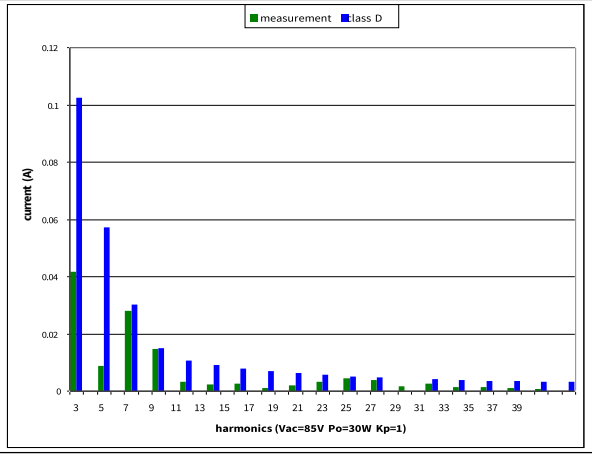


Figure 12 Harmonics in normal operation

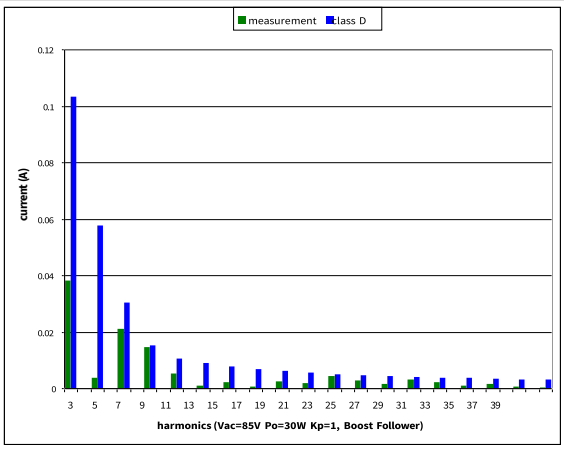


Figure 13 Harmonics in boost follower

Test report

Test condition III: 265 VAC input

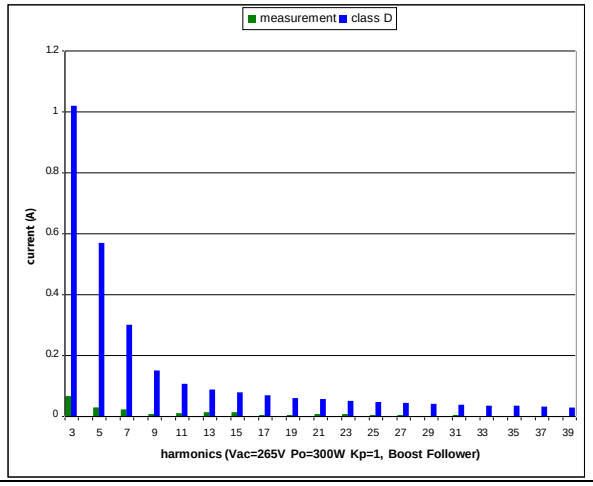


Figure 14 Harmonics at 300 W output

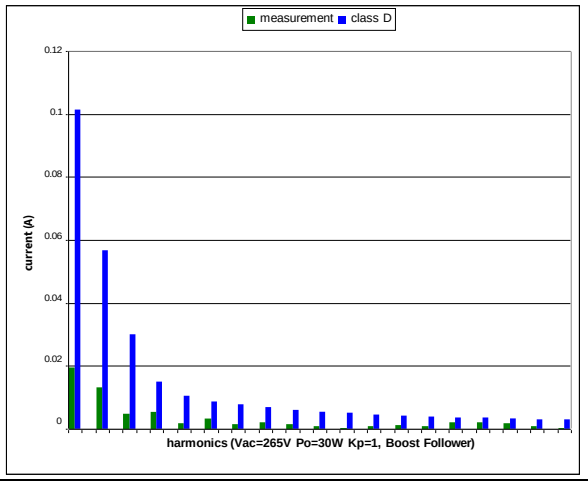
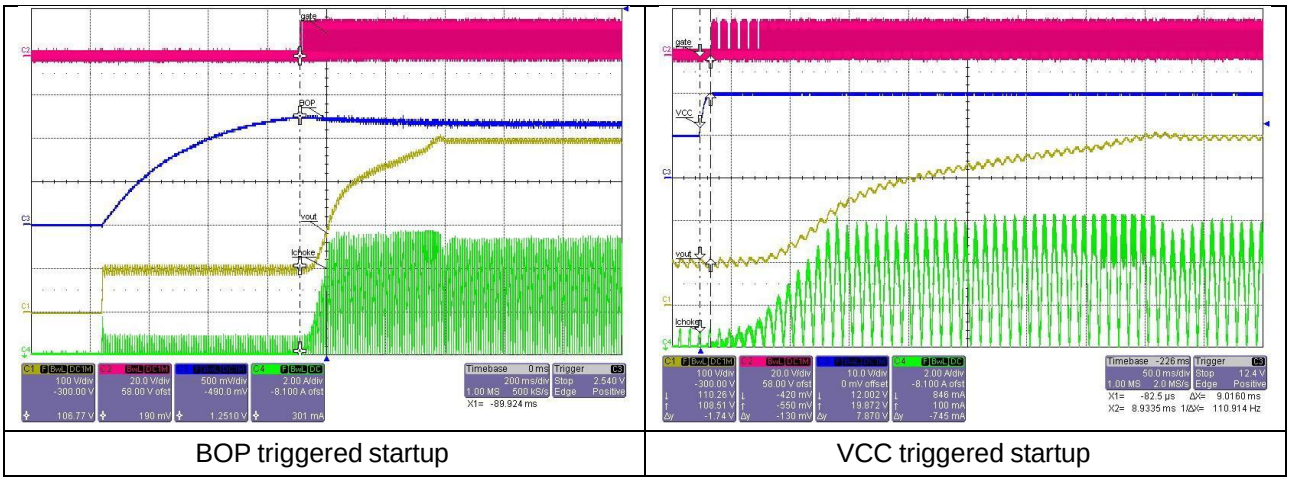


Figure 15 Harmonics at 30 W output

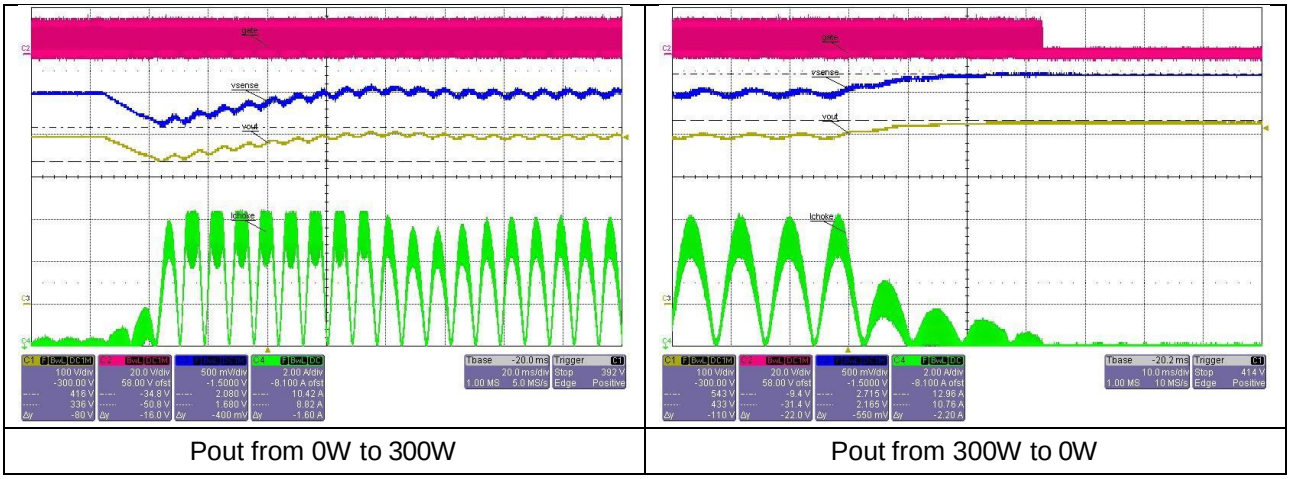
10 Test waveforms



BOP triggered startup	VCC triggered startup

Figure 16 Startup test at 85 VAC, 300 W

During startup the average current of PFC choke increases from zero to maximum limited by PCL and PFC output voltage rises gradually with very slight overshoot.

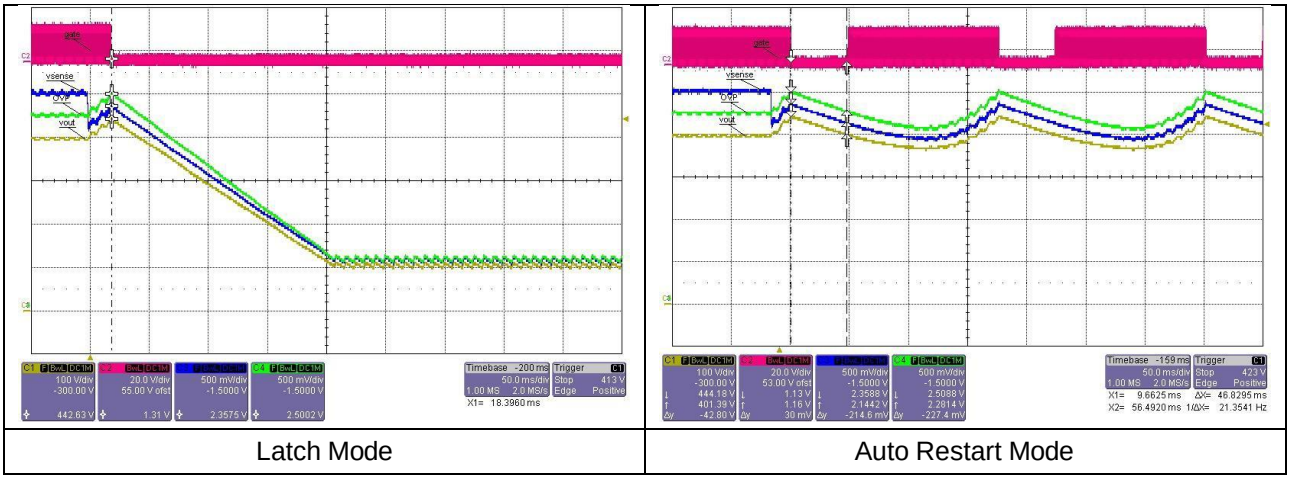


Pout from 0W to 300W	Pout from 300W to 0W

Figure 17 Load jump test at 85 VAC

The under shoot of output voltage is only 60 V when load jump from no load to full load at 85Vac while the overshoot is within 35 V vice versa. The choke current shows no distortion during load dynamic change.

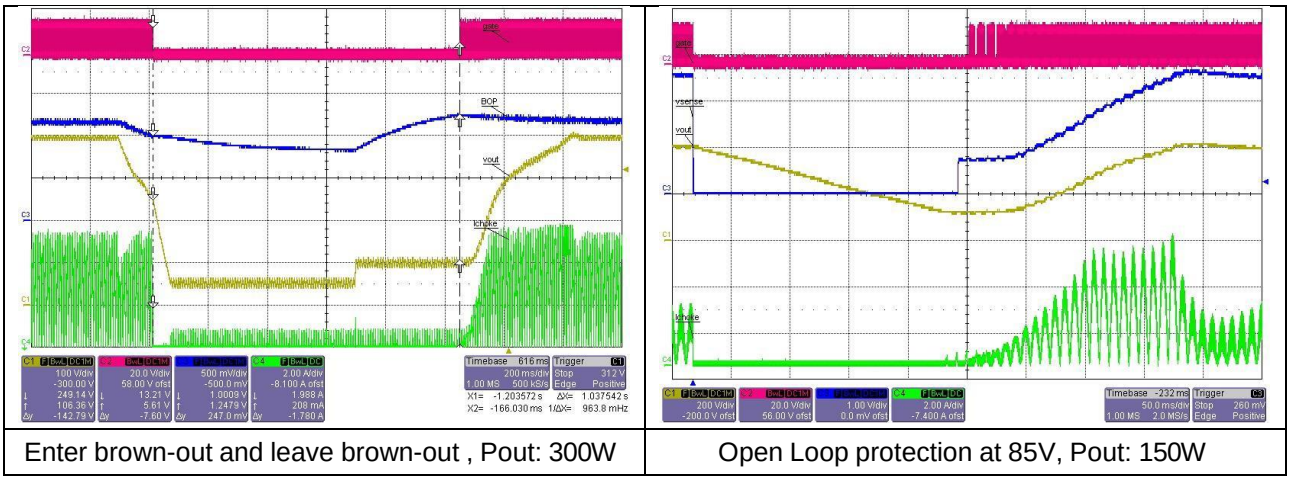
Test waveforms



Latch Mode	Auto Restart Mode

Figure 18 OVP2 test

Wen OVP2 happens the gate drive can be latched off continuously as shown in left picture or enter auto startup as shown in right picture depending on the equivalent resistance at VBTHL pin.



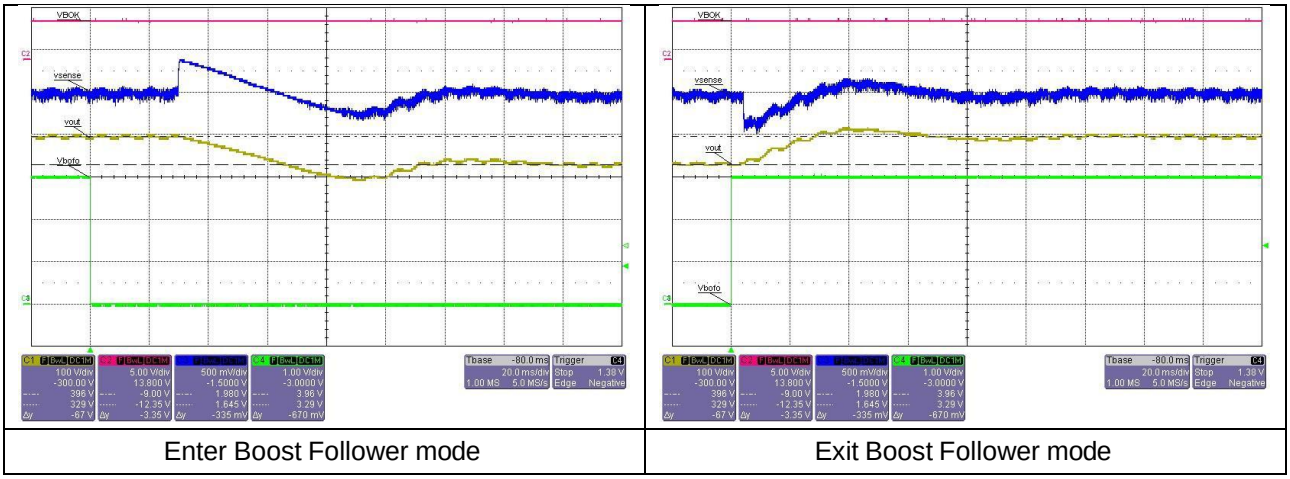
Enter brown-out and leave brown-out , Pout: 300W	Open Loop protection at 85V, Pout: 150W

Figure 19 Brownout and OLP test

The gate drive is latched off once BOP pin voltage is lower than 1 V and initiates another soft-startup once BOP voltage is higher than 1.25 V as shown in the left picture.

The gate drive can also be latched off once Vsense pin voltage is below 0.5 V indicating an inadequate output voltage and initiates another soft-startup once Vsense voltage is higher than 0.5 V as shown in the right picture.

Test waveforms



Enter Boost Follower mode	Exit Boost Follower mode

Figure 20 Boost follower mode test

During low line condition the output voltage is able to step down to 329 V by pulling BOFO pin voltage below 0.5 V in left picture and recovers to normal output voltage 400 V vice versa in right picture.

11 References

[1] ICE3PCS01G datasheet, Infineon Technologies AG, 2010.

[2] “Design tips for CCM PFC controller ICE2PCSxx”, Application Note, Infineon Technologies AG, 2008.

[3] “300W PFC evaluation board with CCM PFC controller ICE2PCS01”, Application Note, Infineon Technologies AG, 2009.

[4] “ICE1PCS01 based boost type CCM PFC design guide – control loop modeling”, Application Note, Infineon Technologies AG, 2007.

12 Revision history

Document version	Date of release	Description of changes
2.1	2023-01-11	Editorial changes
2.0	2018-01-20	Figure 2: Maximum switching frequency changed to 100 kHz Page 5, 6 ,7: Maximum switching frequency changed to 100 kHz Page 5: Maximum synchronous switching frequency changed to 100 kHz
1.1	2013-06-13	Editiorial changes
1.0	2012-10-21	Initial release

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