CoolGaN™ application note

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About this document

Scope and purpose

This document describes the main features of Infineon's 600 V CoolGaN™ enhancement-mode (normally off) gallium nitride (GaN) power transistors. The main focus is on the differences between GaN transistors and the more well-known silicon (Si) power transistors, and how these differences can benefit power converter applications like high-performance power supplies used in data centers and telecom applications.

The purpose of the document is to enable the reader to successfully use CoolGaN™ devices and obtain the best possible performance.

Intended audience

This application note is intended for readers familiar with power electronic design, power supply design, and the use of existing 600 V power transitors like Infineon CoolMOS™.

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1 What is CoolGaN™?

CoolGaN™ is a high-performance transistor technology for power conversion in the voltage range up to 600 V. The active region of the transistor is fabricated using GaN and AlGaN semiconductor materials grown on top of a Si substrate. The lateral transistor structure features very low gate and output charge, fast switching, and no body diode or reverse recovery charge. As a result of these characteristics, CoolGaN™ transistors can be used to design very high-efficiency and high-frequency power-conversion circuits, especially in topologies like half-bridge where conventional Si MOSFETs do not perform well because of their very large reverse recovery charge.

A native GaN transistor has a depletion-mode gate, meaning it has a normally on characteristic, making it unsuitable for power electronic applications by itself. By adding a p-type gate, however, the threshold voltage is increased from a negative to a positive voltage, thus making an enhancement-mode (normally off) transistor. Infineon's CoolGaN™ is made with a self-clamping p-gate structure that additionally solves the problem of gate Over Voltage (OV) sensitivity found in reverse-Schottky p-gate GaN transistors manufactured by others. The following sections give more detail about the device structure and performance characteristics, and compare these transistors to conventional superjunction (SJ) MOSFETs.

1.1 Device structure

The GaN High Electron Mobility Transistor (HEMT) is a planar device with lateral current flow, compared to a Si SJ MOSFET in which the current flow is predominantly vertical. A cross-section is shown in Figure 1. The starting point is a Si substrate, which is used because of its mature supply infrastructure and low cost. Transition layers are then epitaxially grown onto the Si substrate for the purpose of providing a better match between the crystal lattice and thermal expansion coefficient differences between Si and GaN. Following the transition layers, additional layers of GaN, AlGaN and p-doped GaN are deposited and etched to create the structure seen in Figure 1. Finally metallization and passivation layers are added to complete the transistor structure.

The conduction path between the drain and source contacts is the so called Two-Dimensional Electron Gas (2DEG) that is formed at the heterojunction between the GaN and AlGaN layers (shown in red in Figure 1). The 2DEG is enhanced or depleted by the potential difference between the gate and the 2DEG below it. This is how the transistor is turned on and off. The p-gate raises the potential high enough to make the device have a positive threshold voltage and therefore operate in enhancement mode (normally off). Otherwise the device would be normally on and require a negative bias to remain off, which is not preferred for power electronic applications.

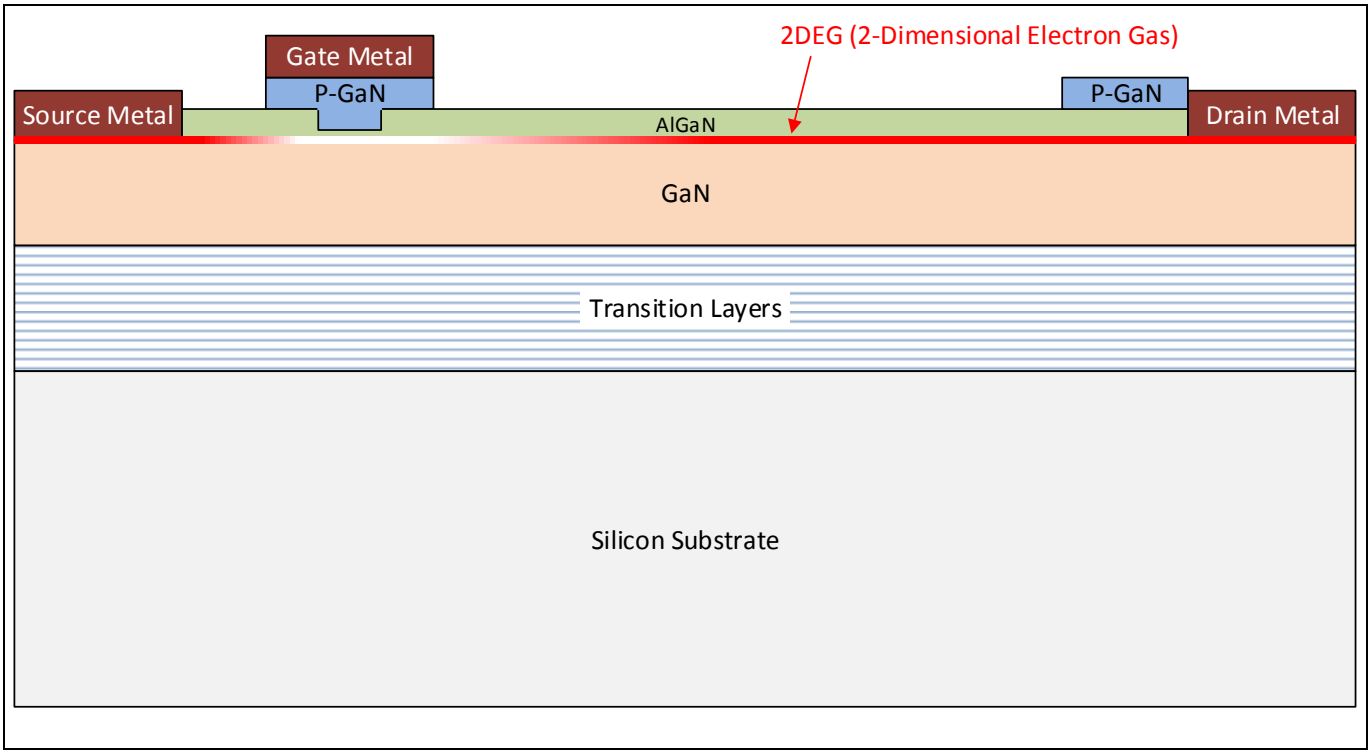

Figure 1 Cross-section of a p-gate GaN HEMT

1.2 Electrical model of the p-gate GaN HEMT

In its simplest form, the GaN HEMT can be thought of as a resistor whose conductivity is controlled by an applied gate voltage – in many ways, very similar to a MOSFET. A more detailed equivalent circuit is shown in Figure 2. The heart of this model is a bidirectional current source between D'' and S''. This current source represents the current conducting channel (2DEG), which is enhanced or depleted depending on $V_{G''S''}$. Assuming a non-negative V_{DS}, when $V_{G''S''}$ is less than the threshold voltage (approximately 1.4 V), the current source is an open circuit and the HEMT is in the off-state. As gate drive is increased, $V_{G''S''}$ exceeds V_{th} and the 2DEG conducts current. When fully enhanced, the current source resistance becomes zero, and the overall on-resistance is then represented by the sum of 0.2 $R_{DS(on)}$ + 0.8 $R_{DS(on)}$

The channel resistance $R_{DS(on)}$ is shown split into the lower portion (20 percent of $R_{DS(on)}$), and the remaining upper portion (80 percent of $R_{DS(on)}$). This represents the physical position of the gate – the distance between gate and source is four times smaller than the distance between gate and drain. The reason for this asymmetry is to optimize the electric field distribution in the region between the gate and drain.

Also note that in Figure 2, there are two source connections: one is the main source connection for high current (S), and the other is the source Kelvin connection (SK) for the gate-driver circuit. The purpose of the SK connection is to provide the gate-driver circuit with direct access to the source bond-pad. This helps to minimize common source impedance effects which can slow down the switching speed of the device, because voltage developed across the common source impedance will subtract from the applied gate voltage, thus reducing the effective gate drive.

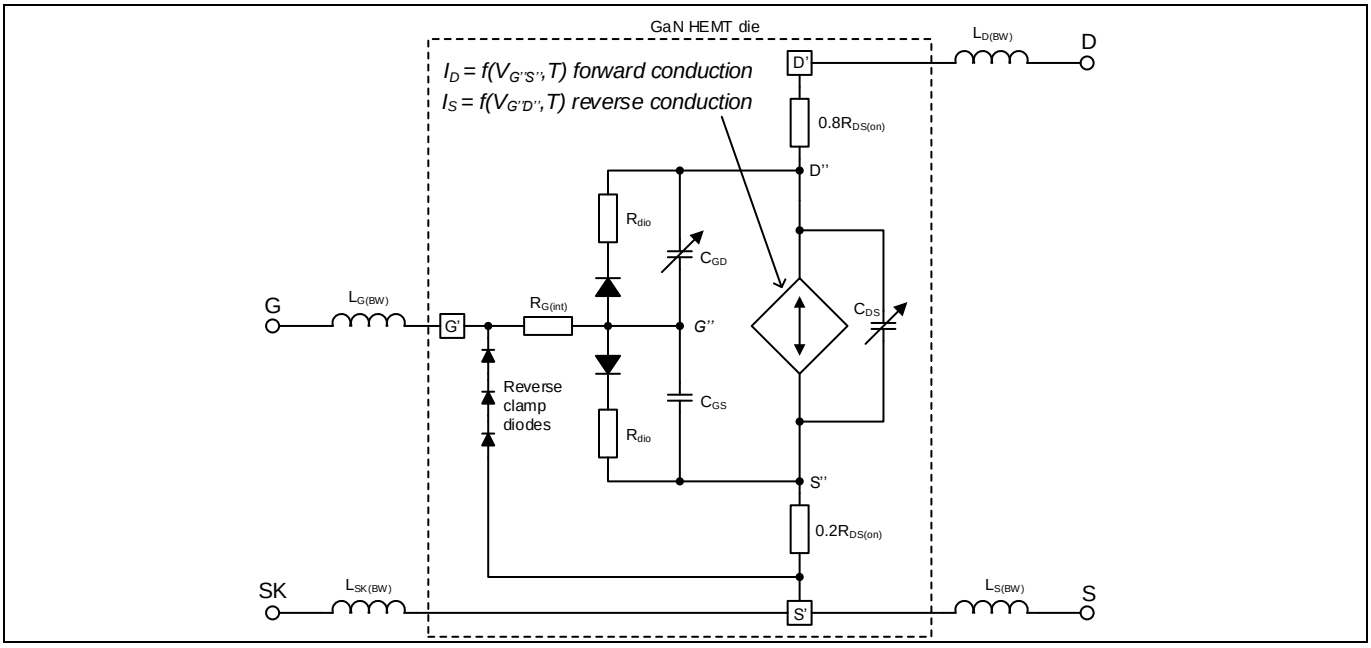

Figure 2 Electrical model of a p-gate GaN HEMT

The model in Figure 2 is similar to a traditional MOSFET with two important differences. First, the GaN HEMT has no intrinsic body diode from source to drain like a SJ MOSFET, for example. And second, the gate does have a diode structure that clamps the gate-source (or gate-drain) voltage to approximately 3.5 V. The exact voltage will vary with the temperature-dependent diode forward voltage, and the gate current running through the internal $R_{G(int)}$ plus the diode impedance R_{dio}. As a result of these impedances and shared current paths, $V_{G''S''}$, which controls the 2DEG enhancement, is a function of both gate current and drain current.

Due to these factors, it is not feasible to specify a single externally measured gate-source voltage that will properly enhance the gate under all variations of temperature and drain current. For example, at high temperature and maximum drain current, a V_{GS} of 4V may be just enough to keep the device on and result in a gate current of 10 mA. But at a lower temperature and zero drain current, the same applied V_{GS} could result in hundreds of mA of unnecessary gate current. Moreover, specifying an absolute maximum gate voltage is not feasible due to the I_D and temperature dependency.

For these reasons, the nominal and maximum gate voltages in the forward direction are not specified: only the gate current is specified, as the p-gate diode will clamp the voltage to a safe level even at the maximum specified gate current.

When V_{DS} goes negative, in a traditional MOSFET, the parasitic body diode begins to conduct. But in the GaN HEMT, there is no intrinsic body diode – instead the HEMT turns back on and behaves like a diode with a forward voltage that depends on gate voltage. The reason for this behavior is that the HEMT will turn on when the gate voltage is higher than either the source or the drain voltage. So if V_{GS} is at zero, and the drain goes negative by more than the threshold voltage, the HEMT turns back on, with the drain acting as an alternate source. Normally this diode mode is only used during a short dead-time interval in the circuit operation, then the gate is turned back on using the normal forward-biased gate source, and the transistor will conduct drain current in either direction again.

1.3 Key advantages of GaN HEMT

CoolGaN™ transistors offer improved performance over silicon transistors (like SJ MOSFETs) due to several key characteristics:

Output charge Q_{oss}: Traditional Si SJ 600 V power transistors have a very non-linear output charge characteristic. As V_{DS} is increased from 0 to about 25 V, the charge increases rapidly at a steep slope. Then suddenly the slope flattens out, and the charge only increases a small additional amount as V_{DS} is further increased all the way to 400 V or more. CoolGaN™ has a mostly linear characteristic, and the overall charge is much lower. Comparing the same $R_{DS(on)}$ CoolGaN™ with the SJ, the CoolGaN™ Q_{oss} is about 10 times lower. This is a significant benefit in soft-switching circuits, shortening the required dead-time and enabling higher-frequency operation without additional loss.

E_{oss} – the energy stored in Q_{oss}: While the Q_{oss} mentioned above is an order of magnitude improved in GaN compared to SJ, the difference in the energy stored in C_{oss} is much smaller. This paradox is due to the non-linear nature of the output capacitance of SJ, where most of the charge is accumulated at low V_{DS} and therefore lower energy compared to the more linear capacitance of the GaN HEMT. The result is that E_{oss} is a relatively modest 25 percent improvement compared to SJ. So the big advantage of GaN in hard-switching applications is not primarily that E_{oss} is lower, the key benefit is that the GaN HEMT has no body diode recovery issues, so it can be applied effectively in hard-switching half-bridge applications like totem-pole Power Factor Correction (PFC) circuits operating in Continuous Current Mode (CCM) and achieve extremely high efficiencies. This is covered in the next section.

Reverse-recovery charge Q_{rr}: The reverse recovery performance of CoolGaN™ is perhaps the biggest single benefit of GaN compared to Si transistors. 600 V Si power transistors have intrinsic body diode structures with a large reverse recovery charge and associated peak current. It is so large that SJ is generally not applied to topologies or control strategies that include repetitive reverse recovery requirements, for example hard-switching half-bridge. CoolGaN™ transistors have no Q_{rr} because there are no minority carriers in the channel to recover. Because of this, GaN enables a whole new class of topologies that, for the first time, can be effectively and efficiently deployed for improved performance.

Gate charge Q_g: Gate charge affects how quickly the transistor can be switched on and off, and how frequently – as in the power required to operate the gate-drive circuit at high frequencies. Low gate charge is a desired characteristic in power transistors. Again, comparing CoolGaN™ to SJ with the same $R_{DS(on)}$, GaN has about seven times lower Q_g than SJ.

Conduction losses: The temperature coefficient of $R_{DS(on)}$ for CoolGaN™ is lower than for Si SJ. Over the range from 25°C to 150°C, the typical temperature coefficient of $R_{DS(on)}$ for GaN is 2.0, compared to 2.4 for SJ. The 20 percent difference in temperature coefficient means that for the same $R_{DS(on)}$ rating, the CoolGaN™ conduction losses will be lower at operating temperature.

As a result of these key transistor characteristics, switched-mode power circuits using CoolGaN™ can benefit from improved energy efficiency and/or improved power density that is not possible with state-of-the-art Si devices.

2 Key differences between 600 V CoolGaN™ and 600 V silicon power transistors

Most power electronic designers are already familiar with using conventional HV Si power transistors like SJ MOSFETs. The following section covers the key differences between these technologies.

2.1 Gate characteristics

One of the biggest differences between a Si MOSFET and a CoolGaN™ HEMT is the structure and characteristics of the gate. Si MOSFET gates are insulated, so behave essentially like a non-linear capacitor. The CoolGaN™ gate is not insulated, so it does not have any dielectric breakdown voltage. The ohmic p-gate forms a GaN diode that becomes forward biased as the gate is driven in the forward direction. If the gate is driven to a negative voltage, the gate diode is reverse biased, so there is no continuous current, unless the voltage is large enough to turn on the protection diodes (see Figure 6).

2.1.1 Gate threshold voltage

CoolGaN™ HEMTs are enhancement-mode devices, meaning normally off when V_{GS} = 0 V. The threshold voltage of V_{GS} is defined as the gate-source voltage at which measurable drain current begins to flow. In the case of 70 mΩ HEMT, the drain current for defining threshold voltage is 2.6 mA.

The temperature coefficient of $V_{GS(th)}$ has a small negative slope of approximately -750 µV/°C, as can be seen in Figure 3, which shows the typical threshold voltage with upper and lower limits across the full temperature range.

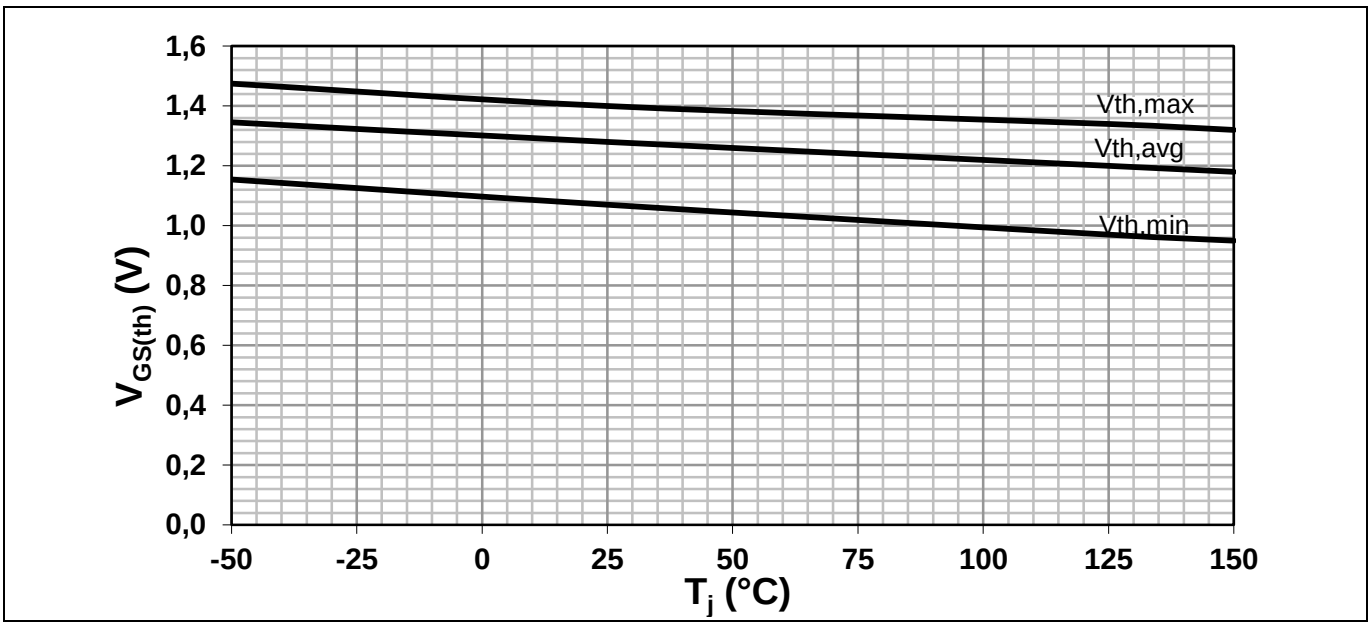

Figure 3 Gate threshold voltage vs temperature

2.1.2 V_{GS} voltage and current limits

As described in section 1.2, the gate voltage in the forward direction is a function of both gate current and drain current. Therefore, the datasheet does not specify a forward gate voltage limit, only a forward gate current limit, as shown in Figure 4. In the negative direction, the gate voltage is clamped by a protection diode circuit

(seen in Figure 2), which begins clamping at about -12 V. The peak voltage in the negative direction is also shown in the example table of Figure 4.

Gate current, continuous	I_G	-	-	20	mA	T_J = 0 to 150°C; Refer to gate-drive AN
Gate current, pulsed	$I_{G,pulse}$	-	-	2000	mA	T_J = 0 to 150°C; t_{PULSE} = 50 ns, f = 100 kHz Refer to gate-drive AN
Gate-source voltage, continuous	V_{GS}	-10	-	-	V	T_J = 0 to 150°C; Refer to gate-drive AN
Gate-source voltage, pulsed	$V_{GS,pulse}$	-25	-	-	V	T_J = 0 to 150°C; t_{PULSE} = 50 ns, f = 100 kHz; open drain Refer to gate-drive AN

Figure 4 Example gate voltage and current limits for 70 mΩ

The gate diode characteristic can be measured by itself using a two-terminal measurement (with the drain open). This result is shown in Figure 5. Note that this shows only the intrinsic characteristic of the gate diode itself, without the added influence of drain current (which will shift the curve left or right depending on the magnitude and direction of the drain current).

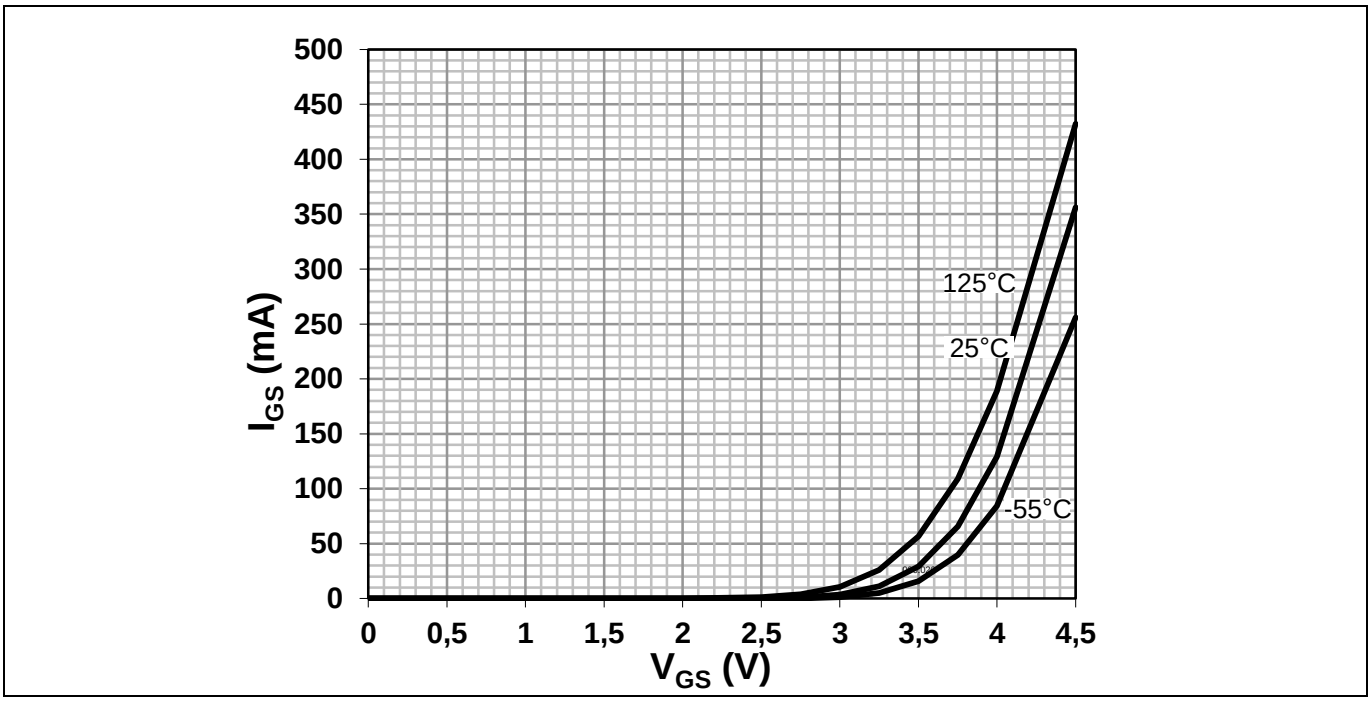

Figure 5 70 mΩ HEMT gate forward characteristics, open drain

In Figure 6, the reverse voltage characteristic of the gate is shown. The I-V behavior is not intrinsic to the device, but due to the presence of a protection diode structure (see Figure 2 equivalent circuit) that begins clamping at about -12 V.

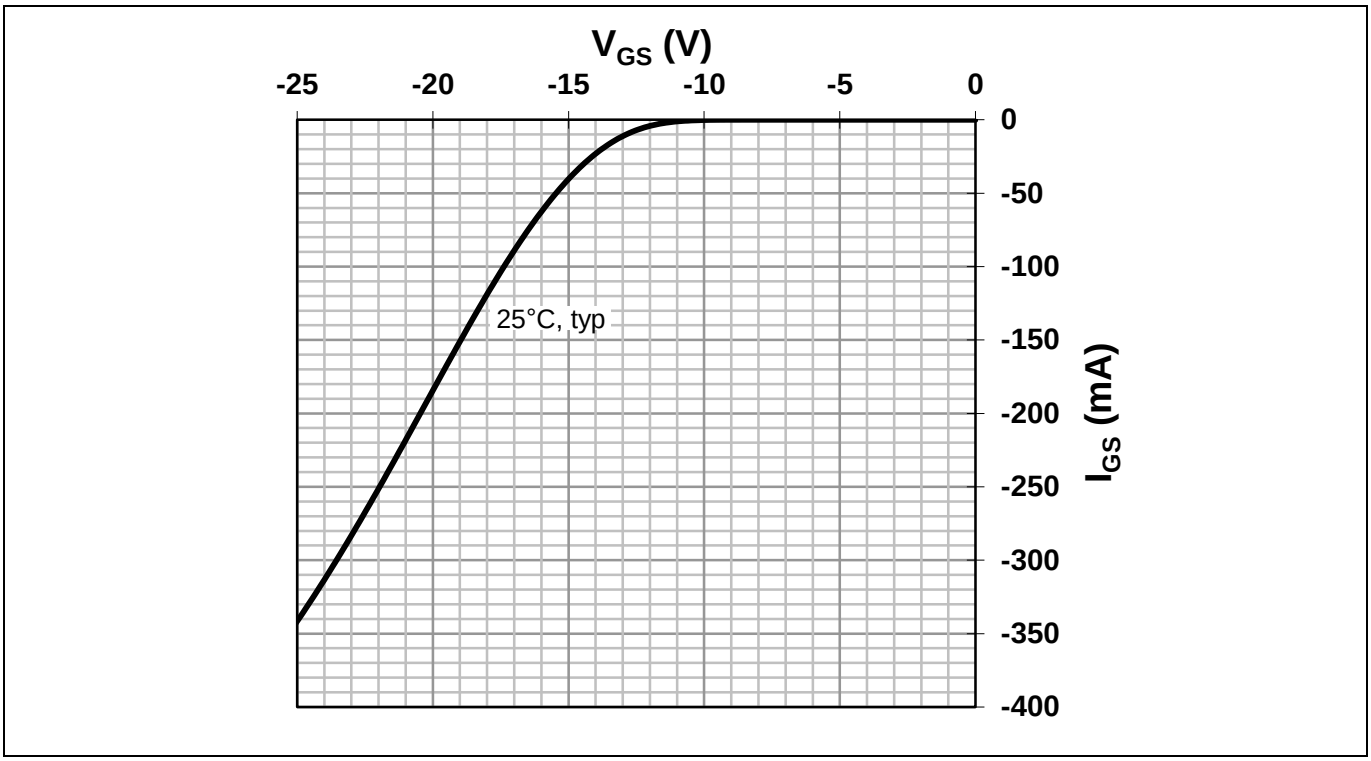

Figure 6 70 mΩ HEMT gate reverse characteristics, open drain

2.1.3 Gate charge

Gate charge is always a parameter of interest for high-frequency and/or high-speed switching circuits. For a given gate-drive circuit, the switching speed will be directly proportional to gate charge. Gate drive power consumption will also directly correlate to gate-charge Q_G. Figure 7 compares the gate-charge characteristic for two 70 mΩ transistors. Figure 7a (left) is the GaN HEMT, and Figure 7b (right) is a Si SJ MOSFET. A silicon carbide (SiC) FET has a total gate charge similar to a Si MOSFET, so GaN has a significantly lower total gate charge than either Si or SiC devices with similar ratings. The graph in Figure 7 represents the charge required to drive the gate from 0 V to fully on in a hard-switching mode. Once the transistor is on, a steady-state gate current of several mA is needed to keep the gate diode fully biased in the forward direction, thus ensuring that the transistor has sufficient gate drive to maintain full-rated drain current. The additional steady-state charge Q_{SS} is the integral of the steady-state gate current during the on-time, which can be expressed in simplified form as $Q_{SS} = I_{SS}t_{SS}$.

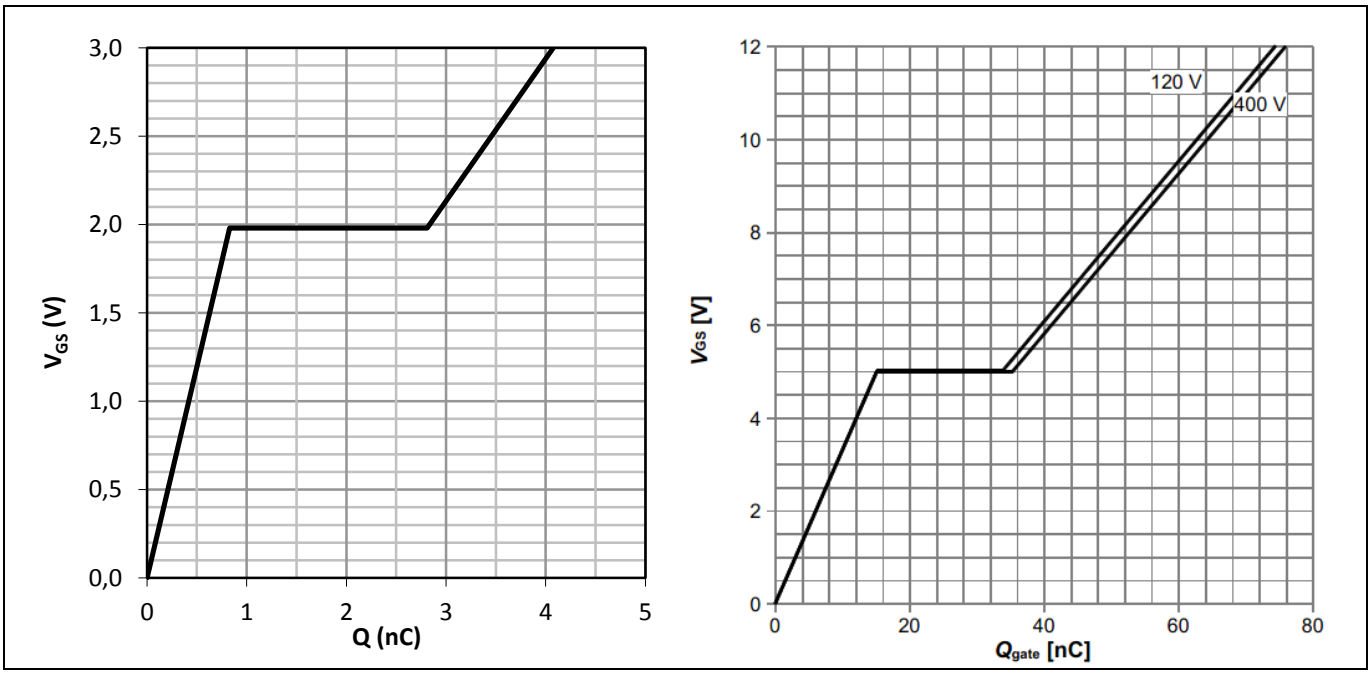

Figure 7 Typical gate-charge characteristics for 70 mΩ transistors: GaN on the left, Si SJ on the right

2.2 Output charge Q_{oss}

In soft-switching circuits, energy stored in an inductor is used to drive the transistor V_{DS} to the positive or negative voltage rail. The time required to make the transition is directly proportional to the inductor current and the output charge of the transistor. This is where the GaN HEMT has a big advantage over both Si and SiC transistors because of the much smaller Q_{oss}. Figure 8 shows the GaN HEMT Q_{oss} is about 10 times smaller than a corresponding SJ transistor. This translates to shorter dead-time and therefore higher-frequency capability for the GaN HEMT.

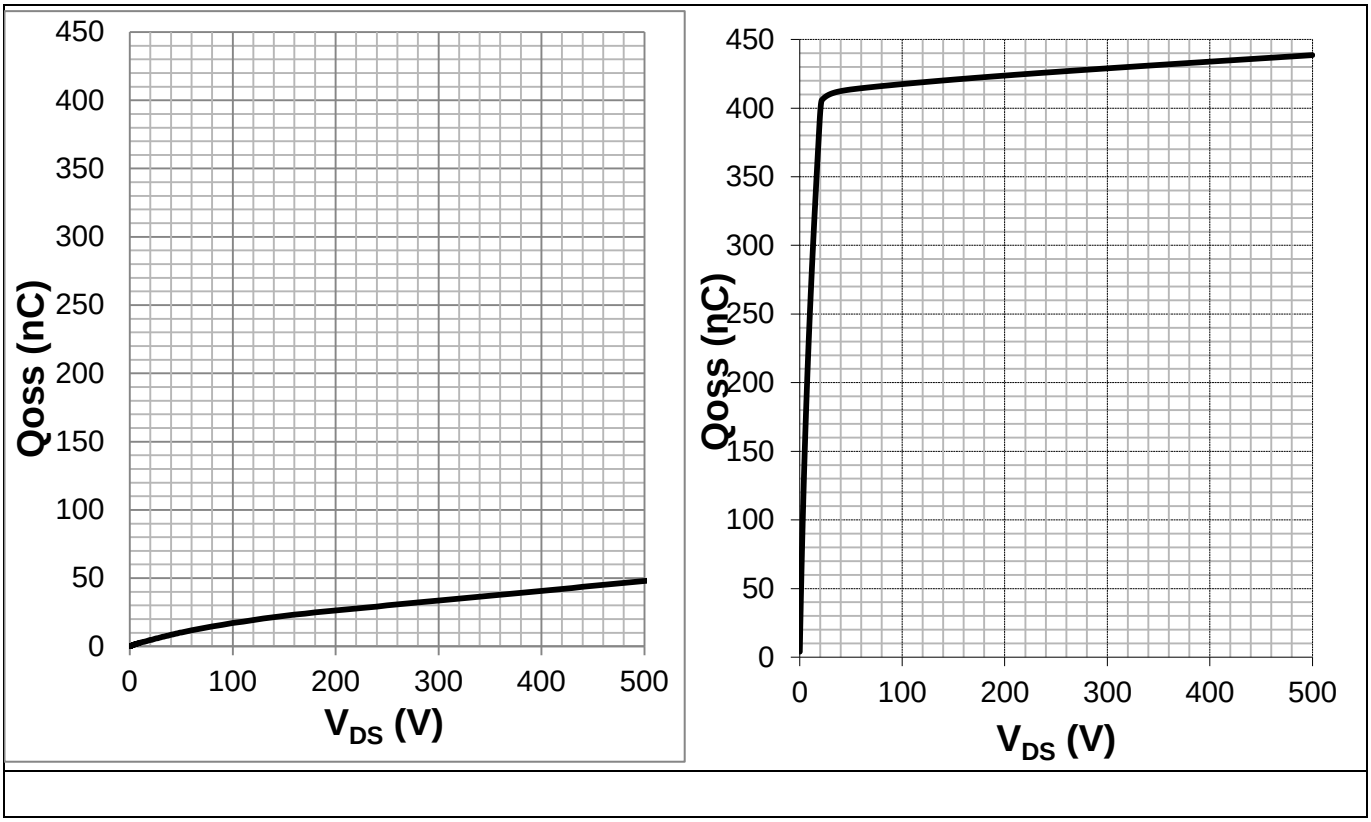

Figure 8 Output charge for 70 mΩ GaN HEMT (left) vs SJ MOSFET (right)

2.3 Energy stored in Q_{oss} : E_{oss}

From Figure 8, it is clear that the output capacitance and resulting charge of a SJ MOSFET is very non-linear. To determine the energy stored in the non-linear capacitance requires integrating the product of QV/dv. Doing so reveals one of the paradoxes of SJ having a high charge – that it also has a relatively small E_{oss}. This is because, even though the charge is very high near 0 V, the energy is low because the product of QV is also low. At higher voltages, the incremental change in charge is small, so energy is also low. This can be clearly seen in Figure 9 where the E_{oss} of a GaN HEMT is compared to a SJ MOSFET. At a bus voltage of 380 V, the SJ MOSFET has only about 25 percent higher E_{oss}, compared to a 10-fold difference In Q_{oss}.

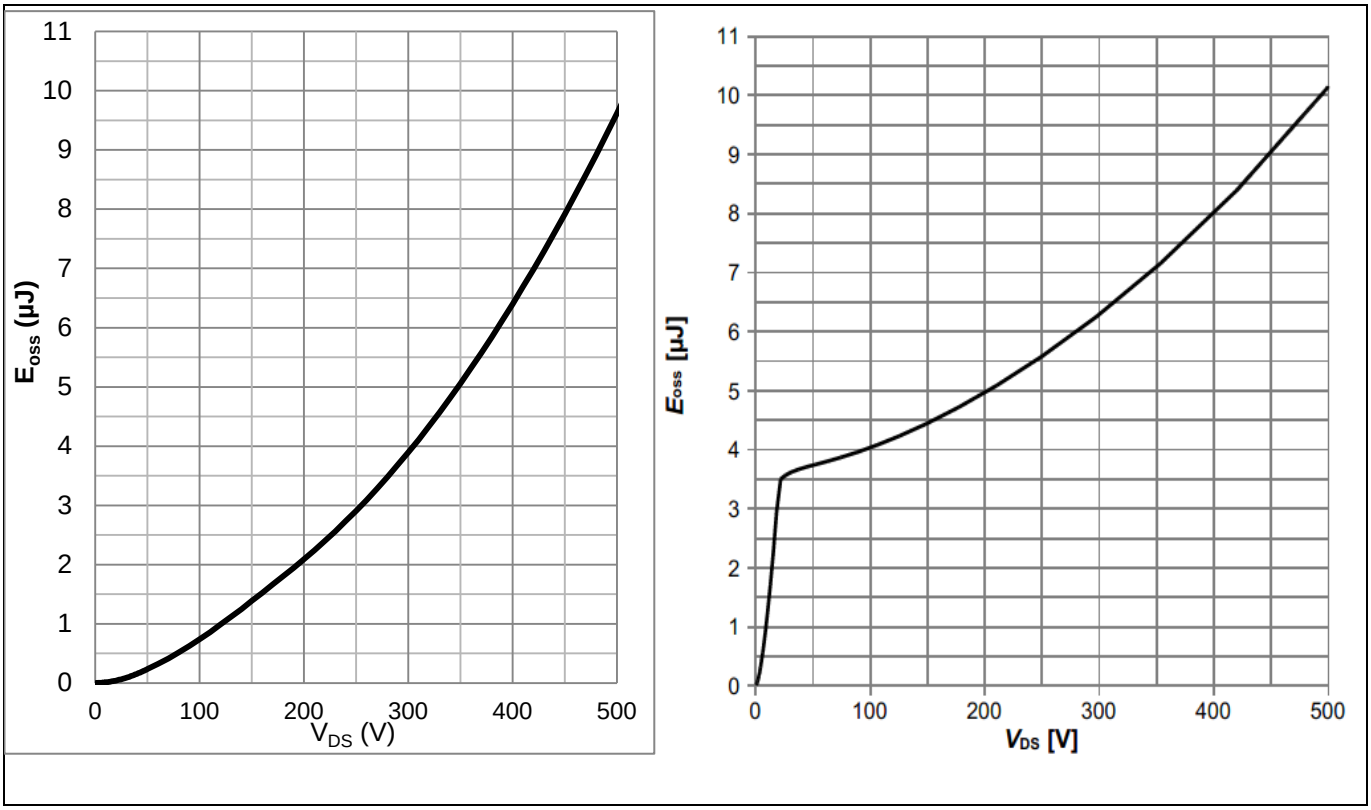

Figure 9 GaN 70 mΩ E_{oss} (left) vs SJ (right)

2.4 Peak current capability limited by saturation

As in MOSFETS, GaN HEMT channel mobility is reduced as temperature increases. This then reduces the maximum current-carrying capability of the transistor, and also increases the effective $R_{DS(on)}$ at higher temperatures. Care must be taken to make sure that the application circuit has appropriate current-limiting circuits to prevent the HEMT from being driven to current levels exceeding the datasheet maximum limits. Exceeding the limits could result in the transistor saturating and subsequently exceeding the safe operating area explained in section 2.5. Figure 10 shows the output characteristic of a 70 mΩ GaN HEMT at various gate-drive levels, at room temperature and at 125°C.

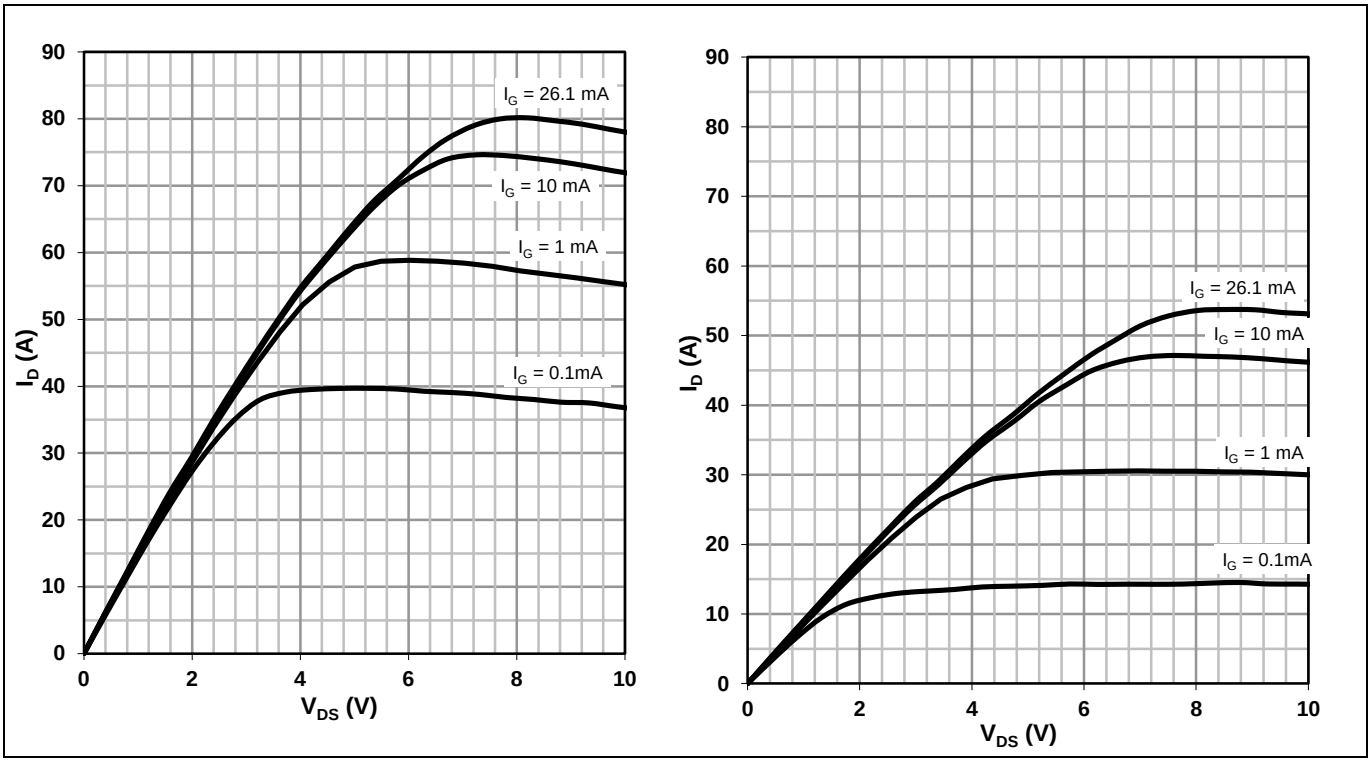

Figure 10 Typical 70 mΩ HEMT output characteristics at 25°C (left) and 125°C (right)

2.5 Safe Operating Area (SOA)

Safe Operating Area (SOA) curves show the limits of how much energy can be dissipated by a device for various duration, voltage and current levels. Like modern high-performance Si transistors, GaN HEMTs are designed for switched-mode operation, not linear mode. Nevertheless, GaN HEMTs are capable of supporting simultaneous voltage and current within reasonable limits as shown in Figure 11 at two different case temperatures.

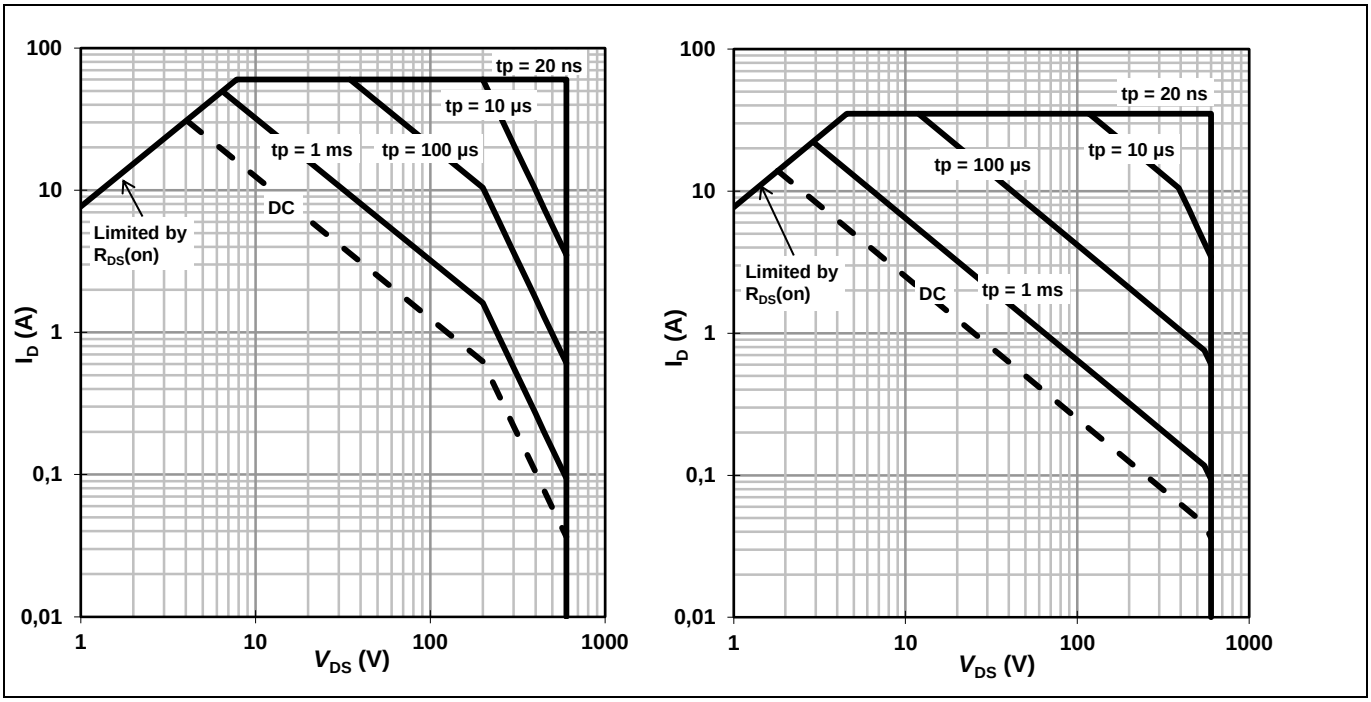

Figure 11 70 mΩ GaN HEMT SOA at 25°C (left) and at 125°C (right)

2.5.1 Repetitive Safe Operating Area (SOA)

The SOA curves in Figure 11 are based on a combination of thermal and electrical device limits including calculated and measured test-to-failure data. The circuit designer must ensure that the device operates within the SOA and also keep the junction temperature below datasheet limits to ensure reliable operation over the product lifetime.

Repetitive excursions to the maximum SOA limits (simultaneous maximum voltage and current) can result in cumulative damage that could shorten the device lifetime, even if each pulse is within the SOA and maximum rated junction temperature is never exceeded. As an example, a 10 ns hard-switching turn-on transient that causes the device to reach 35 A while VDS is 500 V, operating continuously at 125°C, is within (on the edge of) the SOA of Figure 11b. Because of the short pulse duration, the energy dissipated per pulse is relatively small, so the thermal rise due to repetitive pulses could be managed. But this extreme condition is outside of the recommended repetitive pulse SOA shown in Figure 12.

If your application conditions approach the datasheet repetitive SOA boundaries, an Infineon application engineer can help assess the conditions and provide modeled lifetime estimates for your particular application. Contact your local Infineon sales office for assistance on this topic.

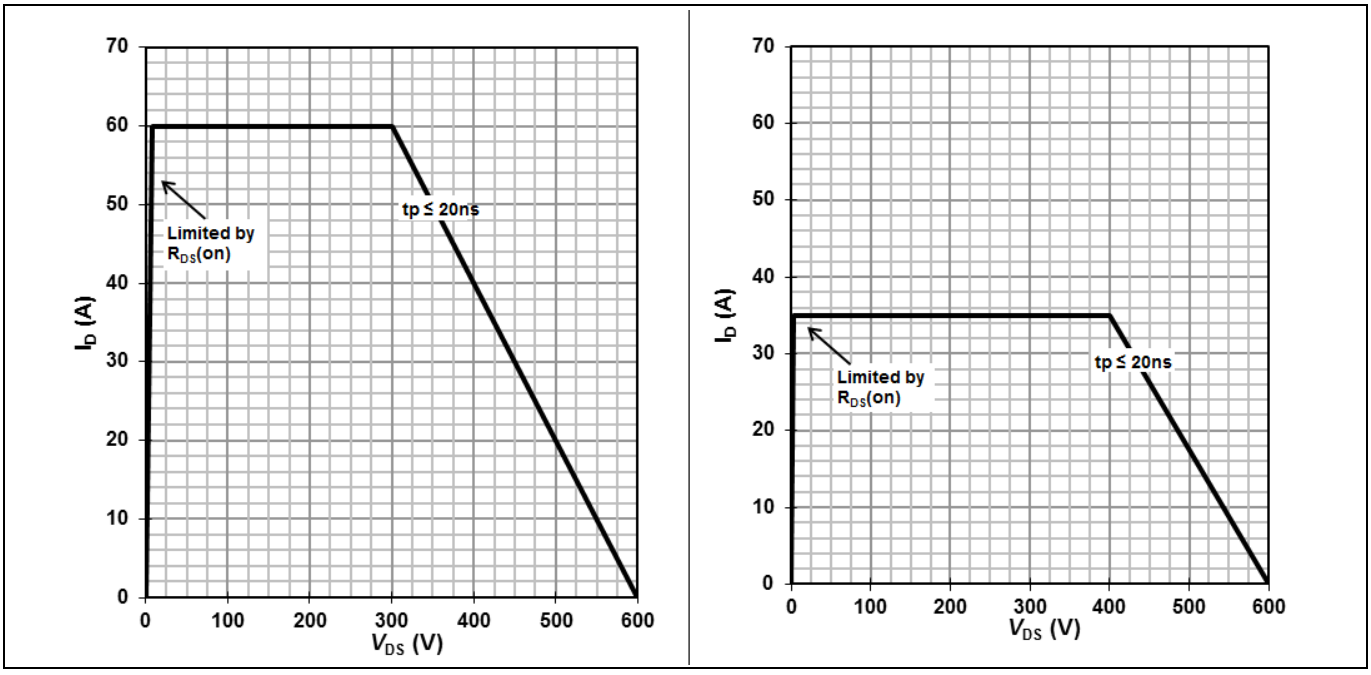

Figure 12 70 mΩ CoolGaN™ repetitive SOA at 25°C (left) and at 125°C (right)

2.6 Breakdown voltage, avalanche capability

GaN is a wide-bandgap material with very high critical electric field strength, 13 times higher than silicon. However when used in a lateral device structure, the critical field limit of GaN is not the limiting factor – it is the dielectric strength of the surface materials of the GaN HEMT that limit the breakdown voltage. As a result, the breakdown mechanism is not a junction avalanche as in silicon, but a dielectric breakdown mechanism more like a ceramic capacitor. The destructive failure limit is at least 50 percent greater than the maximum rated CoolGaN™ peak voltage, so there is a large guardband. So why is the HEMT rated at only 600 V if it can survive much higher transients? The answer lies in the lifetime models, which predict the useful lifetime vs degradation stress from OV, for example. In other words, the device lifetime will be reduced by the cumulative time accrued at higher-voltage stress conditions. If your application has occasional OV conditions, you can discuss this with

your local Infineon application engineer to see how your specific condition might affect the useful lifetime of the device.

Figure 13 shows the drain current vs applied V_{DS} at room temperature. Destructive breakdown occurs at much higher current levels far beyond the 1 mA level shown here. For example, all Infineon 70 mΩ GaN HEMTs are tested to a drain current of 12 mA to ensure the drain voltage is greater than 800 V as specified in a footnote in the datasheet.

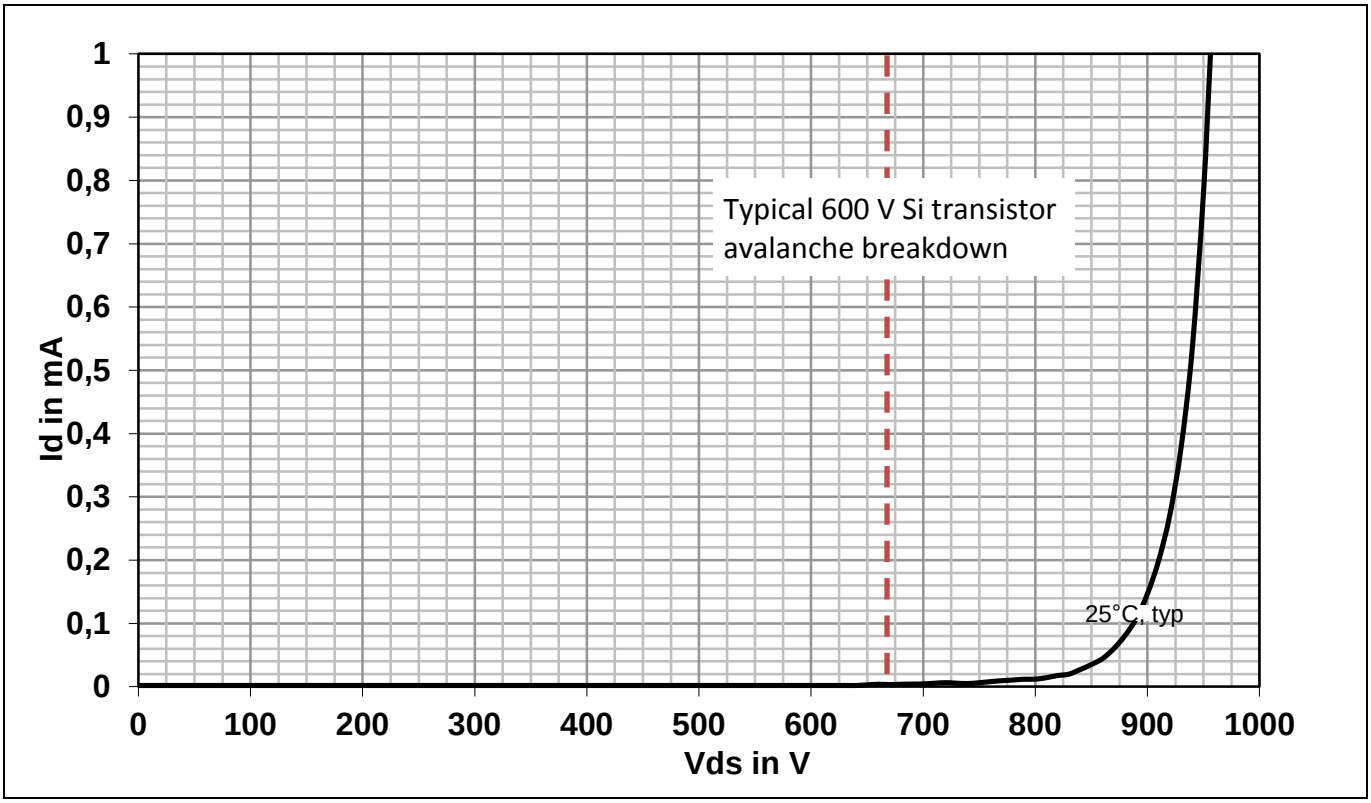

Figure 13 Drain leakage current versus applied V_{DS} up to more than 900 V

2.7 Reverse conduction characteristics, third-quadrant diode-mode

With the gate driven to the on-state, the GaN HEMT will conduct current equally well in either direction, just like a MOSFET. But when the gate is off, at 0 V for example, what happens when the drain is pulled below ground? Referring back to Figure 1, even though the HEMT is not symmetrical from drain to source, either terminal can act as a source. So if the gate and source are at 0 V, and the drain goes negative by more than the gate threshold voltage, the HEMT turns back on and begins conducting again in the reverse direction, with a voltage drop of about 2 V. If the gate-source voltage is at -2 V instead of 0 V, then the “diode drop” becomes 4 V. This can be seen in Figure 13 where the V_{DS} versus I_D curves are plotted in the third quadrant at varying V_{GS} voltages.

Normally, the HEMT is only in this “diode-like” mode for a brief period during the dead-time between switching intervals.

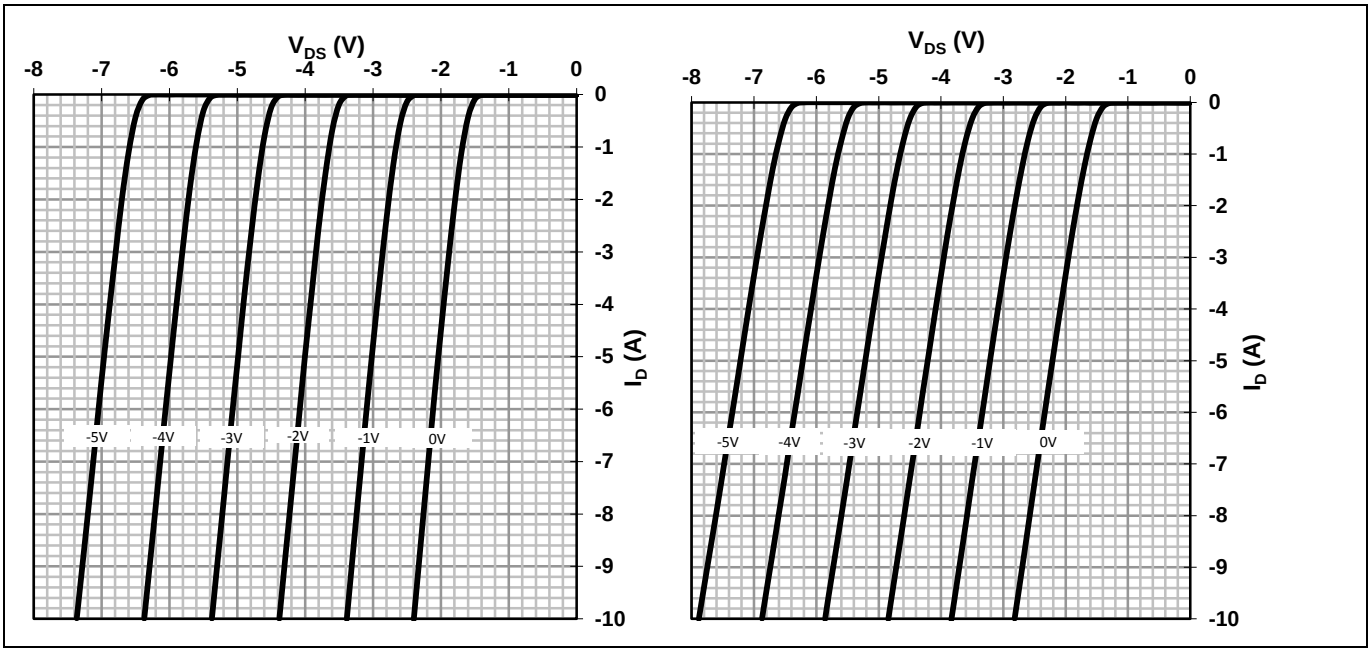

Figure 14 70 mΩ GaN HEMT third-quadrant conduction characteristics at 25°C (left) and 125°C (right)

2.8 Summary

CoolGaN™ can offer significant performance improvements for many power electronic application circuits. It is particularly useful in half-bridge configurations because it can operate either hard- or soft-switching without the concern of body diode recovery issues common to Si transistors. Its combination of low gate and output charge enables CoolGaN™ to switch rapidly, minimizing switching-related losses. For further information and additional application information, please visit www.infineon.com/GaN.

3 Revision history

Major changes since the last revision

Page or reference	Description of change

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