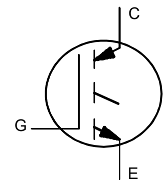
Insulated Gate Bipolar Transistor



n-channel

V_{CES} = 600V

$V_{CE(ON)}$ typ. = 1.32V

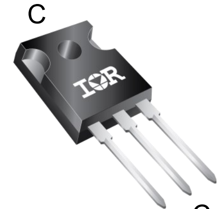
@ V_{GE} = 15V, IC = 31A

Features

- Standard: Optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AD package
- Lead-Free
- Automotive Qualified*

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



AUIRG4PC40S-E
TO-247AD

G	C	E
Gate	Collector	Emitter

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRG4PC40S-E	TO-247AD	Tube	25	AUIRG4PC40S-E

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	60	A
I_C @ T_C = 100°C	Continuous Collector Current	31	
I_{CM}	Pulse Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
V_{GE}	Continuous Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	——	0.77	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	0.24	——	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	——	40	
Wt	Weight	6 (0.21)	——	g (oz)

* Qualification standard can be found at www.infineon.com/

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—		V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.32	1.5	V	I_C = 31A, V_{GE} = 15V, T_J = 25°C
		—	1.68	—		I_C = 60A, V_{GE} = 15V, See Fig. 2,5
		—	1.32	—		I_C = 31A, V_{GE} = 15V, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage Temperature Coeff.	—	-9.3	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
gfe	Forward Transconductance⑤	12	21	—	S	V_{CE} = 100V, I_C = 31A
I_{CES}	Collector-to-Emitter Leakage Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	100	150	nC	I_C = 31A
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	14	21		V_{GE} = 15V See Fig.8
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	34	51		V_{CC} = 400V
$t_{d(on)}$	Turn-On delay time	—	22	—	ns	I_C = 31A, V_{CC} = 480V, V_{GE}=15V
t_r	Rise time	—	18	—		R_G = 10Ω, T_J = 25°C
$t_{d(off)}$	Turn-Off delay time	—	650	980		Energy losses include “tail”
t_f	Fall time		380	570		See Fig. 10, 11, 13, 14
E_{on}	Turn-On Switching Loss	—	0.45	—	mJ	
E_{off}	Turn-Off Switching Loss	—	6.5	—		
E_{ts}	Total Switching Loss	—	6.95	9.9		
$t_{d(on)}$	Turn-On delay time	—	23	—	ns	I_C = 31A, V_{CC} = 480V, V_{GE}=15V
t_r	Rise time	—	21	—		R_G = 10Ω, T_J = 150°C
$t_{d(off)}$	Turn-Off delay time	—	1000	—		Energy losses include “tail”
t_f	Fall time	—	940	—		See Fig. 13, 14
E_{ts}	Total Switching Loss	—	12	—	mJ	
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2200	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	26	—		f = 1.0Mhz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)
② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)
③ Repetitive rating; pulse width limited by maximum junction temperature.
④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.
⑤ Pulse width 5.0µs, single shot.

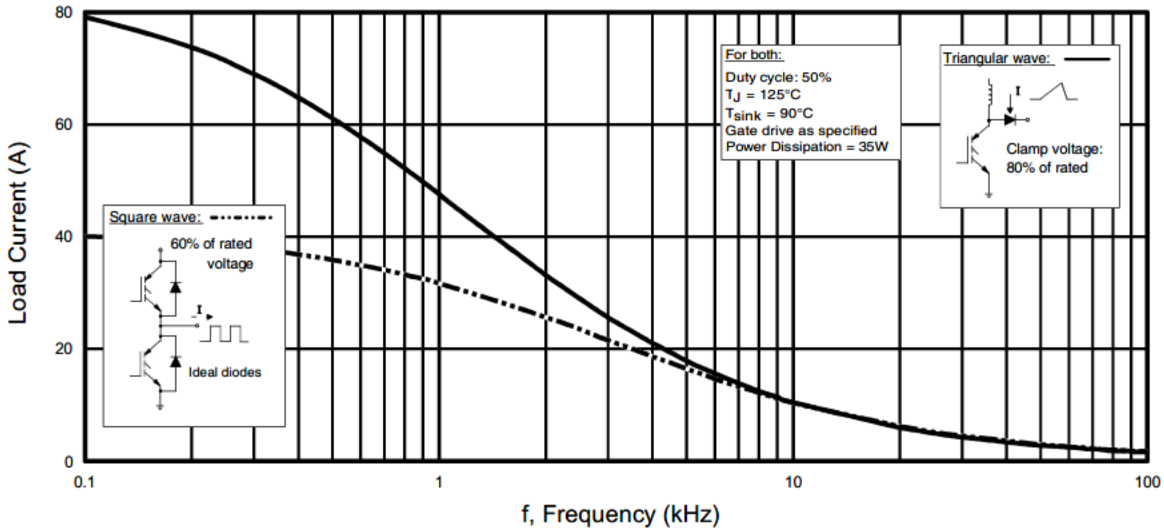


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

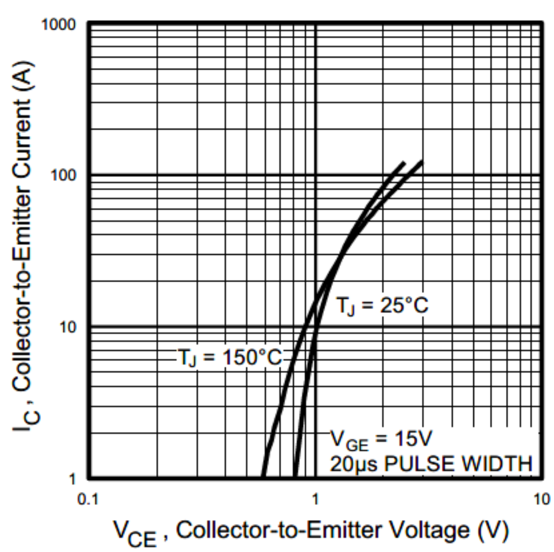


Fig. 2 - Typical Output Characteristics

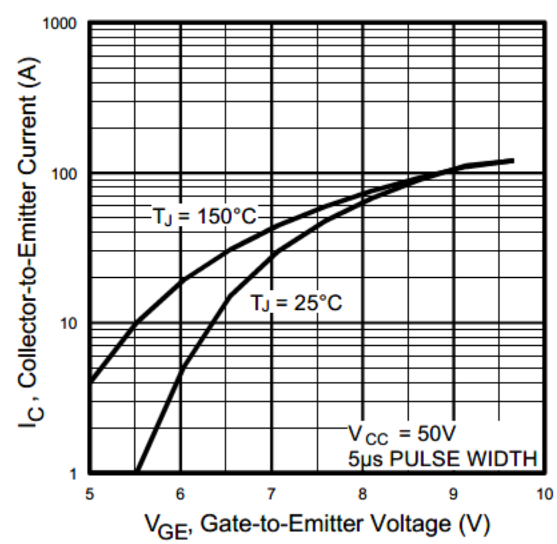


Fig. 3 - Typical Transfer Characteristics

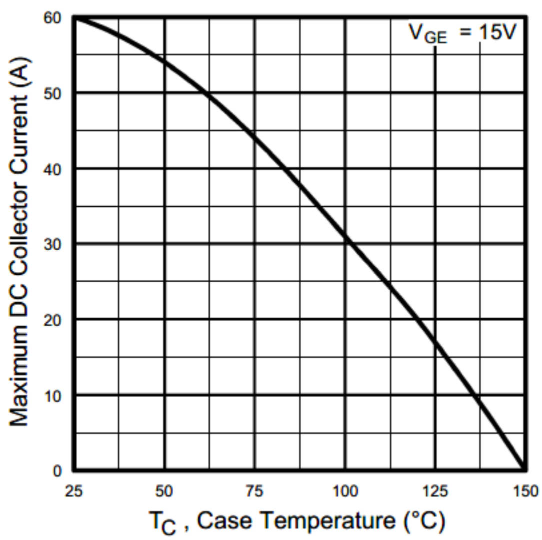


Fig. 4 - Maximum Collector Current vs. Case Temperature

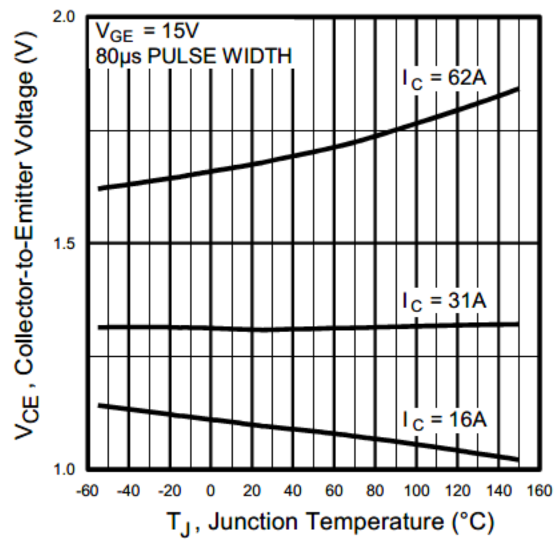


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

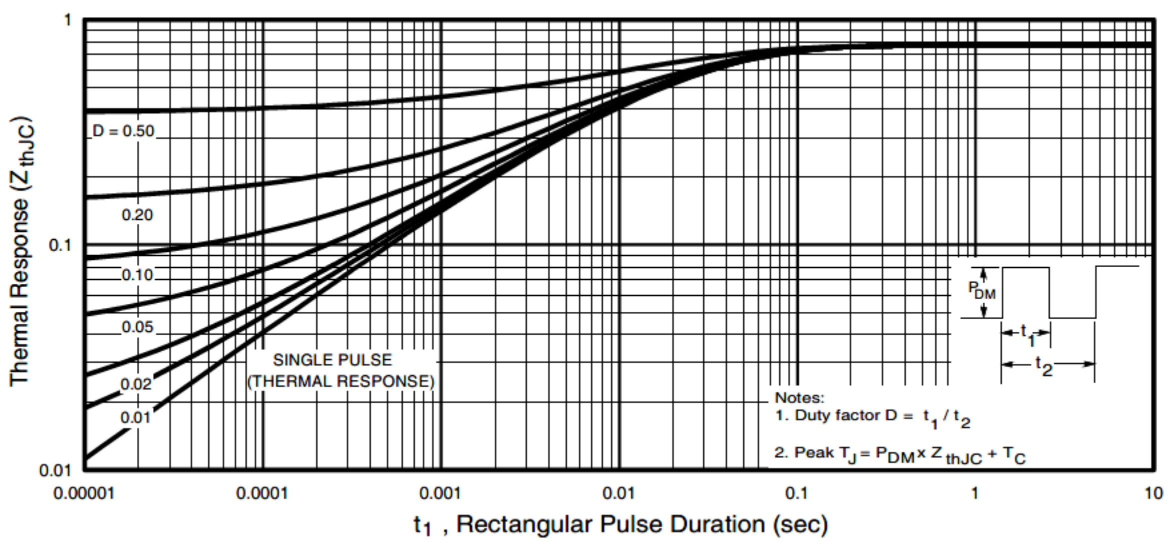


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

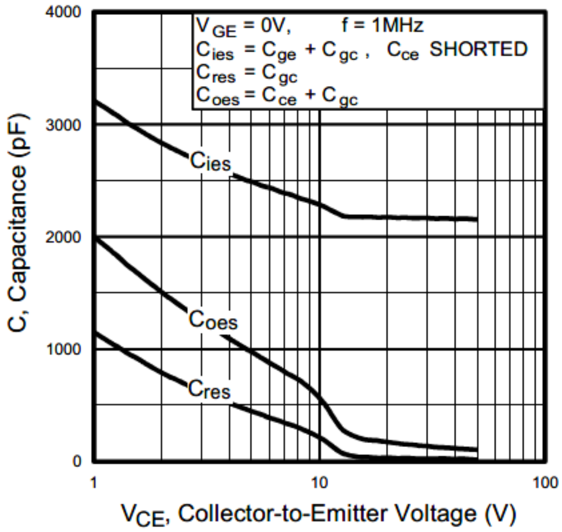


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

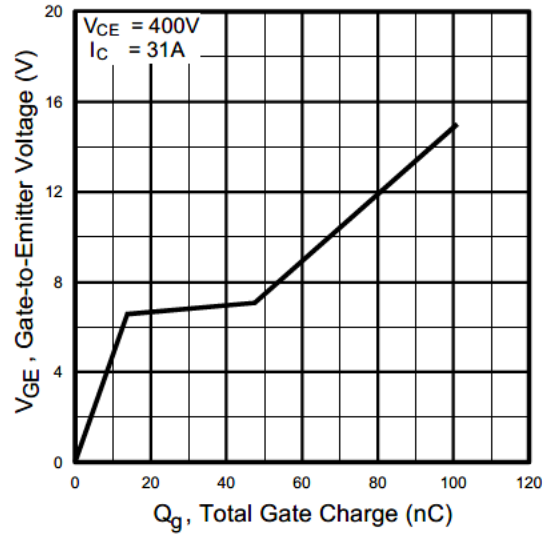


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

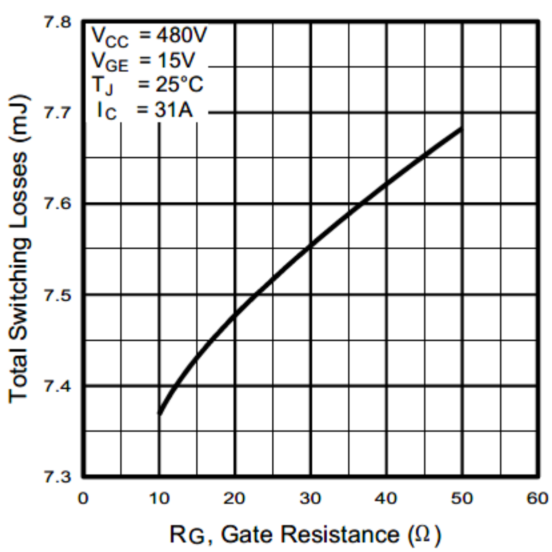


Fig. 9 - Typical Switching Losses vs. Gate Resistance

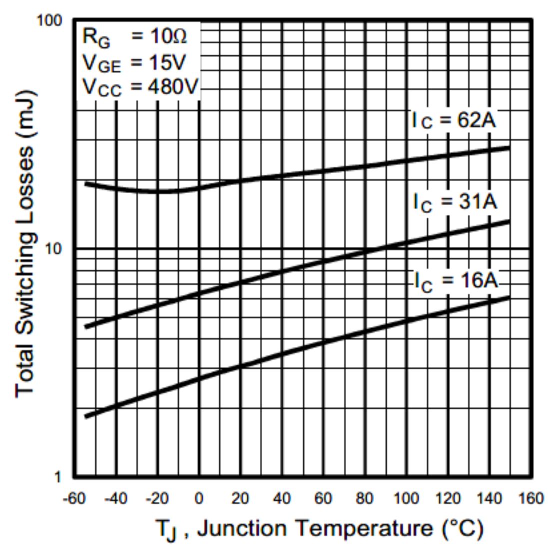


Fig. 10 - Typical Switching Losses vs. Junction Temperature

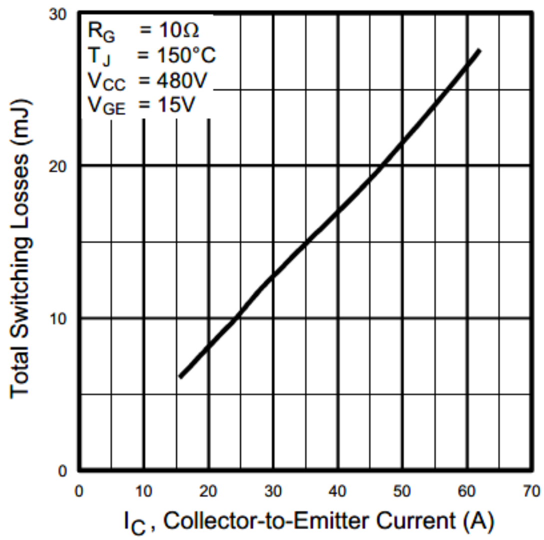


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

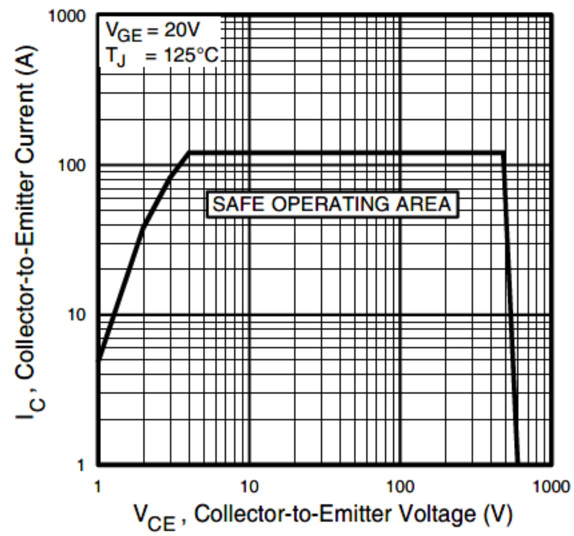
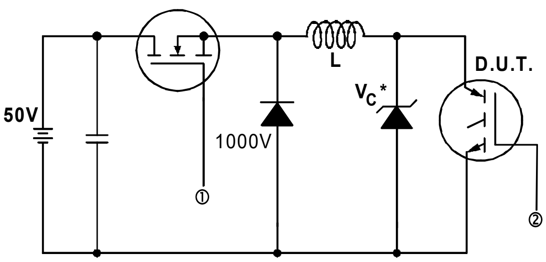


Fig. 12 - Turn-Off SOA



* Driver same type as D.U.T.; Vc = 80% of Vce(max)
* Note: Due to the 50V power supply, pulse width and inductor will increase to obtain rated Id.

Fig. 13a - Clamped Inductive Load Test Circuit

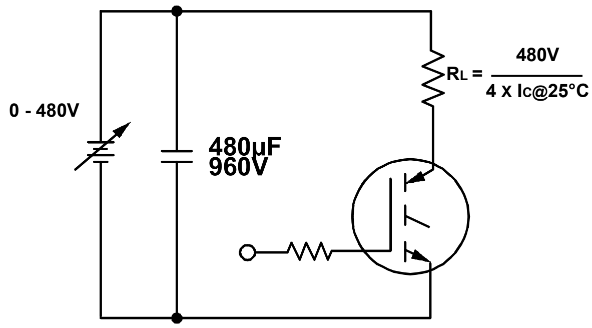
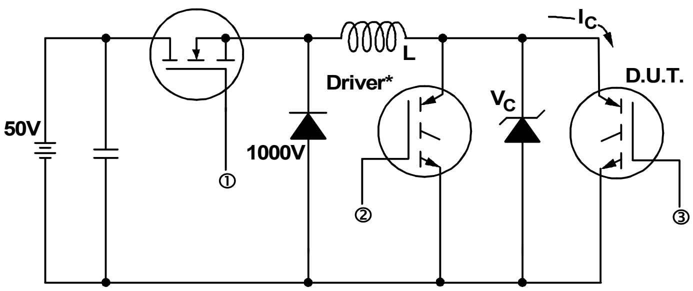


Fig. 13b - Pulsed Collector Current Test Circuit



* Driver same type as D.U.T., VC = 480V

Fig. 14a - Switching Loss Test Circuit

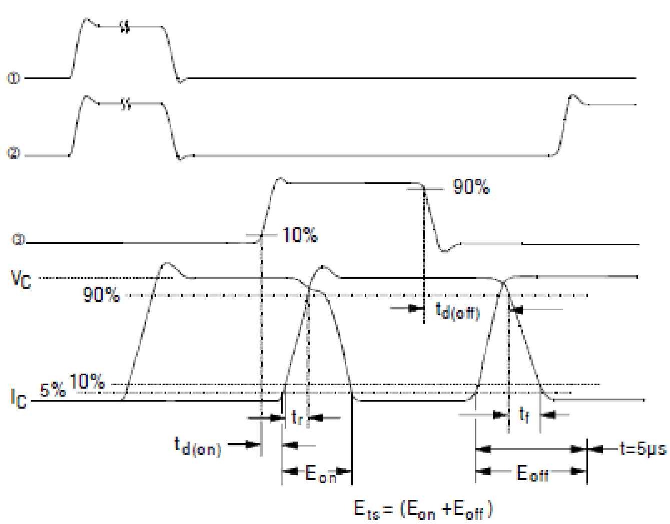
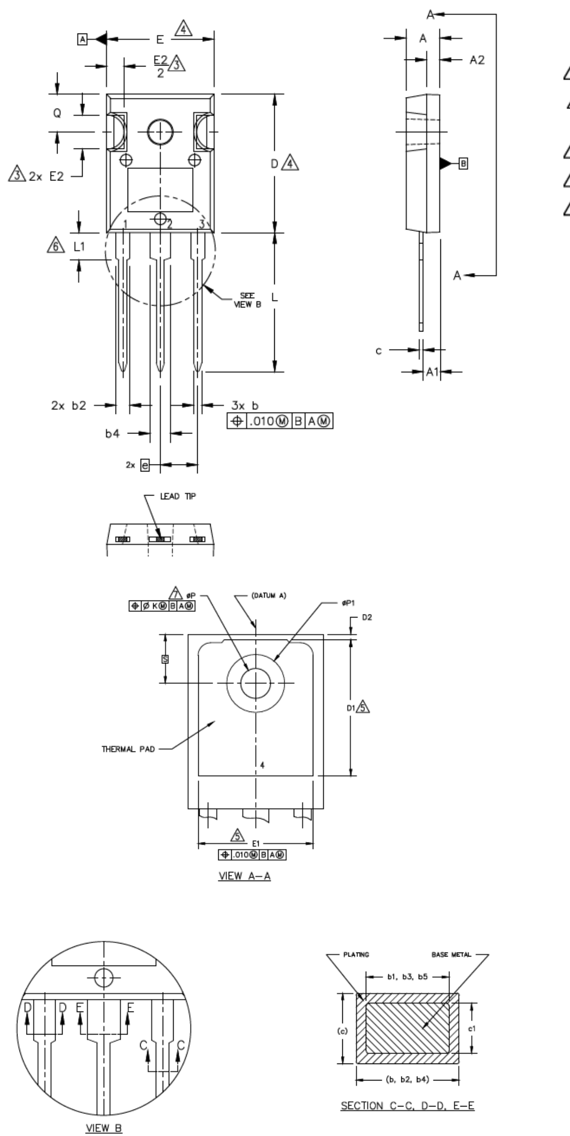


Fig. 14b - Switching Loss Waveforms

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.190	.203	4.83	5.13	
A1	.087	.102	2.21	2.59	
A2	.072	.084	1.83	2.13	
b	.041	.051	1.04	1.30	
b1	.041	.050	1.04	1.28	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.017	.035	0.44	0.88	
c1	.017	.034	0.44	0.84	
D	.776	.795	19.71	20.20	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.604	.625	15.35	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.791	.823	20.10	20.90	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

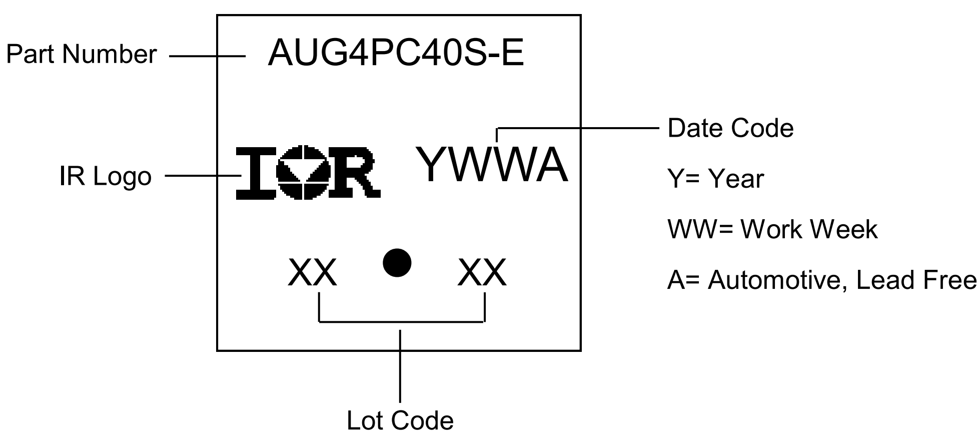
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AD Part Marking Information



TO-247AD package is not recommended for Surface Mount Application.

Qualification Information†

Qualification Level		Automotive (per AEC-Q101) ††	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-247AD	N/A
ESD	Human Body Model	Class H1C (+/- 2000V) AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: www.infineon.com

†† Exceptions to AEC-Q101 requirements are noted in the qualification report.

Revision History

Date	Comments
08/12/2020	• Updated datasheet with corporate template. • Update the Dimensions table and package outline drawing on page 8

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